

## 70A, 60V, 0.014 Ohm, N-Channel Power MOSFET

The RFK70N06 N-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49007.

### Ordering Information

| PART NUMBER | PACKAGE  | BRAND    |
|-------------|----------|----------|
| RFK70N06    | TO-204AE | RFK70N06 |

NOTE: When ordering, use the entire part number.

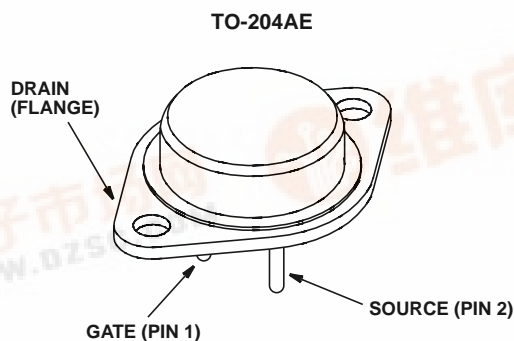
### Features

- 70A, 60V
- $r_{DS(ON)} = 0.014\Omega$
- Temperature Compensating PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

### Symbol



### Packaging



## RFK70N06

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ Unless Otherwise Specified

|   | RFK70N06                    | UNITS                     |
|---|-----------------------------|---------------------------|
| Drain to Source Voltage (Note 1) . . . . .  | 60                          | V                         |
| Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .                  | 60                          | V                         |
| Continuous Drain Current . . . . .  | 70                          | A                         |
| Pulsed Drain Current (Note 3) . . . . .   | Refer to Peak Current Curve |                           |
| Gate to Source Voltage . . . . .  | $\pm 20$                    | V                         |
| Pulsed Avalanche Rating . . . . .   | Refer to UIS Curve          |                           |
| Power Dissipation . . . . .   | 150                         | W                         |
| Linear Derating Factor . . . . .  | 1.0                         | $\text{W}/^\circ\text{C}$ |
| Operating and Storage Temperature . . . . .   | -55 to 175                  | $^\circ\text{C}$          |
| Maximum Temperature for Soldering<br>Leads at 0.063in (1.6mm) from Case for 10s . . . . . | 260                         | $^\circ\text{C}$          |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

| PARAMETER                              | SYMBOL          | TEST CONDITIONS  | MIN | TYP  | MAX       | UNITS                     |
|--|-----------------|--|-----|------|-----------|---------------------------|
| Drain to Source Breakdown Voltage      | $BV_{DSS}$      | $I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$  | 60  | -    | -         | V                         |
| Gate to Source Threshold Voltage       | $V_{GS(TH)}$    | $V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$   | 2   | -    | 4         | V                         |
| Zero Gate Voltage Drain Current        | $I_{DSS}$       | $V_{DS} = \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$   | -   | -    | 1         | $\mu\text{A}$             |
|  |                 | $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$  | -   | -    | 25        | $\mu\text{A}$             |
| Gate to Source Leakage Current         | $I_{GSS}$       | $V_{GS} = \pm 20\text{V}$  | -   | -    | $\pm 100$ | nA                        |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$    | $I_D = 70\text{A}$ , $V_{GS} = 10\text{V}$ (Figure 10)   | -   | -    | 0.014     | $\Omega$                  |
| Turn-On Time                           | $t_{ON}$        | $V_{DD} = 30\text{V}$ , $I_D \approx 70\text{A}$ , $R_L = 0.43\Omega$ ,<br>$V_{GS} = 10\text{V}$ , $R_G = 2.5\Omega$<br>(Figures 14, 17, 18) | -   | -    | 125       | ns                        |
| Turn-On Delay Time                     | $t_{d(ON)}$     |  | -   | 12   | -         | ns                        |
| Rise Time                              | $t_r$           |  | -   | 50   | -         | ns                        |
| Turn-Off Delay Time                    | $t_{d(OFF)}$    |  | -   | 40   | -         | ns                        |
| Fall Time                              | $t_f$           |  | -   | 15   | -         | ns                        |
| Turn-Off Time                          | $t_{OFF}$       |  | -   | -    | 125       | ns                        |
| Total Gate Charge                      | $Q_{g(TOT)}$    | $V_{GS} = 0\text{V}$ to $20\text{V}$   | -   | 185  | 215       | nC                        |
| Gate Charge at 10V                     | $Q_{g(10)}$     | $V_{GS} = 0\text{V}$ to $10\text{V}$   |     |      |           |                           |
| Threshold Gate Charge                  | $Q_{g(TH)}$     | $V_{GS} = 0\text{V}$ to $2\text{V}$  |     |      |           |                           |
| Input Capacitance                      | $C_{ISS}$       | $V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$<br>(Figure 13)  | -   | 3000 | -         | pF                        |
| Output Capacitance                     | $C_{OSS}$       |  | -   | 900  | -         | pF                        |
| Reverse Transfer Capacitance           | $C_{RSS}$       |  | -   | 300  | -         | pF                        |
| Thermal Resistance Junction to Case    | $R_{\theta JC}$ |  | -   | -    | 1.0       | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ |  | -   | -    | 80        | $^\circ\text{C}/\text{W}$ |

### Source to Drain Diode Specifications

| PARAMETER                     | SYMBOL   | TEST CONDITIONS  | MIN | TYP | MAX | UNITS |
|-------------------------------|----------|--|-----|-----|-----|-------|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD} = 70\text{A}$  | -   | -   | 1.5 | V     |
| Reverse Recovery Time         | $t_{rr}$ | $I_{SD} = 70\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | -   | -   | 125 | ns    |

**NOTES:**

2. Pulse test: pulse width  $\leq 300\text{ms}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width is limited by maximum junction temperature. See Transient Thermal Temperature curve (Figure 3).

Typical Performance Curves

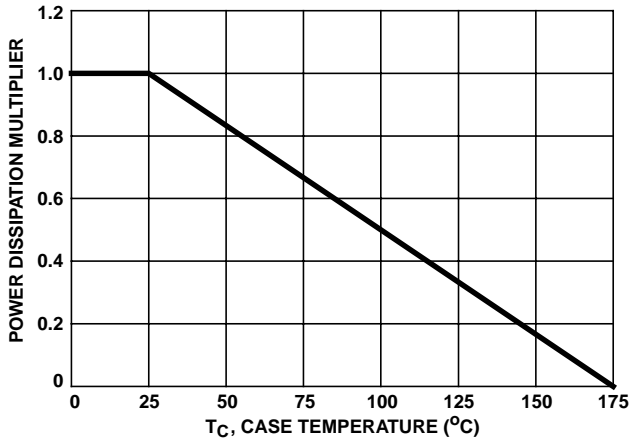


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

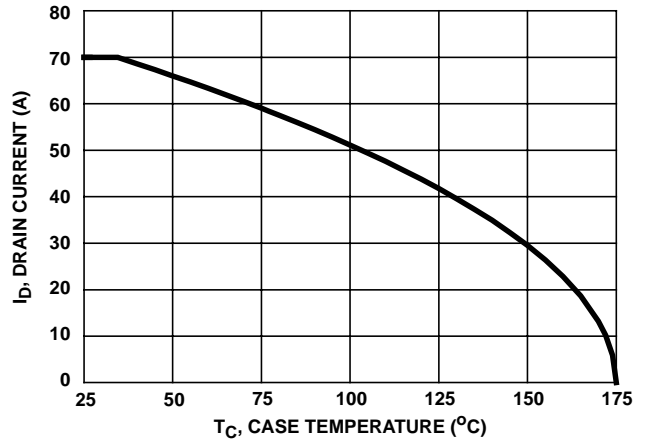


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

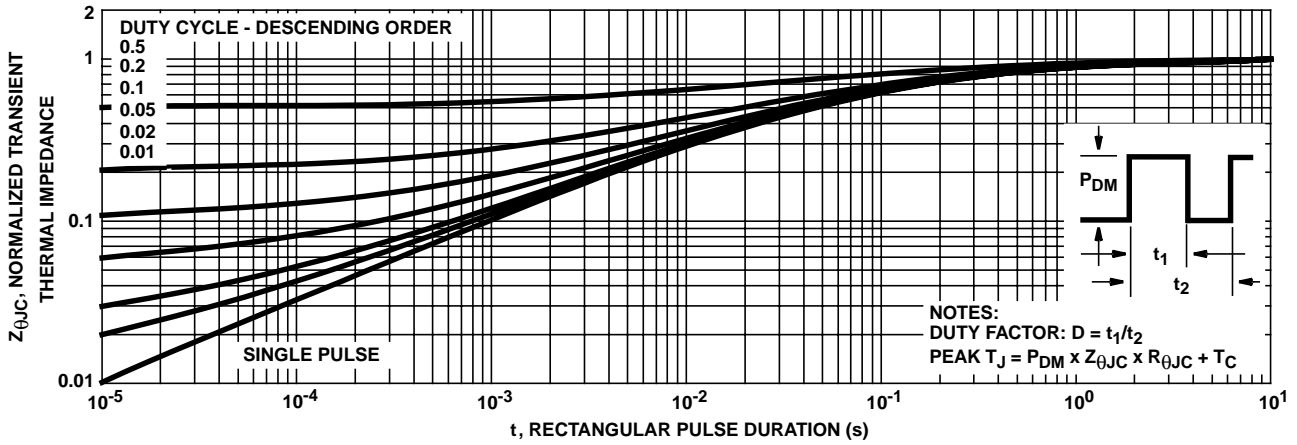


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

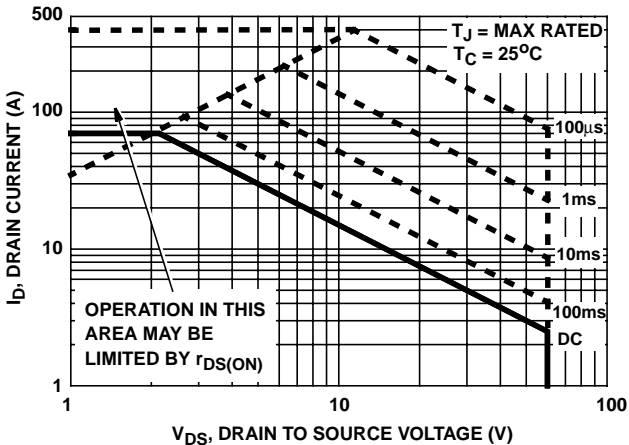


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

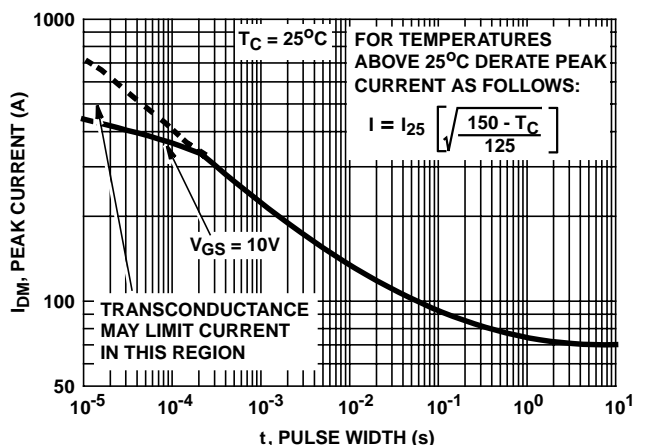
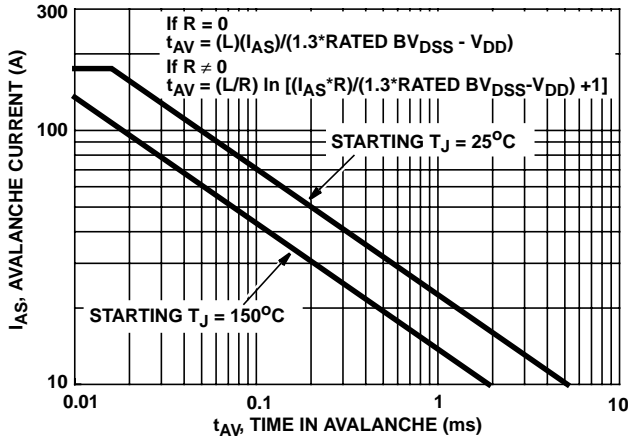
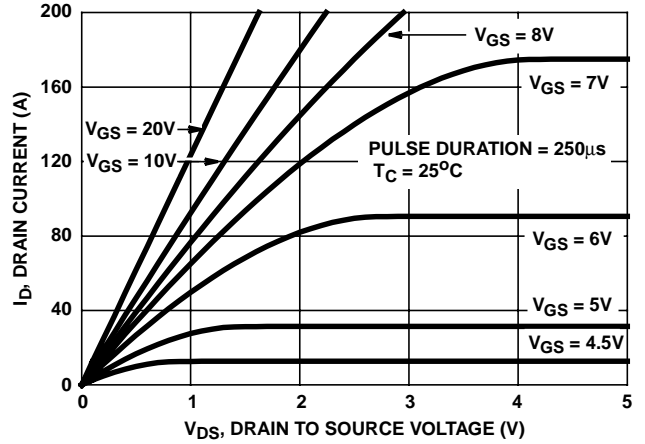


FIGURE 5. PEAK CURRENT CAPABILITY

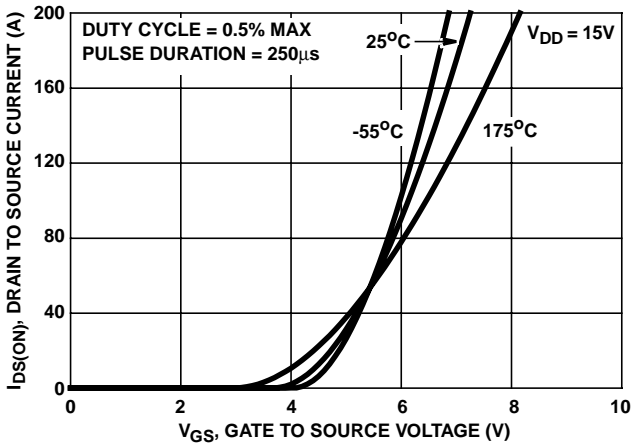
Typical Performance Curves (Continued)



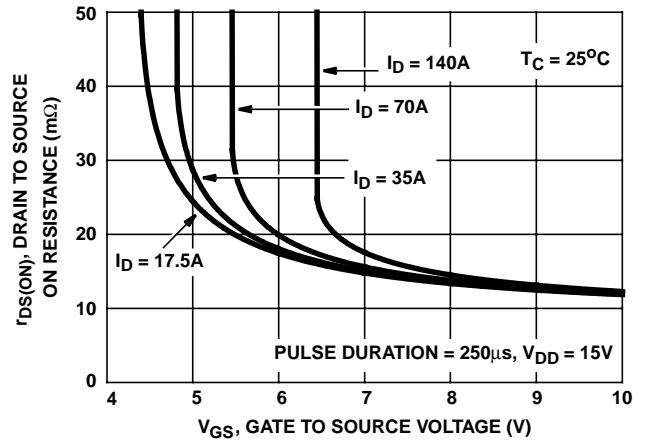
NOTE: Refer to Intersil Application Notes AN9321 and AN9322.  
**FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**



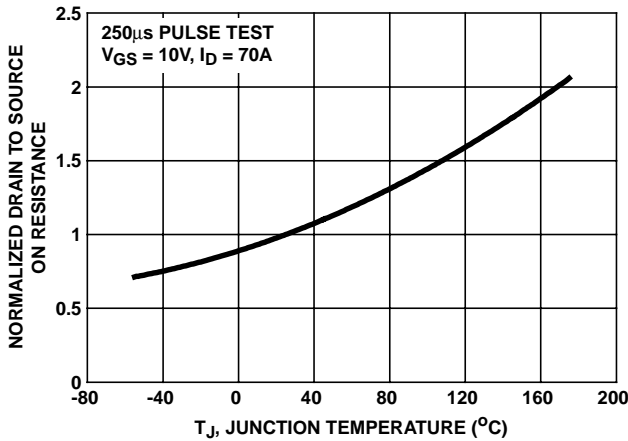
**FIGURE 7. SATURATION CHARACTERISTICS**



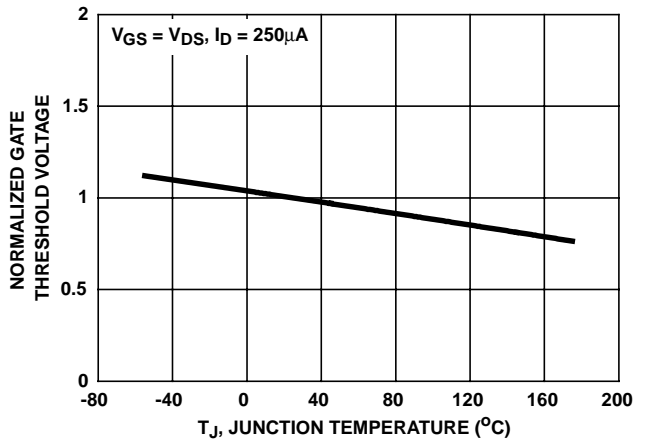
**FIGURE 8. TRANSFER CHARACTERISTICS**



**FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT**



**FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**



**FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE**

Typical Performance Curves (Continued)

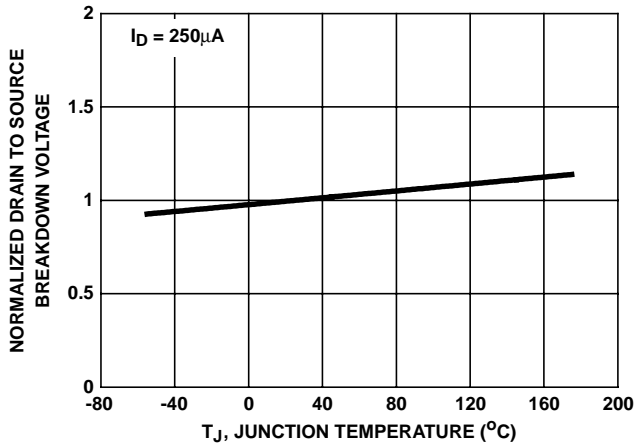


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

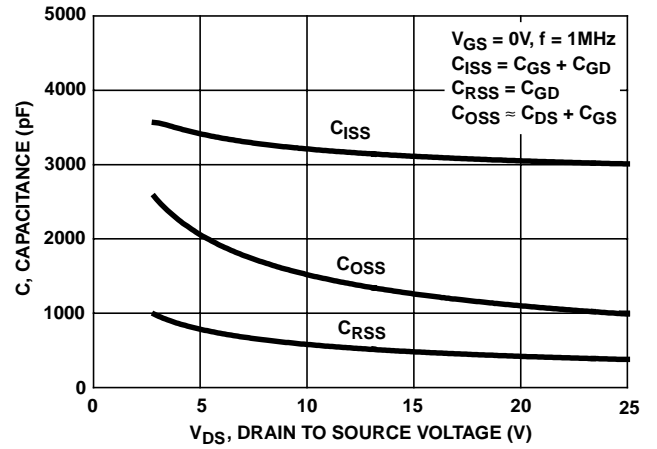
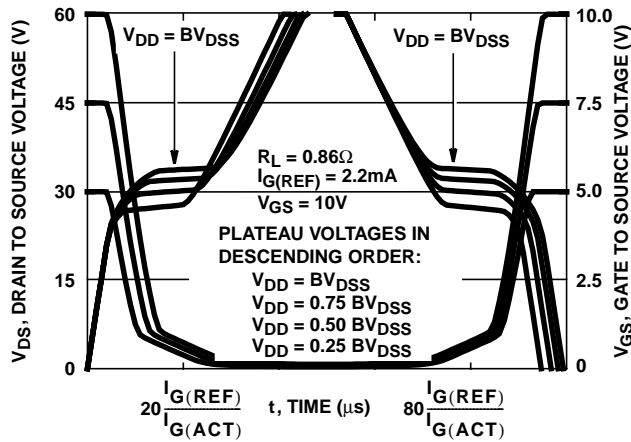


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

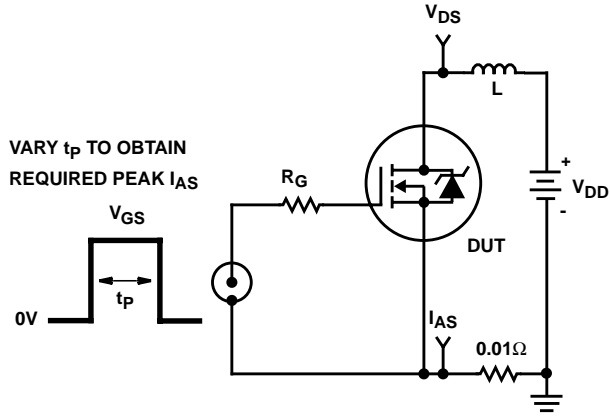


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

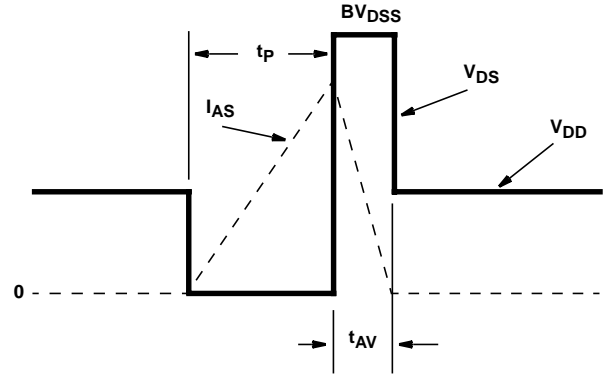


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

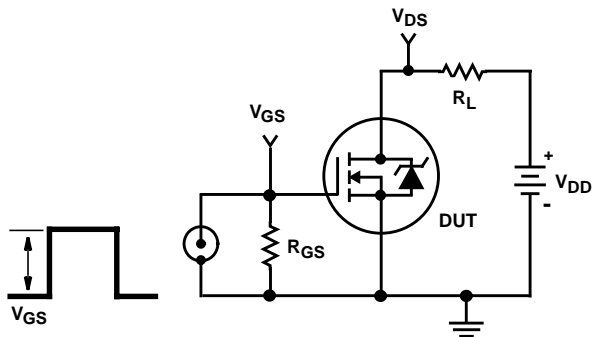


FIGURE 17. SWITCHING TIME TEST CIRCUIT

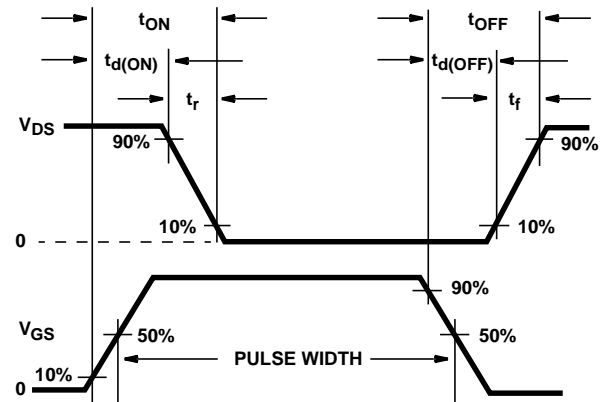


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

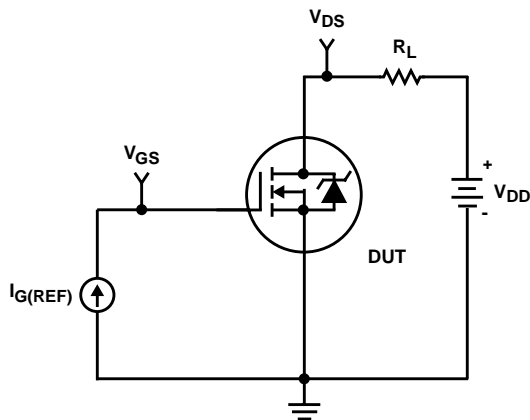


FIGURE 19. GATE CHARGE TEST CIRCUIT

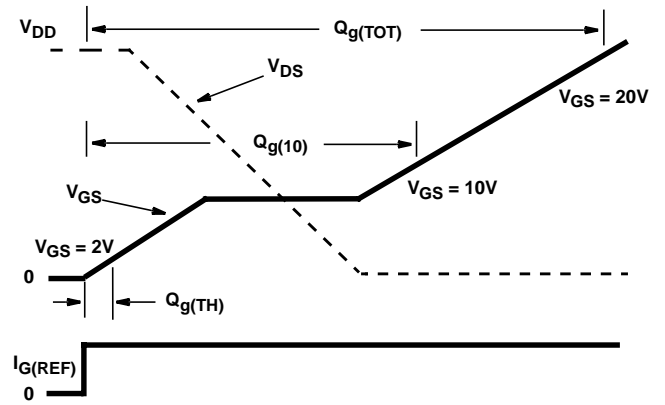


FIGURE 20. GATE CHARGE WAVEFORMS

## RFK70N06

### PSPICE Electrical Model

.SUBCKT RFK70N06 2 1 3 ; rev 1/16/97

CA 12 8 5.56e-9  
 CB 15 14 5.30e-9  
 CIN 6 8 2.63e-9

DBODY 7 5 DBDMOD  
 DBREAK 5 11 DBKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.18  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTO 20 6 18 8 1

IT 8 17 1

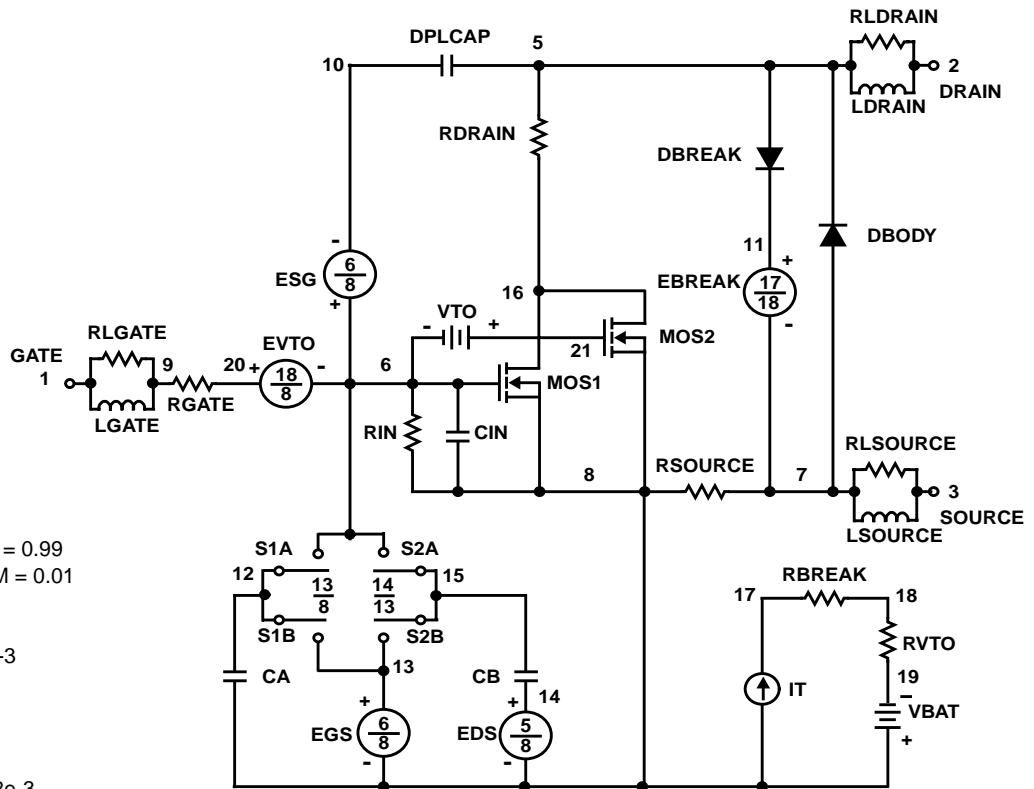
LDRAIN 2 5 1e-9  
 LGATE 1 9 11.45e-9  
 LSOURCE 3 7 4.60e-9

MOS1 16 6 8 8 MOSMOD M = 0.99  
 MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1  
 RDRAIN 5 16 RDSMOD 4.66e-3  
 RLDRAIN 2 5 10  
 RGATE 9 20 1.21  
 RLGATE 1 9 114.5  
 RIN 6 8 1e9  
 RSOURCE 8 7 RDSMOD 3.92e-3  
 RLSOURCE 3 7 46  
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1  
 VTO 21 6 0.605



.MODEL DBDMOD D (IS = 7.91e-12 RS = 3.87e-3 TRS1 = 2.71e-3 TRS2 = 2.50e-7 CJO = 4.84e-9 TT = 4.51e-8)  
 .MODEL DBKMOD D (RS = 3.9e-2 TRS1 = 1.05e-4 TRS2 = 3.11e-5)  
 .MODEL DPLCAPMOD D (CJO = 4.8e-9 IS = 1e-30 N = 10)  
 .MODEL MOSMOD NMOS (VTO = 3.46 KP = 47 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL RBKMOD RES (TC1 = 8.46e-4 TC2 = -8.48e-7)  
 .MODEL RDSMOD RES (TC1 = 2.23e-3 TC2 = 6.56e-6)  
 .MODEL RVTOMOD RES (TC1 = -3.29e-3 TC2 = 3.49e-7)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -8.35 VOFF = -6.35)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.35 VOFF = -8.35)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = 3.0)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.0 VOFF = -2.0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### **Sales Office Headquarters**

#### **NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (407) 724-7000  
FAX: (407) 724-7240

#### **EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### **ASIA**

Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029