HARRIS Semiconductor

RFL1P08, RFL1P10

1A, -80V and -100V, 3.65 Ohm, P-Channel Power MOSFETs

July 1998

Features

- 1A, -80V and -100V
- $r_{DS(ON)}$ = 3.65Ω
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

These are P-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

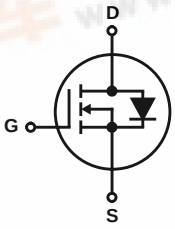
Formerly developmental type TA9400.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFL1P08	TO-205AF	RFL1P08
RFL1P10	TO-205AF	RFL1P10

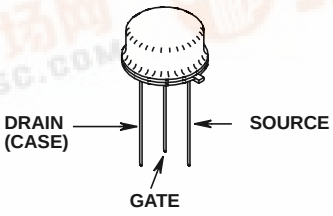
NOTE: When ordering, include the entire part number.

Symbol



Packaging

JEDEC TO-205AF



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFL1P08	RFL1P10	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	-80	-100	V
Drain to Gate Voltage (R_{GS} = 20KΩ) (Note 1)	V_{DGR}	-80	-100	V
Continuous Drain Current	I_D	1	1	A
Pulsed Drain Current (Note 3)	I_{DM}	5	5	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^oC

AUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFL1P08	BV_{DSS}	I_D = 250μA, V_{GS} = 0	-80	-	-	V
RFL1P10			-100			
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	-1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0, $T_C = 125^oC$			25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	-	±100	nA
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	I_D = 1A, V_{GS} = -10V	-	-	-3.65	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1A, V_{GS} = -10V (Figures 6, 7)	-	-	3.65	Ω
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx$ 1A, V_{DD} = -50V, R_G = 50Ω, V_{GS} = -10V, R_L = 47Ω (Figures 10, 11, 12)	-	7	25	ns
Rise Time	t_r		-	15	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	14	45	ns
Fall Time	t_f		-	11	25	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz (Figure 9)	-	-	150	pF
Output Capacitance	C_{OSS}		-	-	80	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	30	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	15	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = -1A	-	-	-1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = -1A, dI_{SD}/dt = 50A/μs	-	135	-	ns

NOTES:

2. Pulse test: pulse width ≤ 300μs maximum, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by mazimum junction temperature.

Typical Performance Curves Unless Otherwise Specified

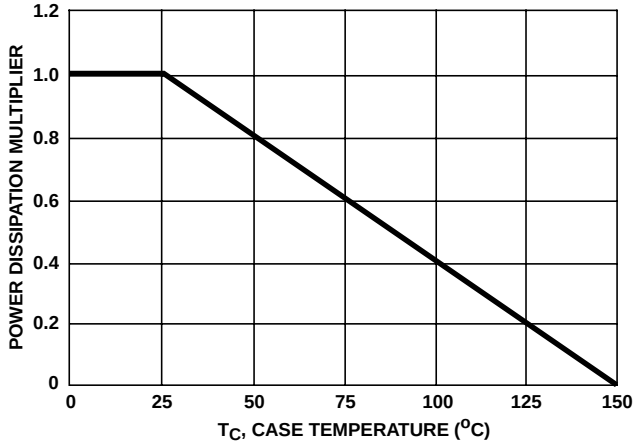


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

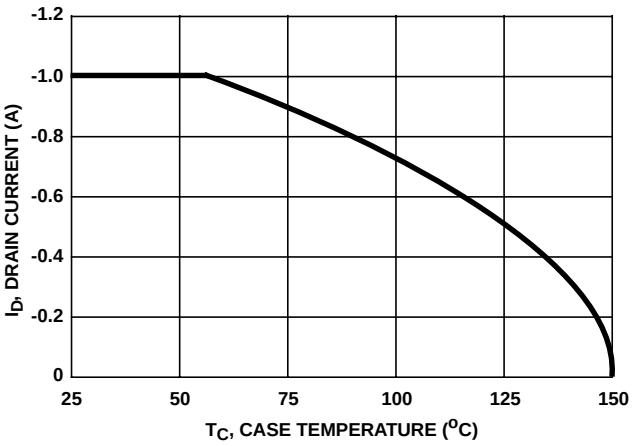


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

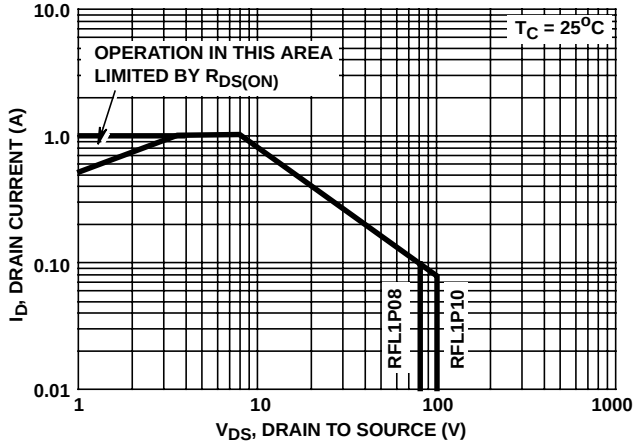


FIGURE 3. FORWARD BIAS OPERATING AREA

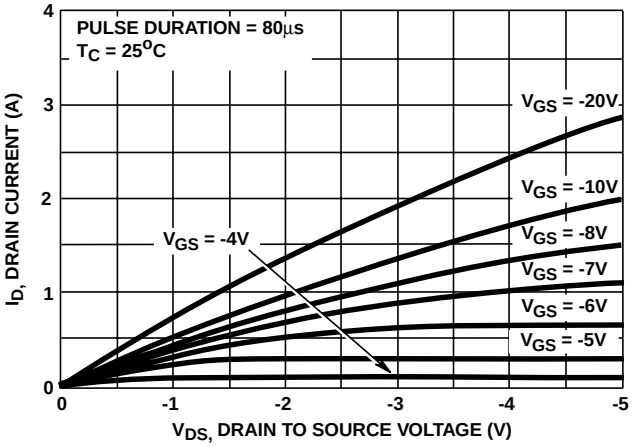


FIGURE 4. SATURATION CHARACTERISTICS

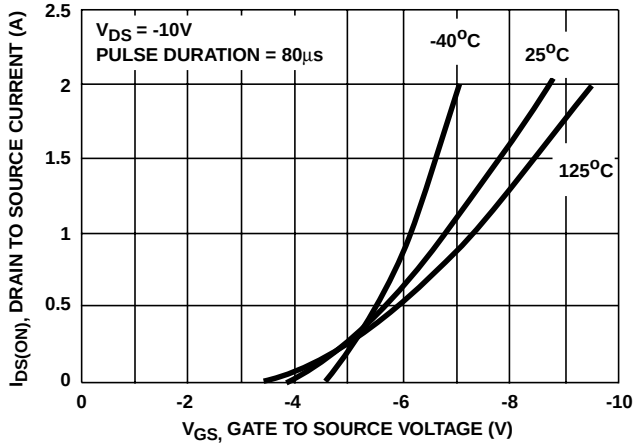


FIGURE 5. TRANSFER CHARACTERISTICS

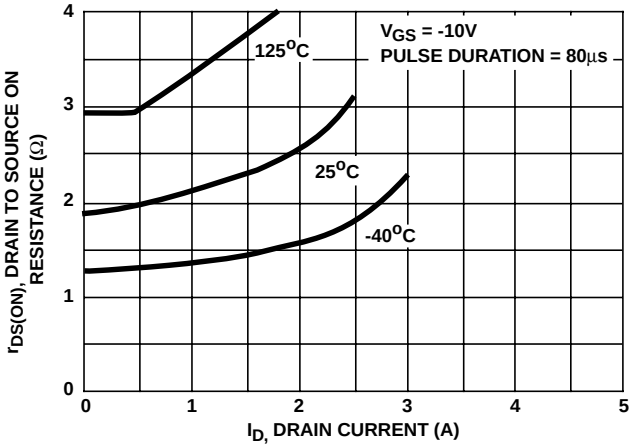


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

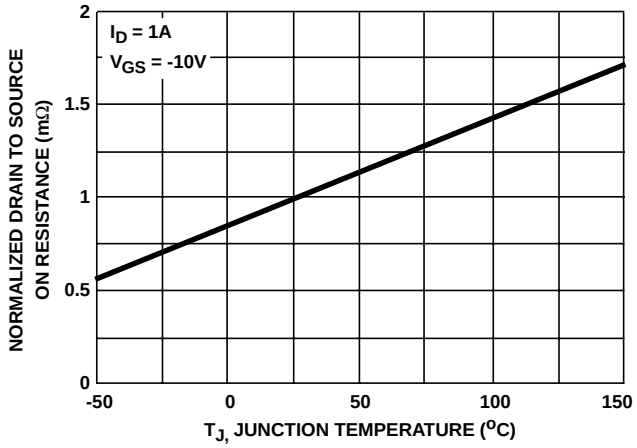


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

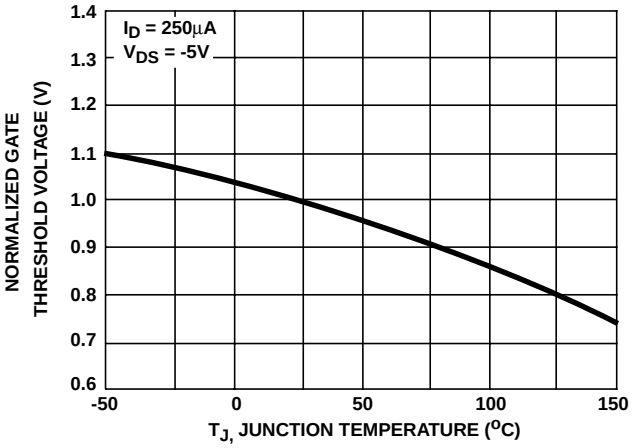


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

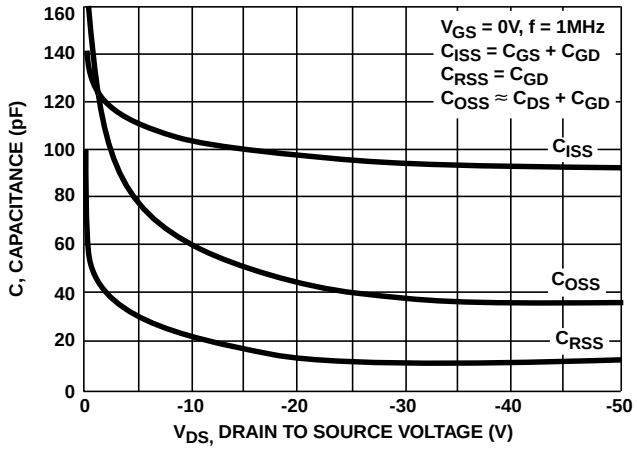
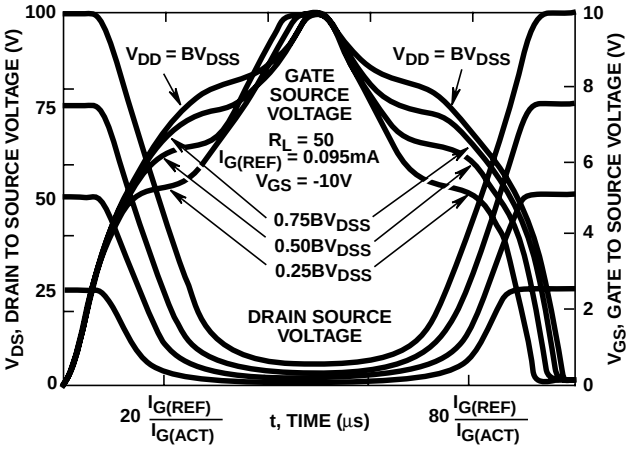


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

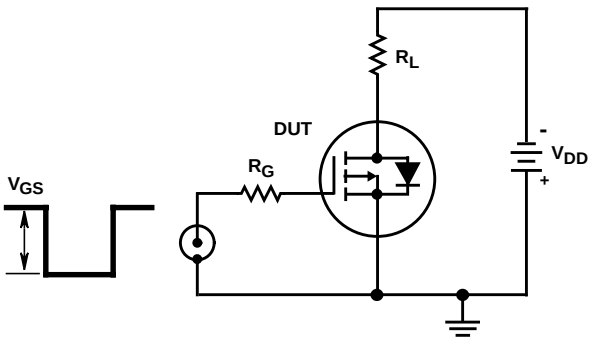


FIGURE 11. SWITCHING TIME TEST CIRCUIT

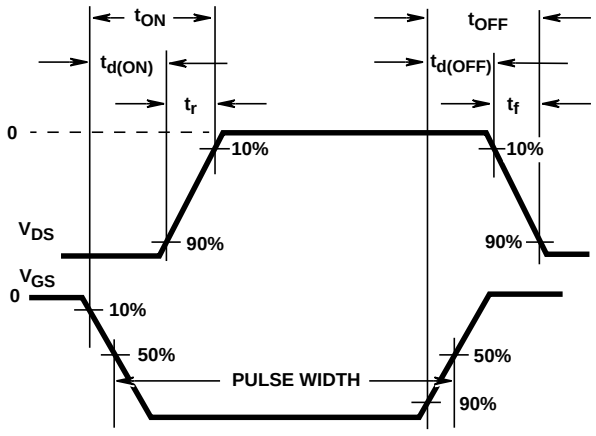


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS