intersil

Data Sheet July 1999 File Number 2881.2

2A, 200V, 3.500 Ohm, N-Channel Power MOSFET

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09289.

Ordering Information

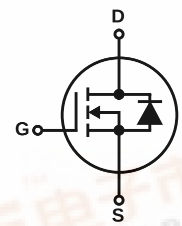
PART NUMBER	PACKAGE	BRAND
RFP2N20	TO-220AB	RFP2N20

NOTE: When ordering, include the entire part number.

Features

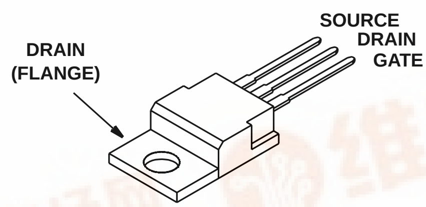
- 2A, 200V
- $r_{DS(ON)} = 3.500\Omega$

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings
$T_C = 25^oC$, Unless Otherwise Specified

		RFP2N20	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	200	V
Drain to Gate Voltage (RGS = 20kΩ) (Note 1)	V_{DGR}	200	V
Continuous Drain Current	I_D	2	A
Pulsed Drain Current (Note 3)	I_{DM}	5	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	25	W
Linear Derating Factor		0.2	W/ ^oC
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications
$T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0$	200	-	-	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$, (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}	-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 125^oC$	-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0$	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 2A$, $V_{GS} = 10V$, (Figures 6, 7)	-	-	3.500	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 2A$, $V_{GS} = 10V$	-	-	7.0	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx 1A$, $V_{DD} = 100V$, $R_G = 50\Omega$ $V_{GS} = 10V$, $R_L = 96.5\Omega$ (Figure 10)	-	15	25	ns
Rise Time	t_r		-	20	30	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	25	40	ns
Fall Time	t_f		-	15	25	ns
Input Capacitance	C_{ISS}	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1MHz, (Figure 9)	-	-	200	pF
Output Capacitance	C_{OSS}		-	-	60	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	25	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 1A$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 2A$, $dI_{SD}/dt = 50A/\mu s$	-	200	-	ns

NOTES:

2. Pulsed test: width ≤ 300µs duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

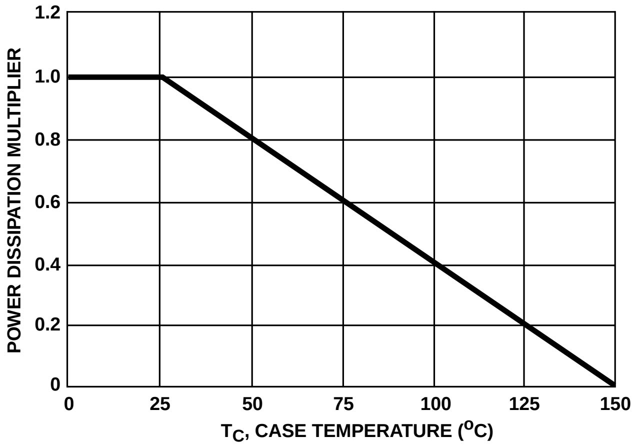


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

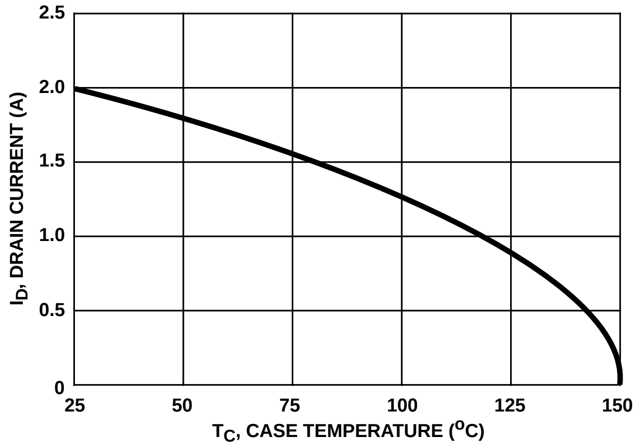


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

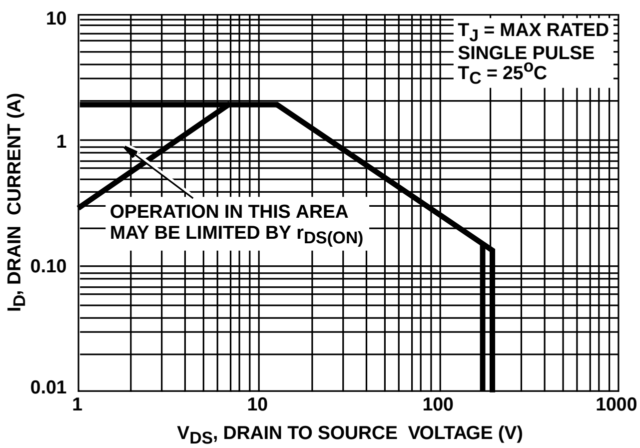


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

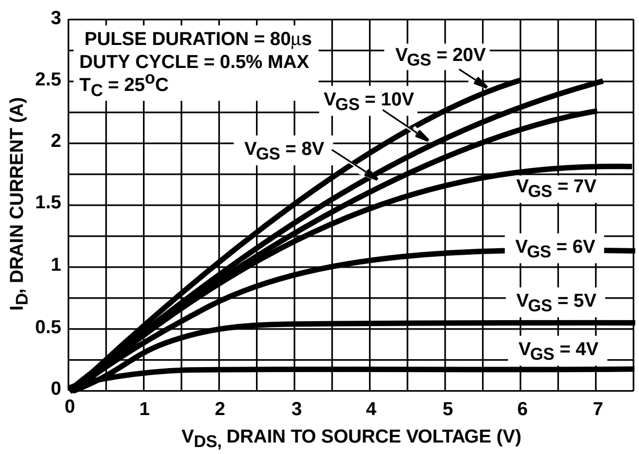


FIGURE 4. SATURATION CHARACTERISTICS

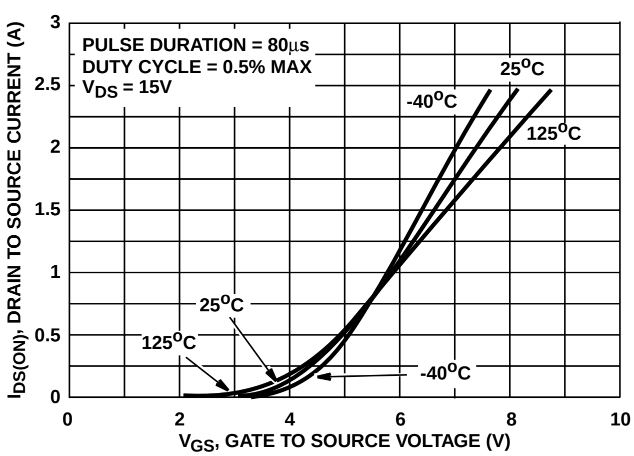


FIGURE 5. TRANSFER CHARACTERISTICS

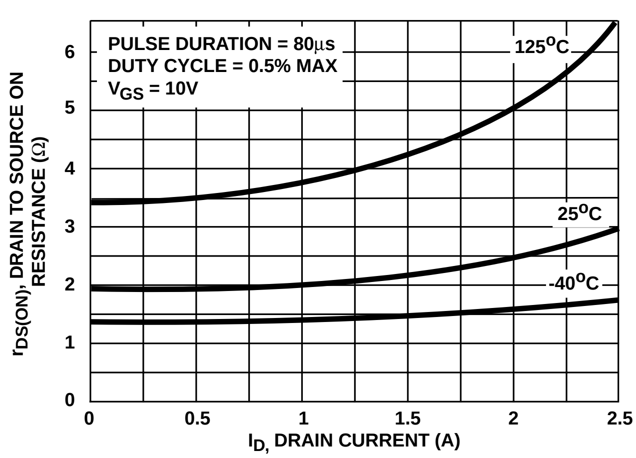


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

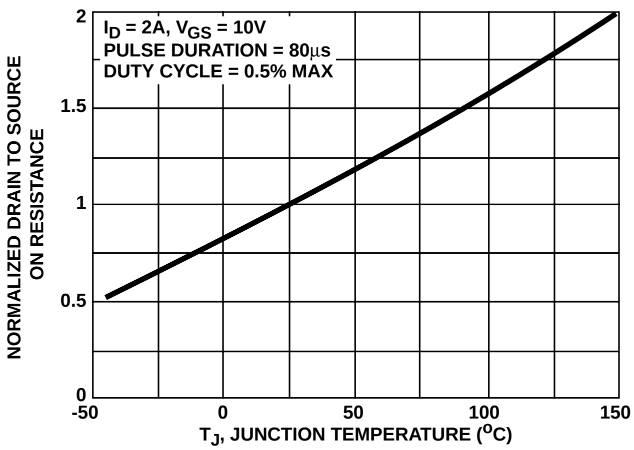


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

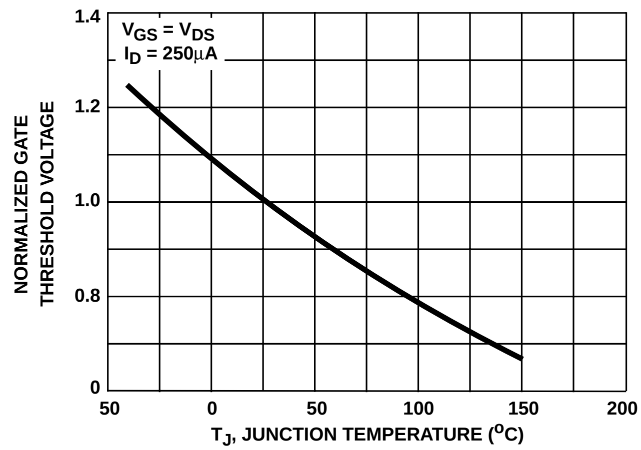


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

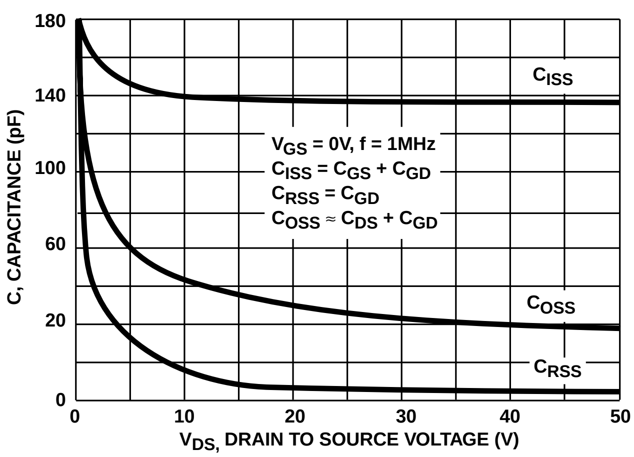
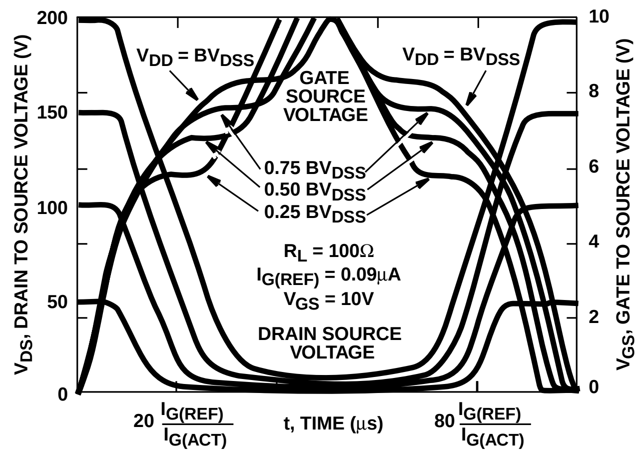


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Applications Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

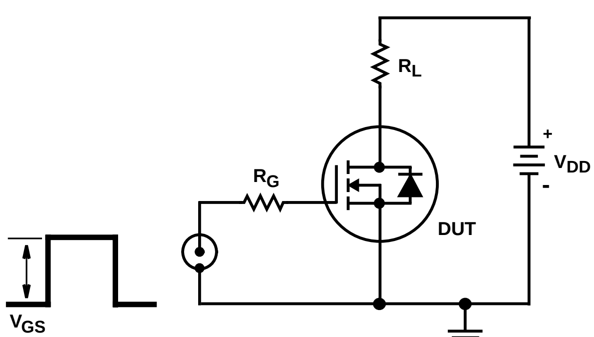


FIGURE 11. SWITCHING TIME TEST CIRCUIT

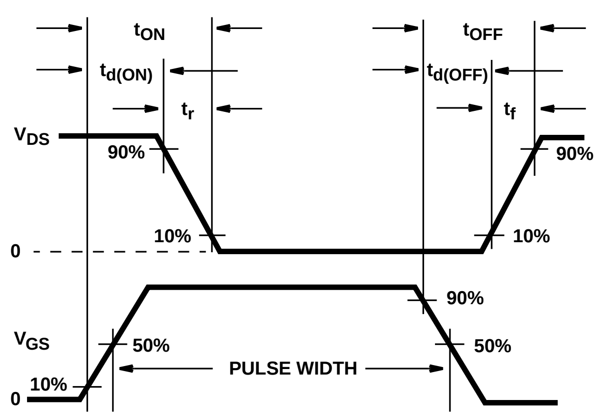


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms

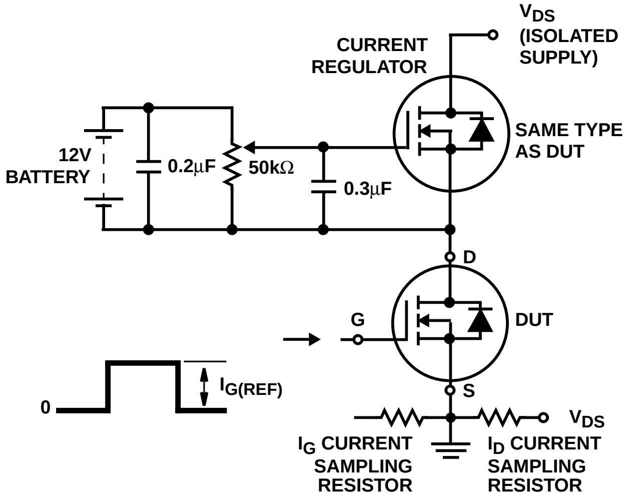


FIGURE 13. GATE CHARGE TEST CIRCUIT

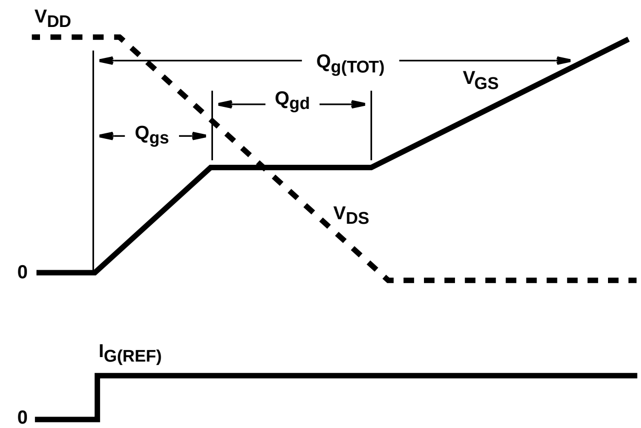


FIGURE 14. GATE CHARGE WAVEFORMS

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