



RFV10N50BE

10A, 500V, Fast Switching N-Channel Enhancement-Mode Power MOSFETs

August 1995

Features

- 10A, 500V
- $r_{DS(ON)} = 0.480\Omega$
- Very Fast Turn-Off Characteristics
- Nanosecond Switching Speeds
- Electrostatic Discharge Protected
- UIS Rating Curve
- SOA is Power Dissipation Limited
- High Input Impedance

Description

The RFV10N50BE is an N-Channel fast switching MOSFET transistor that is designed for switching regulators, inverters and motor drivers. The RFV10N50BE is a monolithic structure incorporating a high voltage, high current MOSFET, a control MOSFET and ESD protection diodes. As indicated in the symbol to the right, the turn-on of the main MOSFET is controlled by Gate 1 (G_1). The control MOSFET, controlled by Gate 2 (G_2), is distributed throughout the structure. Gate 2 provides a very low impedance and inductive path to rapidly discharge the gate of the main MOSFET. Gate 2 affords very fast turn-off (typically less than 25ns) when desired. A separate return connection, Source Kelvin (S_K), is supplied for the gate drive circuit to avoid voltage induced transients from the output circuit during switching. The RFV10N50BE can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

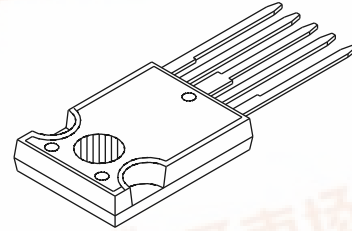
PART NUMBER	PACKAGE	BRAND
RFV10N50BE	TO-247	V10N50BE

NOTE: When ordering use the entire part number.

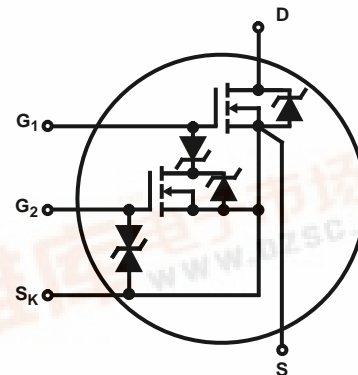
Formerly developmental type TA9881.

Package

JEDEC STYLE 5 LEAD TO-247



Terminal Diagram



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

		UNITS
Drain Source Voltage	V_{DSS}	500 V
Gate Source Voltage	V_{GS}	+14, -0.3 V
Control FET Gate Source Voltage	V_{GS}	+14, -0.3 V
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2 KV
Drain Current		
RMS Continuous	I_D	10 A
Pulsed Drain Current	I_{DM}	25 A
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve
Control FET Avalanche Current	I_{AS}	1.5 A
Control FET Single Pulse Avalanche Rating	E_{AS}	50 mJ
Power Dissipation		
$T_C = +25^\circ\text{C}$	P_D	156 W
Derate Above $+25^\circ\text{C}$		1.25 W/ $^\circ\text{C}$
Control FET Power Dissipation		
$T_C = +25^\circ\text{C}$	P_D	21 W
Derate Above $+25^\circ\text{C}$		0.17 W/ $^\circ\text{C}$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150 $^\circ\text{C}$

Specifications RFV10N50BE

Electrical Specifications Case Temperature (T_C) = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage	BV _{DSS}	I _D = 0.25mA, V _{GS} = 0V	500	-	-	V	
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 0.25mA	2	-	4	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500V, V _{GS} = 0V	T _C = +25°C	-	-	1	μA
			T _C = +125°C	-	-	250	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = +12V, V _{DS} = -0.3V	-	-	±500	nA	
On Resistance	r _{DS(ON)}	I _D = 10A, V _{GS} = 10V	-	-	0.480	Ω	
Turn-On Time	t _{ON}	V _{DD} = 250V, I _D = 10A, R _L = 25Ω, V _{GS1} = V _{GS2} = +10V, R _{GS1} = 6.25Ω, R _{GS2} = 20Ω	-	-	75	ns	
Turn-On Delay Time	t _{D(ON)}		-	20	-	ns	
Rise Time	t _R		-	30	-	ns	
Turn-Off Delay Time	t _{D(OFF)}		-	21	-	ns	
Fall Time	t _F		-	5	-	ns	
Turn-Off Time	t _{OFF}		-	-	50	ns	
Total Gate Charge	Q _{G10}		V _{GS} = 0V to 10V	V _{DD} = 400V, I _D = 10A, R _L = 40Ω	-	145	190
Gate Source Charge	Q _{GS}		-		17	22	nC
Gate Drain ("Miller") Charge	Q _{GD}		-		57	74	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz	-	3800	-	pF	
Output Capacitance	C _{OSS}		-	290	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	75	-	pF	
Thermal Resistance	R _{θJC}	Junction to Case	-	-	0.8	°C/W	
Thermal Resistance	R _{θJA}	Junction to Ambient	-	-	40	°C/W	

Control FET Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Static Drain to Source	r _{DS(ON)}	V _{GS} = 10V, I _D = 1.0A	-	1.6	-	Ω
Drain Source Breakdown Voltage	BV _{DSS}	I _D = 1.0mA, V _{GS} = 0V	14	15	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 0.25mA	2	-	4	V
Total Gate Charge	Q _{G10}	I _D = 1.0A, V _{GS} = 10V	-	-	5	nC

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Continuous Source Current	I _S		-	-	10	A
Pulsed Source Current	I _{SM}		-	-	25	A
Forward Voltage	V _{SD}	I _{SD} = 10A, V _{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t _{RR}	I _{SD} = 10A, V _{GS} = 0V, dI _{SD} /dt = 100A/μs	-	-	750	ns

RFV10N50BE

Typical Performance Curves

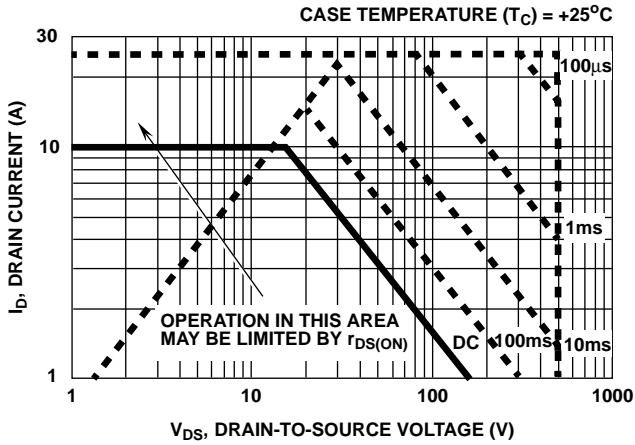


FIGURE 1. SAFE OPERATING AREA CURVE

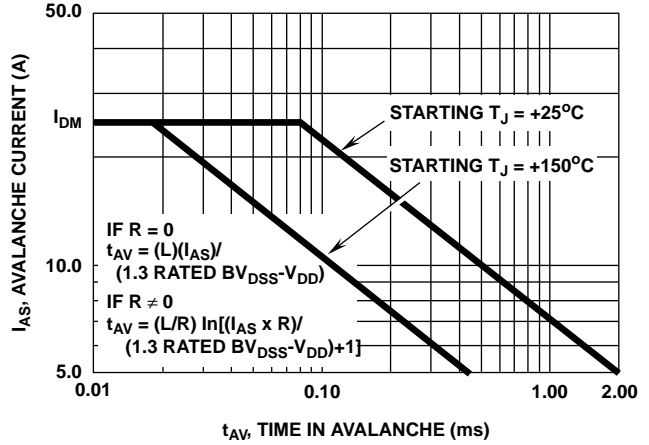


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

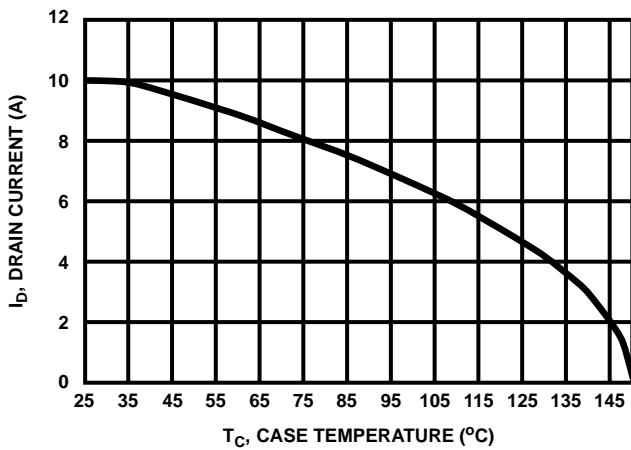


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

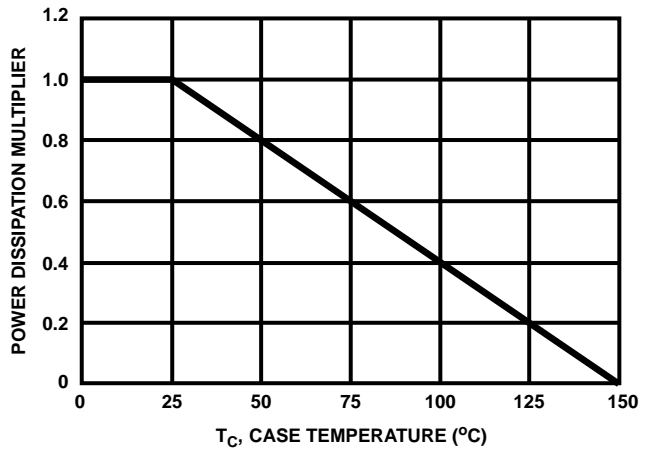


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

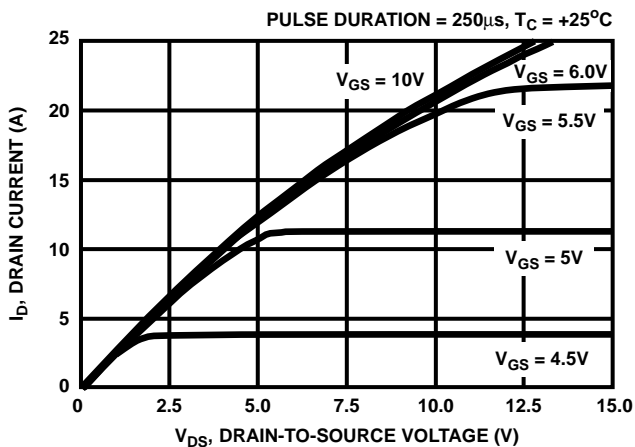


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

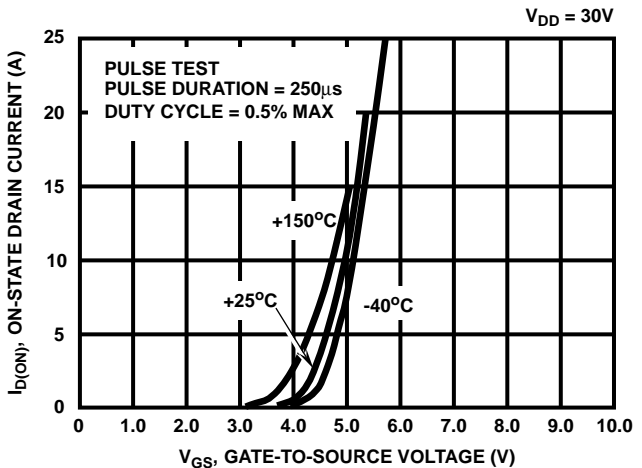


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

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Typical Performance Curves (Continued)

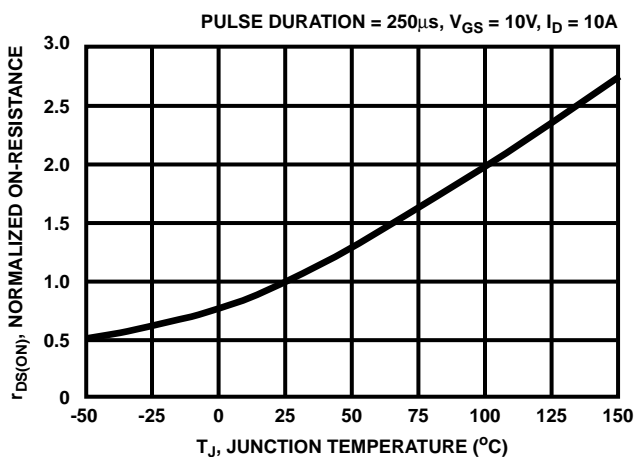


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs JUNCTION TEMPERATURE

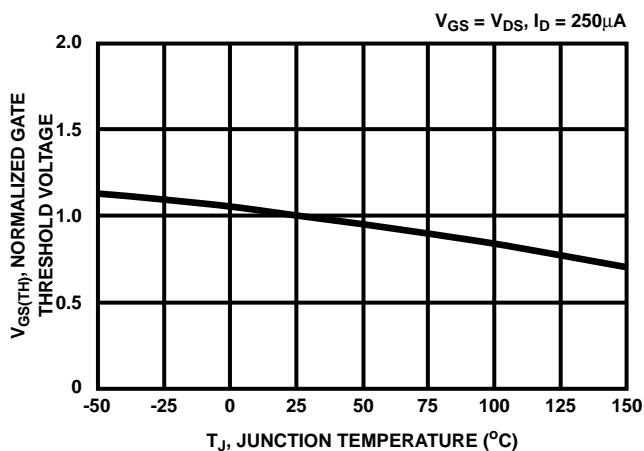


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

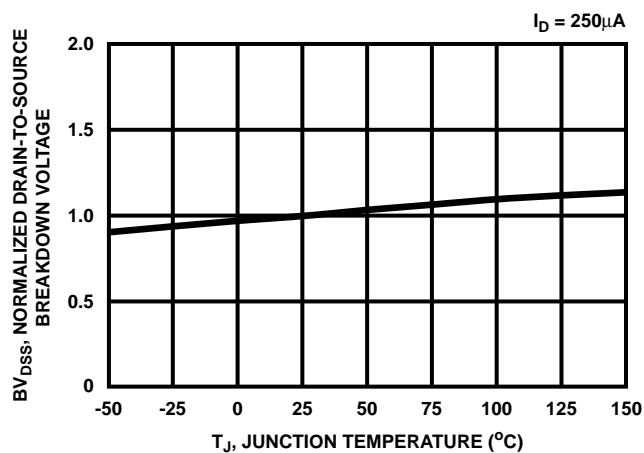


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

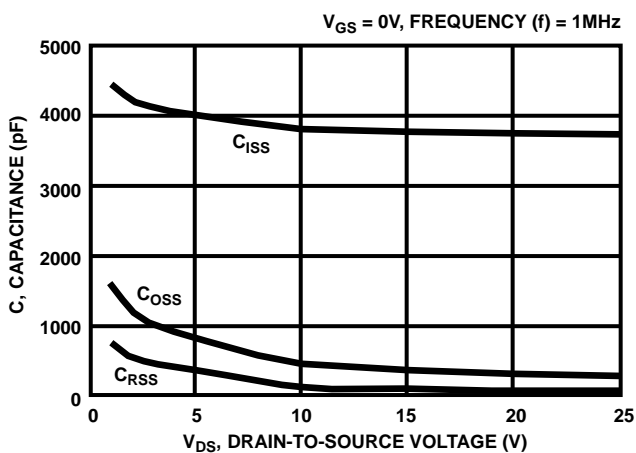


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

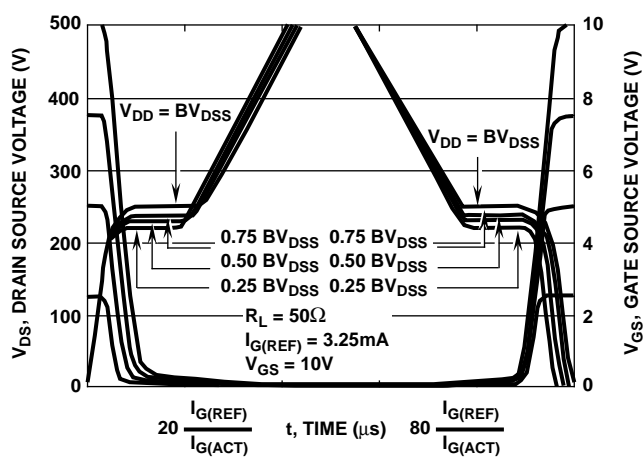


FIGURE 11. TYPICAL SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

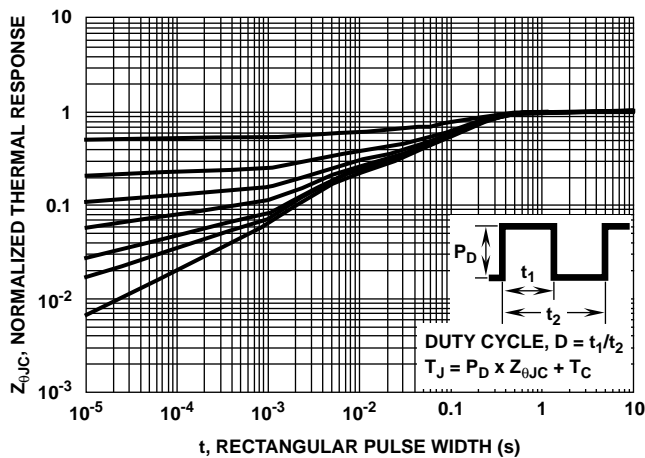


FIGURE 12. MAXIMUM NORMALIZED TRANSIENT THERMAL IMPEDANCE

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Test Circuits and Waveforms

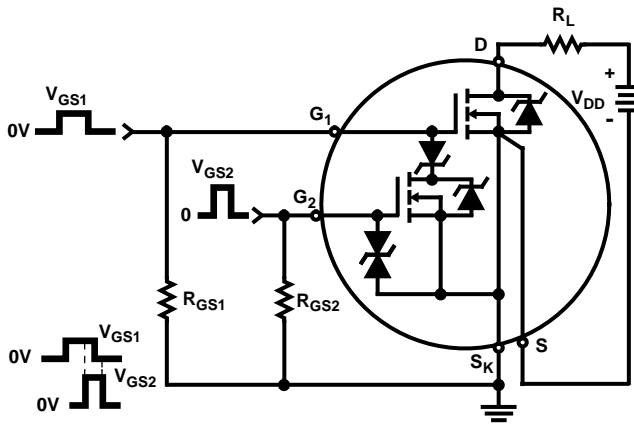


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUITS

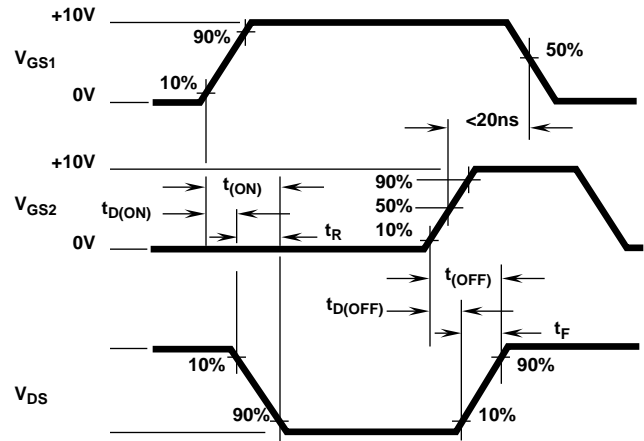
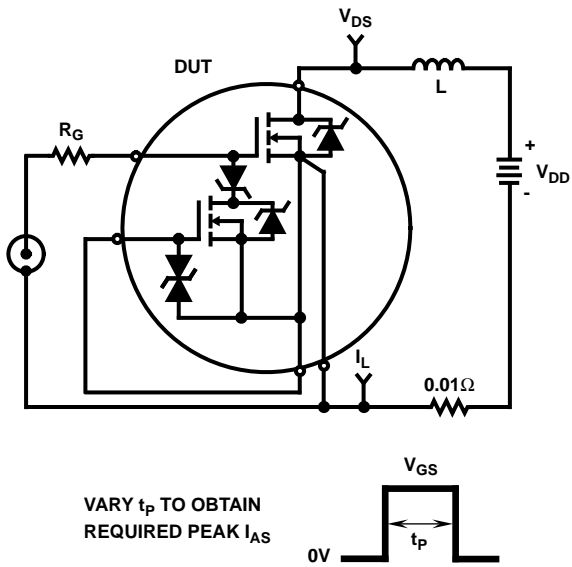


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS



VARY t_p TO OBTAIN
REQUIRED PEAK I_{AS}

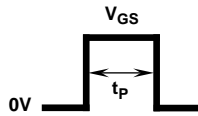


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

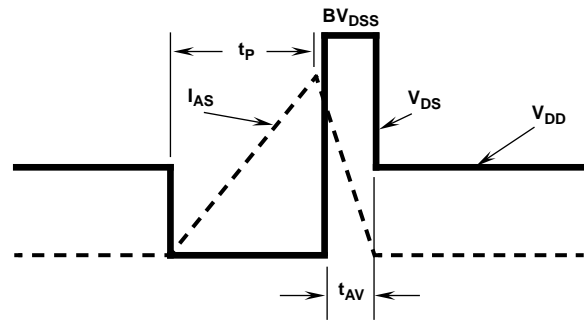
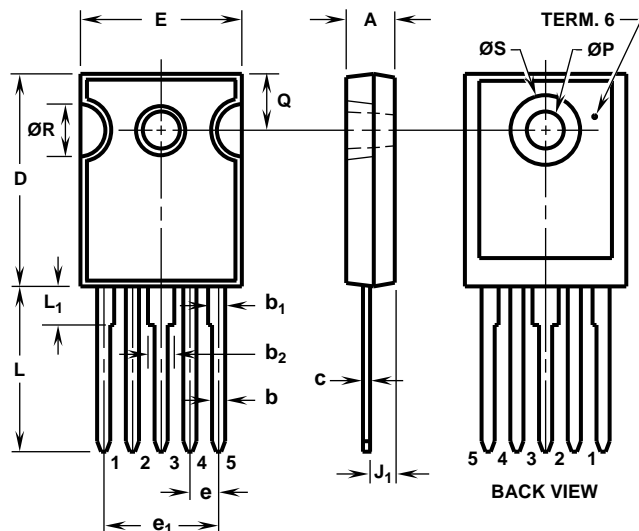


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

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Packaging



TERMINAL CONNECTIONS

- Lead No. 1 - Gate 1 (G_1)
- Lead No. 2 - Gate 2 (G_2)
- Lead No. 3 and Mounting Flange - Drain (D)
- Lead No. 4 - Source Kelvin (S_K)
- Lead No. 5 - Source (S)

TO-247

5 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.110 TYP		2.79 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

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UNITED STATES

Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE

Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

