RHR1K160D

Data Sheet | **January 2000** | **File Number 4788**

1A, 600V Hyperfast Dual Diode

The RHR1K160D is a hyperfast dual diode with soft recovery characteristics (t_{rr} < 25ns). It has about half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

Formerly developmental type TA49185.

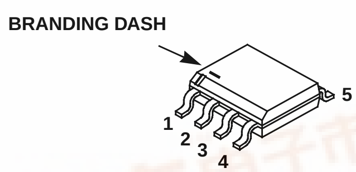
Ordering Information

PART NUMBER	PACKAGE	BRAND
RHR1K160D	MS-012AA	RHR1K160D

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RHR1K160D96.

Packaging

JEDEC MS-012AA



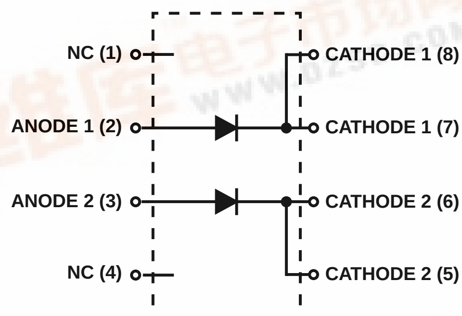
Features

- Hyperfast with Soft Recovery . . . . <25ns
- Operating Temperature. . . . . .150^{o}C
- Reverse Voltage 600V
- *Thermal Impedance* SPICE® Model
- *Thermal Impedance* SABER© Model
- Avalanche Energy Rated
- Planar Construction
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Symbol



Absolute Maximum Ratings (Per Leg) T_A = 25^{o}C, Unless Otherwise Specified

		RHR1K160D	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	600	V
Working Peak Reverse Voltage	V_{RWM}	600	V
DC Blocking Voltage	V_R	600	V
Average Rectified Forward Current T_A = 65^{o}C	$I_{F(AV)}$	1	A
Repetitive Peak Surge Current Square Wave, 20kHz	I_{FRM}	2	A
Nonrepetitive Peak Surge Current Halfwave, 1 phase, 60Hz	I_{FSM}	10	A
Maximum Power Dissipation (Note 1)	P_D	2.5	W
Avalanche Energy (See Figures 11 and 12)	E_{AVL}	5	mJ
Operating and Storage Temperature	T_{STG}, T_J	-55 to 150	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

Electrical Specifications (Per Leg) $T_A = 25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	$I_F = 1A$	-	-	2.1	V
	$I_F = 1A$, $T_A = 150^oC$	-	-	1.7	V
I_R	$V_R = 600V$	-	-	100	μA
	$V_R = 600V$, $T_A = 150^oC$	-	-	500	μA
t_{rr}	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	-	25	ns
t_a	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	10.5	-	ns
t_b	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	5	-	ns
Q_{RR}	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	20	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	10	-	pf
$R_{\theta JA}$	Pad Area = 0.483 in^2 (Note 1)	-	-	50	$^oC/W$
	Pad Area = 0.027 in^2 (Note 2) (Figure 13)	-	-	201	$^oC/W$
	Pad Area = 0.006 in^2 (Note 2) (Figure 13)	-	-	239	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{rr} = Reverse recovery time (See Figure 10), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current (See Figure 10).

t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 10).

Q_{rr} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JA}$ = Thermal resistance junction to ambient.

pw = Pulse width.

D = Duty cycle.

NOTES:

1. Measured using FR-4 copper board at 0.8 seconds.
2. 2. Measured using FR-4 copper board at 1000 seconds.

Typical Performance Curve

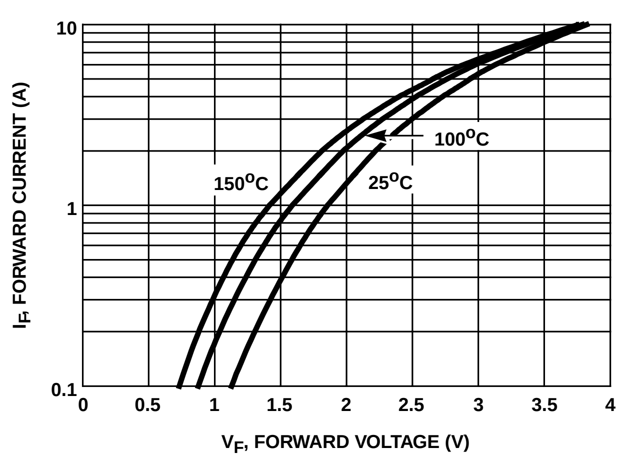


FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE

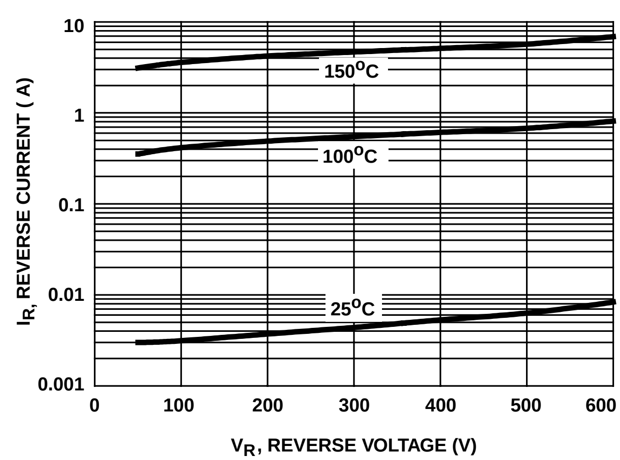


FIGURE 2. REVERSE CURRENT vs REVERSE VOLTAGE

Typical Performance Curve (Continued)

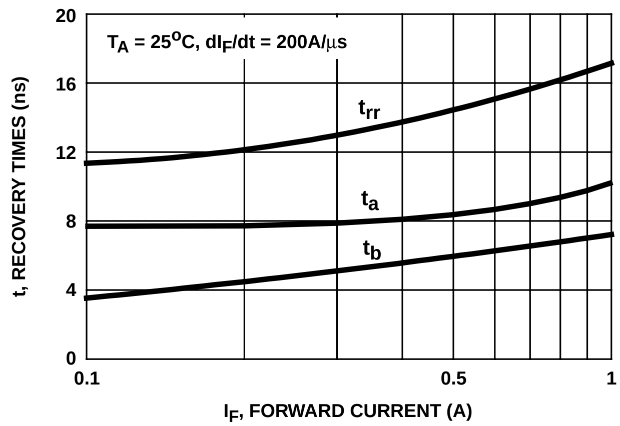


FIGURE 3. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

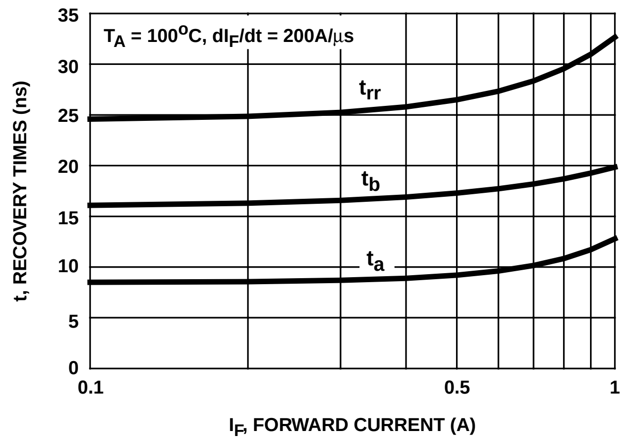


FIGURE 4. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

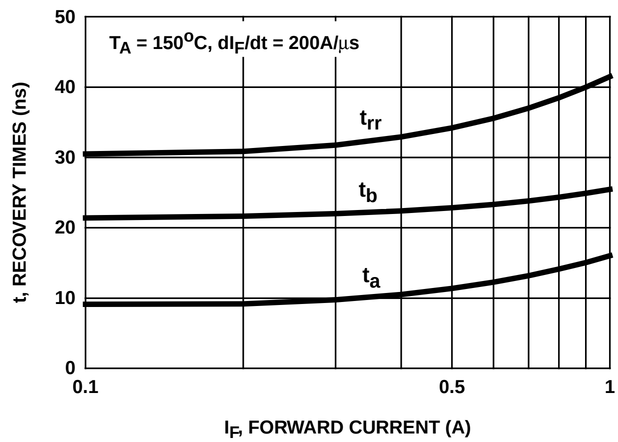


FIGURE 5. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

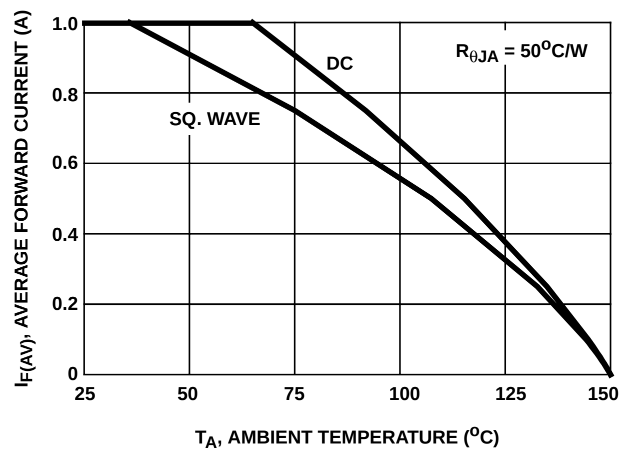


FIGURE 6. CURRENT DERATING CURVE

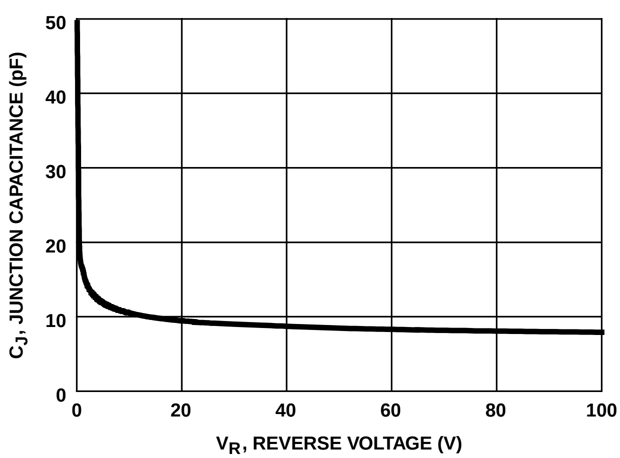


FIGURE 7. JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Typical Performance Curve **(Continued)**

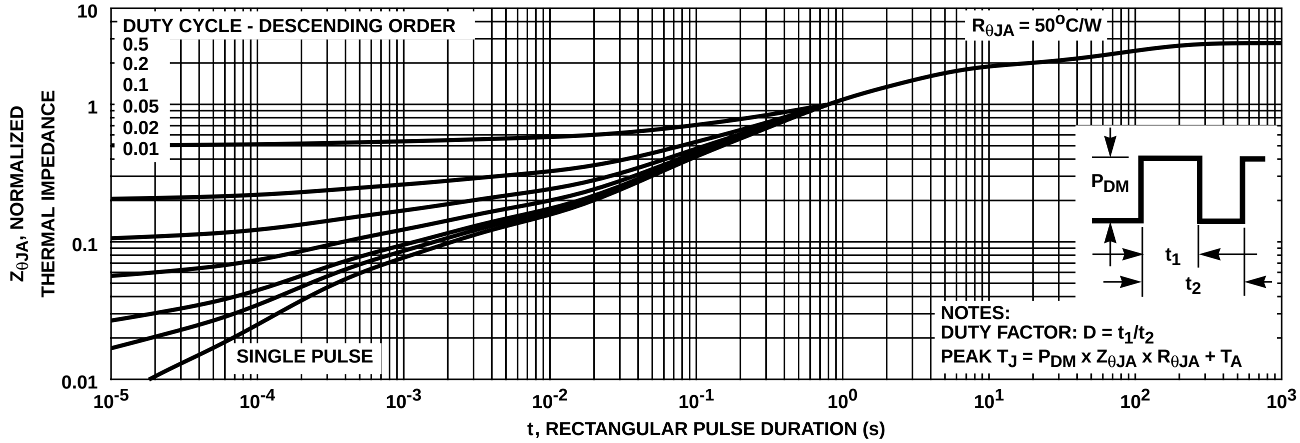


FIGURE 8. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

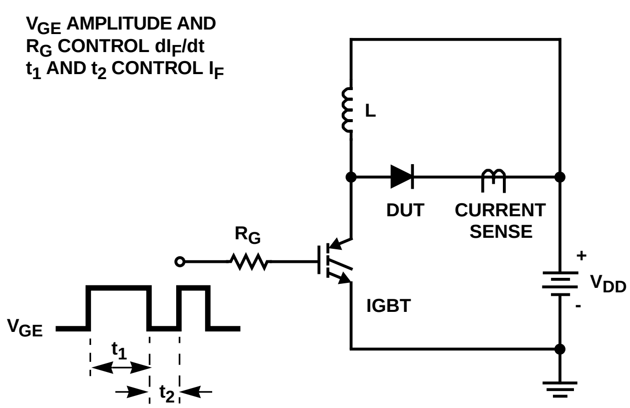


FIGURE 9. t_{rr} TEST CIRCUIT

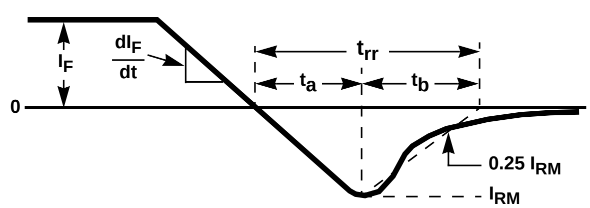


FIGURE 10. t_{rr} WAVEFORMS AND DEFINITIONS

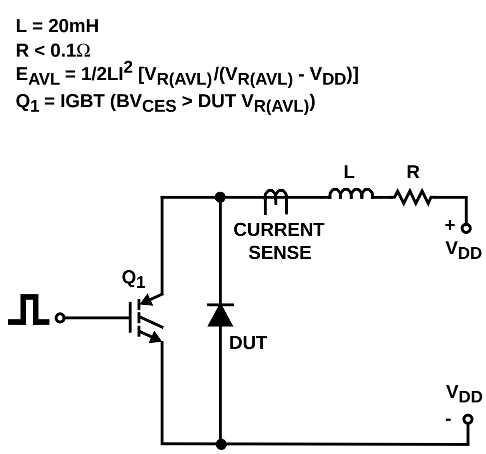


FIGURE 11. AVALANCHE ENERGY TEST CIRCUIT

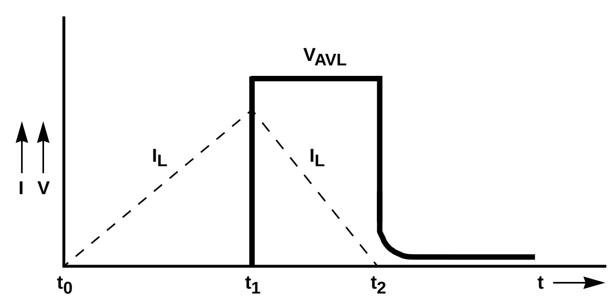


FIGURE 12. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

Thermal Resistance vs Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the SOP-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Intersil provides thermal information to assist the designer's preliminary application evaluation. Figure 13 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 2 oz. copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Intersil device SPICE thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

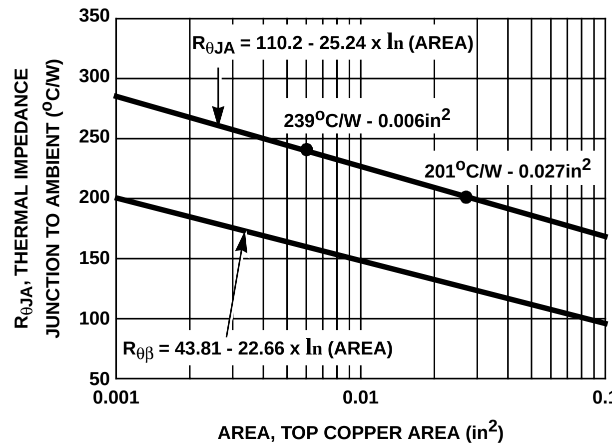


FIGURE 13. THERMAL RESISTANCE vs MOUNTING PAD AREA

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. These points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}. Thermal resistances corresponding to other component side copper areas can be obtained from Figure 13 or by calculation using Equation 2. The area, in square inches is the top copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

$$R_{\theta JA} = 110.18 - 25.24 \times \ln(\text{Area}) \quad \text{(EQ. 2)}$$

While Equation 2 describes the thermal resistance of a single die, the dual die SOP-8 package introduces an additional thermal component, thermal coupling resistance, $R_{\theta\beta}$. Equation 3 describes $R_{\theta\beta}$ as a function of the top copper mounting pad area.

$$R_{\theta\beta} = 43.81 - 22.66 \times \ln(\text{Area}) \quad \text{(EQ. 3)}$$

The thermal coupling resistance vs. copper area is also graphically depicted in Figure 13. It is important to note the thermal resistance ($R_{\theta JA}$) and thermal coupling resistance ($R_{\theta\beta}$) are equivalent for both die. For example at 0.1 square inches of copper:

$R_{\theta JA1} = R_{\theta JA2} = 168^oC/W$

$R_{\theta\beta 1} = R_{\theta\beta 2} = 96^oC/W$

T_{J1} and T_{J2} define the junction temperature of the respective die. Similarly, P_1 and P_2 define the power dissipated in each die. The steady state junction temperature can be calculated using Equation 4 for die 1 and Equation 5 for die 2.

Example: Use Equation 4 to calculate T_{J1} and Equation 5 to calculate T_{J2} with the following conditions. Die 2 is dissipating 0.5W; die 1 is dissipating 0W; the ambient temperature is 60^{o}C; the package is mounted to a top copper area of 0.1 square inches per die.

$$T_{J1} = P_1 R_{\theta JA} + P_2 R_{\theta \beta} + T_A \quad \text{(EQ. 4)}$$

$T_{J1} = (0W)(168^oC/W) + (0.5W)(96^oC/W) + 60^oC$

$T_{J1} = 108^oC$

$$T_{J2} = P_2 R_{\theta JA} + P_1 R_{\theta \beta} + T_A \quad \text{(EQ. 5)}$$

$T_{J2} = (0.5W)(168^oC/W) + (0W)(96^oC/W) + 60^oC$

$T_{J2} = 144^oC$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 14 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. SPICE and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM6 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

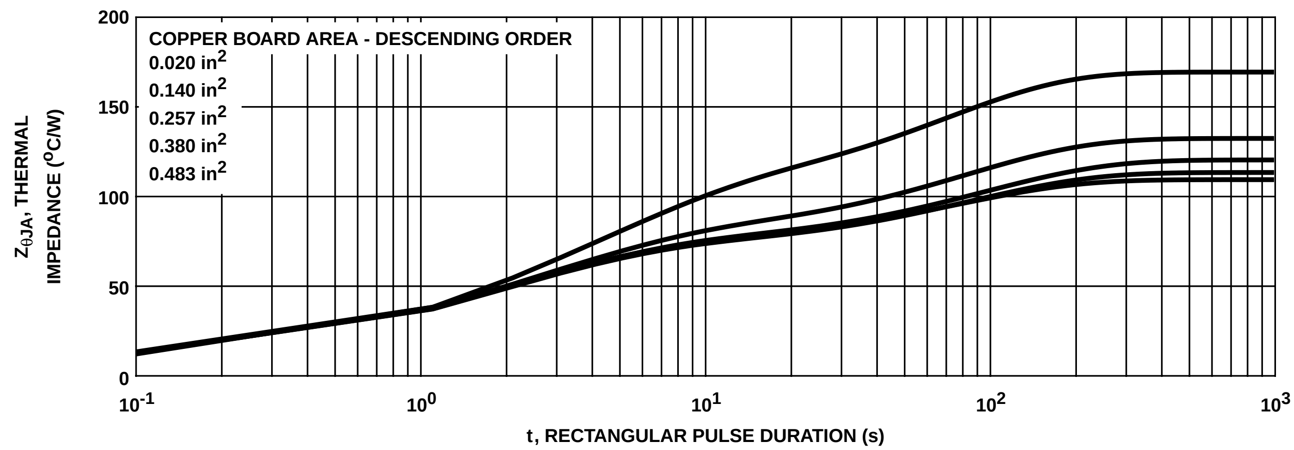
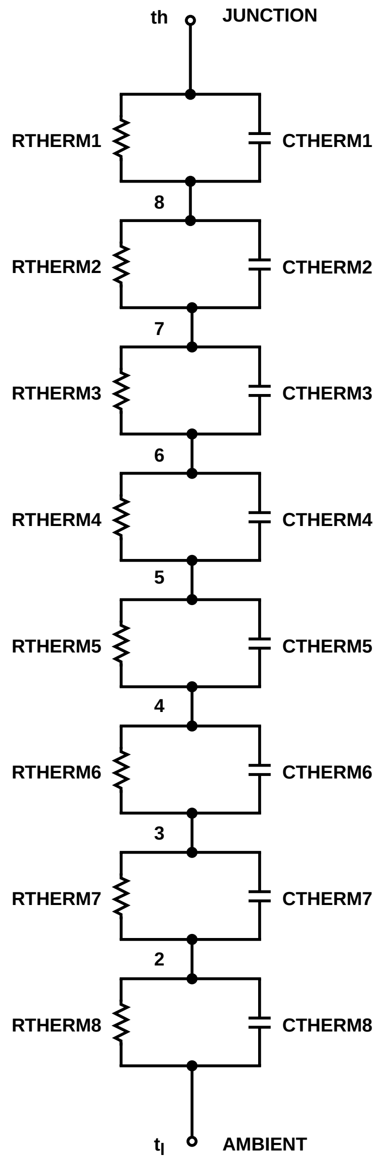


FIGURE 14. TRANSIENT THERMAL IMPEDANCE vs MOUNTING PAD AREA

SPICE Thermal Model

REV October 1998
RHR1K160D
Copper Area = 0.483 in^2
CTHERM1 th 8 6e-6
CTHERM2 8 7 4e-5
CTHERM3 7 6 1.5e-4
CTHERM4 6 5 7.5e-4
CTHERM5 5 4 7e-3
CTHERM6 4 3 2e-2
CTHERM7 3 2 8e-2
CTHERM8 2 tl 2.5

RTHERM1 th 8 5e-2
RTHERM2 8 7 2.5e-1
RTHERM3 7 6 1.5
RTHERM4 6 5 2.5
RTHERM5 5 4 7.5
RTHERM6 4 3 22
RTHERM7 3 2 38
RTHERM8 2 tl 38



SABER Thermal Model

Copper Area = 0.483 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 = 6e-6
ctherm.ctherm2 8 7 = 4e-5
ctherm.ctherm3 7 6 = 1.5e-4
ctherm.ctherm4 6 5 = 7.5e-4
ctherm.ctherm5 5 4 = 7e-3
ctherm.ctherm6 4 3 = 2e-2
ctherm.ctherm7 3 2 = 8e-2
ctherm.ctherm8 2 tl = 2.5

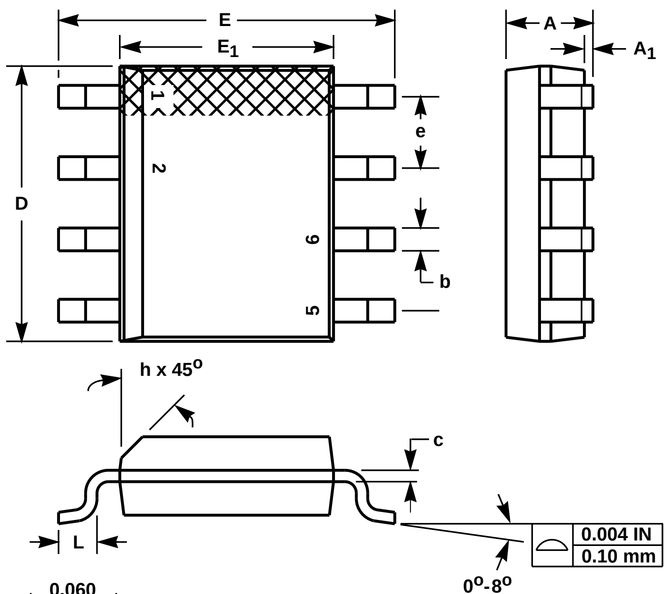
rtherm.rtherm1 th 8 = 5e-2
rtherm.rtherm2 8 7 = 2.5e-1
rtherm.rtherm3 7 6 = 1.5
rtherm.rtherm4 6 5 = 2.5
rtherm.rtherm5 5 4 = 7.5
rtherm.rtherm6 4 3 = 22
rtherm.rtherm7 3 2 = 38
rtherm.rtherm8 2 tl = 38
}

TABLE 1. THERMAL MODELS

COMPONENT	0.02 in^2	0.14 in^2	0.257 in^2	0.38 in^2	0.483 in^2
CTHERM7	7.5e-2	8e-2	8e-2	8e-2	8e-2
CTHERM8	1	1.5	2	2	2.5
RTHERM6	25	22	22	22	22
RTHERM7	65	45	40	38	38
RTHERM8	70	55	48	43	38

MS-012AA

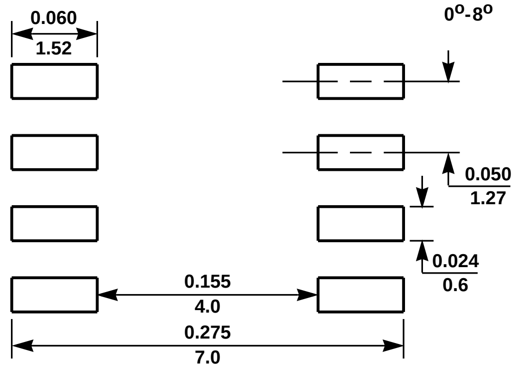
8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

NOTES:

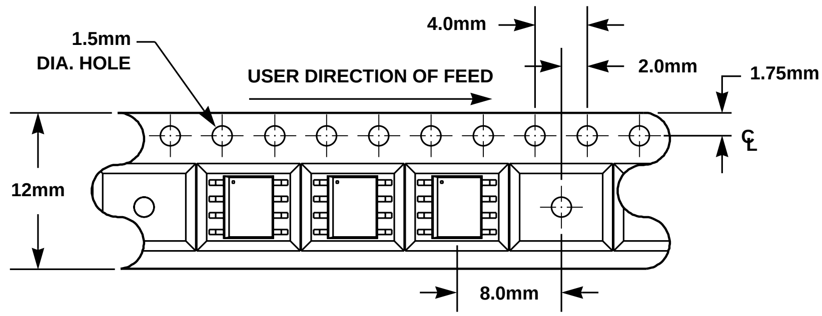
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension “E_1” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. “L” is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 8 dated 5-99.

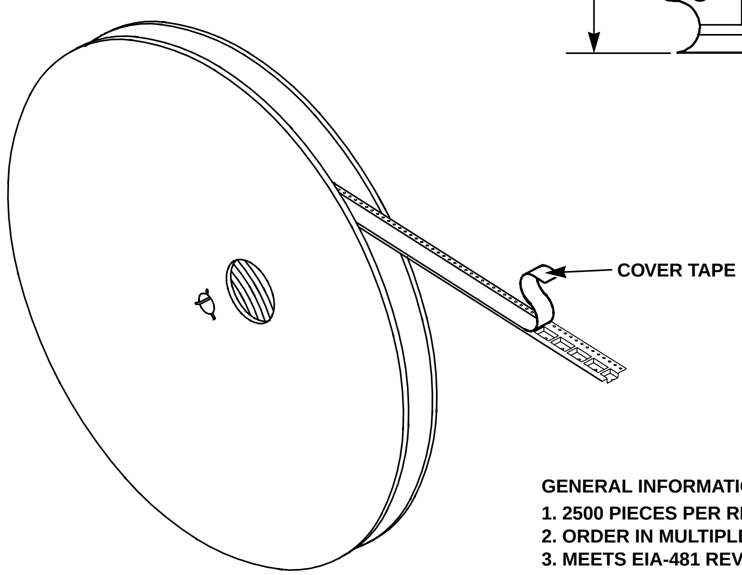


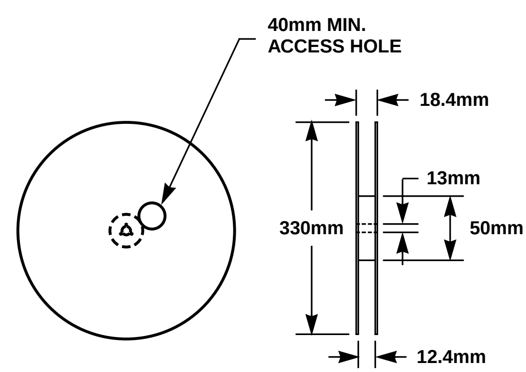
MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

MS-012AA

12mm TAPE AND REEL







GENERAL INFORMATION

1. 2500 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION “A” SPECIFICATIONS.

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
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EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029