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FAIRCHILD SEMICONDUCTOR®

May 2004

RMLA3565C

Wideband Low Noise MMIC Amplifier

General Description

The Fairchild Semiconductor's RMLA3565C is a single bias wideband low noise MMIC amplifier designed for the 3.5–6.5 GHz frequency range. The MMIC requires no external matching circuits or external gate bias supply. This device uses our advanced 0.25µm PHEMT process to provide low noise, high linearity, and low current.

Features

- 20dB Gain typical
- 1.2dB Noise Figure Typical 5.0–6.5GHz
- 4.0V Single Positive Bias
- Small Outline Metal Base Quad Plastic Package
- Internal 50Ω Matching

Device

Absolute Ratings

Symbol	Parameter	Ratings	Units
V_{dd}	Positive Drain DC Voltage	6.5	V
P_{IN} (CW)	RF Input Power (from 50Ω source)	0	dBm
I_{dd}	Drain Current	130	mA
T_{case}	Case Operating Temperature	-30 to 85	°C
$T_{storage}$	Storage Temperature Range	-40 to 110	°C
T_{solder}	Soldering Temperature	220	°C
R_{jc}	Thermal Resistance (Channel to Case)	8	°C/W

Electrical Characteristics (50Ω System, V_{dd} = 4V, T = +25°C)

Parameter	Min	Typ	Max	Units
Frequency Range	3.5		6.5	GHz
Gain (Small Signal)[1, 2]	17.0	20		dB
Gain Variation vs Temp		0.013		dB/C°
Noise Figure[2]				
3.5–5 GHz		1.5	2.2	dB
5–6.5 GHz		1.2	1.6	dB
Power Out, P-1dB	8.0	13		dBm
OIP3 @ 5.5 GHz, 0 dBm per tone Pout		25.5		dBm
Idd		80	90	mA
Vdd	3.0	4.0	6.0	V
Input/Output Return Loss		10.0		dB

Notes:
1. Pin = -20, V_d = 4.0V, Frequency 3.5–6.5Ghz
2. Data de-embedded from fixture loss.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

The following briefly describes a procedure for evaluating the high efficiency PHEMT amplifier packaged in a surface mount package. It may be noted that the chip is a fully monolithic single ended two stage amplifier for 3.5 to 6.5 GHz applications. Figure 1 shows the functional block diagram of the packaged product.

Test Fixture

Figure 2 shows the outline and pin-out descriptions for the packaged device. A typical test fixture schematic showing external bias components is shown in Figure 3. Figure 4 shows typical layout of an evaluation board corresponding to the schematic diagram. Typical performance of the test fixture is shown in the performance data section. The following should be noted:

(1) Package pin designations are shown in Figure 2.

(2) Vd is the drain voltage (positive) applied at the pins of the package.

(3) Vdd is the positive supply voltage at the evaluation board terminal.

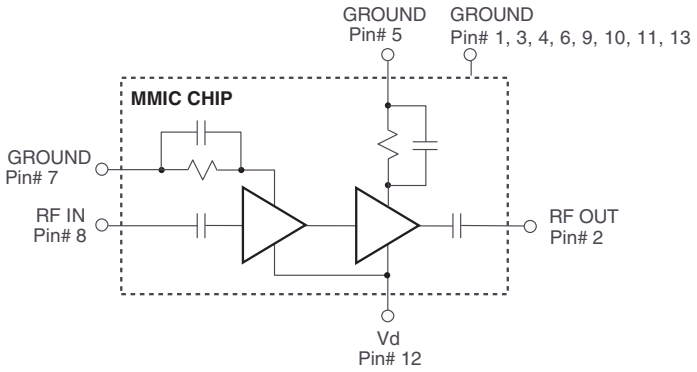
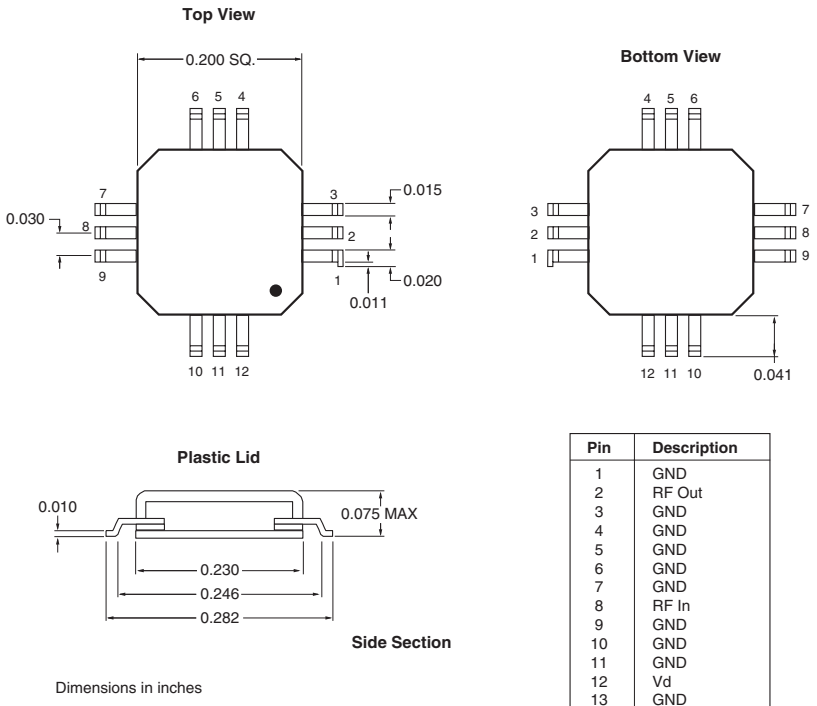


Figure 1. Functional Block Diagram



Pin	Description
1	GND
2	RF Out
3	GND
4	GND
5	GND
6	GND
7	GND
8	RF In
9	GND
10	GND
11	GND
12	Vd
13	GND (Package Base)

Figure 2. Package Outline Dimensions

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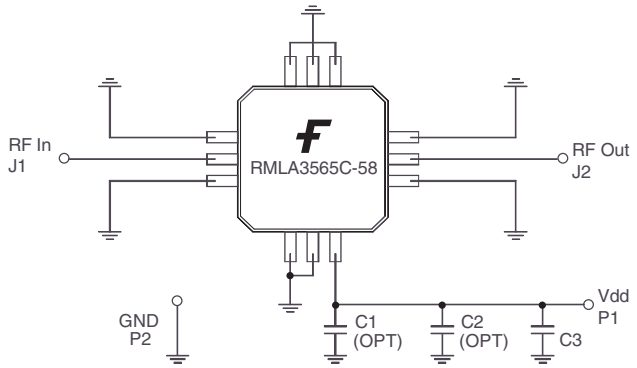


Figure 3. Schematic for a Typical Test Evaluation Board (RMLA3565C-TB)

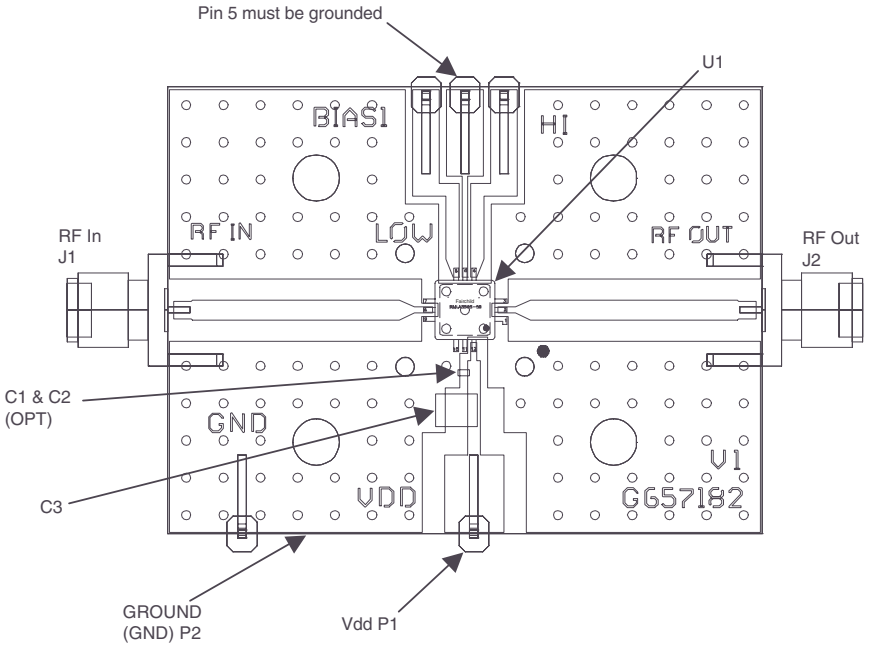


Figure 4. Layout and Assembly of Test Evaluation Board (RMLA3565C-TB)

Test Procedure for the evaluation board (RMLA3565C-TB)

The following sequence of procedure must be followed to properly test the power amplifier:

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board to connect DC supply grounds and Pin 5.

Step 3: Apply drain supply voltage of +4.0V to evaluation board terminal Vdd.

Step 4: After the bias condition is established, RF input signal may now be applied.

Step 5: Follow turn-off sequence of:

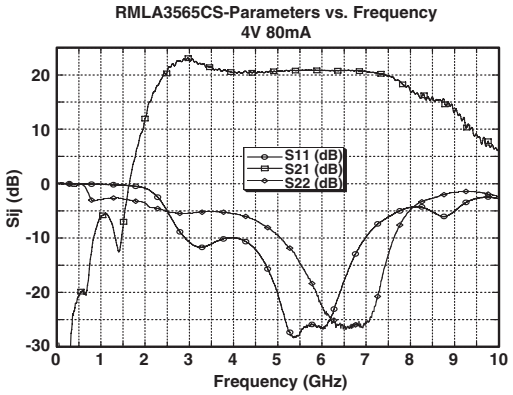
(i) Turn off RF input power.

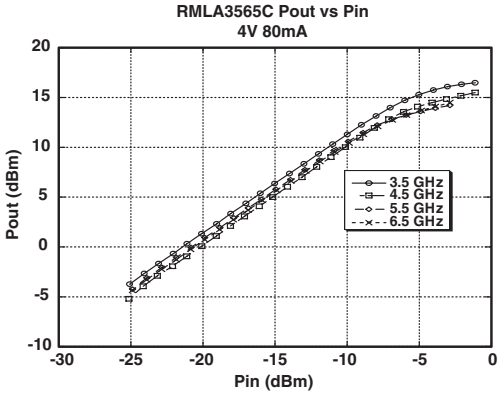
(ii) Turn down and off Vdd.

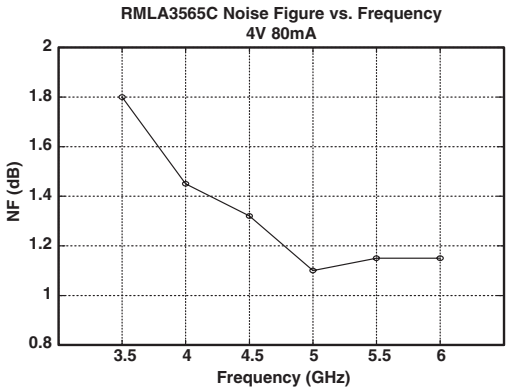
Parts List For Test Evaluation Board (RMLA3565C-TB)

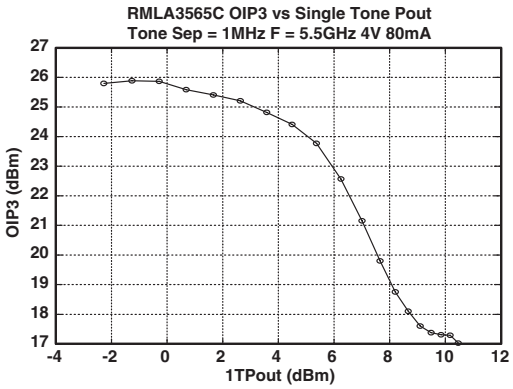
Part	Value	Size (EIA)	Vendor(s)
C1	330 pF	.04” x .02”	AVX, Murata, Novacap
C2	1000 pF	.04” x .02”	AVX, Murata, Novacap
C3	4.75 µF	.14” x .11”	Sprague, ATC, AVX, Murata
U1	RMLA3565C	.28” x .28” x .07”	Fairchild
P1, P2	Terminals		Samtec
J1, J2	SMA Connectors		E.F. Johnson
Board	RO4003 (Rogers)	1.99 x 1.50 x .032	Fairchild

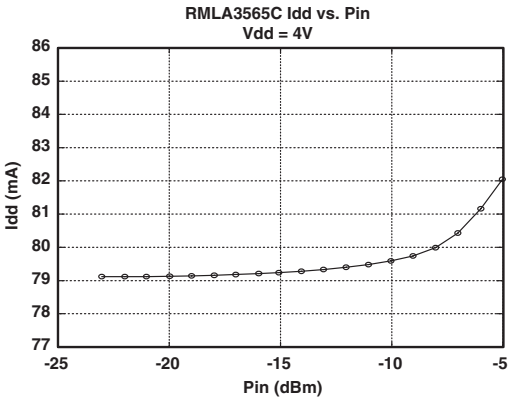
Typical Characteristics











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