FAIRCHILD SEMICONDUCTOR®

September 2004

RMPA1759

Korean-PCS PowerEdge™ Power Amplifier Module

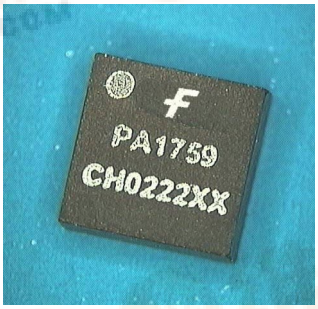
General Description

The RMPA1759 power amplifier module (PAM) is designed for Korean CDMA and CDMA2000-1X personal communications system (PCS) applications. The 2 stage PAM is internally matched to 50Ω to minimize the use of external components and features a low-power mode to reduce standby current and DC power consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) process.

Features

- Single positive-supply operation and low power and shutdown modes
- 38% CDMA efficiency at +28dBm average output power
- Compact LCC package- 4.0 x 4.0 x 1.5 mm with industry standard pinout
- Internally matched to 50Ω and DC blocked RF input/output.
- Meets CDMA2000-1XRTT performance requirements

Device

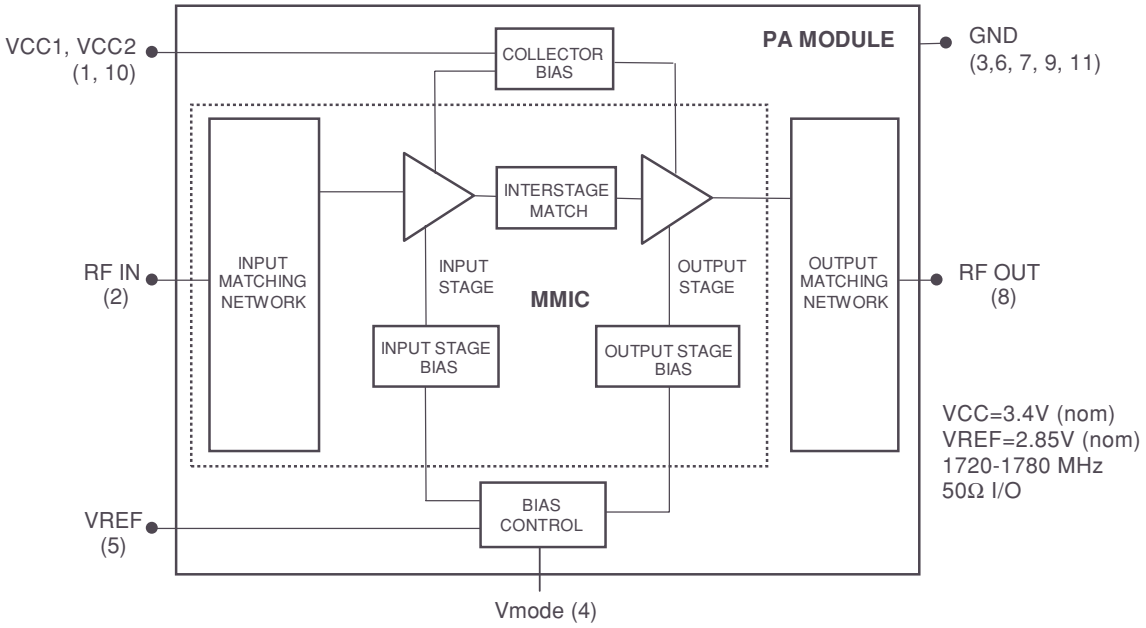


Absolute Ratings[1]

Symbol	Parameter	Value	Units
Vcc1, Vcc2	Supply Voltages	5.0	V
Vref	Reference Voltage	2.6 to 3.5	V
Vmode	Power Control Voltage	3.5	V
Pin	RF Input Power	+10	dBm
T_{STG}	Storage Temperature	-55 to +150	°C

Note:
1: No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Module Block Diagram



Electrical Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units	Comments
f	Operating Frequency	1720		1780	MHz	
CDMA Operation						
SSg	Small-Signal Gain		26		dB	Po = 0 dBm
Gp	Power Gain		27		dB	Po = +28 dBm; Vmode = 0V
Po	Linear Output Power	28 16			dBm dBm	Vmode = 0V Vmode ≥ 2.0V
PAEd	PAE (digital) @ +28 dBm		38		%	Vmode = 0V
	PAE (digital) @ +16 dBm		9		%	Vmode ≥ 2.0V
	PAEd (digital) @ +16 dBm		20		%	Vmode ≥ 2.0V, Vcc = 1.4V
Itot	High Power Total Current		490		mA	Po = +28 dBm, Vmode = 0V
	Low Power Total Current		120		mA	Po = +16 dBm, Vmode = 2.0V
	Adjacent Channel Power Ratio					
ACPR1	±1.25 MHz Offset		-50 -48		dBc dBc	Po = +28 dBm; Vmode = 0V, IS-95 Po = +28 dBm; Vmode = 0.0V, CDMA2000-1X
ACPR2	±2.25 MHz Offset		-60 -62		dBc dBc	Po = +28 dBm; Vmode = 0V, IS-95 Po = +28 dBm; Vmode = 0.0V, CDMA2000-1X
General Characteristics						
VSWR	Input Impedance		2.0:1			
NF	Noise Figure		4		dB	
Rx No	Receive Band Noise Power		-139		dBm/Hz	Po ≤ +28 dBm; 1920 to 1980 MHz
2fo-5fo	Harmonic Suppression			-30	dBc	Po ≤ +28 dBm
S	Spurious Outputs[2, 3]			-60	dBc	Load VSWR ≤ 5.0:1
	Ruggedness w/ Load Mismatch[3]			10:1		No permanent damage.
Tc	Case Operating Temperature	-30		85	°C	

Symbol	Parameter	Min	Typ	Max	Units	Comments
DC Characteristics						
Iccq	Quiescent Current		50		mA	Vmode ≥ 2.0V
Iref	Reference Current		5	8	mA	Po ≤ +28 dBm
Icc(off)	Shutdown Leakage Current		1	10	µA	No applied RF signal.

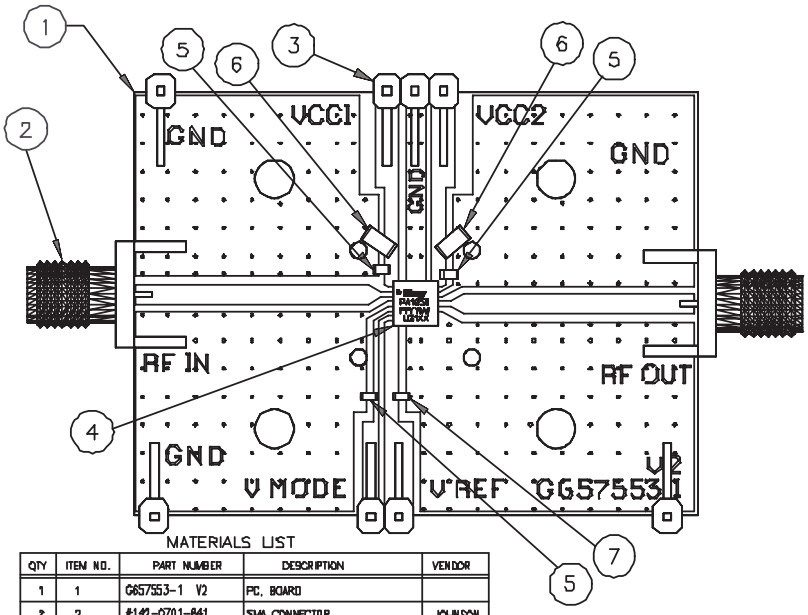
Notes:
1: All parameters met at Tc = +25°C, Vcc = +3.4V, f=1950 MHz and load VSWR ≤ 1.2:1.
2: All phase angles.
3: Guaranteed by design.

Recommend Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
f	Operating Frequency	1720		1780	MHz
Vcc1, Vcc2	Supply Voltage	3.0	3.4	4.2	V
Vref	Reference Voltage				
	(Operating)	2.7	2.85	3.1	V
	(Shutdown)	0		0.5	V
Vmode	Bias Control Voltage				
	(low-power)	1.8	2.0	3.0	V
	(high-power)	0		0.5	V
Pout	Linear Output Power				
	(high-power)			+28	dBm
	(low-power)			+16	dBm
Tc	Case Operating Temperature	-30		+85	°C

Note:
1: RF input power for CDMA Pout = +28dBm.

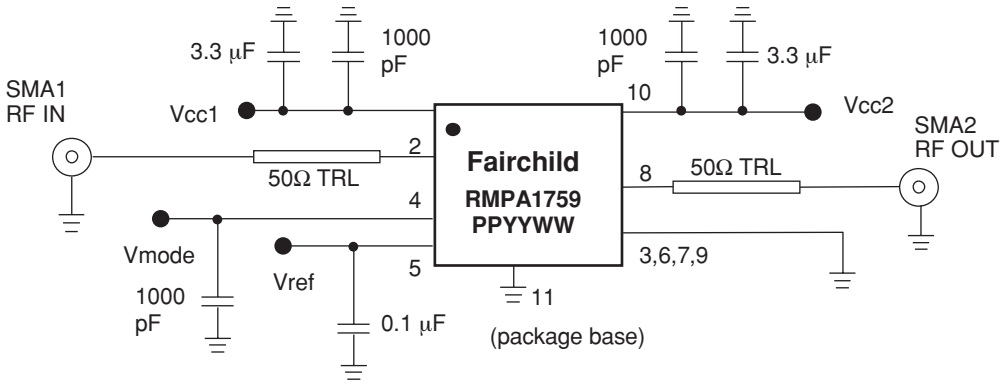
Evaluation Board Layout



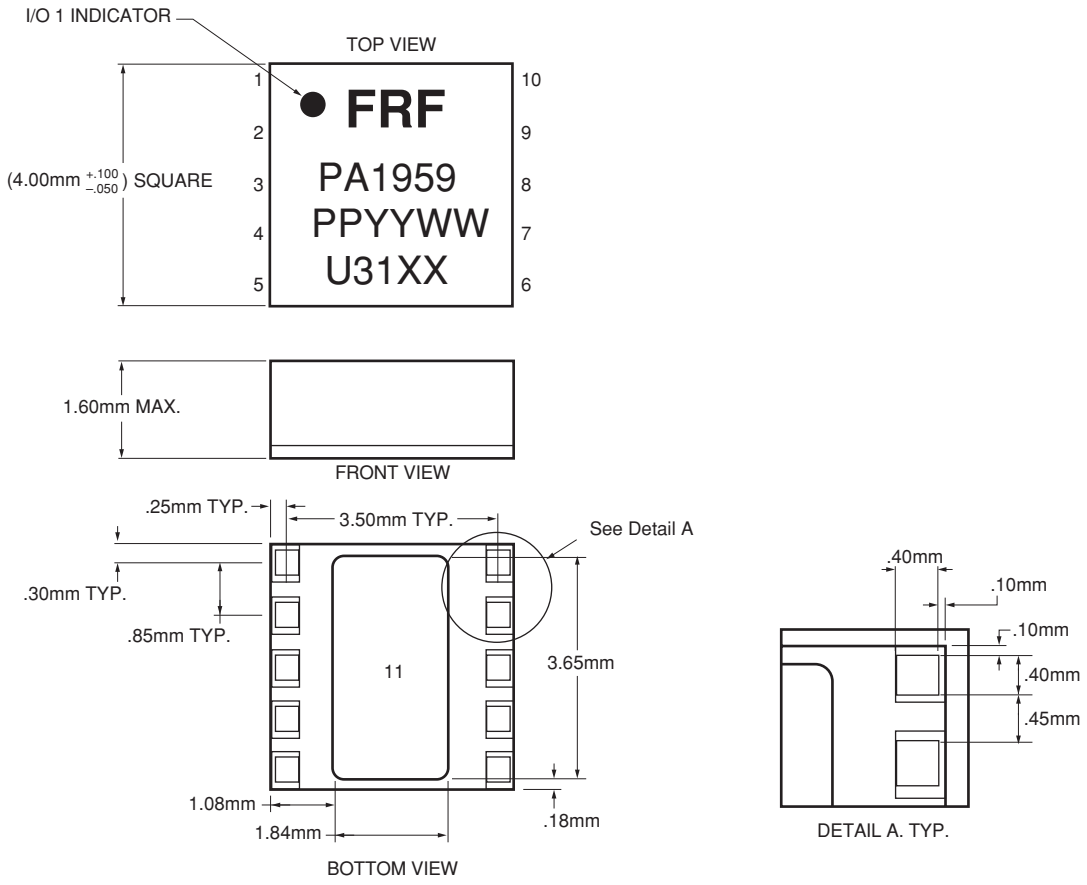
MATERIALS LIST

QTY	ITEM NO.	PART NUMBER	DESCRIPTION	VENDOR
1	1	G657553-1 V2	PC, BOARD	
2	2	#142-0701-841	SMA CONNECTOR	JOHNSON
5	3	#2340-5211TN	TERMINALS	3N
REF	4	G657684	ASSEMBLY, RMPA1959	
3	5	GRM39X7R102K50V	1000 pF CAPACITOR (0603)	MURATA
3	5 (ALT)	ECJ-1VB1H102K	1000 pF CAPACITOR (0603)	PANASONIC
2	6	C3216X5R1A335M	3.3 uF CAPACITOR (1206)	TDK
1	7	GRM39Y5V104Z16V	0.1uF CAPACITOR (0603)	MURATA
1	7 (ALT)	ECJ-1VB1C104K	0.1uF CAPACITOR (0603)	PANASONIC
A/R	8	SN63	SOLDER PASTE	INDIUM CORP
A/R	9	SN96	SOLDER PASTE	INDIUM CORP

Evaluation Board Schematic



Package Outline



Package Pinout

Pin #	Symbol	Description
1	Vcc1	Supply Voltage to Input Stage
2	RF In	RF Input Signal
3	GND	Ground
4	Vmode	High-Power/Low-Power Mode Control
5	Vref	Reference Voltage
6	GND	Ground
7	GND	Ground
8	RF Out	RF Output Signal
9	GND	Ground
10	Vcc2	Supply Voltage to Output Stage
11	GND	Paddle Ground

DC Turn-On Sequence

1) Vcc1 = Vcc2 = 3.4V (typical)

2) Vref = 2.85V (typical)

3) Vmode = 2.0V (Pout < 16dBm), 0V (Pout > 16dBm)

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
- Assemble the dry-baked devices within 7 days of removal from the oven.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

Solder Materials & Temperature Profile: Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

- **Reflow Profile**
  - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
  - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
  - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
  - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

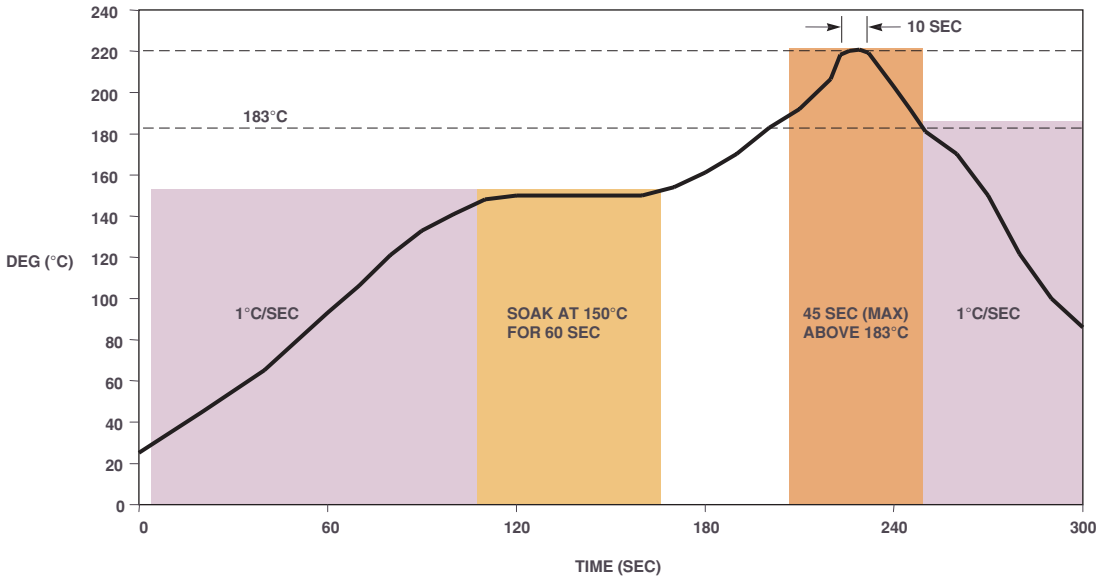


Figure 1. Recommended Solder Reflow Profile

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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