FAIRCHILD SEMICONDUCTOR®

September 2004

RMPA1959

PCS 3.4V CDMA & CDMA2000-1X PowerEdge™ Power Amplifier Module

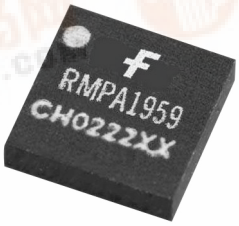
General Description

The RMPA1959 power amplifier module (PAM) is designed for CDMA and CDMA2000-1X personal communications system (PCS) applications. The 2 stage PAM is internally matched to 50Ω to minimize the use of external components and features advanced DC power management to reduce current consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Features

- Single positive-supply operation and low power and shutdown modes
- 39% CDMA efficiency at +28dBm average output power
- Compact LCC package- 4.0 x 4.0 x 1.5 mm with industry standard pinout
- Internally matched to 50Ω and DC blocked RF input/ output.
- Meets CDMA2000-1XRTT performance requirements

Device



Absolute Ratings[1]

Symbol	Parameter	Min	Max	Units
Vcc1, Vcc2	Supply Voltages	0	5.0	V
Vref	Reference Voltage	2.6	3.5	V
Vmode	Power Control Voltage	0	3.5	V
Pin	RF Input Power	–	+10	dBm
T_{STG}	Storage Temperature	-55	+150	°C

Note:
1: No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Module Block Diagram

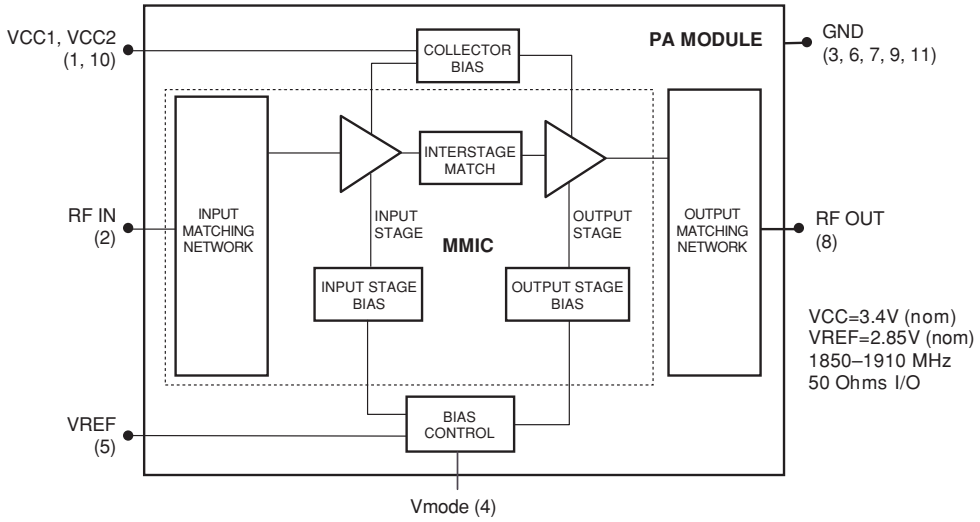


Figure 1. RMPA1959 US PCS CDMA Power Amplifier Module Functional Block Diagram

Electrical Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
f	Operating Frequency		1850		1910	MHz
CDMA Operation						
SSg	Small-Signal Gain	P_O = 0dBm	23	25		dB
Gp	Power Gain	P_O = +28dBm, Vmode = 0V P_O = +16dBm, Vmode ≥ 2.0V	25	28 24.5		dB dB
P_O	Linear Output Power	Vmode = 0V Vmode ≥ 2.0V	28		 16	dBm dBm
PAEd	PAEd (digital) @ +28 dBm	Vmode = 0V	36	39		%
	PAEd (digital) @ +16 dBm	Vmode ≥ 2.0V		10		%
	PAEd (digital) @ +16 dBm	Vmode ≥ 2.0V, V_{CC} = 1.4V		20		%
Itot	High Power Total Current	P_O = +28dBm, Vmode = 0V		460	530	mA
	Low Power Total Current	P_O = +16dBm, Vmode = 2.0V		120		mA
	Adjacent Channel Power Ratio	IS-95				
ACPR1	±1.25 MHz Offset	P_O = +28dBm; Vmode = 0V		-50	-46	dBc
		P_O = +16dBm; Vmode = 2.0V		-52		dBc
ACPR2	±2.25 MHz Offset	P_O = +28dBm; Vmode = 0V		-60	-57	dBc
		P_O = +16dBm; Vmode = 2.0V		-68		dBc
General Characteristics						
VSWR	Input Impedance		2.5:1	2.0:1		
NF	Noise Figure			4		dB
Rx No	Receive Band Noise Power	P_O ≤ +28dBm; 1850 to 1910 MHz		-139		dBm/Hz
2fo-5fo	Harmonic Suppression	P_O ≤ +28dBm			-30	dBc
S	Spurious Outputs[2,3]	Load VSWR ≤ 5.0:1			-60	dBc
	Ruggedness w/Load Mismatch[3]	No permanent damage			10:1	
Tc	Case Operating Temperature		-30		85	°C
DC Characteristics						
Iccq	Quiescent Current	Vmode ≥ 2.0V		50		mA
Iref	Reference Current	P_O ≤ +28dBm		5	8	mA
Icc (off)	Leakage Shutdown Current	No applied RF signal		1	5	µA

Notes:
1: All parameters met at Tc = +25°C, Vcc = +3.4V, f = 1880 MHz, and load VSWR ≤ 1.2:1.
2: All phase angles.
3: Guaranteed by design

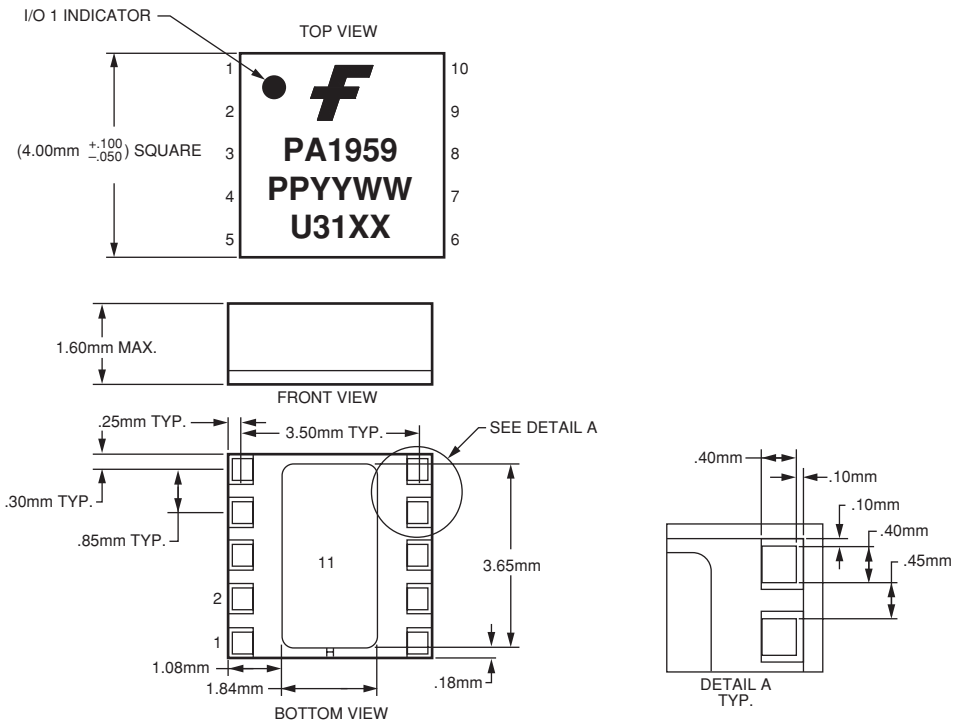
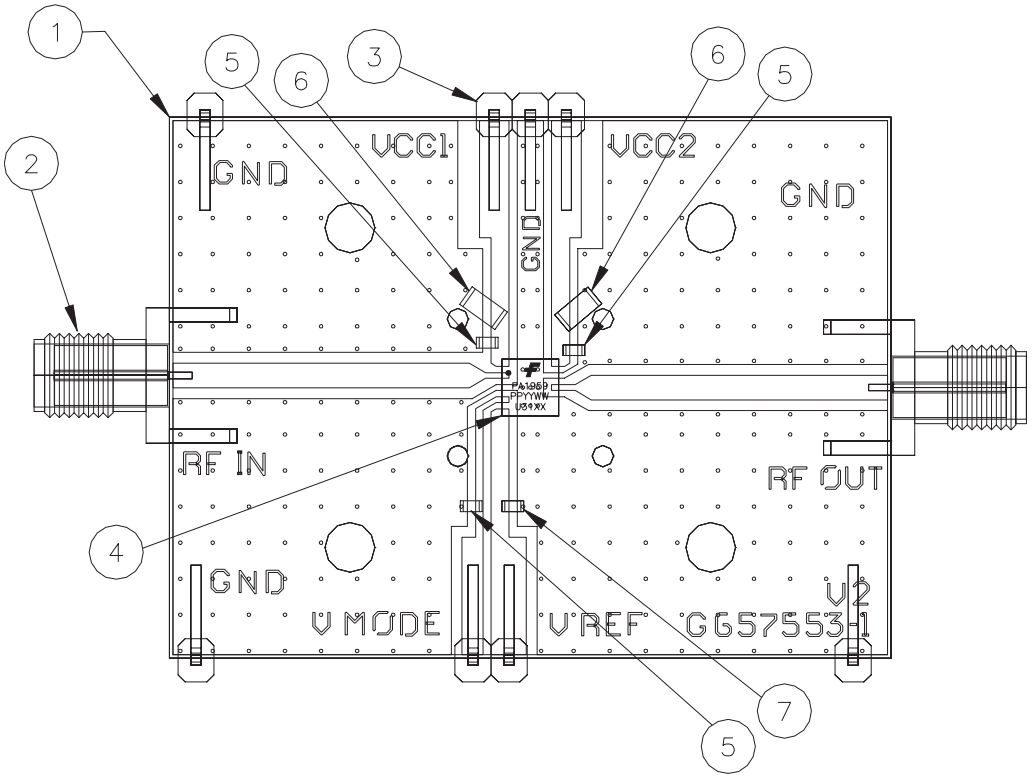


Figure 2. Package Outline

Package Pinout

Parameter	Symbol	Description	Pin#
RF	RF In	RF Input Signal	2
	RF Out	RF Output Signal	8
DC Power	Vcc1	Supply Voltage to Input Stage	1
	Vcc2	Supply Voltage to Output Stage	10
Ground	Gnd	Signal Ground	3, 6, 7, 9
		Paddle Ground	11
Control	Vmode	High Power/Low Power Mode Control	4
	Vref	Reference Voltage	5



MATERIALS LIST

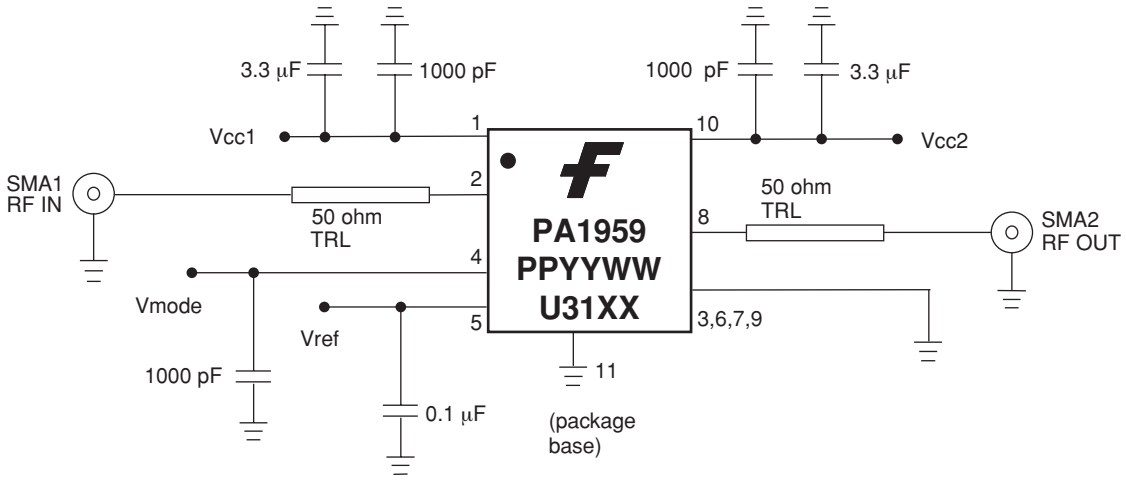
QTY	ITEM NO.	PART NUMBER	DESCRIPTION	VENDOR
1	1	G657553-1 V2	PC, BOARD	FAIRCHILD
2	2	#142-0701-841	SMA CONNECTOR	JOHNSON
5	3	#2340-5211TN	TERMINALS	3M
REF	4	G657584	ASSEMBLY, RMPA1959	FAIRCHILD
3	5	GRM39X7R102K50V	1000 pF CAPACITOR (0603)	MURATA
3	5 (ALT)	ECJ-1VB1H102K	1000 pF CAPACITOR (0603)	PANASONIC
2	6	C3216X5R1A335M	3.3 μF CAPACITOR (1206)	TDK
1	7	GRM39Y5V104Z16V	0.1μF CAPACITOR (0603)	MURATA
1	7 (ALT)	ECJ-1VB1C104K	0.1μF CAPACITOR (0603)	PANASONIC
A/R	8	SN63	SOLDER PASTE	INDIUM CORP.
A/R	9	SN96	SOLDER PASTE	INDIUM CORP.

Figure 3. Evaluation Board Layout

DC Turn-On Sequence

1) Vcc1 = Vcc2 = 3.4V (typ)
2) Vref = 2.85V (typ)
3) High-Power: Vmode = 0V (Pout > 16dBm)
   Low-Power: Vmode = 2.0V (Pout < 16dBm)

Evaluation Board Schematic

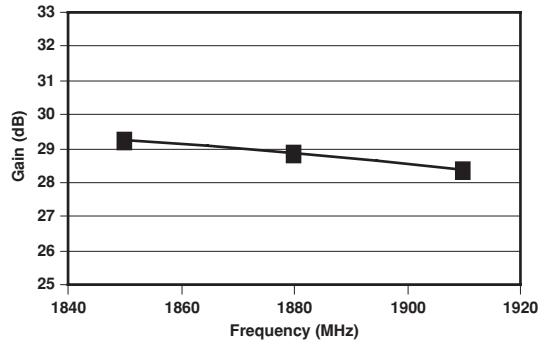


Recommended Operating Conditions

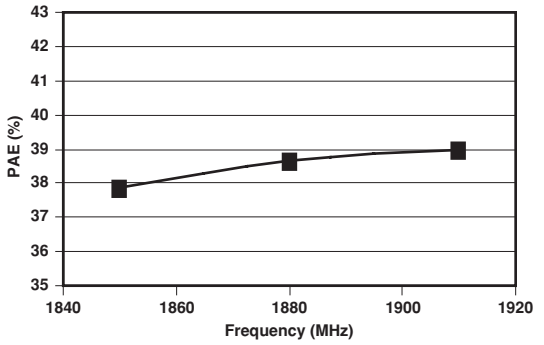
Parameter		Symbol	Min	Typ	Max	Units
Operating Frequency		f	1850		1910	MHz
Supply Voltage		Vcc1, Vcc2	3.0	3.4	4.2	V
Reference Voltage	(operating)	Vref	2.7	2.85	3.1	V
	(shutdown)		0		0.5	V
Bias Control Voltage	(low-power)	Vmode	1.8	2.0	3.0	V
	(high-power)		0		0.5	V
Linear Output Power	(high-power)	Pout			+28	dBm
	(low-power)				+16	dBm
Case Operating Temperature		Tc	-30		+85	°C

Performance Data

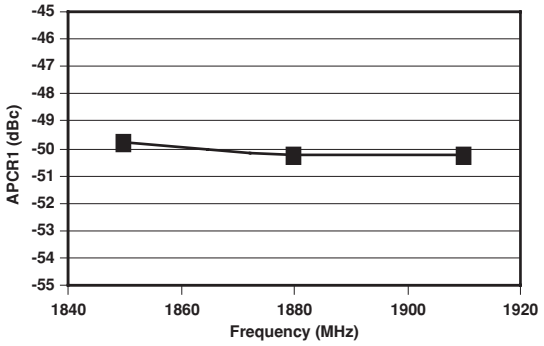
RMPA1959
Vcc=3.4V, Vref = 2.85V, Pout=28dBm, Vmode=0V



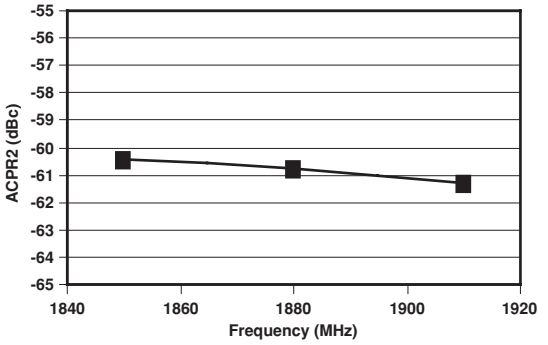
RMPA1959
Vcc=3.4V, Vref = 2.85V, Pout=28dBm, Vmode=0V



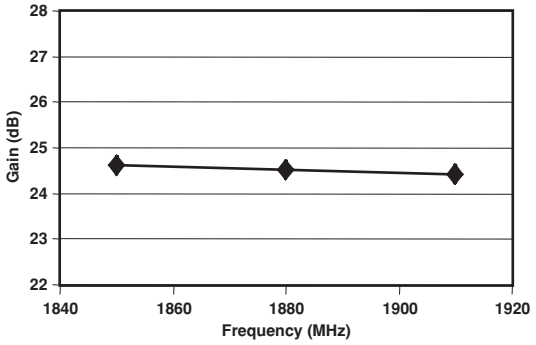
RMPA1959
Vcc=3.4V, Vref = 2.85V, Pout=28dBm, Vmode=0V, IS-95



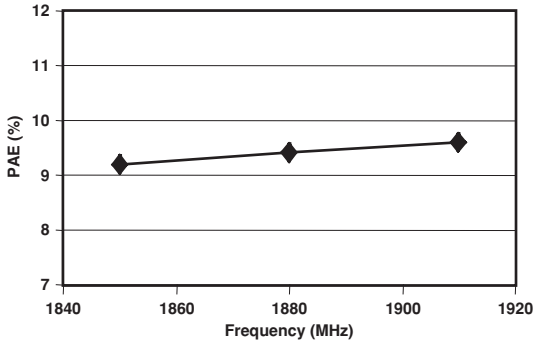
RMPA1959
Vcc=3.4V, Vref = 2.85V, Pout=28dBm, Vmode=0V, IS-95



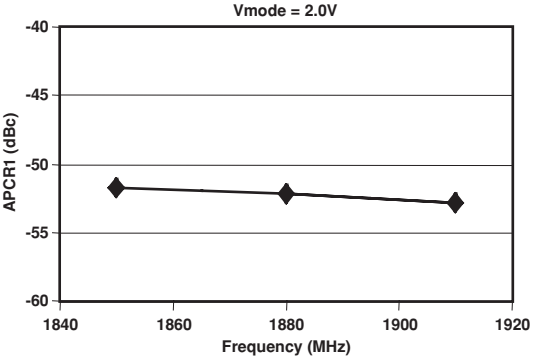
RMPA1959 16dBm Pout
Vcc = 3.4V, Vref = 2.85V
Vmode = 2.0V



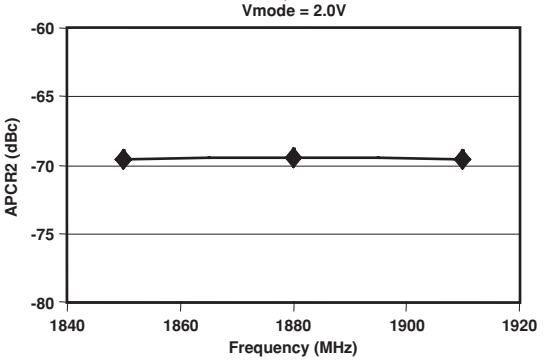
RMPA1959 16dBm Pout
Vcc = 3.4V, Vref = 2.85V
Vmode = 2.0V



RMPA1959 16dBm Pout
Vcc = 3.4V, Vref = 2.85V
Vmode = 2.0V



RMPA1959 16dBm Pout
Vcc = 3.4V, Vref = 2.85V
Vmode = 2.0V

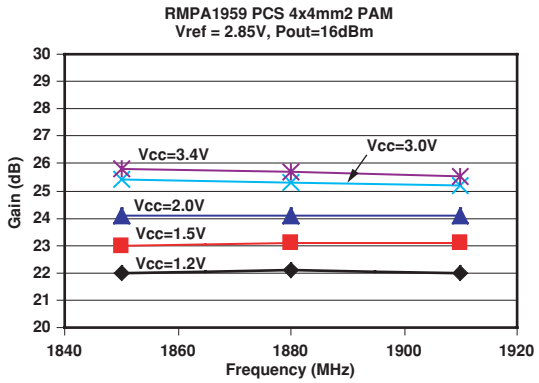


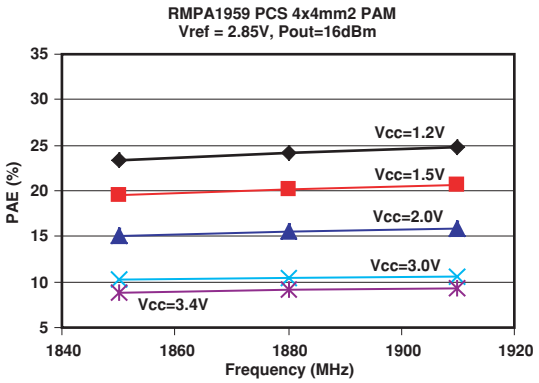
Efficiency Improvement Application

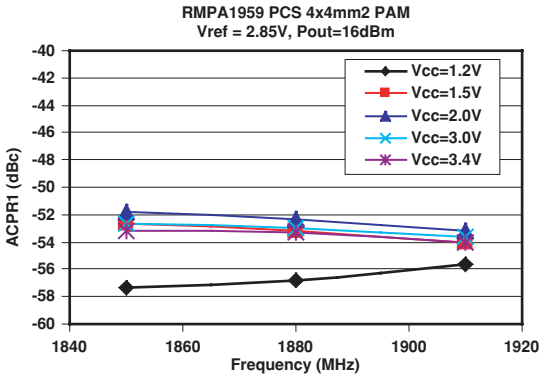
In addition to high-power/low-power bias modes, the efficiency of the PA module can be significantly increased at backed-off RF power levels by dynamically varying the supply voltage (Vcc) applied to the amplifier. Since mobile handsets and power amplifiers frequently operate at 10–20 dB back-off, or more, from maximum rated linear power, battery life is highly dependent on the DC power consumed at antenna power levels in the range of 0 to +16 dBm. The reduced demand on transmitted RF power allows the PA supply voltage to be reduced for improved efficiency, while still meeting linearity requirements for CDMA modulation with excellent margin. High-efficiency DC-DC converters are now available to implement switched-voltage operation.

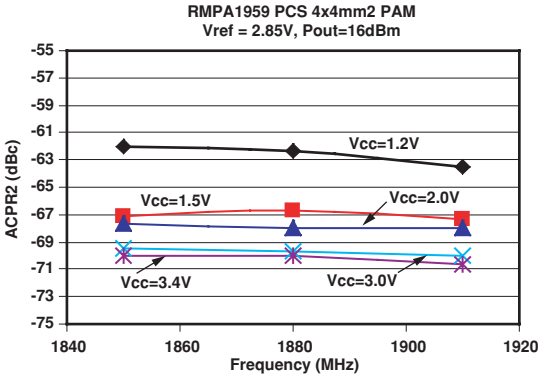
The following figures show measured performance of the PA module in low-power mode (Vmode = +2.0V) at +16dBm output power and over a range of supply voltages from 3.4V nominal down to 1.2V. Power-added efficiency is more than doubled from 10 percent to nearly 25 percent (Vcc = 1.2V) while maintaining a typical ACPR1 of –52dBc and ACPR2 of less than –61dBc.

Operation at even lower levels of Vcc supply voltage are possible with a further restriction on the maximum RF output power. As shown below, the PA module can be biased at a supply voltage of as low as 0.7V with an efficiency as high as 10–12 percent at +8dBm output power. Excellent signal linearity is still maintained even under this low supply voltage condition.



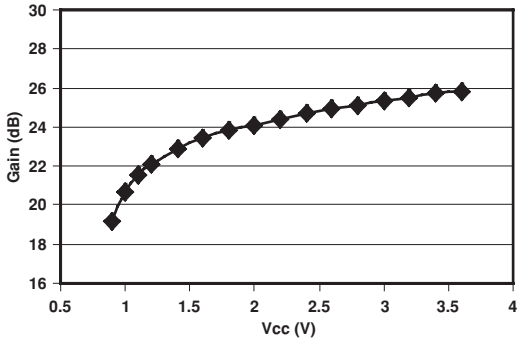




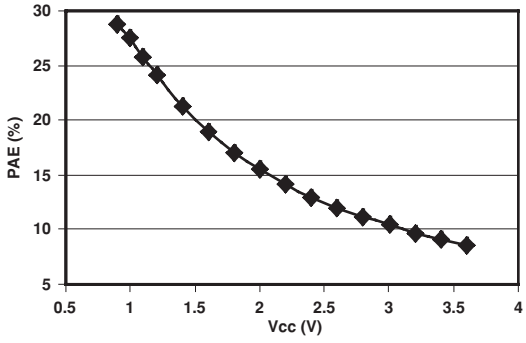


Efficiency Improvement Application (continued)

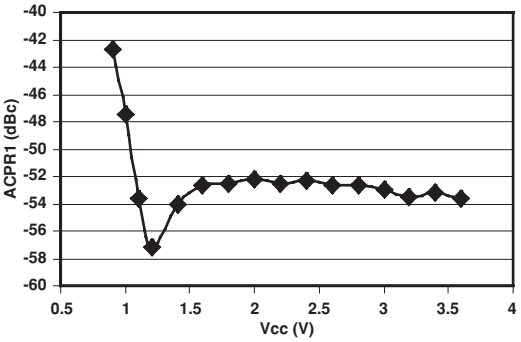
RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=16dBm, Freq=1.88GHz



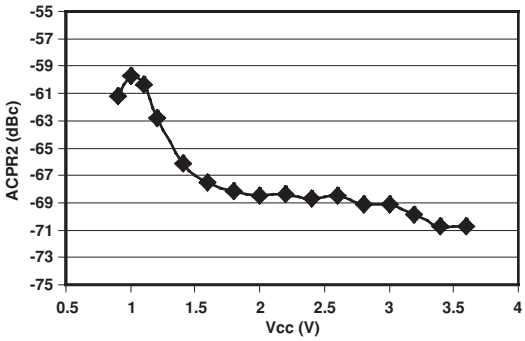
RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=16dBm, Freq=1.88GHz



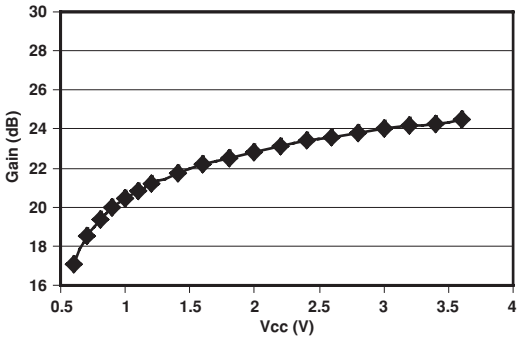
RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=16dBm, Freq=1.88GHz



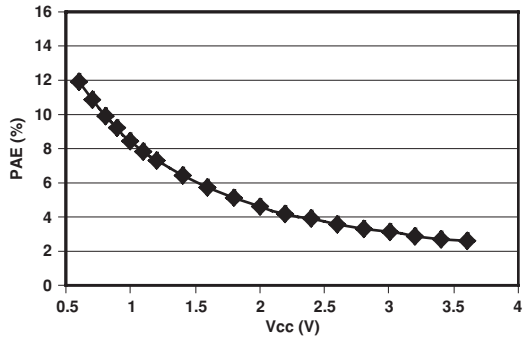
RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=16dBm, Freq=1.88GHz



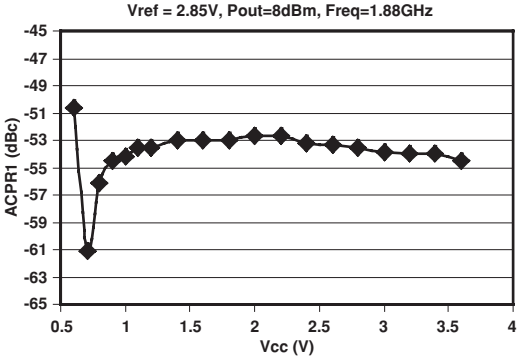
RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=8dBm, Freq=1.88GHz



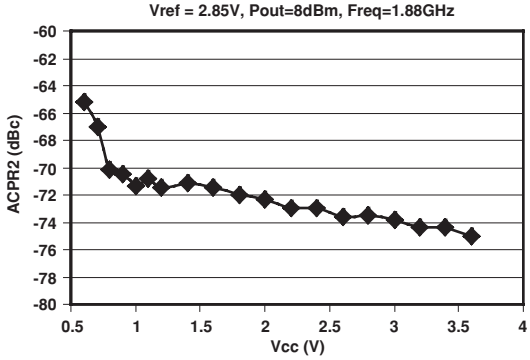
RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=8dBm, Freq=1.88GHz



RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=8dBm, Freq=1.88GHz



RMPA1959 PCS 4x4mm2 PAM
Vref = 2.85V, Pout=8dBm, Freq=1.88GHz



Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping reels cannot withstand 125°C baking temperature.
- Assemble the dry-baked devices within 7 days of removal from the oven.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

Solder Materials & Temperature Profile: Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

- **Reflow Profile**
  - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
  - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
  - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
  - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

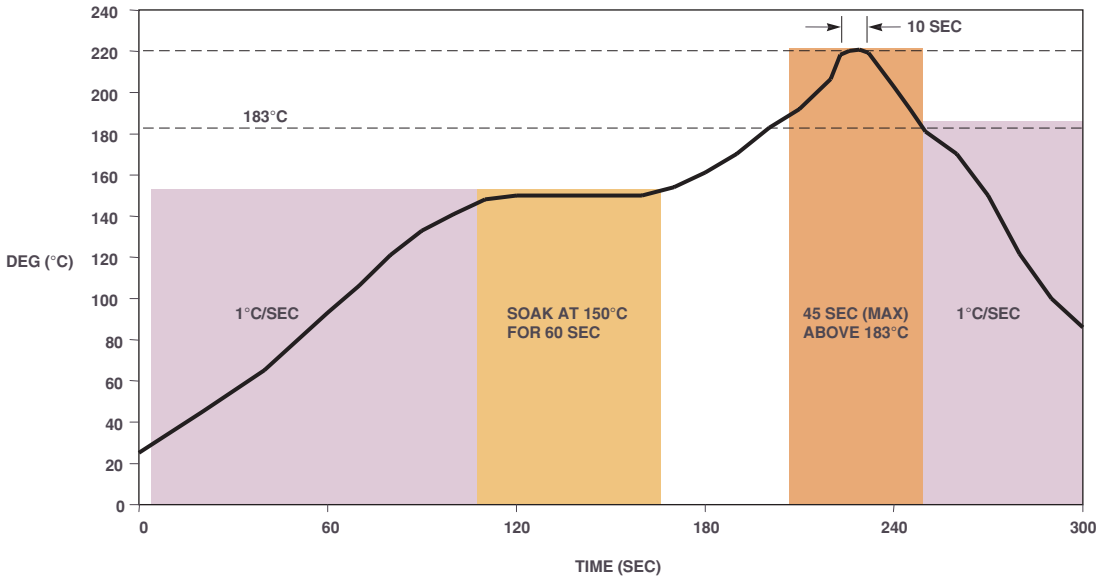


Figure 4. Recommended Solder Reflow Profile

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	Power247™	Stealth™
ActiveArray™	FASTr™	LittleFET™	PowerEdge™	SuperFET™
Bottomless™	FPS™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CoolFET™	FRFET™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QFET®	SuperSOT™-8
DOME™	GTO™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	HiSeC™	MSX™	QT Optoelectronics™	TinyLogic®
E^2CMOS™	I^2C™	MSXPro™	Quiet Series™	TINYOPTO™
EnSigna™	*i-Lo*™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	µSerDes™	UltraFET®
Across the board. Around the world.™		OPTOPLANAR™	SILENT SWITCHER®	VCX™
The Power Franchise®		PACMAN™	SMART START™	
Programmable Active Droop™		POP™	SPM™	

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.