FAIRCHILD SEMICONDUCTOR®

May 2005

RMPA2059

WCDMA PowerEdge™ Power Amplifier Module

Features

- 40% CDMA efficiency at +27dBm average output power
- Single positive-supply operation and low power and shutdown modes
- Meets UTMS/WCDMA and HSDPA performance requirements
- Compact Lead-free compliant LCC package - 4.0 x 4.0 x 1.5 mm
- Industry standard pinout
- Internally matched to 50Ω and DC blocked RF input/ output

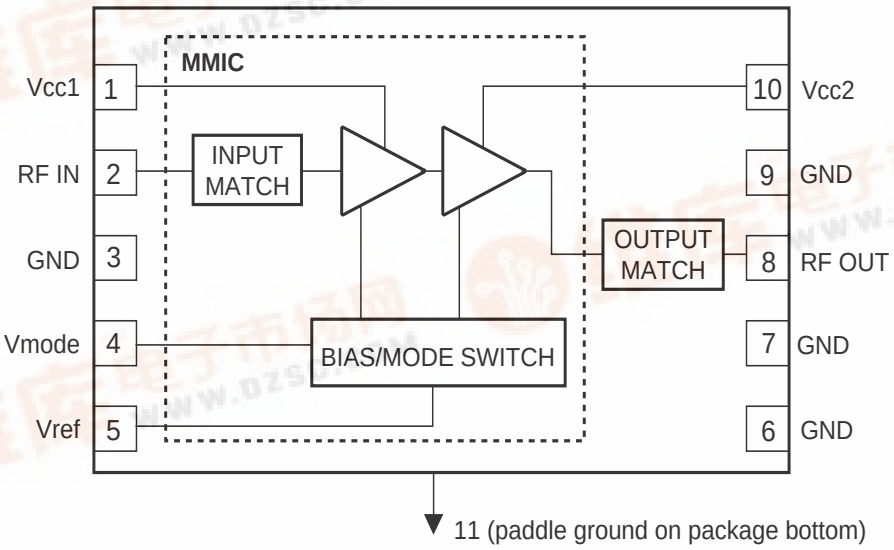
General Description

The RMPA2059 power amplifier module (PAM) is designed for WCDMA applications. The 2 stage PAM is internally matched to 50Ω to minimize the use of external components and features a low-power mode to reduce standby current and DC power consumption during peak phone usage. High power-added efficiency and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) process.

Device

Functional Block Diagram

(Top View)



Absolute Ratings[1]

Symbol	Parameter	Min	Max	Units
Vcc1, Vcc2	Supply Voltages	0	5.0	V
Vref	Reference Voltage	2.7	5.0	V
Vmode	Power Control Voltage	0	3.0	V
Pin	RF Input Power	–	+5	dBm
T_{STG}	Storage Temperature	-55	+150	°C

Note:
1: No permanent damage with only one parameter set at extreme limit. Other parameters set to typical values.

Electrical Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units	Comments
f	Operating Frequency	1920		1980	MHz	
WCDMA Operation						
Gp	Power Gain		26.5		dB	Po=+27dBm; Vmode=0V
			24		dB	Po=+16dBm; Vmode≥2.0V
Po	Linear Output Power	27			dBm	Vmode=0V
		16			dBm	Vmode≥2.0V
PAEd	PAEd (digital) @ +27dBm		40		%	Vmode=0V
	PAEd (digital) @ +16dBm		9.5		%	Vmode≥2.0V
	PAEd (digital) @ +16dBm		20		%	Vmode≥2.0V, Vcc=1.4V
Itot	High Power Total Current		365		mA	Po=+27dBm, Vmode=0V
	Low Power Total Current		120		mA	Po=+16dBm, Vmode≥2.0V
	Adjacent Channel Leakage Ratio					WCDMA Modulation 3GPP 3.2 03-00 DPCCH+1 DCDCH
ACLR1	±5.0MHz Offset		-40		dBc	Po=+27 dBm; Vmode=0V
			-44		dBc	Po=+16 dBm; Vmode≥2.0V
ACLR2	±10.0MHz Offset		-55		dBc	Po=+27 dBm; Vmode=0V
			-63		dBc	Po=+16 dBm; Vmode≥2.0V
General Characteristics						
VSWR	Input Impedance		2.0:1			
NF	Noise Figure		3		dB	
Rx No	Receive Band Noise Power		-139		dBm/Hz	Po<+27dBm; 2110 to 2170MHz
2fo-5fo	Harmonic Suppression[3]			-30	dBc	Po≤+27 dBm
S	Spurious Outputs[2,3]			-60	dBc	Load VSWR ≤ 5.0:1
	Ruggedness w/ Load Mismatch[3]			10:1		No permanent damage
Tc	Case Operating Temperature	-30		85	°C	
DC Characteristics						
Iccq	Quiescent Current		50		mA	Vmode≥2.0V
Iref	Reference Current		4	8	mA	Po≤+27dBm
Icc(off)	Shutdown Leakage Current		1	5	µA	No applied RF signal

Notes:
1: All parameters met at Tc = +25°C, Vcc = +3.4V, f = 1950MHz, and load VSWR ≤ 1.2:1.
2: All phase angles.
3: Guaranteed by design.

Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ	Max	Units
f	Operating Frequency	1920		1980	MHz
Vcc1, Vcc2	Supply Voltage	3.0	3.4	4.2	V
Vref	Reference Voltage Operating Shutdown	 2.7 0	 2.85	 3.1 0.5	 V V
Vmode	Bias Control Voltage Low-Power High-Power	 1.8 0	 2.0	 3.0 0.5	 V V
Pout	Linear Output Power High-Power Low-Power			 +27 +16	 dBm dBm
Tc	Case Operating Temperature	-30		+85	°C

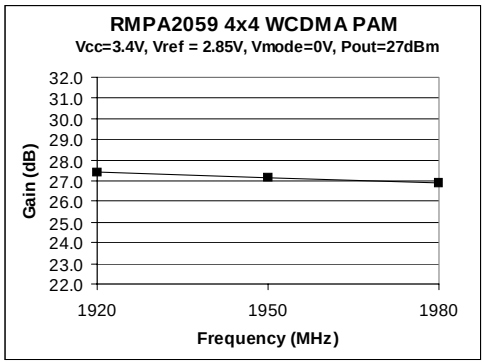
Note:

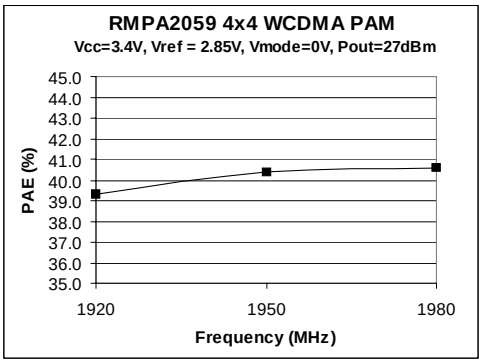
1: RF input power for WCDMA Pout = +27dBm.

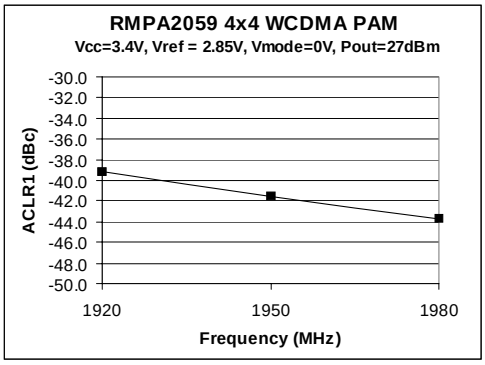
DC Turn On Sequence:

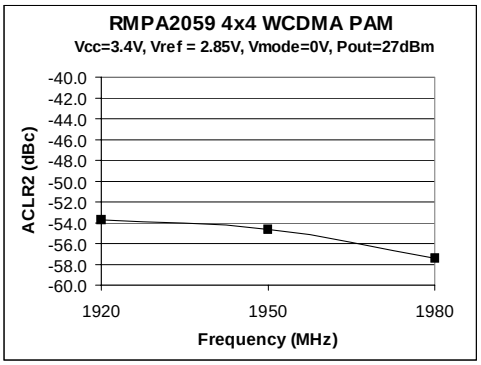
1. Vcc1 = Vcc2 = 3.4V (typical)
2. Vref = 2.85V (typical)
3. High-Power: Vmode = 0V (Pout > 16dBm)
   Low-Power: Vmode = 2.0V (Pout < 16dBm)

Performance Data

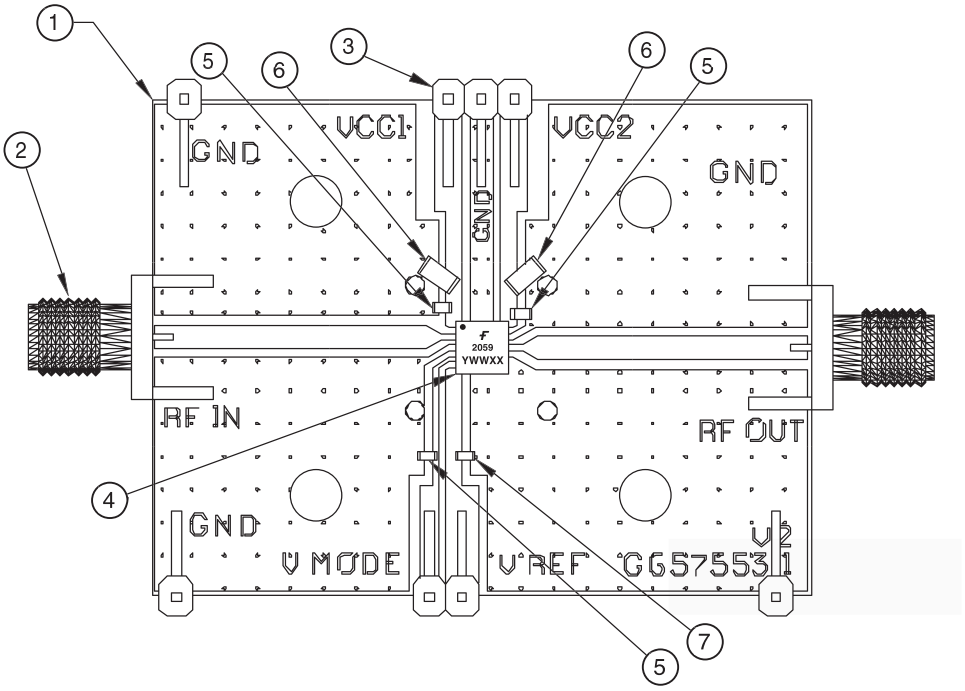








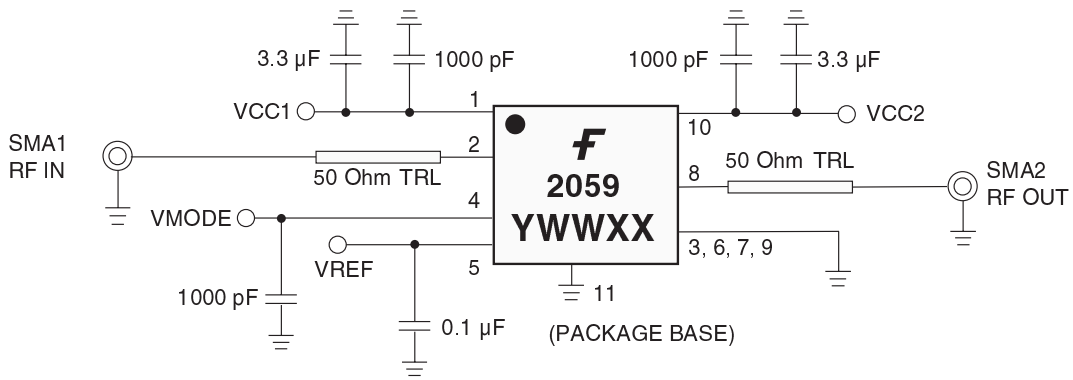
Evaluation Board Layout



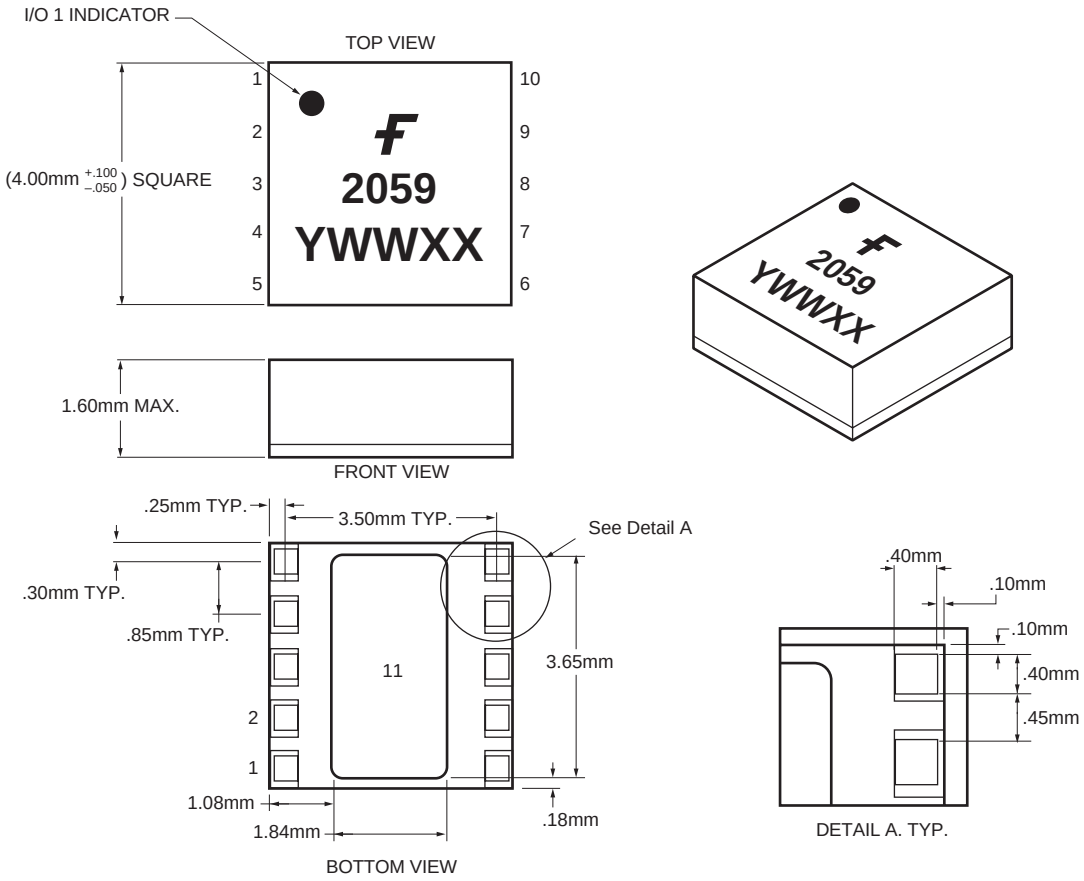
Materials List

Qty	Item No.	Part Number	Description	Vendor
1	1	G657553-1 V2	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
3	3	#2340-5211TN	Terminals	3M
Ref	4	G657637	Assembly, RMPA2059	Fairchild
3	5	GRM39XR102KS0V	1000pF Capacitor (0603)	Murata
3	5 (Alt)	ECJ-1V81H102K	1000pF Capacitor (0603)	Panasonic
2	6	C3216X5R1A335M	3.3µF Capacitor (1206)	TDK
1	7	GRM39YSV104Z16V	0.1µF Capacitor (0603)	Murata
1	7 (Alt)	ECJ-1VB1CID4K	0.1µF Capacitor (0603)	Panasonic
A/R	8	SN63	Solder Paste	Indium Corp.
A/R	9	SN96	Solder Paste	Indium Corp

Evaluation Board Schematic



Package Outline



Signal Descriptions

Pin #	Signal Name	Description
1	Vcc1	Reference Voltage
2	RF In	High Power/Low Power Mode Control
3	GND	Ground
4	Vmode	RF Input Signal
5	Vref	Supply Voltage to Input Stage
6	GND	Ground
7	GND	Ground
8	RF Out	RF Output Signal
9	GND	Ground
10	Vcc2	Supply Voltage to Output Stage
11	GND	Paddle Ground

Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
- Assemble the dry-baked devices within 7 days of removal from the oven.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.

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FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
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Rev. I15