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# **ULTRA-COMPACT SERIAL ALARM REAL-TIME CLOCK ICs**

**RS5C316A/B**

## **APPLICATION MANUAL**

**RICOH**

**ELECTRONIC DEVICES DIVISION**

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June 1995

# RS5C316A/B

## APPLICATION MANUAL

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## OUTLINE

The RS5C316A/B are CMOS type real-time clock ICs which are connected to the CPU via three signal lines and capable of serial transmission of clock and calendar data to the CPU.

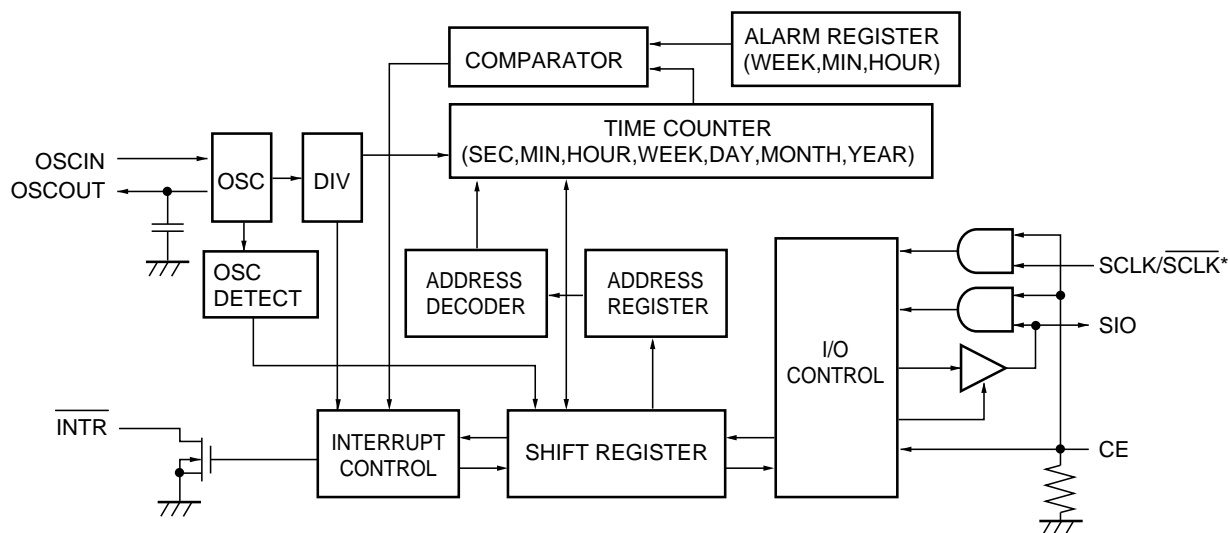
The RS5C316A/B can generate various periodic interrupt clock pulses lasting for long period (one month), further alarm interrupt can be made by days of the week, hours, and minutes. Driving an oscillation circuit at constant voltage, the circuit undergoes few voltage fluctuations and consequently realizes low current consumption (0.6 $\mu$ A at 3V). It also provides an oscillator halt sensing function for application to data validity at power-on and other occasions. Integrated into an ultra compact and ultra thin 8pin SSOP (0.65mm pitch), the RS5C316A/B are the optimum choice for equipment requiring small size and low power consumption.

The RS5C316A and the RS5C316B reads/writes data at falling and rising edge of serial clock respectively.

## FEATURES

- Time keeping voltage 1.6V to 6.0V
- Lowest supply current 0.6 $\mu$ A TYP. (1.5 $\mu$ A MAX.) at 3V
- Connection to the CPU via only three pins: CE, SCLK/ $\overline{\text{SCLK}}$  and SIO for addressing and data read/write
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in BCD code
- Periodic interrupt pulses to the CPU with cycles ranging from one month to 1/1024Hz, with interrupt flags and interrupt halt
- Alarm interrupt (days of the week, hours, minutes)
- Oscillator halt sensing to judge internal data validity
- Second digit adjustment by  $\pm 30$  seconds
- 12-hour or 24-hour time display selectable
- Automatic leap year recognition up to the year 2099
- CMOS logic
- Package: 8pin SSOP (0.65mm pitch)

## BLOCK DIAGRAM



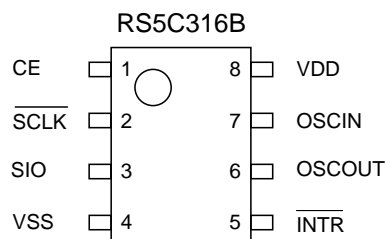
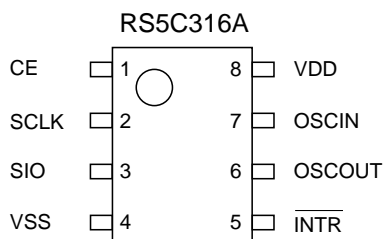
\*) RS5C316A: SCLK RS5C316B:  $\overline{\text{SCLK}}$

## APPLICATIONS

- Communication equipment (Multi-function telephone, portable telephone, PHS, pager)
- Business machines (Facsimile, portable facsimile)
- Personal computer (Desktop type, notebook type, word processor, PDA, electronic notebook, TV games)
- Audio visual equipment (Portable audio equipment, video camera, camera, digital camera, remote control equipment)
- Home use (Rice cooker, microwave range)

## PIN CONFIGURATION

- 8pin SSOP (0.65mm pitch)



## PIN DESCRIPTIONS

Pin No.	Symbol	Name	Description
1	CE	Chip enable input	The CE pin is used to interface the CPU and is accessible when held at the high level. This pin is connected to a pull-down resistor. It should be switched to the low level or opened when not accessed or when powering off the system. Holding the CE pin high for more than 2.5 seconds forces 1Hz interrupt pulses to be output from the $\overline{\text{INTR}}$ pin for oscillation frequency measurement. (No “1Hz pulse” is output for less than 1.5 seconds.)
2	SCLK (A type) $\overline{\text{SCLK}}$ (B type)	Shift clock input	This pin is used to input shift clock pulses to synchronize data input to, and output from, the SIO pin. SCLK and $\overline{\text{SCLK}}$ are for writing data at falling and rising edge of clock pulses respectively and also reading data at rising and falling edge of clock pulses respectively.
3	SIO	Serial input/output	The SIO pin inputs and outputs written or read data in synchronization with shift clock pulses from the SCLK/ $\overline{\text{SCLK}}$ pin. The SIO pin causes high impedance when CE pin is held at the low level (CMOS input/output). After the CE pin is switched to the high level and the control bits and the address bits are input from the SIO, the SIO pin performs serial input and output operations.
5	$\overline{\text{INTR}}$	Interrupt output	The $\overline{\text{INTR}}$ pin outputs periodic interrupt pulses and alarm interrupt to the CPU. This pin functions as an Nch open drain output even when the CE pin is held at the low level.
7 6	OSCIN OSCOUT	Oscillator circuit input/output	These pins configure an oscillator circuit by connecting a 32.768kHz crystal oscillator between the OSCIN and OSCOUT pins and by connecting a capacitor between the OSCIN and Vss pins. (Any other oscillator circuit components are built into the RS5C316A/B.)
8 4	VDD VSS	Positive/Negative power supply input	The VDD pin and Vss pin are connected to the positive power supply and to the ground level respectively.

## ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub>=0V)

Symbol	Item	Conditions	Ratings	Unit
V <sub>DD</sub>	Supply voltage		−0.3 to +7.0	V
V <sub>I</sub>	Input voltage		−0.3 to V <sub>DD</sub> +0.3	V
V <sub>O1</sub>	Output voltage 1	SIO	−0.3 to V <sub>DD</sub> +0.3	V
V <sub>O2</sub>	Output voltage 2	INTR	−0.3 to +12	V
P <sub>D</sub>	Power dissipation	T <sub>opt</sub> =25°C	300	mW
T <sub>opt</sub>	Operating temperature		−40 to +85	°C
T <sub>stg</sub>	Storage temperature		−55 to +125	°C

### ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

## RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub>=0V, T<sub>opt</sub>=−40 to +85°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V <sub>DD</sub>	Supply voltage		2.5		6.0	V
V <sub>CLK</sub>	Time keeping voltage		1.6		6.0	V
f <sub>XT</sub>	Oscillation frequency			32.768		kHz
C <sub>G</sub>	External oscillation capacitance	CL value of crystal=6 to 8pF	5	10	24	pF
V <sub>PUP</sub>	Pull-up voltage	INTR			10	V



## DC CHARACTERISTICS

Unless otherwise specified: VSS=0V, VDD=3V, T<sub>opt</sub>=−40 to +85°C, Oscillation frequency=32.768kHz, (C<sub>L</sub>=6pF, R<sub>1</sub>=30kΩ, C<sub>G</sub>=10pF

Symbol	Item	Pin name	Conditions	MIN.	TYP.	MAX.	Unit
V <sub>IH</sub>	“H” input voltage	CE, SCLK/SCLK, SIO		0.8V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IL</sub>	“L” input voltage	CE, SCLK/SCLK, SIO		0		0.2V <sub>DD</sub>	V
I <sub>OH</sub>	“H” output current	SIO	V <sub>OH</sub> =V <sub>DD</sub> −0.5V			−0.5	mA
I <sub>OL1</sub>	“L” output current	SIO	V <sub>OL1</sub> =0.5V	0.5			mA
I <sub>OL2</sub>		INTR	V <sub>OL2</sub> =0.4V	1			
R <sub>DN</sub>	Pull-down resistance	CE		45	150	450	kΩ
I <sub>ILK</sub>	Input leakage current	SCLK/SCLK	V <sub>I</sub> =V <sub>DD</sub> or V <sub>SS</sub>	−1		1	μA
I <sub>OZ1</sub>	Output off-state leakage current	SIO	V <sub>O</sub> =V <sub>DD</sub> or V <sub>SS</sub>	−2		2	μA
I <sub>OZ2</sub>		INTR	V <sub>O</sub> =10V	−5		5	
I <sub>DD1</sub>	Standby current 1	V <sub>DD</sub>	V <sub>DD</sub> =3V Input/Output: open		0.6	1.5	μA
I <sub>DD2</sub>	Standby current 2	V <sub>DD</sub>	V <sub>DD</sub> =6V Input/Output: open		0.8	2.0	μA
C <sub>D</sub>	Internal oscillation capacitance	OSCOUT			10		pF

## AC CHARACTERISTICS

(V<sub>SS</sub>=0V, T<sub>opt</sub>=−40 to +85°C, C<sub>L</sub>=50pF)

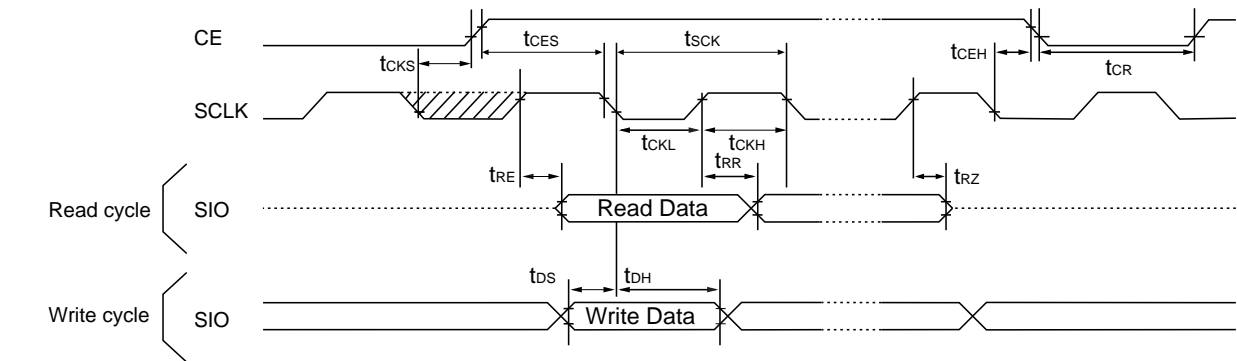
Symbol	Item	V <sub>DD</sub> ≥4.5V		V <sub>DD</sub> ≥4.0V		V <sub>DD</sub> ≥2.5V		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>CES</sub>	CE set-up time	175		200		400		ns
t <sub>CEH</sub>	CE hold time	175		200		400		ns
t <sub>CR</sub>	CE inactive time	350		400		800		ns
t <sub>SCK</sub>	SCLK clock cycle time	350		400		800		ns
t <sub>CKH</sub>	SCLK high time	175		200		400		ns
t <sub>CKL</sub>	SCLK low time	175		200		400		ns
t <sub>CKS</sub>	SCLK to CE set-up time	60		80		120		ns
t <sub>RE</sub>	Data output start time (from rising of SCLK) (from falling of SCLK)		120		135		300	ns
t <sub>RR</sub>	Data output delay time (from rising of SCLK) (from falling of SCLK)		120		135		300	ns
t <sub>rz</sub>	Output floating time		120		135		300	ns
t <sub>DS</sub>	Input data set-up time	50		60		120		ns
t <sub>DH</sub>	Input data hold time	50		50		80		ns

# TIMING CHARTS

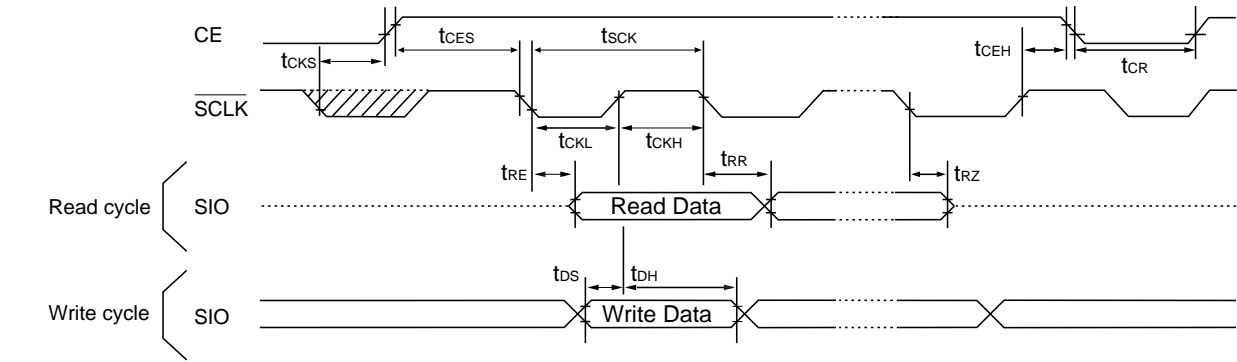
Input/Output conditions:  $V_{IH}=0.8\times V_{DD}$ ,  $V_{IL}=0.2\times V_{DD}$ ,  $V_{OH}=0.8\times V_{DD}$ ,  $V_{OL}=0.2\times V_{DD}$

\*) Any SCLK/SCLK state is allowed in the hatched area.

## • RS5C316A



## • RS5C316B



# FUNCTIONAL DESCRIPTIONS

## 1. Addressing

	Address				Registers	Data *1			
	A3	A2	A1	A0		D3	D2	D1	D0
0	0	0	0	0	1-second counter (BANK=0)	S8	S4	S2	S1
					Day of the week alarm register 1 (BANK=1)	AW3	AW2	AW1	AW0
1	0	0	0	1	10-second counter (BANK=0)	—*2	S40	S20	S10
					Day of the week alarm register 2 (BANK=1)	ALC	AW6	AW5	AW4
2	0	0	1	0	1-minute counter (BANK=0)	M8	M4	M2	M1
					1-minute alarm register (BANK=1)	AM8	AM4	AM2	AM1
3	0	0	1	1	10-minute counter (BANK=0)	—	M40	M20	M10
					10-minute alarm register (BANK=1)	—	AM40	AM20	AM10
4	0	1	0	0	1-hour counter (BANK=0)	H8	H4	H2	H1
					1-hour alarm register (BANK=1)	AH8	AH4	AH2	AH1
5	0	1	0	1	10-hour counter (BANK=0)	—	—	P/A, H20	H10
					10-hour alarm register (BANK=1)	ALE	—	AP/A, AH20	AH10
6	0	1	1	0	Day of the week counter (BANK=0)	—	W4	W2	W1
7	0	1	1	1	Interrupt cycle register (BANK=0, 1)	CT3	CT2	CT1	CT0
8	1	0	0	0	1-day counter (BANK=0)	D8	D4	D2	D1
9	1	0	0	1	10-day counter (BANK=0)	—	—	D20	D10
A	1	0	1	0	1-month counter (BANK=0)	MO8	MO4	MO2	MO1
B	1	0	1	1	10-month counter (BANK=0)	—	—	—	MO10
C	1	1	0	0	1-year counter (BANK=0)	Y8	Y4	Y2	Y1
D	1	1	0	1	10-year counter (BANK=0)	Y80	Y40	Y20	Y10
E	1	1	1	0	Control register 1 (BANK=0, 1)	CTFG	ALFG	WTEN/XSTP*4	ADJ/BSY*3
F	1	1	1	1	Control register 2 (BANK=0, 1)	12/24	NOP	BANK*5	TEST*6

\*1) All the listed data can be read and written.

\*2) The "—" mark indicates data which can be read only and set to "0" when read.

\*3) The ADJ/BSY bit of the control register is set to ADJ for write operation and BSY for read operation.

\*4) The WTEN/XSTP bit of the control register is set to WTEN for write operation and XSTP for read operation.

\*5) The clock/calendar counter and the alarm register can be selected when the BANK=0 and BANK=1 respectively. To designate the BANK is unnecessary for interrupt cycle register and control register 1/2.

\*6) The WTEN bit and TEST bit are set to "1" when CE is "L".

## 2. Registers

### 2.1 Control Register 1 (at Eh)

D3	D2	D1	D0	
CTFG	ALFG	WTEN	ADJ	(For write operation)
CTFG	ALFG	XSTP	BSY	(For read operation)

±30-second Adjustment Bit	
ADJ	Description
0	Ordinary operation
1	Second digit adjustment

Clock/Counter Busy-state Indication Bit	
BSY	Description
0	Ordinary operation
1	Second digit carry or adjustment

Clock Counter Enable/Disable Setting Bit	
WTEN	Description
0	Disabling of 1-second digit carry for clock counter
1	Enabling of 1-second digit carry for clock counter

Oscillator Halt Sensing Bit	
XSTP	Description
0	Ordinary oscillation
1	Oscillator halt sensing

Alarm Flag Bit	
ALFG	Description
0	Unmatched alarm register with clock counter
1	Matched alarm register with clock counter

Interrupt Flag Bit	
CTFG	Description
0	$\overline{\text{INTR}}$ =OFF enabling of write operation when CT <sub>3</sub> bit is set to 1
1	$\overline{\text{INTR}}$ =L enabling of write operation when CT <sub>3</sub> bit is set to 1

#### 2.1-1 (ADJ)

The following operations are performed by setting the ADJ bit to 1.

After this bit is set to 1, the BSY bit is set to 1 for the maximum duration of 122.1μs.

If the WTEN bit is 0, these adjustment operations are started after the WTEN bit is set to 1.

1) For second digits ranging from “00” to “29” seconds:

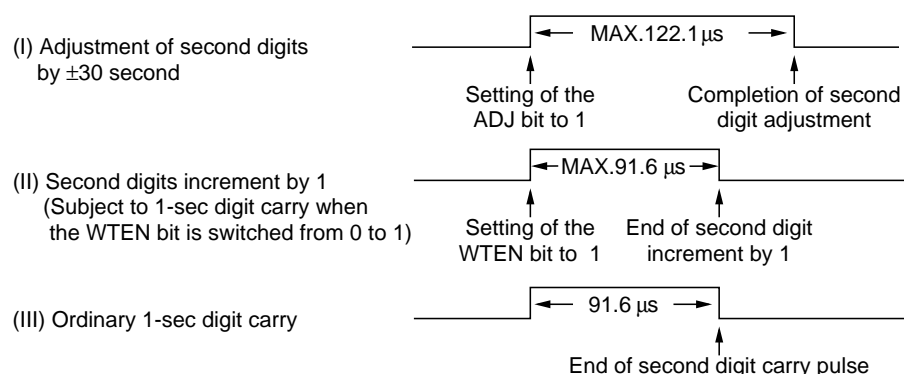
Time counters smaller than seconds are reset and second digits are set to “00”.

2) For second digits ranging from “30” to “59” seconds:

Time counters smaller than seconds are reset and second digits are set to “00”. Minute digits are incremented by 1.

### 2.1-2 (BSY)

When the BSY bit is 1, the clock and calendar counter are being updated. Consequently, write operation should be performed for the counters when the BSY bit is 0. Meanwhile, read operation is normally performed for the counters when the BSY bit is 0, but can be performed without checking the BSY bit as long as appropriate software is provided for preventing read errors. (Refer to 13. Typical Software-based Operations.) The BSY bit is set to 1 in the following three cases:



### 2.1-3 (WTEN)

The WTEN bit should be set to 0 to check that the BSY bit is 0 when performing read and write operations for the clock and calendar counters. For read operation, the WTEN bit may be left as 1 without checking the BSY bit as long as appropriate measures such as read repetition are provided for preventing read errors. The WTEN bit should be set to 1 after completing read and write operations, or will automatically be set to 1 by switching the CE pin to the low level. If 1-second digit carry occurs when the WTEN bit is 0, a second digit increment by 1 occurs when the WTEN bit is set to 1. There may be a possibility causing a time delay when it takes 1/1024 second or more to set WTEN bit from 0 to 1, Read data in state of WTEN=1 in such a case. (Refer to the item 13.3)

### 2.1-4 (XSTP)

The XSTP bit senses the oscillator halt. When the CE pin is held at the low level, the XSTP bit is set to 1 once the crystal oscillator is stopped after initial power-on or supply voltage drop and left to be 1 after it is restarted. When the CE pin is held at the high level, the XSTP bit is left as it was when the CE pin was held at the low level without checking oscillation stop. As such, the XSTP bit can be used to validate clock and calendar count data after power-on or supply voltage drop. The XSTP bit is set to 0 when any data is written to the control register 1 (at Eh) with ordinary oscillation.

### 2.1-5 (ALFG)

The ALFG bit can be set to 1 when the ALE bit set to 1 with alarm interruption ( $\overline{\text{INTR}}=\text{L}$ ).



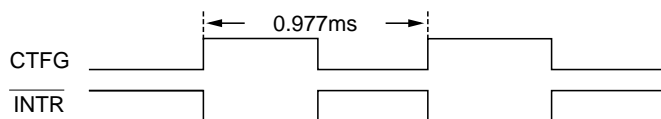
## 2.1-6 (CTFG)

The CTFG bit is set to 1 when interrupt pulses are output from the  $\overline{\text{INTR}}$  pin held at the low level. There are two interrupt modes selectable: the pulse mode (when the CT3 bit is set to 0) and the level mode (when the CT3 bit is set to 1). The CTFG bit can be set only when the CT3 is set to 1. Setting the CTFG bit to 1 switches the  $\overline{\text{INTR}}$  pin to the low level while setting the CTFG bit to 0 turns off the  $\overline{\text{INTR}}$  pin.

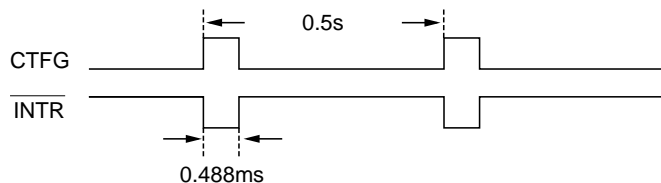
Interrupt cycle register				$\overline{\text{INTR}}$ output	Description
CT3	CT2	CT1	CT0		
0	* * <sup>1</sup>	0	0	OFF	Interrupt halt
0	*	0	1	ON	Fixing the $\overline{\text{INTR}}$ pin at low level
0	*	1	0	0.977ms	Cycle: 0.977ms (1/1024Hz) Duty 50% * <sup>2</sup>
0	*	1	1	0.5s	Cycle: 0.5s (1/2Hz) * <sup>3</sup>
1	0	0	0	1s	Every second * <sup>4</sup>
1	0	0	1	10s	Every 10 seconds * <sup>4</sup> (For display of second digits: 00, 10, 20, 30, 40 and 50)
1	0	1	0	1 minute	Every minute (00 second) * <sup>4</sup>
1	0	1	1	10 minutes	Every 10 minutes (00 second) * <sup>4</sup> (For display of minute digits: 00, 10, 20, 30, 40 and 50)
1	1	0	0	1 hour	Every hour (00 minute and 00 second) * <sup>4</sup>
1	1	0	1	1 day	Every day (00 hour, 00 minute and 00 second a.m.) * <sup>4</sup>
1	1	1	0	1 week	Every week * <sup>4</sup> (0 week, 0 hour, 00 minute and 00 second a.m.)
1	1	1	1	1 month	Every month * <sup>4</sup> (1 day, 0 hour, 00 minute and 00 second a.m.)

\*1) The symbol "\*" in the above table indicates 0 or 1.

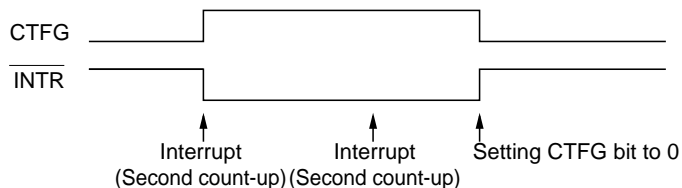
\*2)



\*3)



\*4)



## 2.2 Control Register 2 (at Fh)

D3	D2	D1	D0	
$\overline{12/24}$	NOP	BANK	$\overline{\text{TEST}}$	(For write operation)
$\overline{12/24}$	NOP	BANK	$\overline{\text{TEST}}$	(For read operation)

Bit for Testing \*1

$\overline{\text{TEST}}$	Description
0	Testing mode
1	Ordinary operation mode

Bank Selection Bit \*2

BANK	Description
0	Clock/calendar counter
1	Alarm register

The NOP bit can be set to 0 for ordinary operation having no use for anything.

$\overline{12/24}$ -hour Time Display System Selection Bit \*3

$\overline{12/24}$	Description
0	12-hour time display system (separate for mornings and afternoons)
1	24-hour time display system

\*1) ( $\overline{\text{TEST}}$ ) Set the  $\overline{\text{TEST}}$  bit to 1 in ordinary operation.  $\overline{\text{TEST}}$  bit is set automatically to 1 when the CE pin is "L".

\*2) (BANK) There is no need to designate BANK bit for Interrupt cycle register and Control register 1/2.

\*3) ( $\overline{12/24}$ ) The  $\overline{12/24}$  bit specifies time digit display in BCD code.

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

Either the 12-hour or 24-hour time display system should be selected before time setting.

### 2.3 Interrupt cycle Register (at 7h)

D3	D2	D1	D0	
CT <sub>3</sub>	CT <sub>2</sub>	CT <sub>1</sub>	CT <sub>0</sub>	(For write operation)
CT <sub>3</sub>	CT <sub>2</sub>	CT <sub>1</sub>	CT <sub>0</sub>	(For read operation)

Bits for selecting the interrupt cycle and output mode at the  $\overline{\text{INTR}}$  pin \*1

\*1) (CT<sub>3</sub> to CT<sub>0</sub>)

The CT<sub>3</sub> to CT<sub>0</sub> bits are used to select the interrupt cycle and output mode at the  $\overline{\text{INTR}}$  pin. There are two interrupt modes selectable: the pulse mode (when the CT<sub>3</sub> bit is set to 0) and the level mode (when the CT<sub>3</sub> bit is set to 1). The interrupt cycle and output mode at the INTR pin are shown in detail in the section on the CTFG bit in "2.1 Control Register 1 (at Eh)".

### 2.4 Alarm registers for day-of-the-week, 1-minute, 10-minute, 1-hour, 10-hour (BANK1, at 0h-5h)

D3	D2	D1	D0	
AW <sub>3</sub>	AW <sub>2</sub>	AW <sub>1</sub>	AW <sub>0</sub>	(For read/write) day-of-the-week 1 (at 0h)
$\overline{\text{ALC}}$	AW <sub>6</sub>	AW <sub>5</sub>	AW <sub>4</sub>	(For read/write) day-of-the-week 2 (at 1h)
AM <sub>8</sub>	AM <sub>4</sub>	AM <sub>2</sub>	AM <sub>1</sub>	(For read/write) 1-minute time digit (at 2h)
*	AM <sub>40</sub>	AM <sub>20</sub>	AM <sub>10</sub>	(For read/write) 10-minute time digit (at 3h)
AH <sub>8</sub>	AH <sub>4</sub>	AH <sub>2</sub>	AH <sub>1</sub>	(For read/write) 1-hour time digit (at 4h)
ALE	*	AP/ $\overline{\text{A}}$ , AH <sub>20</sub>	AH <sub>10</sub>	(For read/write) 10-hour time digit (at 5h)

\*1) The "\*" mark in the above table indicates data which are set to 0 for read cycle and not set for write cycle.

\*2) 10-hour time digit indicates AP/ $\overline{\text{A}}$  and AH<sub>20</sub> with 12-hour and 24-hour time system respectively.

\*3) Make sure set an actual time-data to the alarm registers when the alarm function is activated as any imaginary alarm-data will never be match with the actual time.

\*4) The  $\overline{\text{INTR}}$  pin can output matched alarm interruption when the  $\overline{\text{ALC}}$  bit is set 0 and halt output when the  $\overline{\text{ALC}}$  bit is set to 1.

\*5) The alarm function is disabled when the ALE bit is set 0 and is enables when the ALE bit is set 1.

\*6) Examples of setting alarm time

Setting alarm time	Day-of-the-week							12-hour system				12-hour system			
	Sun. AW <sub>0</sub>	Mon. AW <sub>1</sub>	Tue. AW <sub>2</sub>	Wed. AW <sub>3</sub>	Thu. AW <sub>4</sub>	Fri. AW <sub>5</sub>	Sat. AW <sub>6</sub>	10- hour	1- hour	10- min	1- min	10- hour	1- hour	10- min	1- min
AM 00:00 every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
AM 01:30 every day	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
AM 11: 59 every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
PM 00:00 on Monday through Friday	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
PM 01:30 on Sunday	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
PM 11:59 on Monday, Wednesday, and Friday	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

\*7) Hour digits show "12" and "32" when the time is AM 00:00 and PM 00:00 respectively in the 12-hour system.

\*8) No alarm interruption is output when all the bit from AW<sub>0</sub> through AW<sub>6</sub> is set to 0.

\*9) Each of the AW<sub>0</sub> through AW<sub>6</sub> corresponds to the day-of-the-week counter such as (W<sub>4</sub>, W<sub>2</sub>, W<sub>1</sub>)=(0, 0, 0) through (1, 1, 0). Designation of day-of-the-week and AW<sub>0</sub> through AW<sub>6</sub> in the above table is one example.



### 3. Counters

#### 3.1 Clock counter (BANK 0, at 0h-5h)

D3	D2	D1	D0	
S <sub>8</sub>	S <sub>4</sub>	S <sub>2</sub>	S <sub>1</sub>	(For read/write) 1-second time digit (at0h)
*	S <sub>40</sub>	S <sub>20</sub>	S <sub>10</sub>	(For read/write) 10-second time digit (at1h)
M <sub>8</sub>	M <sub>4</sub>	M <sub>2</sub>	M <sub>1</sub>	(For read/write) 1-minute time digit (at2h)
*	M <sub>40</sub>	M <sub>20</sub>	M <sub>10</sub>	(For read/write) 10-minute time digit (at3h)
H <sub>8</sub>	H <sub>4</sub>	H <sub>2</sub>	H <sub>1</sub>	(For read/write) 1-hour time digit (at4h)
*	*	P/ $\overline{A}$ or H <sub>20</sub>	H <sub>10</sub>	(For read/write) 10-hour time digit (at5h)

- \*1) The "\*" mark indicates data which are set to 0 for read cycle and not set for write cycle.
- \*2) Any carry to 1-second digits from the second counter is disabled when the WTEN bit (of the control register 1) is set to 0.
- \*3) Time digit display (BCD code):  
 Second digits : Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.  
 Minute digits : Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.  
 Hour digits : Range as shown in the section on the 12/24 bit and carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.
- \*4) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.

#### 3.2 Day-of-the-week counter (BANK 0, at 6h)

D3	D2	D1	D0	
*	W <sub>4</sub>	W <sub>2</sub>	W <sub>1</sub>	(For read/write) Day-of-the-week counter

- \*1) The "\*" mark indicates data which are set to 0 for read cycle and not set for write cycle.
- \*2) Day-of-the-week digits are incremented by 1 when carried to 1-day digits.
- \*3) Day-of-the-week digits display (incremented in septimal notation):  
 (W<sub>4</sub>, W<sub>2</sub>, W<sub>1</sub>)=(000) → (001) → ..... → (110) → (000)  
 The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday=000).
- \*4) The (W<sub>4</sub>, W<sub>2</sub>, W<sub>1</sub>) should not be set to (111).

## 3.3 Calendar counter (BANK 0, at 8h-Dh)

D3	D2	D1	D0		
D8	D4	D2	D1	(For read/write) 1-day calendar digit	(at 8h)
*	*	D20	D10	(For read/write) 10-day calendar digit	(at 9h)
MO8	MO4	MO2	MO1	(For read/write) 1-month calendar digit	(at Ah)
*	*	*	MO10	(For read/write) 10-month calendar digit	(at Bh)
Y8	Y4	Y2	Y1	(For read/write) 1-year calendar digit	(at Ch)
Y80	Y40	Y20	Y10	(For read/write) 10-year calendar digit	(at Dh)

\*1) The "\*" mark indicates data which are set to 0 for read cycle and not set for write cycle.

\*2) The automatic calendar function provides the following calendar digit displays in BCD code.

Day digits : Range from 1 to 31 (for January, March, May, July, August, October, and December).

Range from 1 to 30 (for April, June, September, and November).

Range from 1 to 29 (for February in leap years).

Range from 1 to 28 (for February in ordinary years).

Carried to month digits when cycled to 1.

Month digits : Range from 1 to 12 and carried to year digits when cycled to 1.

Year digits : Range from 00 to 99 and counted as 00, 04, 08, ..., 92, and 96 in leap years.

\*3) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.

## USAGES

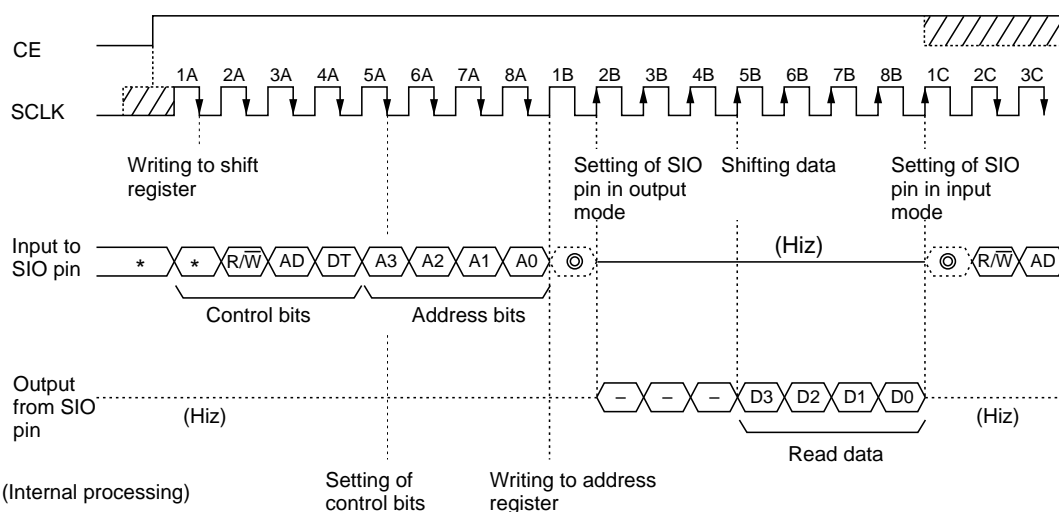
### 1. Read Data (For the RS5C316A)

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the SCLK pin. The input data are registered in synchronization with the falling edge of the SCLK. When the data is read, the read cycle shall be set by control bits then registered data can be read out from SIO pin in synchronization with the rising edge of the SCLK.

- **Control bits**
  - $\overline{R/\overline{W}}$ : Establishes the read mode when set to 1, and the write mode when set to 0.
  - AD: Writes succeeding addressing bits (A3-A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  - DT: Writes data bits to counter or register specified by the address register set just before when set to 1 with the  $\overline{R/\overline{W}}$  and AD bits set equally to 0 and performs no such write operation in any other case.
- **Address bits**
  - A3-A0: Inputs the bits MSB to LSB in the address table describing the functions.

#### 1.1 Read Cycle Flow

- The CE pin is switched from “L” to “H”.
- Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits  $\overline{R/\overline{W}}$  and AD are set equally to 1 while a control bit DT is set to 0. (see the SCLK 1A-8A)
- The SIO pin enters the output mode at the rising edge of the shift clock pulse 2B from the SCLK pin while the four read bits (MSB → LSB) at designated addresses are output at the rising edge of the shift clock pulse 5B. (see the figure below)
- Then, the SIO pin returns to the input mode at the rising edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
- At the end of read cycle, the CE pin is switched from “H” to “L” (after t<sub>CEH</sub> from the falling edge of the eighth shift clock pulse from the SCLK pin). Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at “H”.



- \*) In the above figure, the “\*” mark indicates arbitrary data; the “-” mark indicates unknown data.  
 The “⊙” mark indicates data which are available when the SIO pin is held at “H”, “L”, or Hiz level.  
 The diagonally shaded area of the CE and the SCLK pins indicate “H” or “L”.

## 2. Write Data (For the RS5C316A)

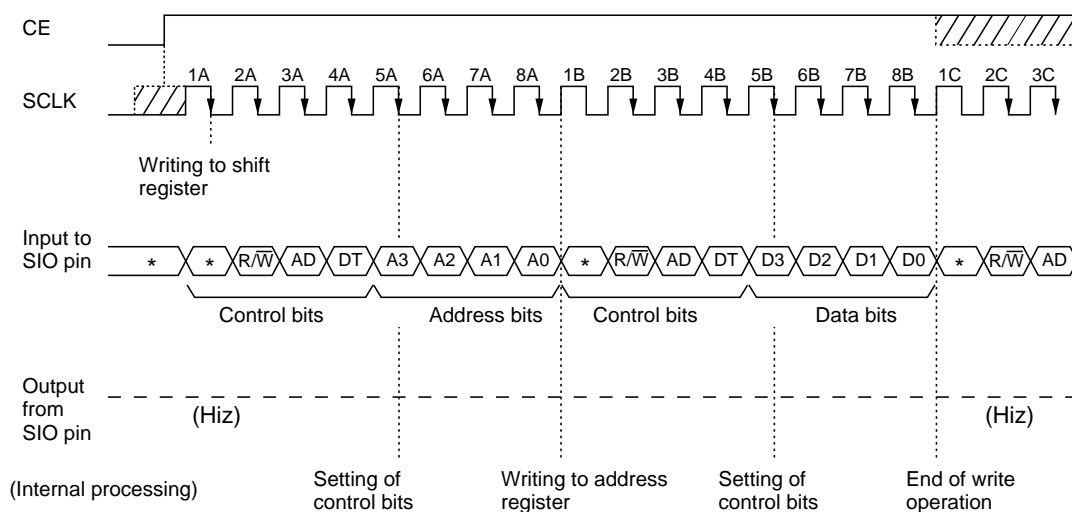
Writing data to the real-time clock requires inputting setting data (control bits, address bits and data bits) to the SIO pin and then establishing the write mode by using a control bit  $R/\overline{W}$  in the same manner as in read operation.

\*) Control bits and address bits are described in the previous section on read cycle.

- **Data bits** D3-D0: Inputs the data bits MSB to LSB in the addressing table describing the functions.

### 2.1 Write Cycle Flow

1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits  $R/\overline{W}$  and DT are set equally to 0 while a control bit AD is set to 1. (see the SCLK 1A-8A)
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits  $R/\overline{W}$  and AD are set equally to 0 while a control bit DT is set to 1. (see the clock 1B-8B)
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits  $R/\overline{W}$ , AD, and DT are set equally to 0 (at the falling edge of shift clock pulse 5A and later from the SCLK pin) or the CE pin is switched from “H” to “L” (after  $t_{CEH}$  from the falling edge of the eighth shift clock pulse from the SCLK pin). Following on write cycle, read operation can be performed by setting control bits in the read mode at the shift clock pulse 1C and later with the CE pin held at “H”.



\*) In the above figure, the “\*” mark indicates arbitrary data; and the diagonally shaded area of CE and SCLK indicates “H” or “L”.

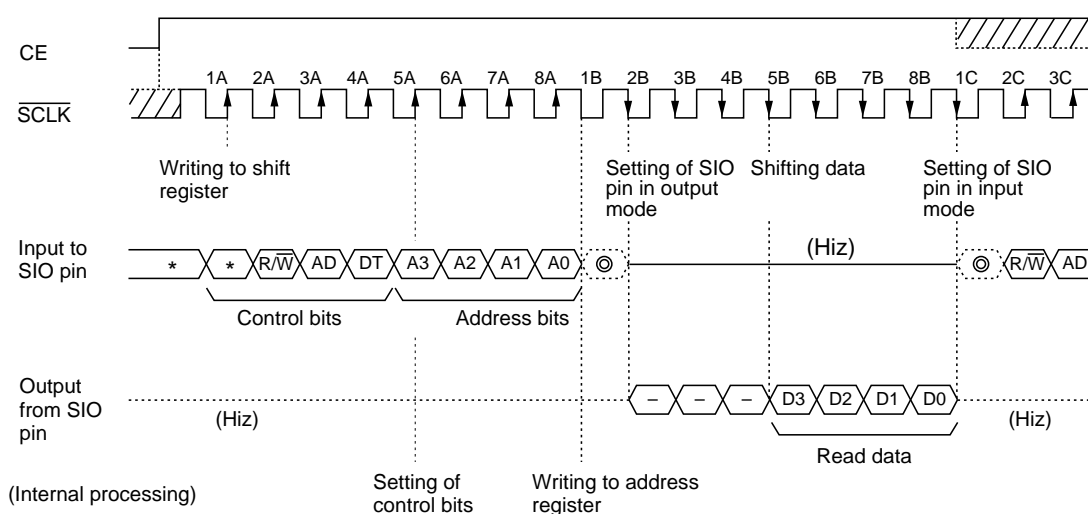
### 3. Read Data (For the RS5C316B)

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the  $\overline{\text{SCLK}}$  pin. The input data are registered in synchronization with the rising edge of the  $\overline{\text{SCLK}}$ . When the data is read, the read cycle shall be set by control bits then registered data can be read out from SIO pin in synchronization with the falling edge of the  $\overline{\text{SCLK}}$ .

- **Control bits**
  - R/ $\overline{\text{W}}$ : Establishes the read mode when set to 1, and the write mode when set to 0.
  - AD: Writes succeeding addressing bits (A3-A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  - DT: Writes data bits to counter or register specified by the address register set just before when set to 1 with the R/ $\overline{\text{W}}$  and AD bits set equally to 0 and performs no such write operation in any other case.
- **Address bits**
  - A3-A0: Inputs the bits MSB to LSB in the address table describing the functions.

#### 3.1 Read Cycle Flow

1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/ $\overline{\text{W}}$  and AD are set equally to 1 while a control bit DT is set to 0. (see the  $\overline{\text{SCLK}}$  1A-8A)
3. The SIO pin enters the output mode at the falling edge of the shift clock pulse 2B from the  $\overline{\text{SCLK}}$  pin while the four read bits (MSB  $\rightarrow$  LSB) at designated addresses are output at the falling edge of the shift clock pulse 5B. (see the figure below)
4. Then, the SIO pin returns to the input mode at the falling edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from “H” to “L” (after  $t_{\text{CEH}}$  from the rising edge of the eighth shift clock pulse from the  $\overline{\text{SCLK}}$  pin). Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at “H”.



- \*) In the above figure, the “\*” mark indicates arbitrary data; the “-” mark indicates unknown data.  
 The “⊙” mark indicates data which are available when the SIO pin is held at “H”, “L”, or Hiz level.  
 The diagonally shaded area of the CE and the  $\overline{\text{SCLK}}$  pins indicate “H” or “L”.

## 4. Write Data (For the RS5C316B)

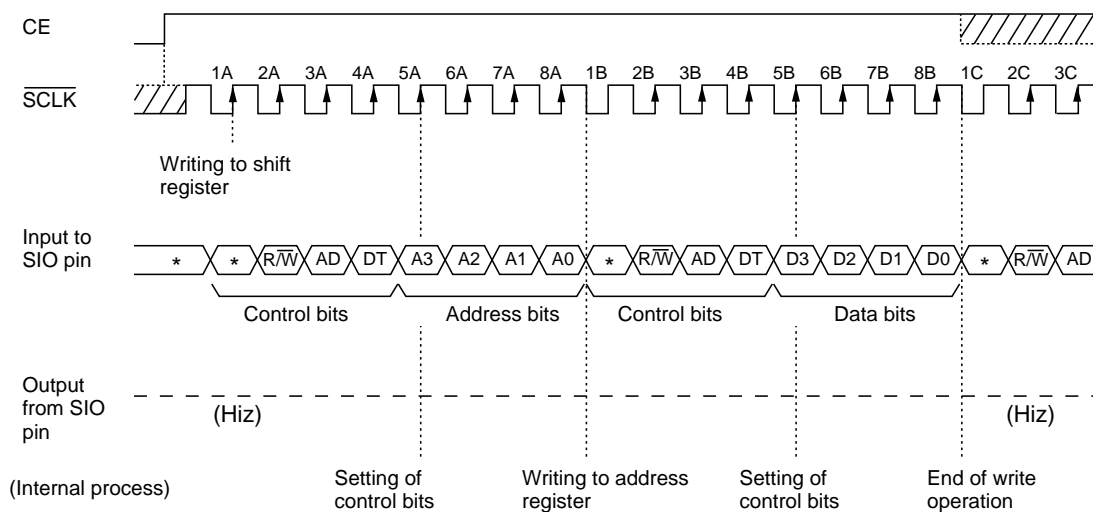
Writing data to the real-time clock requires inputting setting data (control bits, address bits and data bits) to the SIO pin and then establishing the write mode by using a control bit  $R/\overline{W}$  in the same manner as in read operation.

\*) Control bits and address bits are described in the previous section on read cycle.

- **Data bits** D3-D0: Inputs the data bits MSB to LSB in the addressing table describing the functions

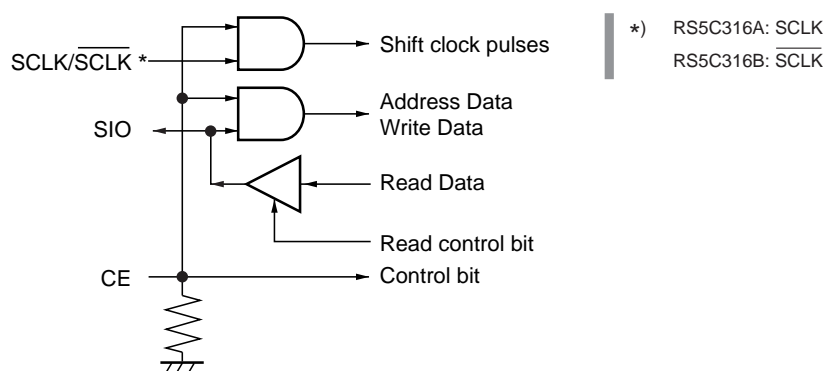
### 4.1 Write Cycle Flow

1. The CE pin is switched from “L” to “H”.
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits  $R/\overline{W}$  and DT are set equally to 0 while a control bit AD is set to 1. (see the  $\overline{SCLK}$  1A-8A)
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits  $R/\overline{W}$  and AD are set equally to 0 while a control bit DT is set to 1. (see the  $\overline{SCLK}$  1B-8B)
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits  $R/\overline{W}$ , AD, and DT are set equally to 0 (at the rising edge of shift clock pulse 5A and later from the  $\overline{SCLK}$  pin) or the CE pin is switched from “H” to “L” (after  $t_{CEH}$  from the rising edge of the eighth shift clock pulse from the  $\overline{SCLK}$  pin). Following on write cycle, read operation can be performed by setting control bits in the read mode at the shift clock pulse 1C and later with the CE pin held at “H”.



\*) In the above figure, the “\*” mark indicates arbitrary data; and the diagonally shaded area of CE and  $\overline{SCLK}$  indicates “H” or “L”.

## 5. CE Pin

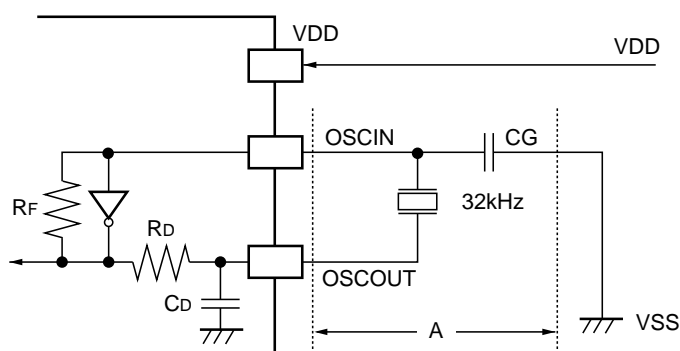


- 1) Switching the CE pin to the high level enables the SCLK/ $\overline{\text{SCLK}}$  and SIO pins, allowing data to be serially read from and written to the SIO pin in synchronization with shift clock pulses input from the SCLK/ $\overline{\text{SCLK}}$  pin.
- 2) Switching the CE pin to the low level or opening disables the SCLK/ $\overline{\text{SCLK}}$  and SIO pins, causing high impedance and resetting the internal interfacing circuits such as the shift register. While data of the address register and bank bit which have been written just before should be preserved.
- 3) The CE pin should be held at the low level or open state when no access is made to the RS5C316.  
The CE pin incorporates a pull-down resistor.
- 4) During system power-down (being back-up battery powered), the low-level input of the CE pin should be brought as close as possible to the VSS level to minimize the loss of charge in the battery.
- 5) Holding the CE pin at the high level for more than 2.5 seconds mainly forces 1Hz interrupt pulses to be output from the INTR pin for oscillation frequency measurement. When the CE pin is held at the high level for less than 1.5 seconds, no pulse is output.
- 6) The CE pin should be held at the low level in order to enable oscillator halt sensing. Holding the CE pin at the high level, therefore, disables oscillator halt sensing, retaining the value of the XSTP (oscillator halt sensing) bit which exists immediately before the CE pin is switched to the high level.

### Considerations

When the power turns on from 0V, the CE pin should be set low or open once.

## 6. Configuration of Oscillating Circuit



Typical external device:

X'tal : 32.768kHz

(R<sub>1</sub>=30kΩ TYP.)

(C<sub>L</sub>=6pF to 8pF)

C<sub>G</sub>=8pF to 20pF

Typical values of internal devices

R<sub>F</sub>=15MΩ (TYP.)

R<sub>D</sub>=60kΩ (TYP.)

C<sub>D</sub>=10pF (TYP.)

- \*) The oscillation circuit is driven at a constant voltage of about 1.5V relative to the Vss level.  
Consequently, it generates a wave form having a peak-to-peak amplitude of about 1.5V on the positive side of the Vss level.

### Considerations in Mounting Components Surrounding Oscillating Circuit

- 1) Mount the crystal oscillators and C<sub>G</sub> in the closest possible position to the IC.
- 2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with "← A →" in the above figure).
- 3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the PCB.
- 4) Avoid using any long parallel line to wire the OSCIN or OSCOUT pin.
- 5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

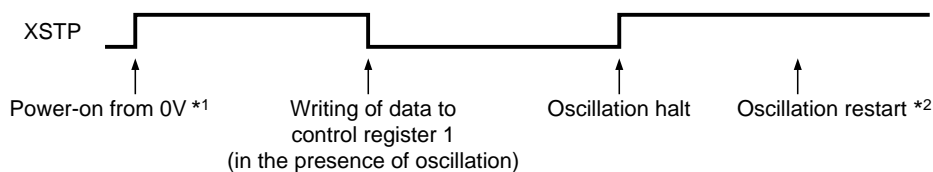
### Other Relevant Considerations

- 1) When applying an external input of clock pulses (32.768kHz) to the OSCIN pin:  
DC coupling .....Prohibited due to mismatching input levels.  
AC coupling.....Permissible except that unpredictable results may occur in oscillator halt sensing due to possible sensing errors caused by noises, etc.
- 2) Avoid using the oscillator output of the RS5C316 (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation.



## 7. Oscillator Halt Sensing

Oscillation Halt can be sensed through monitoring the XSTP bit with preceding setting of the XSTP bit to 0 by writing any data to the control register 1. Upon oscillator halt sensing, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity.



\*1) While the CE pin is held at the low level, the XSTP bit is set to 1 upon power-on from 0V.

Note that any instantaneous power disconnection may cause operational failure. When the CE pin is held at the high level, oscillation halt is not sensed and the value of the XSTP bit when the CE pin is held at the low level is retained.

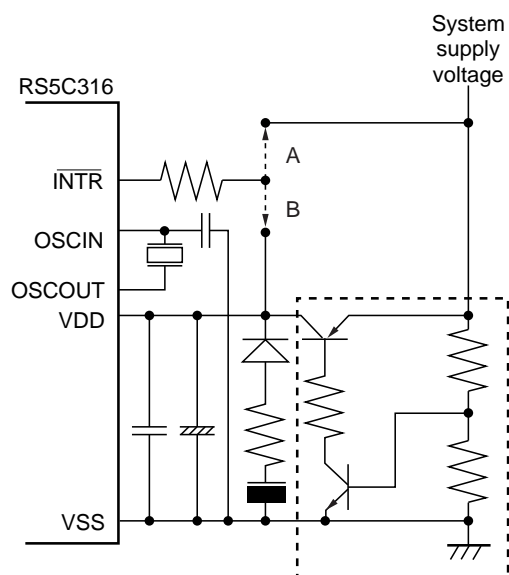
\*2) Once oscillation halt has been sensed, the XSTP bit is held at 1 even if oscillation is restarted.

### Considerations in Use of XSTP Bit

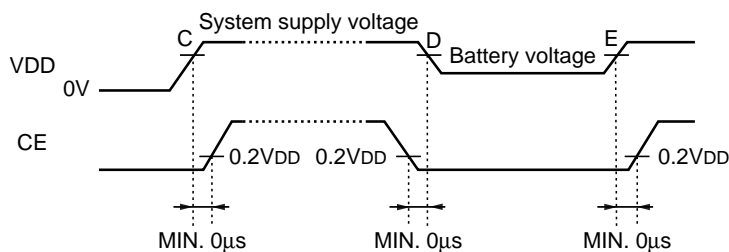
Ensure error-free oscillation halt sensing by preventing the following:

- 1) Instantaneous disconnection of VDD
- 2) Condensation on the crystal oscillator
- 3) Generation of noise on the PCB in the crystal oscillator
- 4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC

## 8. Typical Power Supply Circuit



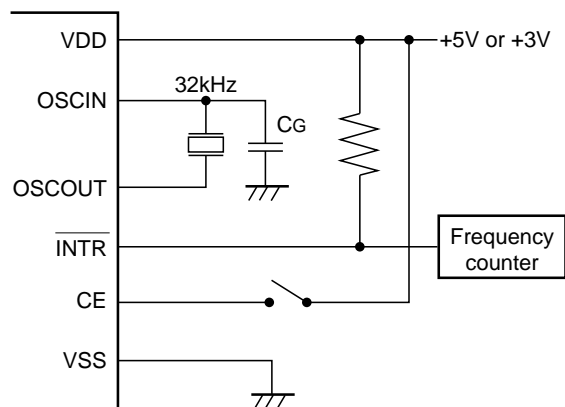
- 1) Connect the capacitance of the oscillation circuit to the Vss pin.
- 2) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C316.
- 3) Connect the pull-up resistor of the  $\overline{\text{INTR}}$  pin to two different positions depending on whether the resistor is in use during battery back-up.
  - When not in use during battery back-up  
.....Position A in the left figure
  - When in use during battery back-up  
.....Position B in the left figure
- 4) Timing of power-on, power-off and CE pin refer to following figure.
- 5) When a diode are in use in place of the components surrounded by dotted lines, note that applying voltage to any input pins should be less than the rating of  $\text{VDD} + 0.3\text{V}$  by using of schotkky diode.



C, D, E: Minimum operating voltage for CPU

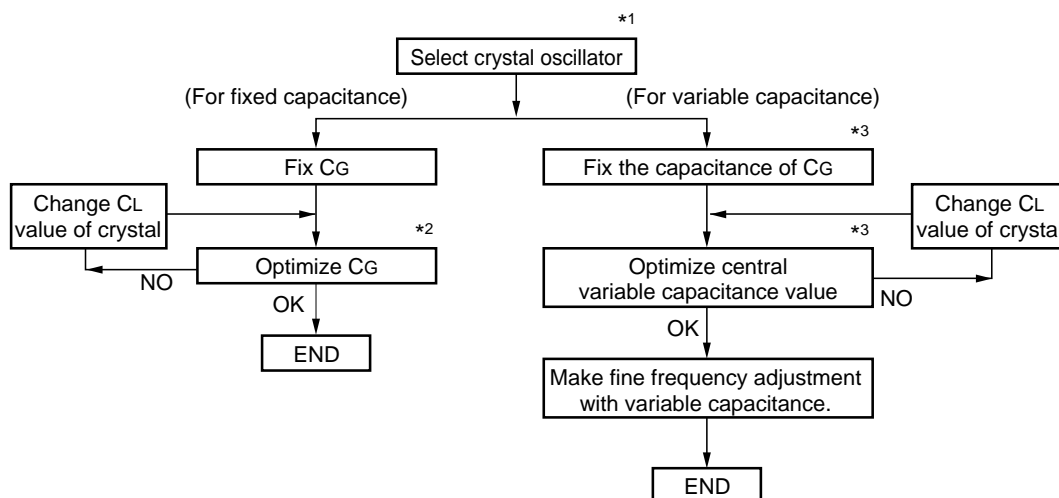
## 9. Oscillation Frequency Adjustment

### 9.1 Oscillation Frequency Measurement



- 1) Switch the CE pin to the high level and use a frequency counter to measure a 1Hz interrupt pulse output from the  $\overline{\text{INTR}}$  pin about 2.5 seconds later.
- 2) Ensure that the frequency counter has more than six digits (on the order of 1 ppm).
- 3) Place the CG between the OSCIN pin and the VSS level and pull up the  $\overline{\text{INTR}}$  pin output to the VDD.

## 9.2 Oscillation Frequency Adjustment



- \*1) To ensure that the crystal is matched to the IC, inquire its crystal supplier about its  $C_L$  (load capacitance) and  $R_1$  (equivalent series resistance) values. It is recommended that the crystal should have the  $C_L$  value range of 6 to 8pF and the typical  $R_1$  value of 30kΩ.
- \*2) To allow for the possible effects of floating capacitance, select the optimum capacitance of the  $C_G$  on the mounted PCB. The standard and recommendable capacitance values of the  $C_G$  range from 5 to 24pF and 8 to 20pF, respectively. When you need to change the frequency to get higher accuracy, change the  $C_L$  value of the crystal.
- \*3) Collate the central variable capacitance value of the  $C_G$  with its oscillation frequency by adjusting the angle of rotation of the variable capacitance of the  $C_G$  in such a manner that the actual variable capacitance value is slightly smaller than the central variable capacitance value. (It is recommended that the central variable capacitance value should be slightly less than one half of the actual variable capacitance value because the smaller is variable capacitance, the greater are fluctuations in oscillation frequency.) In the case of an excessive deviation of the oscillation frequency from its required value, change the  $C_L$  value of the crystal.

After adjustment, oscillation frequency is subject to fluctuations of an ambient temperature and supply voltage. See “12. Typical Characteristic Measurements”.

### Note

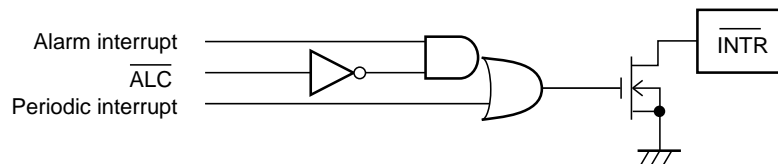
Any rise or fall in ambient temperature from its reference value ranging from 20 to 25 degrees Celsius causes a time delay for a 32kHz crystal oscillator. It is recommendable, therefore, to set slightly high oscillation frequency at room temperature.

## 10. Interrupt Operation

Two interrupt operations are available:

- 1) Alarm interrupt.....When a registered time for alarm (such as day-of-the-week, hour or minute) coincide with calendar counter (such as day-of-the-week, hour or minute) interrupt to the CPU are requested with  $\overline{\text{INTR}}$  pin being "L" (ON).
- 2) Periodic interrupt .....The  $\overline{\text{INTR}}$  pin comes to a "L" (ON) state every registered period outputting interrupt request.

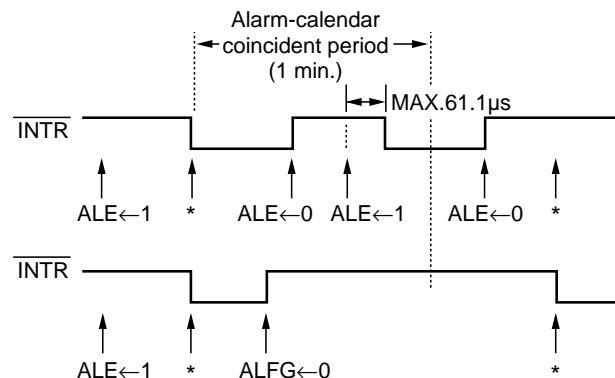
Function diagram of alarm and periodic interrupts are shown as follows:



- \*1) Setting the  $\overline{\text{ALC}}$  into 1 halt output of the alarm interrupt from  $\overline{\text{INTR}}$  pin.
- \*2) Both of alarm and periodic interrupt can operate regardless of the state of CE pin, "H" or "L".

### 10.1 Alarm Interrupt

For setting an alarm time, designated time such as day-of the week, hour or minute should be set to the alarm registers being ALE bit to 0. After that set the ALE bit to 1, from this moment onward when such registered alarm time coincide with the value of calendar counter the  $\overline{\text{INTR}}$  comes down to "L" (ON). The INTR output can be controlled by operating to the ALE and ALFG bits.



- \*1) The "\*" mark indicates the time when the registered alarm day-of-the-week and time coincide with calendar counter.
- \*2) Above figure describes in case of no periodic interruption.
- \*3) ALFG indicates a reverse state of  $\overline{\text{INTR}}$  output.

## 10.2 Periodic (Clock) Interrupt

The  $\overline{\text{INTR}}$  pin output, the interrupt cycle register, and the CTFG bit can be used to interrupt the CPU in a certain cycle. The interrupt cycle register can be used to select either one of two interrupt output modes: the pulse mode (when the CT3 bit is set to 0) and the level mode (when the CT3 bit is set to 1).

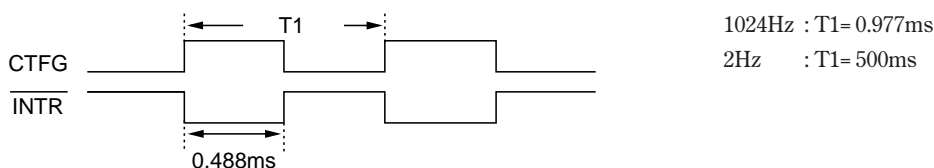
### 10.2-1 Interrupt Cycle Selection

Interrupt cycle register				$\overline{\text{INTR}}$ output	Description
CT3	CT2	CT1	CT0		
0	* <sup>*1</sup>	0	0	OFF	Interrupt halt
0	*	0	1	ON	Fixing the $\overline{\text{INTR}}$ pin to the low level
0	*	1	0	0.977ms	Cycle: 0.977ms (1/1024Hz) Duty 50%
0	*	1	1	0.5s	Cycle: 0.5s (1/2Hz)
1	0	0	0	1s	Every second
1	0	0	1	10s	Every 10 seconds (For display of second digits: 00, 10, 20, 30, 40 and 50)
1	0	1	0	1 minute	Every minute (00 second)
1	0	1	1	10 minutes	Every 10 minutes (For display of minute digits: 00, 10, 20, 30, 40 and 50)
1	1	0	0	1 hour	Every hour (00 minute and 00 second)
1	1	0	1	1 day	Every day (0 hour, 00 minute and 00 second a.m.)
1	1	1	0	1 week	Every week (0 week, 0 hour, 00 minute and 00 second a.m.)
1	1	1	1	1 month	Every month (1st day, 0 hour, 00 minute and 00 second a.m.)

\*1) The "\*" mark indicates 0 or 1.

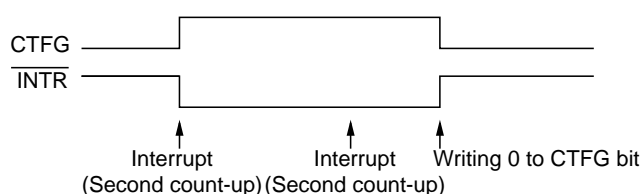
### 10.2-2 Pulse mode Interrupt

When the CT3 bit is set to 0 and provides four interrupt cycles, off, on, 1024Hz, and 2Hz can be selected. The CTFG bit cannot be set because it is used for output monitoring.

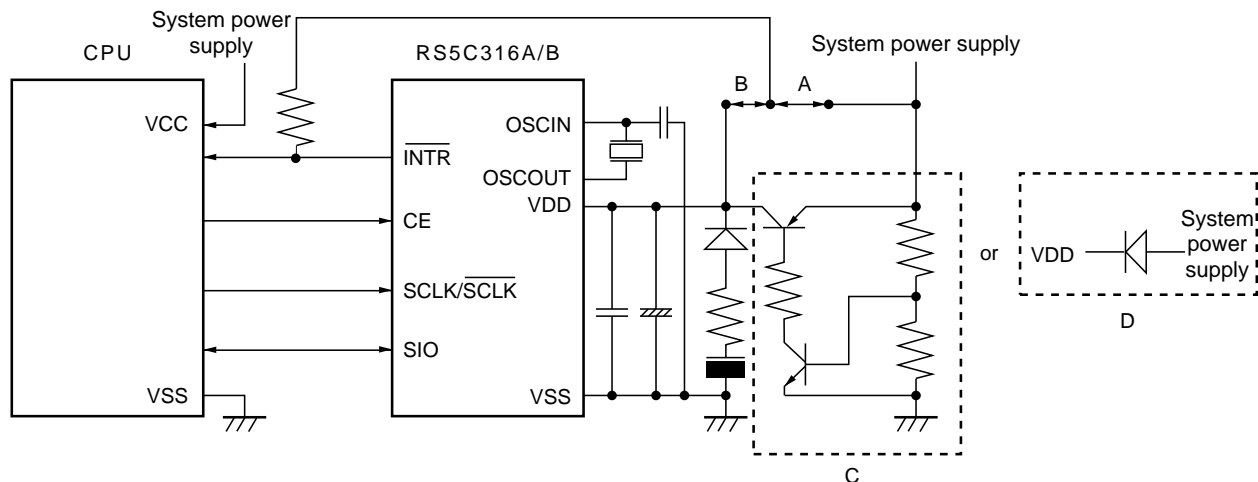


### 10.2-3 Level mode Interrupt

When the CT3 bit is set to 1, clock-interlocked cycles in increments of one second to one month can be selected. The CTFG bit can be written; writing 1 to the CTFG bit switches the  $\overline{\text{INTR}}$  pin to the low level while writing 0 to the CTFG bit turns off the  $\overline{\text{INTR}}$  pin.

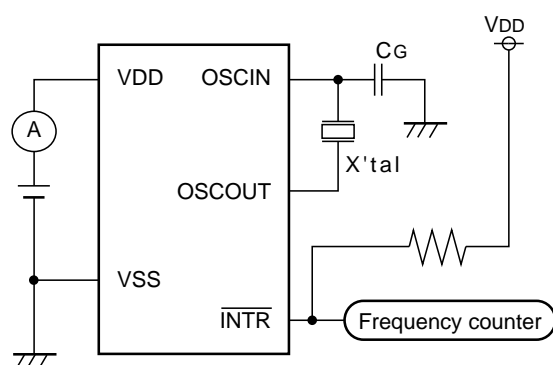


## 11. Typical Application



- \*1) Connect the capacitance of the oscillation circuit to the VSS pin.
- \*2) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C316.
- \*3) Connect the pull-up resistor of the  $\overline{\text{INTR}}$  pin to two different positions depending on whether the resistor is in use during battery back-up:
  - (I) When not in use during battery back-up .....Position A in the above figure
  - (II) When in use during battery back-up .....Position B in the above figure
- \*4) When using a "D" circuit in place of "C", note that forward voltage of diode should be minimized to eliminate applying excess voltage to input pins.  
(Take the utmost care on system powering-ON and-OFF).

## 12. Typical Characteristic Measurements



$C_G = 10\text{pF}$

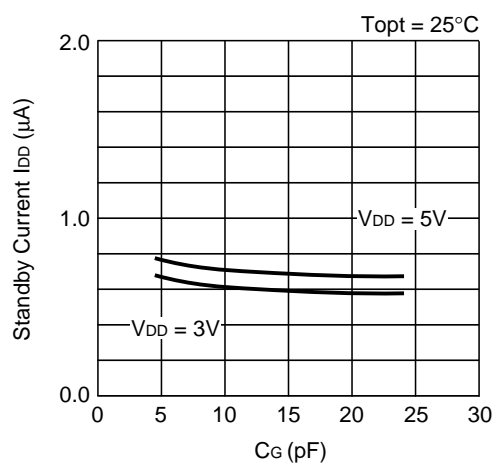
$X'tal : R_1 = 30\text{k}\Omega$

$T_{opt} = 25^\circ\text{C}$

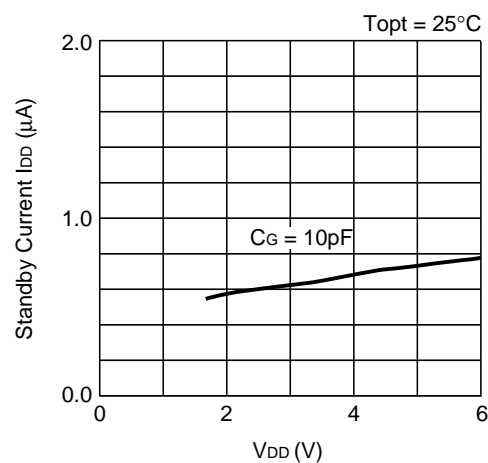
Input Pin : VDD or VSS

Output Pin : Open

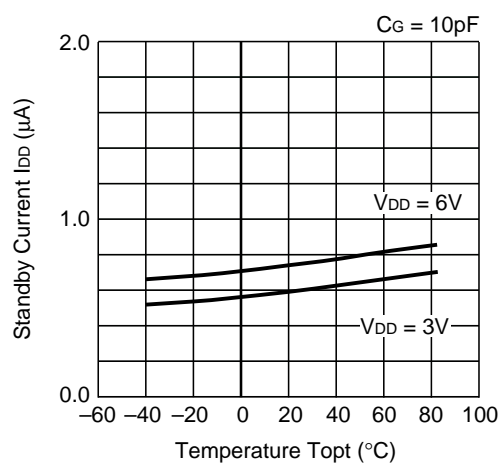
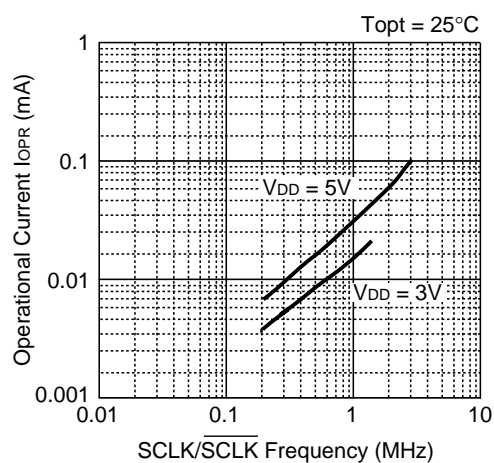
### 12.1 Standby Current vs. $C_G$



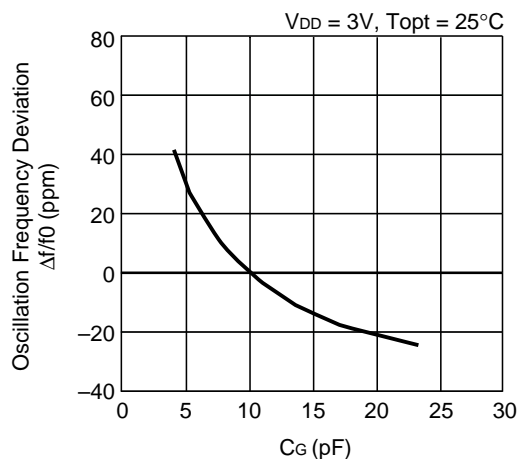
### 12.2 Standby Current vs. $V_{DD}$



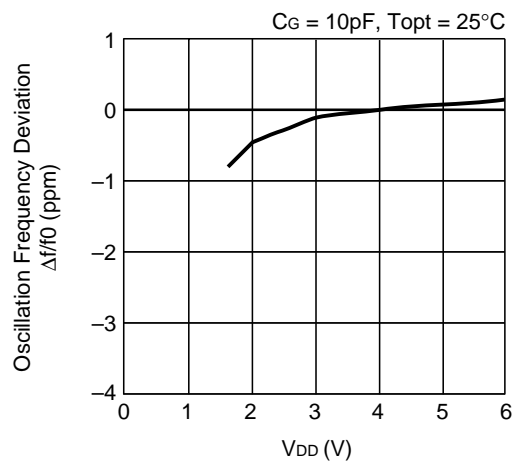
### 12.3 Operational Current vs. SCLK/SCLK Frequency 12.4 Standby Current vs. Temperature



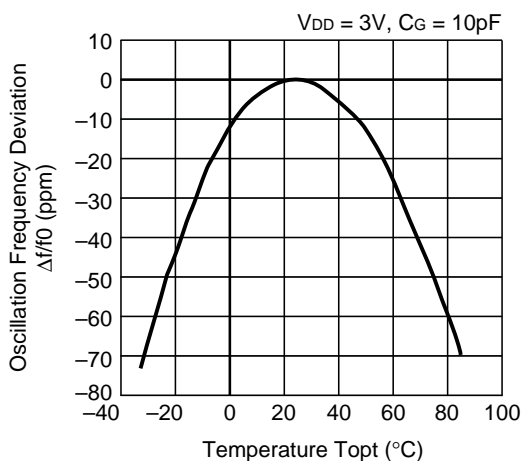
### 12.5 Oscillation Frequency Deviation vs. $C_G$ ( $f_0$ : $C_G=10\text{pF}$ reference)



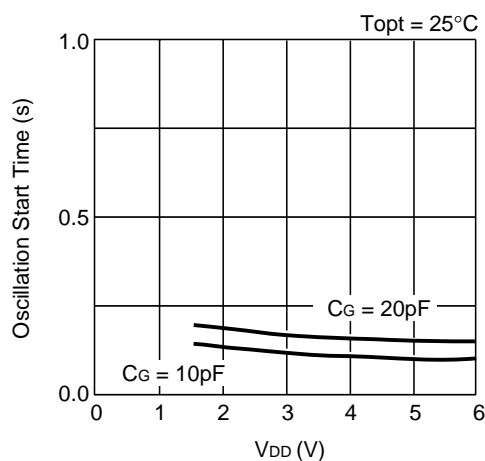
### 12.6 Oscillation Frequency Deviation vs. $V_{DD}$ ( $f_0$ : $V_{DD}=4\text{V}$ reference)



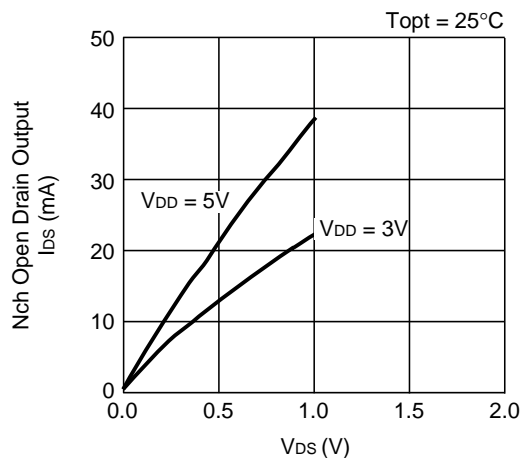
### 12.7 Oscillation Frequency Deviation vs. Temperature ( $f_0$ : $T_{opt}=25^\circ\text{C}$ reference)



### 12.8 Oscillation Start Time vs. $V_{DD}$



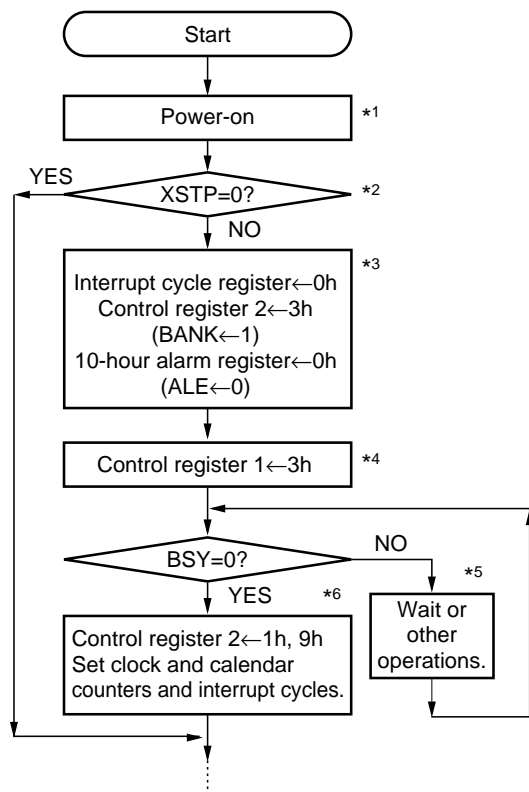
### 12.9 $V_{DS}$ vs. $I_{DS}$ for Nch Open Drain Output





## 13. Typical Software-based Operations

### 13.1 Initialization upon Power-on



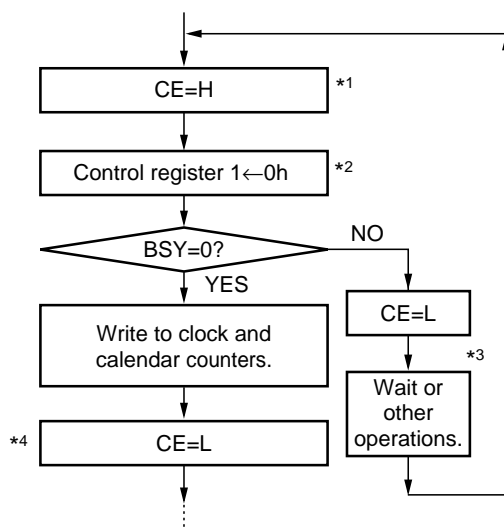
- \*1) Switch the CE pin to the low level immediately after power-on.
- \*2) When not making oscillation halt sensing (data validity), the XSTP bit need not be checked.
- \*3) Turn off the  $\overline{\text{INTR}}$  pin, whose output is uncertain at power-on.
- \*4) Set the ADJ bit to 1. When writing control register 1, if the oscillator has operated, the XSTP bit is changed from 1 to 0.
- \*5) It takes about 0.1 to 2 seconds to be set the BSY bit to 0 from oscillation starting upon power-on from 0V. Provide an exit from an oscillation start loop to prepare for oscillation failure.
- \*6) Set the XSTP bit to 0 by writing data to the control register 1, and set to the control register 2,  
0h for the 12-hour time display system.  
4h for the 24-hour time display system.

#### When Using the XSTP Bit

Ensure stable oscillation by preventing the following:

- 1) Condensation on the crystal oscillator
- 2) Instantaneous disconnection of power
- 3) Generation of clock noises, etc, in the crystal oscillator
- 4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

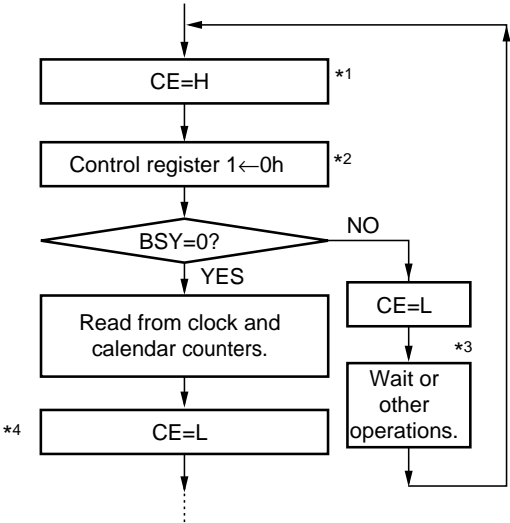
### 13.2 Write Operation to Clock and Calendar Counters



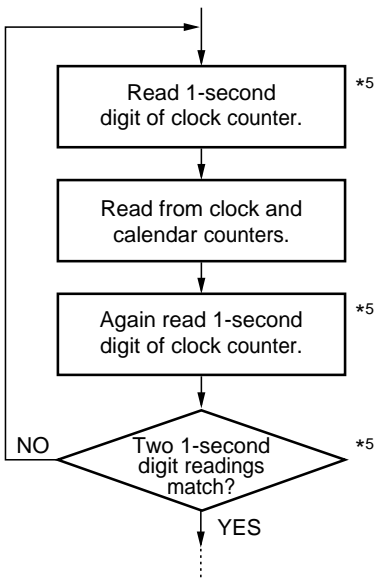
- \*1) After switching the CE pin to the high level, hold it at the high level until any subsequent operation requires switching it to the low level. (Note that switching the CE pin to the low level sets the WTEN bit to 1.)
- \*2) WTEN bit is set to 0.
- \*3) The BSY bit is held at 1 for a maximum duration of 122.1μs.
- \*4) Switch the CE pin to the low level to set the WTEN bit to 1. During write operation to the clock and calendar counters, one 1-second digit carry causes a 1-second increment while two 1-second digit carries also cause only a 1-second increment, which, in turn, causes a time delay.

13.3 Read Operation from Clock and Calendar Counters

13.3-1



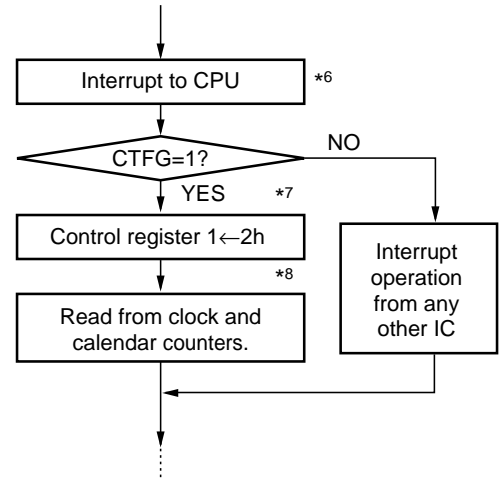
13.3-2



Note

Read data as described in 13.3-2 or 13.3-3 when it takes (1/1024) sec or more to set the WTEN bit from 0 to 1 (CE=L), the read operation described in 13.3-1 is prohibited as such a case.

13.3-3



\*1) to \*4) These notes are the same as 13.2 notes \*1) to \*4).

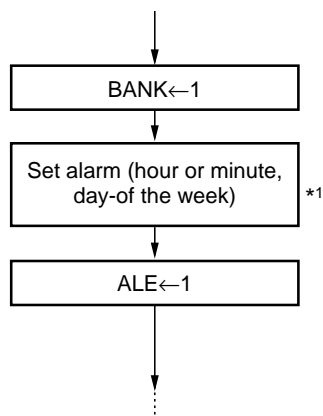
\*5) When needing any higher-order digits than the minute digits, replace second digits with minute digits. (Reading LSD one of the required digits twice.)

\*6) Select the level mode as an interrupt mode by setting the CT3 bit to 1.

\*7) Write 0 to CTFG bit for turning off INTR pin.

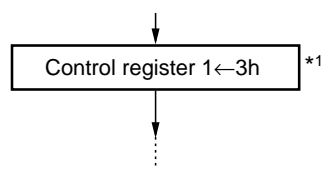
\*8) Complete read operation within an interrupt cycle after interrupt generation. (e.g. within 1 second)

### 13.4 Write Operation to Alarm time



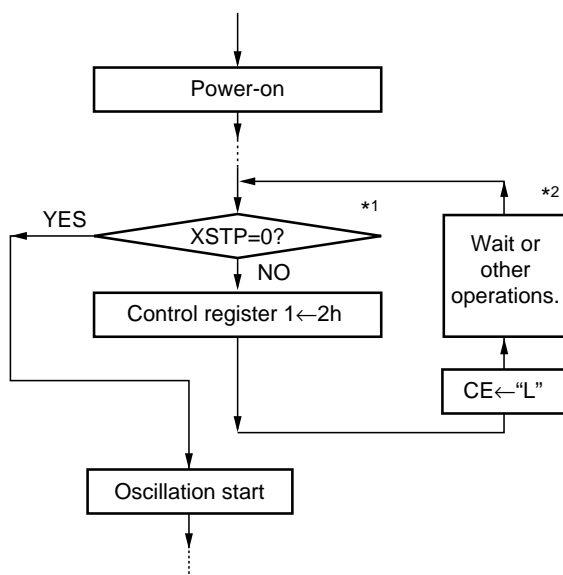
\*1) Non-existent alarm time can set in the alarm registers, but when it sets, an alarm interrupt is disabled. To enable an alarm interrupt, existent alarm time must be set in the alarm registers.

### 13.5 Second-digit Adjustment by $\pm 30$ seconds



\*1) Set the ADJ bit to 1.  
(The BSY bit is held at 1 for a maximum duration of 122.1 $\mu$ s after the ADJ bit is set to 1.)

### 13.6 Oscillation Start Judgment



\*1) The XSTP bit is set to 1 upon power-on from 0V.

\*2) It takes approximately 0.1 to 2 seconds to start oscillation. Provide an exit from an oscillation start loop to prepare for oscillation failure.

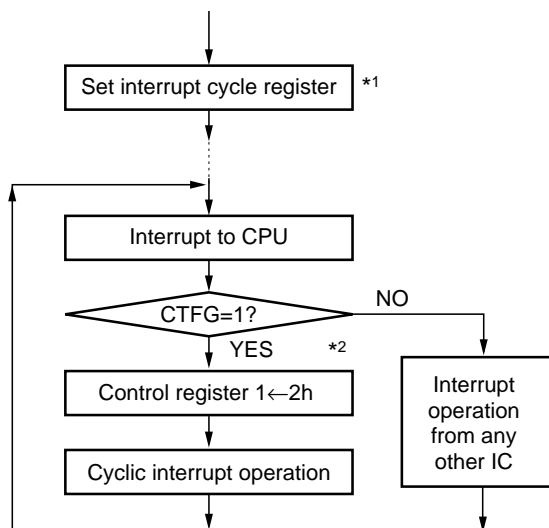
#### When Using the XSTP Bit

Ensure stable oscillation by preventing the following:

- 1) Condensation on the crystal oscillator
- 2) Instantaneous disconnection of power
- 3) Generation of clock noises, etc, in the crystal oscillator
- 4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

## 13.7 Interrupt Operation

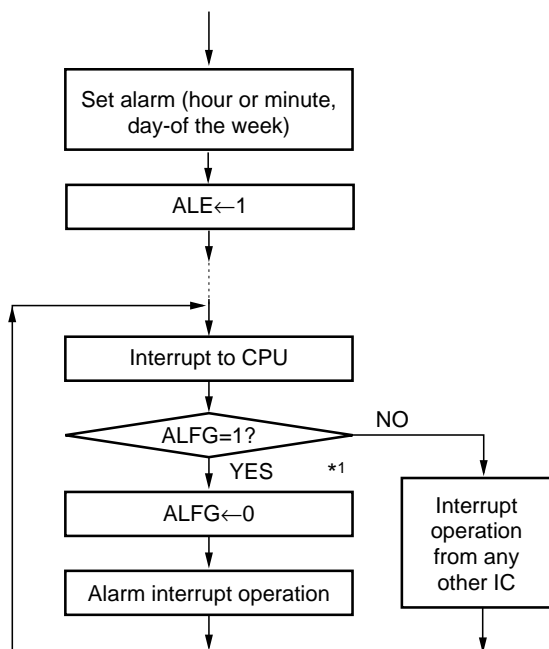
### 13.7-1 Cyclic Interrupt Operation



\*1) Set the interrupt cycle register to the level mode by setting the CT<sub>3</sub> bit to 1.

\*2) Write 0 to CTFG bit for turning off  $\overline{\text{INTR}}$  pin.

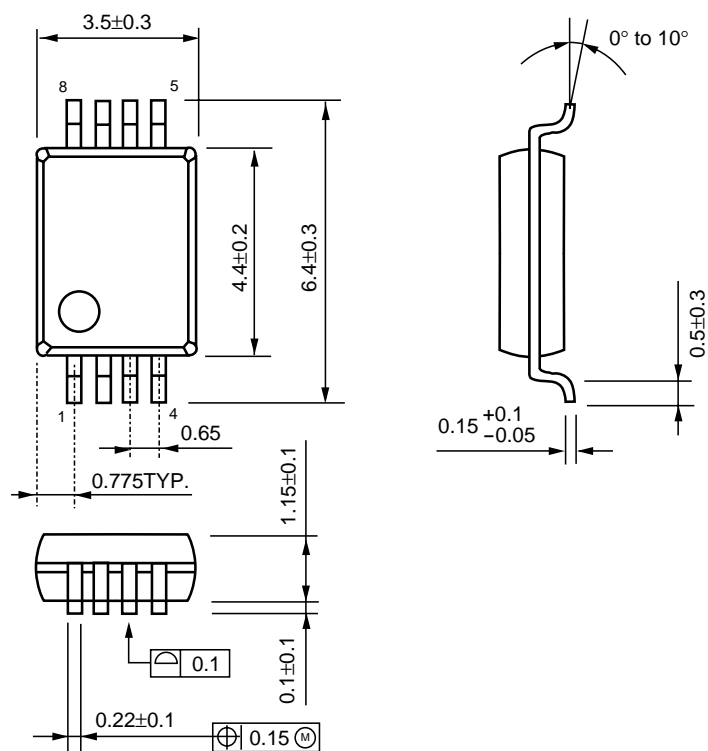
### 13.7-2 Alarm Interrupt Operation



\*1) Write 0 to ALFG bit for turning off  $\overline{\text{INTR}}$  pin.

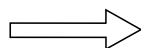
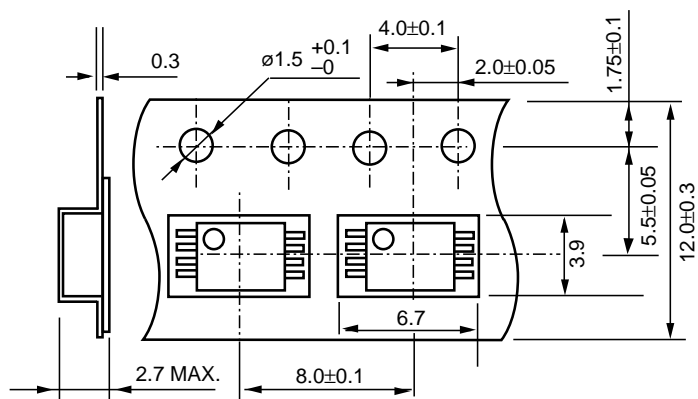
## PACKAGE DIMENSIONS (Unit: mm)

• RS5C316A/B (8pin SSOP, 0.65mm pitch)



## TAPING SPECIFICATION (Unit: mm)

The RS5C316A/B have one designated taping direction. The product designations for the taping components are “RS5C316A-E2” and “RS5C316B-E2”.



User Direction of Feed.



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**RICOH COMPANY, LTD.**  
**ELECTRONIC DEVICES DIVISION**

**HEADQUARTERS**

13-1, Himemuro-cho, Ikeda City, Osaka 563-8501, JAPAN  
Phone +81-727-53-6003 Fax +81-727-53-2120

**YOKOHAMA OFFICE** (International Sales)

3-2-3, Shin-Yokohama, Kohoku-ku, Yokohama City, Kanagawa 222-8530,  
JAPAN

Phone +81-45-477-1697 Fax +81-45-477-1694 · 1695

<http://www.ricoh.co.jp/LSI/english/>

**RICOH CORPORATION**  
**ELECTRONIC DEVICES DIVISION**

**SAN JOSE OFFICE**

1996 Lundy Avenue, San Jose, CA 95131, U.S.A.

Phone +1-408-944-3306 Fax +1-408-432-8375

<http://www.ricoh-usa.com/semicond.htm>