ULTRA-COMPACT HIGH PERFORMANCE SERIAL REAL-TIME CLOCK ICs

RS5C317A/B

APPLICATION MANUAL

RICOH

ELECTRONIC DEVICES DIVISION

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June 1995

RS5C317A/B

APPLICATION MANUAL

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ULTRA-COMPACT HIGH PERFORMANCE SERIAL REAL-TIME CLOCK ICs

RS5C317A/B

OUTLINE

The RS5C317A/B are CMOS type real-time clock ICs which are connected to the CPU via three signal lines and capable of serial transmission of clock and calendar data to the CPU.

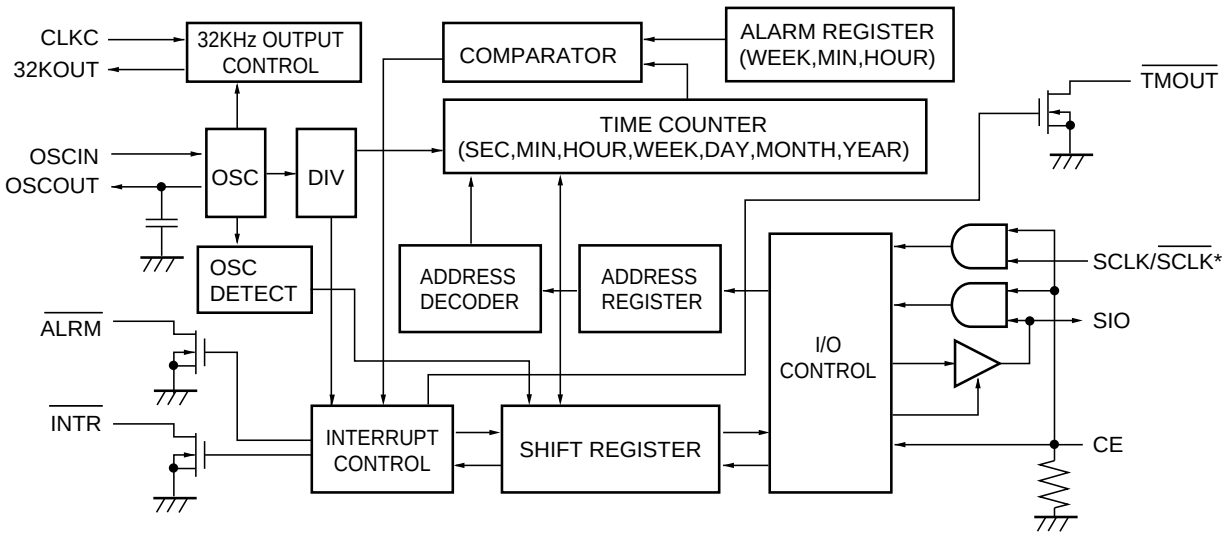
The RS5C317A/B can generate various periodic interrupt clock pulses lasting for long period (one month), further alarm interrupt can be made by days of the week, hours, and minutes. The function of 32kHz clock output and timer counter for watch-dog-timer are also include. Driving an oscillation circuit at constant voltage, the circuit undergoes few voltage fluctuations and consequently realizes low current consumption (0.6µA at 3V). It also provides an oscillator halt sensing function for application to data validity at power-on and other occasions. Integrated into a compact and thin 14pin SSOP (0.65mm pitch), the RS5C317A/B are the optimum choice for equipment requiring small size and low power consumption.

The RS5C317A and the RS5C317B reads/writes data at falling and rising edge of serial clock respectively.

FEATURES

- Time keeping voltage 1.6V to 6.0V
- Lowest supply current 0.6µA TYP. (1.5µA MAX.) at 3V
- Connection to the CPU via only three pins: CE, SCLK/$\overline{\text{SCLK}}$ and SIO for addressing and data read/write
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in BCD code
- Periodic interrupt pulses to the CPU with cycles ranging from one month to 1/1024Hz, with interrupt flags and interrupt halt
- Alarm interrupt (days of the week, hours, minutes)
- Counter for timer with internal clock
- Oscillator halt sensing to judge internal data validity
- 32kHz clock output with enable switch
- Second digit adjustment by ±30 seconds
- 12-hour or 24-hour time display selectable
- Automatic leap year recognition up to the year 2099
- CMOS logic
- Package: 14pin SSOP (0.65mm pitch)

BLOCK DIAGRAM



*) RS5C317A: SCLK RS5C317B: $\overline{SCLK}$

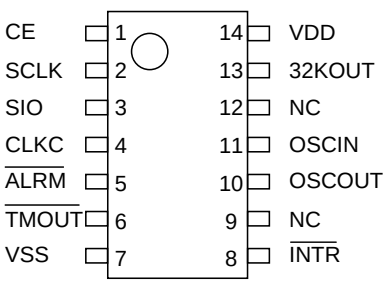
APPLICATIONS

- Communication equipment (Multi-function telephone, portable telephone, PHS, pager)
- Business machine (Facsimile, portable facsimile)
- Personal computer (Desktop type, notebook type, word processor, PDA, electronic notebook, TV games)
- Audio visual equipment (Portable audio equipment, video camera, camera, digital camera, remote control equipment)
- Home use (Rice cooker, microwave range)

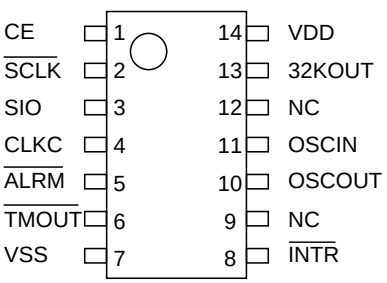
PIN CONFIGURATION

• 14pin SSOP (0.65mm pitch)

RS5C317A



RS5C317B



PIN DESCRIPTIONS

Pin No.	Symbol	Name	Description
1	CE	Chip enable input	The CE pin is used to interface the CPU and is accessible when held at the high level. This pin is connected to a pull-down resistor. It should be switched to the low level or opened when not accessed or when powering off the system. Holding the CE pin high for more than 2.5 seconds forces 1Hz interrupt pulses to be output from the $\overline{\text{INTR}}$ pin for oscillation frequency measurement. (No "1Hz pulse" is output for less than 1.5 seconds.)
2	SCLK (A type) $\overline{\text{SCLK}}$ (B type)	Shift clock input	This pin is used to input shift clock pulses to synchronize data input to, and output from, the SIO pin. SCLK and $\overline{\text{SCLK}}$ are for writing data at falling and rising edge of clock pulses respectively and also reading data at rising and falling edge of clock pulses respectively.
3	SIO	Serial input/output	The SIO pin inputs and outputs written or read data in synchronization with shift clock pulses from the SCLK/$\overline{\text{SCLK}}$ pin. The SIO pin causes high impedance when CE pin is held at the low level (CMOS input/output). After the CE pin is switched to the high level and the control bits and the address bits are input from the SIO, the SIO pin performs serial input and output operations.
8	$\overline{\text{INTR}}$	Interrupt output	The $\overline{\text{INTR}}$ pin outputs periodic interrupt pulses and alarm interrupt to the CPU. This pin functions as an Nch open drain output even when the CE pin is held at the low level.
5	$\overline{\text{ALRM}}$	Alarm output	The $\overline{\text{ALRM}}$ pin outputs alarm interrupt to the CPU. This pin functions as an Nch open drain output even when the CE pin is held at the low level.
6	$\overline{\text{TMOUT}}$	Timer output	$\overline{\text{TMOUT}}$ pin outputs timer counter output pulses for watch-dog-timer and free-run-timer. This pin functions as an Nch open drain output even when the CE pin is held at the low level. Timer function is disabled and $\overline{\text{TMOUT}}$ is OFF state when the RS5C317 is in the oscillation halt sensing state.
11 10	OSCIN OSCOUT	Oscillator circuit input/output	These pins configure an oscillator circuit by connecting a 32.768kHz crystal oscillator between the OSCIN and OSCOUT pins and by connecting a capacitor between the OSCIN and Vss pins. (Any other oscillator circuit components are built into the RS5C317A/B.)
13	32KOUT	32kHz output	32kHz clock output pin for peripheral circuit. The 32kHz clock output is controlled by CLKC pin and 32kHz control register. The 32KOUT pin outputs 32kHz clock when the CLKC pin is held at high and $\overline{\text{CLEN}}$=0, and this pin is held at high impedance state when the CLKC pin and $\overline{\text{CLEN}}$ is in any other states and even when the CLKC pin is open. CMOS output.
4	CLKC	Control input for 32kHz output	Control pin for an output of the 32KOUT pin. This pin incorporates a pull-down-resistor.
14 7	VDD VSS	Positive/Negative power supply input	V_{DD} and V_{SS} is connected to power supply and ground respectively.
9, 12	NC	No Connection	Ordinarily connected to V_{SS} pin.

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply voltage		–0.3 to +7.0	V
V_I	Input voltage		–0.3 to V_{DD}+0.3	V
V_{O1}	Output voltage 1	SIO, 32KOUT	–0.3 to V_{DD}+0.3	V
V_{O2}	Output voltage 2	$\overline{INTR}$, $\overline{ALRM}$, $\overline{TMOUT}$	–0.3 to +12	V
P_D	Power dissipation	Topt=25°C	300	mW
Topt	Operating temperature		–40 to +85	°C
Tstg	Storage temperature		–55 to +125	°C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Topt=–40 to +85°C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Supply voltage		2.5		6.0	V
V_{CLK}	Time keeping voltage		1.6		6.0	V
f_{XT}	Oscillation frequency			32.768		kHz
C_G	External oscillation capacitance	C_L value of crystal=6 to 8pF	5	10	24	pF
V_{PUP}	Pull-up voltage	$\overline{INTR}$, $\overline{ALRM}$, $\overline{TMOUT}$			10	V

DC CHARACTERISTICS

Unless otherwise specified: V_{SS}=0V, V_{DD}=3V, Topt=–40 to +85°C, Oscillation frequency=32.768kHz, (C_L=6pF, R_1=30kΩ), C_G=10pF

Symbol	Item	Pin name	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage	CE, SCLK/$\overline{SCLK}$, SIO, CLKC		0.8V_{DD}		V_{DD}	V
V_{IL}	"L" input voltage	CE, SCLK/$\overline{SCLK}$, SIO, CLKC		0		0.2V_{DD}	V
I_{OH}	"H" output current	SIO, 32KOUT	V_{OH}=V_{DD} –0.5V			–0.5	mA
I_{OL1}	"L" output current	SIO, 32KOUT	V_{OL1}=0.5V	0.5			mA
I_{OL2}		$\overline{INTR}$, $\overline{ALARM}$, $\overline{TMOUT}$	V_{OL2}=0.4V	1			
R_{DN}	Pull-down resistance	CE		45	150	450	kΩ
I_{IH}	Input current	CLKC	V_{IH}=3V		1	5	µA
I_{ILK}	Input leakage current	SCLK/$\overline{SCLK}$	V_I=V_{DD} or V_{SS}	–1		1	µA
I_{OZ1}	Output leakage current	SIO, 32KOUT	V_O=V_{DD} or V_{SS}	–2		2	µA
I_{OZ2}		$\overline{INTR}$, $\overline{ALARM}$, $\overline{TMOUT}$	V_O=10V	–5		5	
I_{DD1}	Standby current 1	V_{DD}	V_{DD}=3V Input/output: open		0.6	1.5	µA
I_{DD2}	Standby current 2	V_{DD}	V_{DD}=6V Input/output: open		0.8	2.0	µA
C_D	Internal oscillation Cap.	OSCOUT			10		pF

AC CHARACTERISTICS

(V_{SS}=0V, Topt=–40 to +85°C, C_L=50pF)

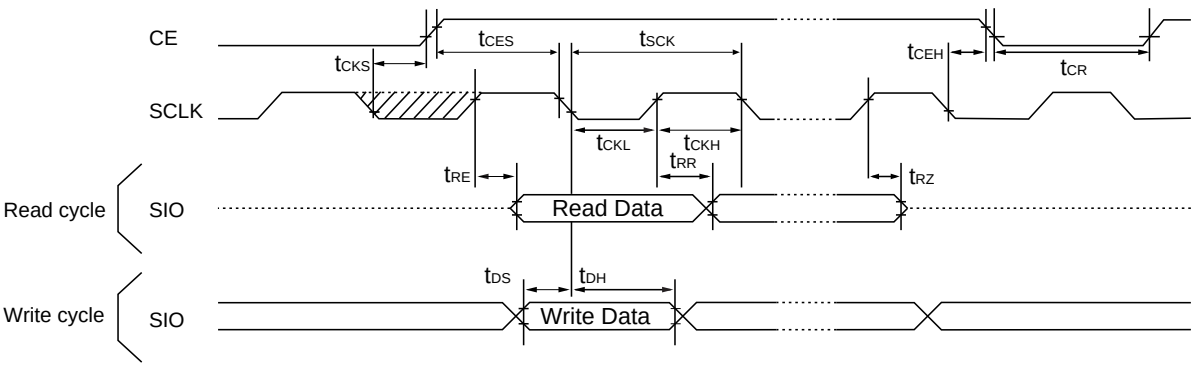
Symbol	Item	V_{DD}≥4.5V		V_{DD}≥4.0V		V_{DD}≥2.5V		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{CES}	CE set-up time	175		200		400		ns
t_{CEH}	CE hold time	175		200		400		ns
t_{CR}	CE inactive time	350		400		800		ns
t_{SCK}	SCLK clock cycle time	350		400		800		ns
t_{CKH}	SCLK high time	175		200		400		ns
t_{CKL}	SCLK low time	175		200		400		ns
t_{CKS}	SCLK to CE set-up time	60		80		120		ns
t_{RE}	Data output start time (from rising of SCLK) (from falling of $\overline{SCLK}$)		120		135		300	ns
t_{RR}	Data output delay time (from rising of SCLK) (from falling of $\overline{SCLK}$)		120		135		300	ns
t_{RZ}	Output floating time		120		135		300	ns
t_{DS}	Input data set-up time	50		60		120		ns
t_{DH}	Input data hold time	50		50		80		ns

TIMING CHARTS

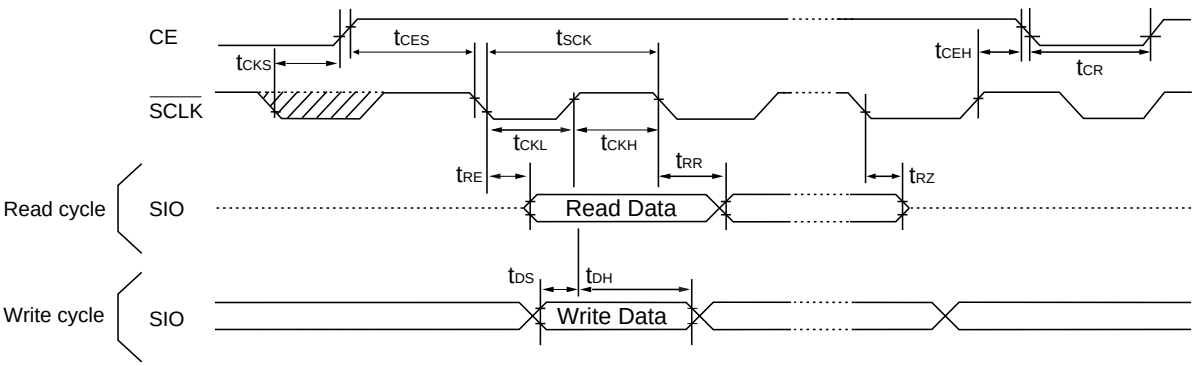
Input/output conditions: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, V_{OH}=0.8×V_{DD}, V_{OL}=0.2×V_{DD}

*) Any SCLK/$\overline{\text{SCLK}}$ state is allowed in the hatched area.

• RS5C317A



• RS5C317B



FUNCTIONAL DESCRIPTIONS

1. Addressing

	Address				Registers		Data *1			
	A3	A2	A1	A0			D3	D2	D1	D0
0	0	0	0	0	1-second counter	(BANK=0)	S_8	S_4	S_2	S_1
					Day-of-the-week alarm register 1	(BANK=1)	AW_3	AW_2	AW_1	AW_0
1	0	0	0	1	10-second counter	(BANK=0)	—*2	S_{40}	S_{20}	S_{10}
					Day-of-the-week alarm register 2	(BANK=1)	$\overline{ALC}$	AW_6	AW_5	AW_4
2	0	0	1	0	1-minute counter	(BANK=0)	M_8	M_4	M_2	M_1
					1-minute alarm register	(BANK=1)	AM_8	AM_4	AM_2	AM_1
3	0	0	1	1	10-minute counter	(BANK=0)	—	M_{40}	M_{20}	M_{10}
					10-minute alarm register	(BANK=1)	—	AM_{40}	AM_{20}	AM_{10}
4	0	1	0	0	1-hour counter	(BANK=0)	H_8	H_4	H_2	H_1
					1-hour alarm register	(BANK=1)	AH_8	AH_4	AH_2	AH_1
5	0	1	0	1	10-hour counter	(BANK=0)	—	—	P/$\overline{A}$, H_{20}	H_{10}
					10-hour alarm register	(BANK=1)	ALE	—	AP/$\overline{A}$, AH_{20}	AH_{10}
6	0	1	1	0	Day-of-the-week counter	(BANK=0)	—	W_4	W_2	W_1
7	0	1	1	1	Interrupt cycle register	(BANK=0, 1)	CT_3	CT_2	CT_1	CT_0
8	1	0	0	0	1-day counter	(BANK=0)	D_8	D_4	D_2	D_1
9	1	0	0	1	10-day counter	(BANK=0)	—	—	D_{20}	D_{10}
					Timer register *7	(BANK=1)	TM_3	TM_2	TM_1	TMCL
A	1	0	1	0	1-month counter	(BANK=0)	MO_8	MO_4	MO_2	MO_1
					32kHz control register *7	(BANK=1)	—	—	—	$\overline{CLEN}$ *8
B	1	0	1	1	10-month counter	(BANK=0)	—	—	—	MO_{10}
C	1	1	0	0	1-year counter	(BANK=0)	Y_8	Y_4	Y_2	Y_1
D	1	1	0	1	10-year counter	(BANK=0)	Y_{80}	Y_{40}	Y_{20}	Y_{10}
E	1	1	1	0	Control register 1	(BANK=0, 1)	CTFG	ALFG	$\overset{*6}{WTEN}/\overset{*4}{XSTP}$	ADJ/BSY*3
F	1	1	1	1	Control register 2	(BANK=0, 1)	$\overline{12}/24$	TMR	BANK *5	$\overline{TEST}$ *6

*1) All the listed data can be read and written.
*2) The "—" mark indicates data which can be read only and set to "0" when read.
*3) The ADJ/BSY bit of the control register is set to ADJ for write operation and BSY for read operation.
*4) The WTEN/XSTP bit of the control register is set to WTEN for write operation and XSTP for read operation.
*5) The clock/calendar counter and the alarm register can be selected when the BANK=0 and BANK=1 respectively. To designate the BANK is unnecessary for Interrupt cycle register and Control register 1/2.
*6) The WTEN bit and $\overline{TEST}$ bit are set to "1" when CE is "Low".
*7) When the crystal oscillator is stopped after initial power-on or supply voltage drop, XSTP=1, the timer register and $\overline{CLEN}$ bit of the 32kHz control register perform as follows:
$\overline{CLEN}$=0 TM3=TM2=TM1=TMCL=0 (Timer halts)
*8) The $\overline{CLEN}$ data can be read only and set to 0 when CLKC is "L".

2. Registers

2.1 Control Register 1 (at Eh)

D3	D2	D1	D0	
CTFG	ALFG	WTEN	ADJ	(For write operation)
CTFG	ALFG	XSTP	BSY	(For read operation)

±30-second Adjustment Bit

ADJ	Description
0	Ordinary operation
1	Second digit adjustment

Clock/Counter Busy-state Indication Bit

BSY	Description
0	Ordinary operation
1	Second digit carry or adjustment

Clock Counter Enable/Disable Setting Bit

WTEN	Description
0	Disabling of 1-second digit carry for clock counter
1	Enabling of 1-second digit carry for clock counter

Oscillator Halt Sensing Bit

XSTP	Description
0	Ordinary oscillation
1	Oscillator halt sensing

Alarm Flag Bit

ALFG	Description
0	Unmatched alarm register with clock counter
1	Matched alarm register with clock counter

Interrupt Flag Bit

CTFG	Description
0	$\overline{INTR}$=OFF enabling of write operation when CT_3 bit is set to 1
1	$\overline{INTR}$=L enabling of write operation when CT_3 bit is set to 1

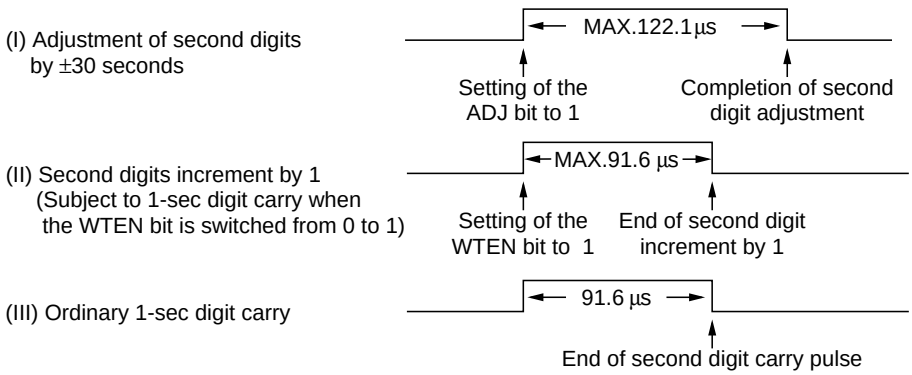
2.1-1 (ADJ)

The following operations are performed by setting the ADJ bit to 1.
After this bit is set to 1, the BSY bit is set to 1 for the maximum duration of 122.1µs.
If the WTEN bit is 0, these adjustment operations are started after the WTEN bit is set to 1.

1) For second digits ranging from “00” to “29” seconds:
   Time counters smaller than seconds are reset and second digits are set to “00”.
2) For second digits ranging from “30” to “59” seconds:
   Time counters smaller than seconds are reset and second digits are set to “00”. Minute digits are incremented by 1.

2.1-2 (BSY)

When the BSY bit is 1, the clock and calendar counter are being updated. Consequently, write operation should be performed for the counters when the BSY bit is 0. Meanwhile, read operation is normally performed for the counters when the BSY bit is 0, but can be performed without checking the BSY bit as long as appropriate software is provided for preventing read errors. (Refer to 15. Typical Software-based Operations.) The BSY bit is set to 1 in the following three cases:



2.1-3 (WTEN)

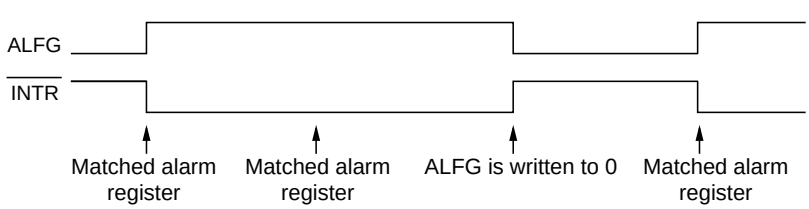
The WTEN bit should be set to 0 to check that the BSY bit is 0 when performing read and write operations for the clock and calendar counters. For read operation, the WTEN bit may be left as 1 without checking the BSY bit as long as appropriate measures such as read repetition are provided for preventing read errors. The WTEN bit should be set to 1 after completing read and write operations, or will automatically be set to 1 by switching the CE pin to the low level. If 1-second digit carry occurs when the WTEN bit is 0, a second digit increment by 1 occurs when the WTEN bit is set to 1. There may be a possibility causing a time delay when it takes 1/1024 second or more to set WTEN bit from 0 to 1, Read data in state of WTEN=1 in such a case. (Refer to the item 15.3)

2.1-4 (XSTP)

The XSTP bit senses the oscillator halt. When the CE pin is held at the low level, the XSTP bit is set to 1 once the crystal oscillator is stopped after initial power-on or supply voltage drop and left to be 1 after it is restarted. When the CE pin is held at the high level, the XSTP bit is left as it was when the CE pin was held at the low level without checking oscillation stop. As such, the XSTP bit can be used to validate clock and calendar count data after power-on or supply voltage drop. The XSTP bit is set to 0 when any data is written to the control register 1 (at Eh) with ordinary oscillation.

2.1-5 (ALFG)

The ALFG bit can be set to 1 when the ALE bit set to 1 with alarm interruption ($\overline{\text{INTR}}$=L).



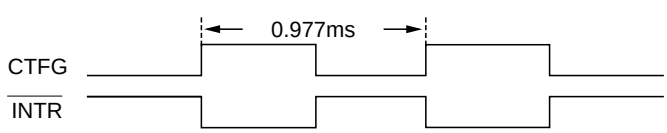
2.1-6 (CTFG)

The CTFG bit is set to 1 when interrupt pulses are output from the $\overline{INTR}$ pin held at the low level. There are two interrupt modes selectable: the pulse mode (when the CT_3 bit is set to 0) and the level mode (when the CT_3 bit is set to 1). The CTFG bit can be set only when the CT_3 is set to 1. Setting the CTFG bit to 1 switches the $\overline{INTR}$ pin to the low level while setting the CTFG bit to 0 turns off the $\overline{INTR}$ pin.

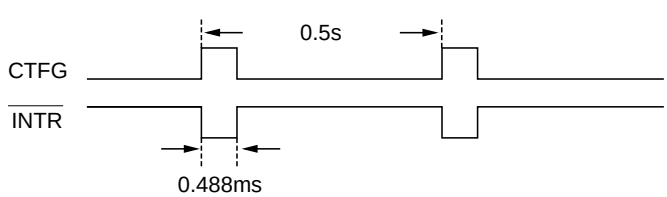
Interrupt cycle register				$\overline{INTR}$ output	Description
CT_3	CT_2	CT_1	CT_0		
0	* *1	0	0	OFF	Interrupt halt
0	*	0	1	ON	Fixing the $\overline{INTR}$ pin at low level
0	*	1	0	0.977ms	Cycle: 0.977ms (1/1024Hz) Duty 50% *2
0	*	1	1	0.5s	Cycle: 0.5s (1/2Hz) *3
1	0	0	0	1s	Every second *4
1	0	0	1	10s	Every 10 seconds *4 (For display of second digits: 00, 10, 20, 30, 40 and 50)
1	0	1	0	1 minute	Every minute (00 second) *4
1	0	1	1	10 minutes	Every 10 minutes (00 second) *4 (For display of minute digits: 00, 10, 20, 30, 40 and 50)
1	1	0	0	1 hour	Every hour (00 minute and 00 second) *4
1	1	0	1	1 day	Every day (0 hour, 00 minute and 00 second a.m.) *4
1	1	1	0	1 week	Every week *4 (0 week, 0 hour, 00 minute and 00 second a.m.)
1	1	1	1	1 month	Every month *4 (1 day, 0 hour, 00 minute and 00 second a.m.)

1) The symbol "" in the above table indicates 0 or 1.

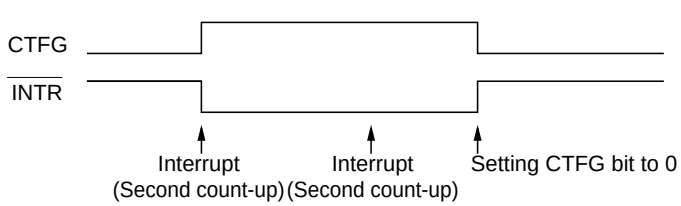
*2)



*3)



*4)



2.2 Control Register 2 (at Fh)

D3	D2	D1	D0	
$\overline{12}$/24	TMR	BANK	$\overline{TEST}$	(For write operation)
$\overline{12}$/24	TMR	BANK	$\overline{TEST}$	(For read operation)

Bit for Testing *1

$\overline{TEST}$	Description
0	Testing mode
1	Ordinary operation mode

Bank Selection Bit *2

BANK	Description
0	Clock/calendar counter
1	Alarm register

Reset Bit for Timer Counter *3

TMR	Description
0	Continuos timer operation
1	Resume timer operation after reset

$\overline{12}$/24-hour Time Display System Selection Bit *4

$\overline{12}$/24	Description
0	12-hour time display system (separate for mornings and afternoons)
1	24-hour time display system

*1) ($\overline{TEST}$) Set the $\overline{TEST}$ bit to 1 in ordinary operation. $\overline{TEST}$ bit is set automatically to 1 when the CE pin is "L".
*2) (BANK) There is no need to designate BANK bit for Interrupt cycle register and Control register 1/2.
*3) (TMR) The period for timer output is set in the "Timer register".
*4) ($\overline{12}$/24) The $\overline{12}$/24 bit specifies time digit display in BCD code.

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

Either the 12-hour or 24-hour time display system should be selected before time setting.

2.3 Interrupt cycle Register (at 7h)

D3	D2	D1	D0	
CT_3	CT_2	CT_1	CT_0	(For write operation)
CT_3	CT_2	CT_1	CT_0	(For read operation)

Bits for selecting the interrupt cycle and output mode at the $\overline{INTR}$ pin *1

*1) (CT_3 to CT_0)
The CT_3 to CT_0 bits are used to select the interrupt cycle and output mode at the $\overline{INTR}$ pin. There are two interrupt modes selectable: the pulse mode (when the CT_3 bit is set to 0) and the level mode (when the CT_3 bit is set to 1). The interrupt cycle and output mode at the $\overline{INTR}$ pin are shown in detail in the section on the CTFG bit in "2.1 Control Register 1 (at Eh)".

2.4 Alarm registers for day-of-the-week, 1-minute, 10-minute, 1-hour, 10-hour (BANK1, at 0h-5h)

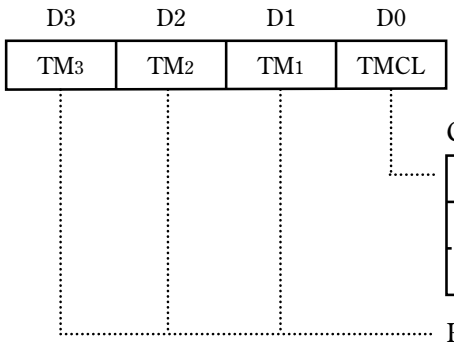
D3	D2	D1	D0		
AW_3	AW_2	AW_1	AW_0	(For read/write) day-of-the-week 1	(at 0h)
$\overline{ALC}$	AW_6	AW_5	AW_4	(For read/write) day-of-the-week 2	(at 1h)
AM_8	AM_4	AM_2	AM_1	(For read/write) 1-minute time digit	(at 2h)
*	AM_{40}	AM_{20}	AM_{10}	(For read/write) 10-minute time digit	(at 3h)
AH_8	AH_4	AH_2	AH_1	(For read/write) 1-hour time digit	(at 4h)
ALE	*	$AP/\overline{A}, AH_{20}$	AH_{10}	(For read/write) 10-hour time digit	(at 5h)

1) The "" mark in the above table indicates data which are set to 0 for read cycle and not set for write cycle.
*2) 10-hour time digit indicates $AP/\overline{A}$ and AH_{20} with 12-hour and 24-hour time system respectively.
*3) Make sure set an actual time-data to the alarm registers when the alarm function is activated as any imaginary alarm-data will never be match with the actual time.
*4) The $\overline{INTR}$ pin can output matched alarm interruption when the $\overline{ALC}$ bit is set 0 and halt output when the $\overline{ALC}$ bit is set to 1.
*5) The alarm function is disabled when the ALE bit is set 0 and is enables when the ALE bit is set 1.
*6) Examples of setting alarm time

Setting alarm time	Day-of-the-week							12-hour system				12-hour system			
	Sun. AW0	Mon. AW1	Tue. AW2	Wed. AW3	Thu. AW4	Fri. AW5	Sat. AW6	10-hour	1-hour	10-min	1-min	10-hour	1-hour	10-min	1-min
AM 00:00 every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
AM 01:30 every day	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
AM 11: 59 every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
PM 00:00 on Monday through Friday	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
PM 01:30 on Sunday	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
PM 11:59 on Monday, Wednesday, and Friday	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

*7) Hour digits show "12" and "32" when the time is AM 00:00 and PM 00:00 respectively in the 12-hour system.
*8) No alarm interruption is output when all the bit from AW_0 through AW_6 is set to 0.
*9) Each of the AW_0 through AW_6 corresponds to the day-of-the-week counter such as (W_4, W_2, W_1)=(0, 0, 0) through (1, 1, 0). Designation of day-of-the-week and AW_0 through AW_6 in the above table is one example.

2.5 Timer register (BANK 1, at 9h)



Clock Frequency Selection Bit for the Timer Counter *1

TMCL	Description
0	Clock frequency=512Hz (1.953ms)
1	Clock frequency=16Hz (62.5ms)

Period Selection Bit for the Timer Counter *2

Cycle time setting table for the time counter (The "*" mark indicates 0 or 1.)

TM_3	TM_2	TM_1	TMCL	T1 (cycle time for watch-dog-timer) *3	T2 (time between setting TMR=1 and $\overline{TMOUT}$ output) *4	T3 (cycle time for free-run timer) *5
0	0	0	*	Timer halts	Timer halts	Timer halts
0	0	1	0	1.953ms	1.953 to 3.907ms	3.906ms
0	1	0	0	5.859ms	5.859 to 7.813ms	7.812ms
0	1	1	0	9.765ms	9.765 to 11.72ms	11.719ms
1	0	0	0	13.67ms	13.67 to 15.63ms	15.625ms
1	0	1	0	17.57ms	17.57 to 19.54ms	19.531ms
1	1	0	0	21.48ms	21.48 to 23.44ms	23.437ms
1	1	1	0	25.39ms	25.39 to 27.35ms	27.344ms
0	0	1	1	62.5ms	62.5 to 125ms	125ms
0	1	0	1	187.5ms	187.5 to 250ms	250ms
0	1	1	1	312.5ms	312.5 to 375ms	375ms
1	0	0	1	437.5ms	437.5 to 500ms	500ms
1	0	1	1	562.5ms	562.5 to 625ms	625ms
1	1	0	1	687.5ms	687.5 to 750ms	750ms
1	1	1	1	812.5ms	812.5 to 875ms	875ms

*1) (TMCL)
"512Hz" and "16Hz" are selectively available. When the "XSTP" bit is set to 1, the "TMCL" bit is automatically set to 0. There may be possibility to be ahead or behind of the clock counter at maximum of a halt of clock frequency (512Hz or 16Hz), when the "ADJ" bit is set to 1 in the control register-1.

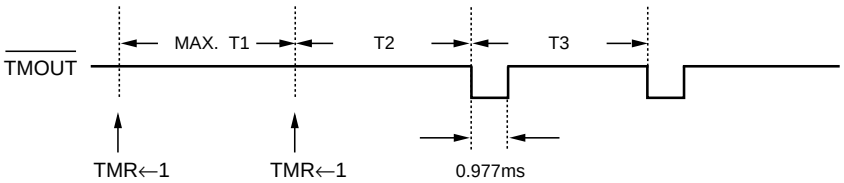
*2) (TM_3-TM_1)
When the "XSTP" bit is set to 1 the "TM_3, TM_2", and "TM_1" is automatically set to 0, the timer counter halts.

*3) T1: The maximum disable time for timer output, $\overline{TMOUT}$=L, after setting the "TMR" bit to 1.

*4) T2: Time between timer output and setting the "TMR" bit to 1, or setting the timer register to any value.

*5) T3: Timer output cycle time without setting "TMR" bit to 1, cycle time for free-run-timer.

∗6) Timing diagram for $\overline{\text{TMOUT}}$



∗7) Writing operation to the timer register makes the timer counter to start operation with resetting.

2.6 32kHz control register (BANK 1, at Ah)

D3	D2	D1	D0	
∗	∗	∗	$\overline{\text{CLEN}}$	(For read/write)

∗1) The "∗" mark indicates data which are set to 0 for read cycle and not set for write cycle.

∗2) ($\overline{\text{CLEN}}$) control bit for 32kHz output
The $\overline{\text{CLEN}}$ bit is set to 0 when the XSTP=1. $\overline{\text{CLEN}}$ is not writable and set to 0 when CLKC pin level low/open.

∗3) 32KOUT condition

CLKC pin	$\overline{\text{CLEN}}$ bit	32KOUT output
L (open)	0 (prohibited to write)	High impedance
H	0	32kHz clock output
H	1	High impedance

3. Counters

3.1 Clock counter (BANK 0, at 0h-5h)

D3	D2	D1	D0			
S_8	S_4	S_2	S_1	(For read/write)	1-second time digit	(at 0h)
∗	S_{40}	S_{20}	S_{10}	(For read/write)	10-second time digit	(at 1h)
M_8	M_4	M_2	M_1	(For read/write)	1-minute time digit	(at 2h)
∗	M_{40}	M_{20}	M_{10}	(For read/write)	10-minute time digit	(at 3h)
H_8	H_4	H_2	H_1	(For read/write)	1-hour time digit	(at 4h)
∗	∗	P/$\overline{\text{A}}$ or H_{20}	H_{10}	(For read/write)	10-hour time digit	(at 5h)

∗1) The "∗" mark indicates data which are set to 0 for read cycle and not set for write cycle.

∗2) Any carry to 1-second digits from the second counter is disabled when the WTEN bit (of the control register 1) is set to 0.

∗3) Time digit display (BCD code):
Second digits : Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
Minute digits : Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
Hour digits : Range as shown in the section on the $\overline{12}$/24 bit and carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

∗4) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.

3.2 Day-of-the-week counter (BANK 0, at 6h)

D3	D2	D1	D0	
*	W_4	W_2	W_1	(For read/write) Day-of-the-week counter

1) The "" mark indicates data which are set to 0 for read cycle and not set for write cycle.
*2) Day-of-the-week digits are incremented by 1 when carried to 1-day digits.
*3) Day-of-the-week digits display (incremented in septimal notation):
(W_4, W_2, W_1)=(000) → (001) → ·····→ (110) → (000)
The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday=000).
*4) The (W_4, W_2, W_1) should not be set to (111).

3.3 Calendar counter (BANK 0, at 8h-Dh)

D3	D2	D1	D0			
D_8	D_4	D_2	D_1	(For read/write)	1-day calendar digit	(at 8h)
*	*	D_{20}	D_{10}	(For read/write)	10-day calendar digit	(at 9h)
MO_8	MO_4	MO_2	MO_1	(For read/write)	1-month calendar digit	(at Ah)
*	*	*	MO_{10}	(For read/write)	10-month calendar digit	(at Bh)
Y_8	Y_4	Y_2	Y_1	(For read/write)	1-year calendar digit	(at Ch)
Y_{80}	Y_{40}	Y_{20}	Y_{10}	(For read/write)	10-year calendar digit	(at Dh)

1) The "" mark indicates data which are set to 0 for read cycle and not set for write cycle.
*2) The automatic calendar function provides the following calendar digit displays in BCD code.
Day digits : Range from 1 to 31 (for January, March, May, July, August, October, and December).
Range from 1 to 30 (for April, June, September, and November).
Range from 1 to 29 (for February in leap years).
Range from 1 to 28 (for February in ordinary years).
Carried to month digits when cycled to 1.
Month digits : Range from 1 to 12 and carried to year digits when cycled to 1.
Year digits : Range from 00 to 99 and counted as 00, 04, 08, ..., 92, and 96 in leap years.
*3) Any registered imaginary time should be replaced with actual time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter to malfunction.

USAGES

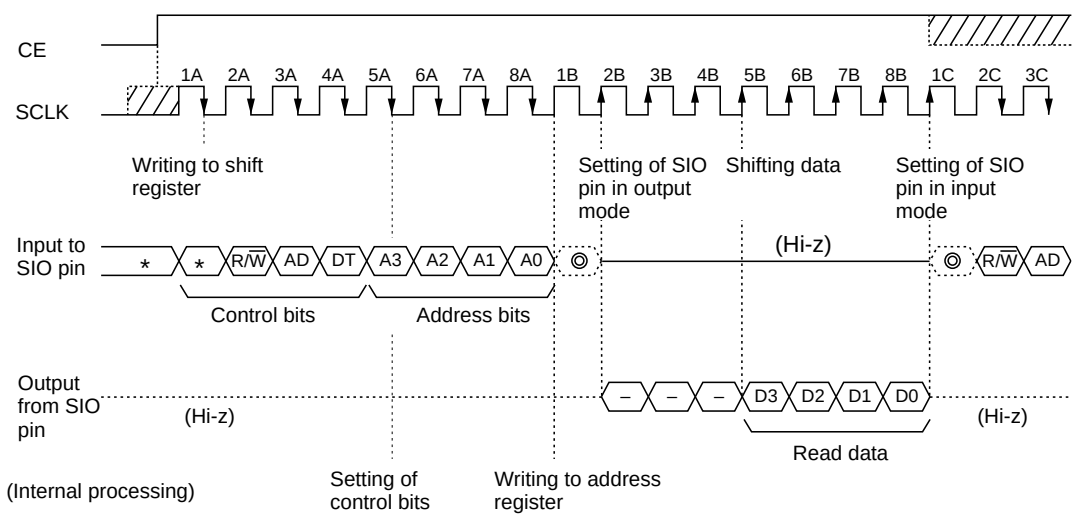
1. Read Data (For the RS5C317A)

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the SCLK pin. The input data are registered in synchronization with the falling edge of the SCLK. When the data is read, the read cycle shall be set by control bits then registered data can be read out from SIO pin in synchronization with the rising edge of the SCLK.

- **Control bits** R/$\overline{W}$: Establishes the read mode when set to 1, and the write mode when set to 0.
  AD: Writes succeeding addressing bits (A3-A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  DT: Writes data bits to counter or register specified by the address register set just before when set to 1 with the R/$\overline{W}$ and AD bits set equally to 0 and performs no such write operation in any other case.
- **Address bits** A3-A0: Inputs the bits MSB to LSB in the address table describing the functions.

1.1 Read Cycle Flow

1. The CE pin is switched from "L" to "H".
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/$\overline{W}$ and AD are set equally to 1 while a control bit DT is set to 0. (see the SCLK 1A-8A)
3. The SIO pin enters the output mode at the rising edge of the shift clock pulse 2B from the SCLK pin while the four read bits (MSB → LSB) at designated addresses are output at the rising edge of the shift clock pulse 5B. (see the figure below)
4. Then, the SIO pin returns to the input mode at the rising edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from "H" to "L" (after t_{CEH} from the falling edge of the eighth shift clock pulse from the SCLK pin). Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at "H".



) In the above figure, the "" mark indicates arbitrary data; the "–" mark indicates unknown data.
The "◎" mark indicates data which are available when the SIO pin is held at "H", "L", or Hiz level.
The diagonally shaded area of the CE and the SCLK pins indicate "H" or "L".

2. Write Data (For the RS5C317A)

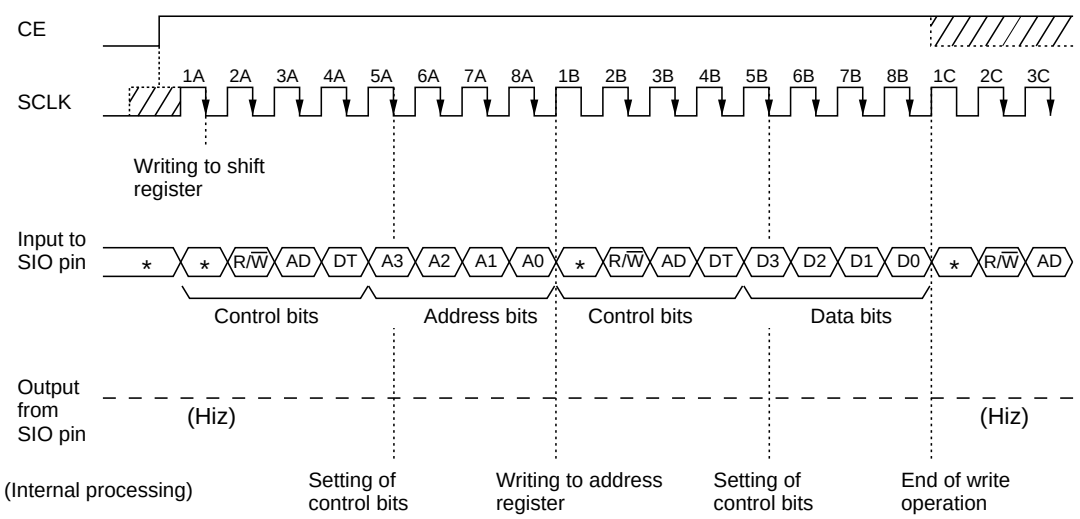
Writing data to the real-time clock requires inputting setting data (control bits, address bits and data bits) to the SIO pin and then establishing the write mode by using a control bit R/$\overline{W}$ in the same manner as in read operation.

*) Control bits and address bits are described in the previous section on read cycle.

• Data bits D3-D0: Inputs the data bits MSB to LSB in the addressing table describing the functions.

2.1 Write Cycle Flow

1. The CE pin is switched from "L" to "H".
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits R/$\overline{W}$ and DT are set equally to 0 while a control bit AD is set to 1. (see the SCLK 1A-8A)
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits R/$\overline{W}$ and AD are set equally to 0 while a control bit DT is set to 1. (see the clock 1B-8B)
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits R/$\overline{W}$, AD, and DT are set equally to 0 (at the falling edge of shift clock pulse 5A and later from the SCLK pin) or the CE pin is switched from "H" to "L" (after t_{CEH} from the falling edge of the eighth shift clock pulse from the SCLK pin). Following on write cycle, read operation can be performed by setting control bits in the read mode at the shift clock pulse 1C and later with the CE pin held at "H".



) In the above figure, the "" mark indicates arbitrary data; and the diagonally shaded area of CE and SCLK indicates "H" or "L".

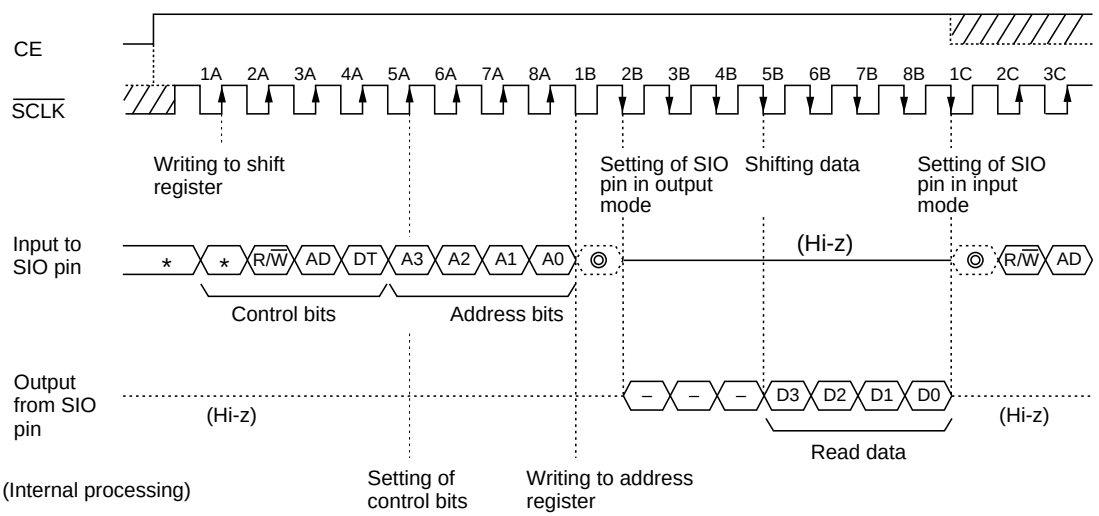
3. Read Data (For the RS5C317B)

The real-time clock becomes accessible by switching the CE pin from the low level to high level to enable interfacing with the CPU and then inputting setting data (control bits and address bits) to the SIO pin in synchronization with shift clock pulses from the $\overline{\text{SCLK}}$ pin. The input data are registered in synchronization with the rising edge of the $\overline{\text{SCLK}}$. When the data is read, the read cycle shall be set by control bits then registered data can be read out from SIO pin in synchronization with the falling edge of the $\overline{\text{SCLK}}$.

- **Control bits** R/$\overline{\text{W}}$: Establishes the read mode when set to 1, and the write mode when set to 0.
  AD: Writes succeeding addressing bits (A3-A0) to the address register when set to 1 with the DT bit set to 0 and performs no such write operation in any other case.
  DT: Writes data bits to counter or register specified by the address register set just before when set to 1 with the R/$\overline{\text{W}}$ and AD bits set equally to 0 and performs no such write operation in any other case.
- **Address bits** A3-A0: Inputs the bits MSB to LSB in the address table describing the functions.

3.1 Read Cycle Flow

1. The CE pin is switched from "L" to "H".
2. Four control bits (with the first bit ignored) and four read address bits are input from the SIO pin. At this time, control bits R/$\overline{\text{W}}$ and AD are set equally to 1 while a control bit DT is set to 0. (see the $\overline{\text{SCLK}}$ 1A-8A)
3. The SIO pin enters the output mode at the falling edge of the shift clock pulse 2B from the $\overline{\text{SCLK}}$ pin while the four read bits (MSB → LSB) at designated addresses are output at the falling edge of the shift clock pulse 5B. (see the figure below)
4. Then, the SIO pin returns to the input mode at the falling edge of the shift clock pulse 1C. Afterwards control bits and address bits are input at the shift clock pulses 1C in the same manner as at the shift clock pulse 1A.
5. At the end of read cycle, the CE pin is switched from "H" to "L" (after t_{CEH} from the rising edge of the eighth shift clock pulse from the $\overline{\text{SCLK}}$ pin). Following on read cycle, write operation can be performed by setting control bits in the write mode at the shift clock pulse 1C and later with the CE pin held at "H".



) In the above figure, the "" mark indicates arbitrary data; the "–" mark indicates unknown data.
The "◎" mark indicates data which are available when the SIO pin is held at "H", "L", or Hiz level.
The diagonally shaded area of the CE and the $\overline{\text{SCLK}}$ pins indicate "H" or "L".

4. Write Data (For the RS5C317B)

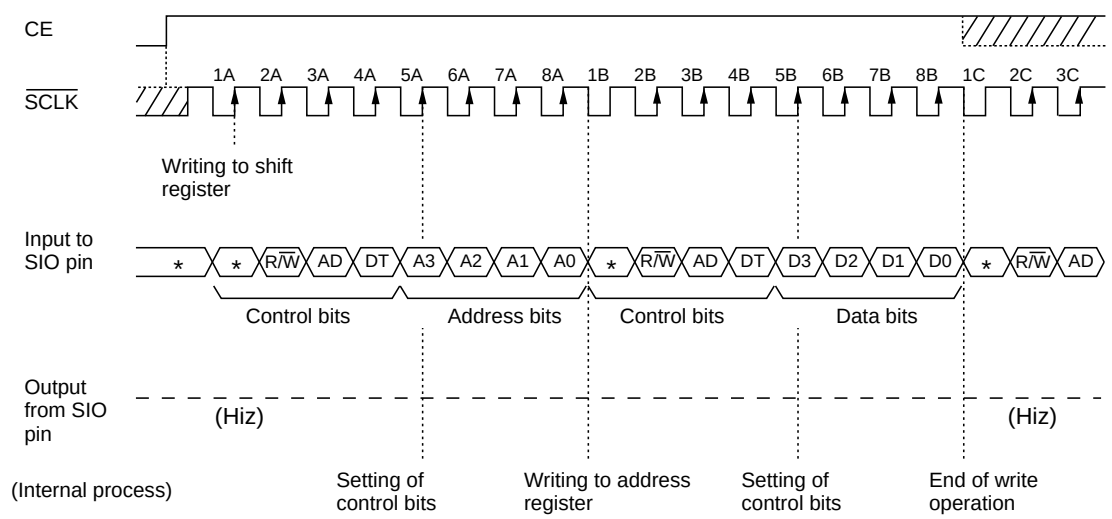
Writing data to the real-time clock requires inputting setting data (control bits, address bits and data bits) to the SIO pin and then establishing the write mode by using a control bit R/$\overline{W}$ in the same manner as in read operation.

*) Control bits and address bits are described in the previous section on read cycle.

• Data bits D3-D0: Inputs the data bits MSB to LSB in the addressing table describing the functions

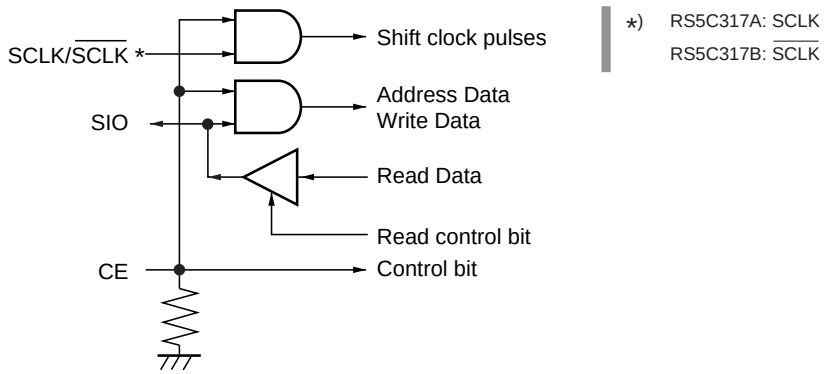
4.1 Write Cycle Flow

1. The CE pin is switched from "L" to "H".
2. Four control bits (with the first bit ignored) and four write address bits are input from the SIO pin. At this time, control bits R/$\overline{W}$ and DT are set equally to 0 while a control bit AD is set to 1. (see the $\overline{SCLK}$ 1A-8A)
3. Four control bits and four bits of data to be written are input in the descending order of their significance. At this time, control bits R/$\overline{W}$ and AD are set equally to 0 while a control bit DT is set to 1. (see the $\overline{SCLK}$ 1B-8B)
4. When write cycle is continued, control bits and address bits are input at the shift clock pulse 1C and later in the same manner as at the shift clock pulse 1A.
5. At the end of write operation, control bits R/$\overline{W}$, AD, and DT are set equally to 0 (at the rising edge of shift clock pulse 5A and later from the $\overline{SCLK}$ pin) or the CE pin is switched from "H" to "L" (after t_{CEH} from the rising edge of the eighth shift clock pulse from the $\overline{SCLK}$ pin). Following on write cycle, read operation can be performed by setting control bits in the read mode at the shift clock pulse 1C and later with the CE pin held at "H".



) In the above figure, the "" mark indicates arbitrary data; and the diagonally shaded area of CE and $\overline{SCLK}$ indicates "H" or "L".

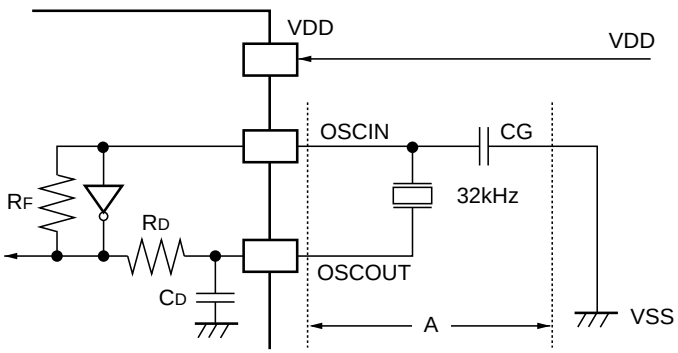
5. CE Pin



1) Switching the CE pin to the high level enables the SCLK/$\overline{\text{SCLK}}$ and SIO pins, allowing data to be serially read from and written to the SIO pin in synchronization with shift clock pulses input from the SCLK/$\overline{\text{SCLK}}$ pin.
2) Switching the CE pin to the low level or opening disables the SCLK/$\overline{\text{SCLK}}$ and SIO pins, causing high impedance and resetting the internal interfacing circuits such as the shift register. While data of the address register and bank bit which have been written just before should be preserved.
3) The CE pin should be held at the low level or open state when no access is made to the RS5C317.
   The CE pin incorporates a pull-down resistor.
4) During system power-down (being back-up battery powered), the low-level input of the CE pin should be brought as close as possible to the VSS level to minimize the loss of charge in the battery.
5) Holding the CE pin at the high level for more than 2.5 seconds mainly forces 1Hz interrupt pulses to be output from the $\overline{\text{INTR}}$ pin for oscillation frequency measurement. When the CE pin is held at the high level for less than 1.5 seconds, no pulse is output.
6) The CE pin should be held at the low level in order to enable oscillator halt sensing. Holding the CE pin at the high level, therefore, disables oscillator halt sensing, retaining the value of the XSTP (oscillator halt sensing) bit which exists immediately before the CE pin is switched to the high level.

Considerations
When the power turns on from 0V, the CE pin should be set low or open once.

6. Configuration of Oscillating Circuit



Typical external device:
X'tal : 32.768kHz
(R_1=30kΩ TYP.)
(C_L=6pF to 8pF)
C_G=8pF to 20pF
Typical values of internal devices
R_F=15MΩ (TYP.)
R_D=60kΩ (TYP.)
C_D=10pF (TYP.)

*) The oscillation circuit is driven at a constant voltage of about 1.5V relative to the Vss level.
Consequently, it generates a wave form having a peak-to-peak amplitude of about 1.5V on the positive side of the Vss level.

Considerations in Mounting Components Surrounding Oscillating Circuit

1) Mount the crystal oscillators and C_G in the closest possible position to the IC.
2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with "← A →" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the PCB.
4) Avoid using any long parallel line to wire the OSCIN or OSCOUT pin.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Other Relevant Considerations

1) When applying an external input of clock pulses (32.768kHz) to the OSCIN pin:
DC coupling .....Prohibited due to mismatching input levels.
AC coupling.....Permissible except that unpredictable results may occur in oscillator halt sensing due to possible sensing errors caused by noises, etc.
2) Avoid using the oscillator output of the RS5C317 (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation.

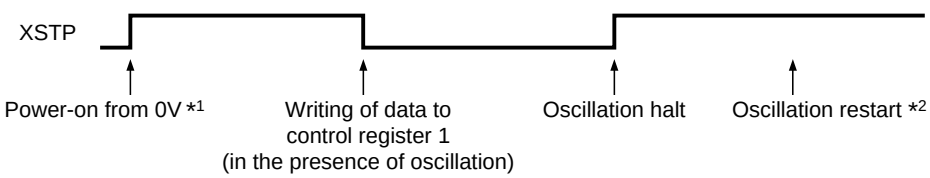
7. Oscillator Halt Sensing

Oscillation Halt can be sensed through monitoring the XSTP bit with preceding setting of the XSTP bit to 0 by writing any data to the control register 1. Upon oscillator halt sensing, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity.

When the XSTP bit is set to 1, the timer register bits and $\overline{\text{CLEN}}$ bit perform as follows:

$\overline{\text{CLEN}}$=0

TM_3=TM_2=TM_1=TMCL=0 (Timer halts)



*1) While the CE pin is held at the low level, the XSTP bit is set to 1 upon power-on from 0V.
Note that any instantaneous power disconnection may cause operational failure. When the CE pin is held at the high level, oscillation halt is not sensed and the value of the XSTP bit when the CE pin is held at the low level is retained.

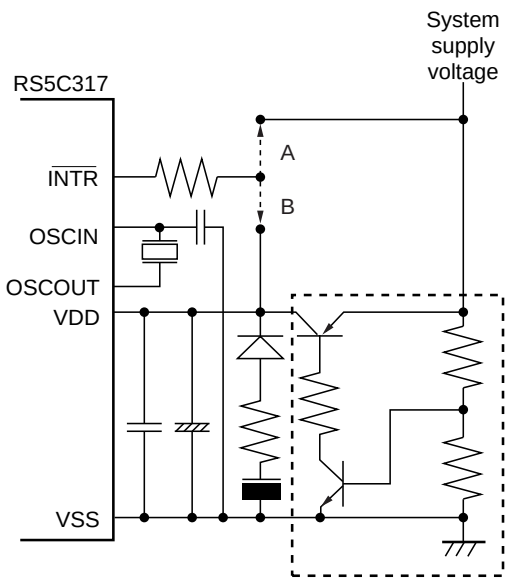
*2) Once oscillation halt has been sensed, the XSTP bit is held at 1 even if oscillation is restarted.

Considerations in Use of XSTP Bit

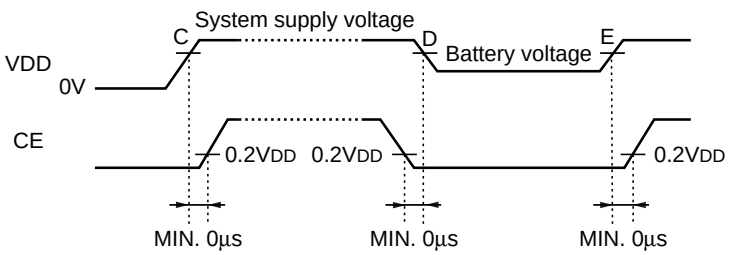
Ensure error-free oscillation halt sensing by preventing the following:

1) Instantaneous disconnection of VDD
2) Condensation on the crystal oscillator
3) Generation of noise on the PCB in the crystal oscillator
4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC

8. Typical Power Supply Circuit



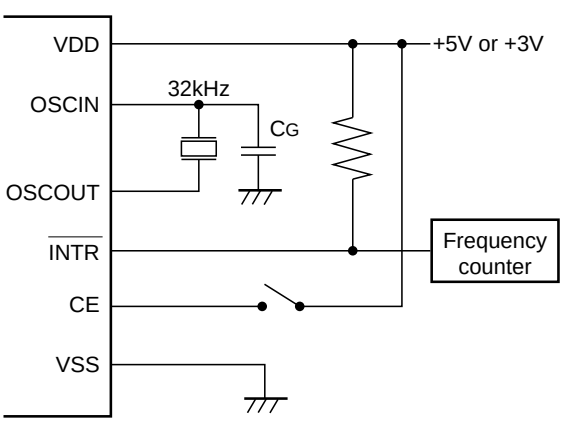
1) Connect the capacitance of the oscillation circuit to the Vss pin.
2) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C317.
3) Connect the pull-up resistor of the $\overline{INTR}$ pin to two different positions depending on whether the resistor is in use during battery back-up.
   - When not in use during battery back-up
     .....Position A in the left figure
   - When in use during battery back-up
     .....Position B in the left figure
4) Timing of power-on, power-off and CE pin refer to following figure.
5) When a diode are in use in place of the components surrounded by dotted lines, note that applying voltage to any input pins should be less than the rating of V_{DD} +0.3V by using of schottky diode.



C, D, E: Minimum operating voltage for CPU

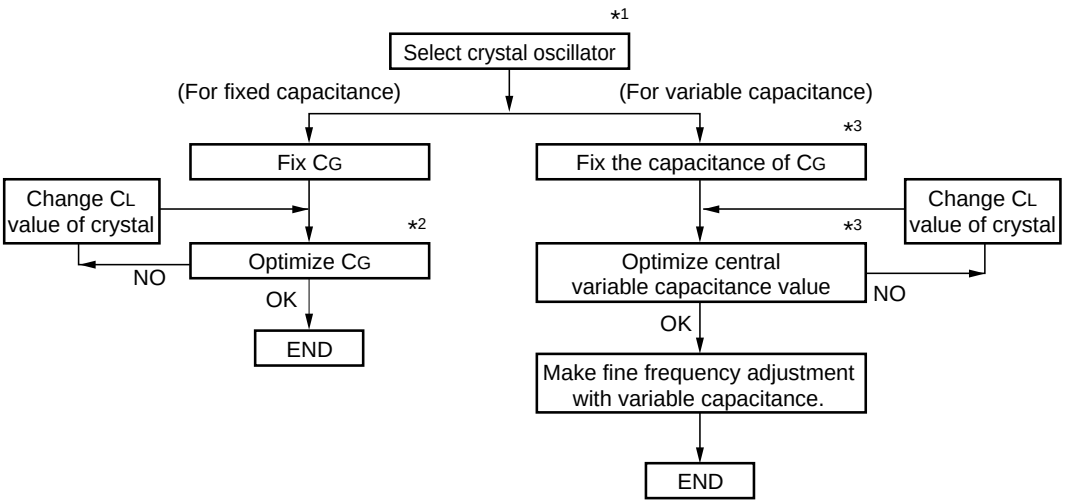
9. Oscillation Frequency Adjustment

9.1 Oscillation Frequency Measurement



1) Switch the CE pin to the high level and use a frequency counter to measure a 1Hz interrupt pulse output from the $\overline{INTR}$ pin about 2.5 seconds later.
2) Ensure that the frequency counter has more than six digits (on the order of 1 ppm).
3) Place the C_G between the OSCIN pin and the VSS level and pull up the $\overline{INTR}$ pin output to the VDD.

9.2 Oscillation Frequency Adjustment



*1) To ensure that the crystal is matched to the IC, inquire its crystal supplier about its C_L (load capacitance) and R_1 (equivalent series resistance) values. It is recommended that the crystal should have the C_L value range of 6 to 8pF and the typical R_1 value of 30kΩ.

*2) To allow for the possible effects of floating capacitance, select the optimum capacitance of the C_G on the mounted PCB. The standard and recommendable capacitance values of the C_G range from 5 to 24pF and 8 to 20pF, respectively. When you need to change the frequency to get higher accuracy, change the C_L value of the crystal.

*3) Collate the central variable capacitance value of the C_G with its oscillation frequency by adjusting the angle of rotation of the variable capacitance of the C_G in such a manner that the actual variable capacitance value is slightly smaller than the central variable capacitance value. (It is recommended that the central variable capacitance value should be slightly less than one half of the actual variable capacitance value because the smaller is variable capacitance, the greater are fluctuations in oscillation frequency.) In the case of an excessive deviation of the oscillation frequency from its required value, change the C_L value of the crystal.

After adjustment, oscillation frequency is subject to fluctuations of an ambient temperature and supply voltage. See "14. Typical Characteristic Measurements".

Note

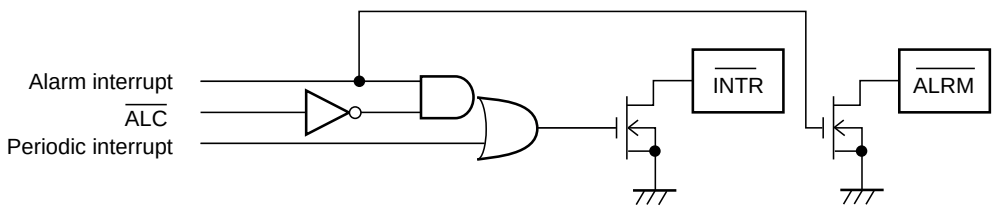
Any rise or fall in ambient temperature from its reference value ranging from 20 to 25 degrees Celsius causes a time delay for a 32kHz crystal oscillator. It is recommendable, therefore, to set slightly high oscillation frequency at room temperature.

10. Interrupt Operation

Two interrupt operations are available:

1) Alarm interrupt.....When a registered time for alarm (such as day-of-the-week, hour or minute) coincide with calendar counter (such as day-of-the-week, hour or minute) interrupt to the CPU are requested with $\overline{\text{INTR}}$ pin or $\overline{\text{ALRM}}$ pin being "L" (ON).
2) Periodic interrupt .....The $\overline{\text{INTR}}$ pin comes to a "L" (ON) state every registered period outputting interrupt request.

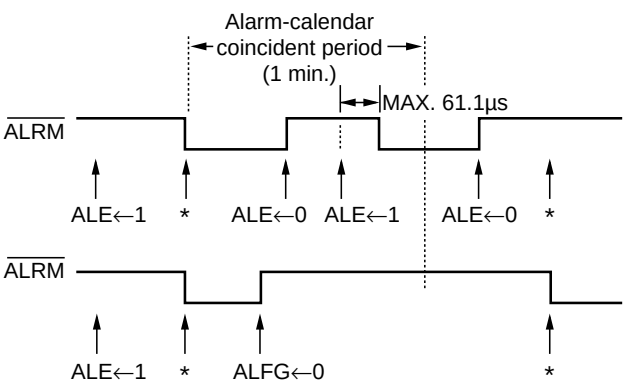
Function diagram of alarm and periodic interrupts are shown as follows:



⋆1) Setting the $\overline{\text{ALC}}$ into 1 halt output of the alarm interrupt from $\overline{\text{INTR}}$ pin.
⋆2) Both of alarm and periodic interrupt can operate regardless of the state of CE pin, "H" or "L".

10.1 Alarm Interrupt

For setting an alarm time, designated time such as day-of the week, hour or minute should be set to the alarm registers being ALE bit to 0. After that set the ALE bit to 1, from this moment onward when such registered alarm time coincide with the value of calendar counter the $\overline{\text{ALRM}}$ comes down to Low (ON). The $\overline{\text{ALRM}}$ output can be controlled by operating to the ALE and ALFG bits.



⋆1) The "⋆" mark indicates the time when the registered alarm day-of-the-week and time coincide with calendar counter.
⋆2) Above figure describes in case of no periodic interruption.
⋆3) ALFG indicates a reverse state of $\overline{\text{ALRM}}$ output.

10.2 Periodic (Clock) Interrupt

The $\overline{INTR}$ pin output, the interrupt cycle register, and the CTFG bit can be used to interrupt the CPU in a certain cycle. The interrupt cycle register can be used to select either one of two interrupt output modes: the pulse mode (when the CT_3 bit is set to 0) and the level mode (when the CT_3 bit is set to 1).

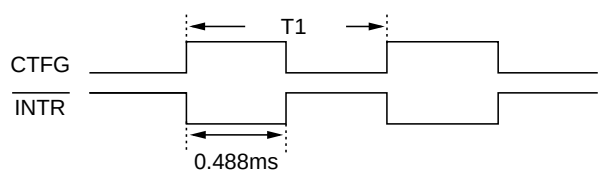
10.2-1 Interrupt Cycle Selection

Interrupt cycle register				$\overline{INTR}$ output	Description
CT_3	CT_2	CT_1	CT_0		
0	*[*1]	0	0	OFF	Interrupt halt
0	*	0	1	ON	Fixing the $\overline{INTR}$ pin to the low level
0	*	1	0	0.977ms	Cycle: 0.977ms (1/1024Hz) Duty 50%
0	*	1	1	0.5s	Cycle: 0.5s (1/2Hz)
1	0	0	0	1s	Every second
1	0	0	1	10s	Every 10 seconds (For display of second digits: 00, 10, 20, 30, 40 and 50)
1	0	1	0	1 min	Every minute (00 second)
1	0	1	1	10 min	Every 10 minutes (For display of minute digits: 00, 10, 20, 30, 40 and 50)
1	1	0	0	1 hour	Every hour (00 minute and 00 second)
1	1	0	1	1 day	Every day (0 hour, 00 minute and 00 second a.m.)
1	1	1	0	1 week	Every week (0 week, 0 hour, 00 minute and 00 second a.m.)
1	1	1	1	1 month	Every month (1st day, 0 hour, 00 minute and 00 second a.m.)

1) The "" mark indicates 0 or 1.

10.2-2 Pulse mode Interrupt

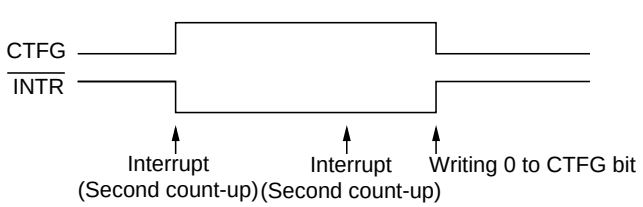
When the CT_3 bit is set to 0 and provides four interrupt cycles, off, on, 1024Hz, and 2Hz can be selected. The CTFG bit cannot be set because it is used for output monitoring.



1024Hz : T1= 0.977ms
2Hz : T1= 500ms

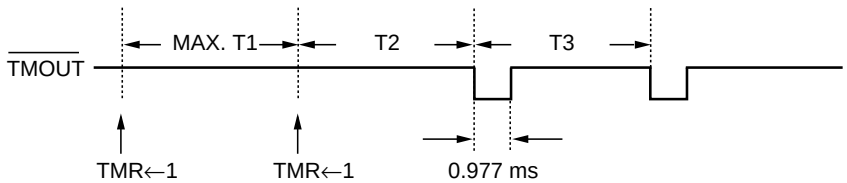
10.2-3 Level mode Interrupt

When the CT_3 bit is set to 1, clock-interlocked cycles in increments of one second to one month can be selected. The CTFG bit can be written; writing 1 to the CTFG bit switches the $\overline{INTR}$ pin to the low level while writing 0 to the CTFG bit turns off the $\overline{INTR}$ pin.



11. Timer

$\overline{\text{TMOUT}}$ outputs periodic pulses every registered time period (in BANK=1, at 9h). Setting TMR bit to 1 makes the timer counter reset and possible to operate as a watch-dog-timer.



*1) Timer counter is available when the CE pin is set 0.
*2) Timer function is disabled when the XSTP bit is set to 1.
(TM3 to TM1 and TMCL of timer register become to 0)
*3) Refer to "Timer register" in FUNCTON section regarding to T1, T2, and T3 in the above figure.
*4) $\overline{\text{TMOUT}}$ will be OFF when the TMR bit is set to one with $\overline{\text{TMOUT}}$=L (ON)
*5) Write operation to the timer registers causes starting to operate of timer counter after resetting.

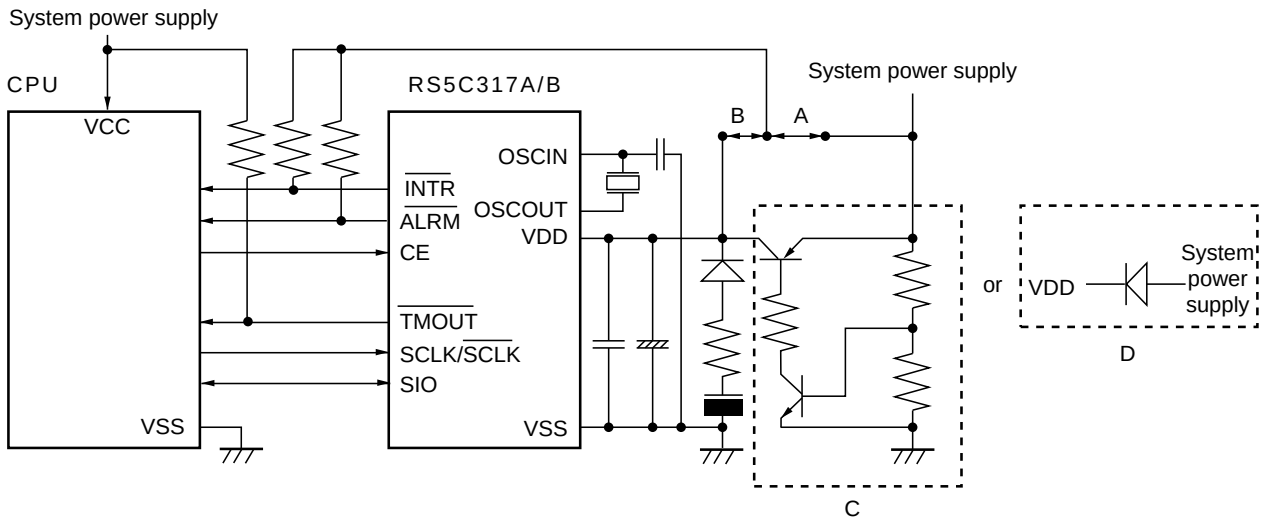
12. 32kHz Clock Output

Clock signal of 32kHz crystal oscillator can be output from the 32KOUT pin. When this function is disabled the 32KOUT pin is held at high impedance.
32kHz clock output can be controlled through CLKC pin and $\overline{\text{CLEN}}$ pin.

CLKC pin	$\overline{\text{CLEN}}$ bit	32KOUT output
L (open)	0 (disabled to write)	High impedance
H	0	Output 32kHz clock
H	1	High impedance

*1) CLKC pin incorporates pulled down resistor.
*2) The CLEN bit will be set to 0 when the XSTP bit is set to 1.
The conditions of the XSTP bit being set to 1 is as follows:
(I) Initial power-on (II) Supply voltage drop (III) Crystal oscillation halt
*3) Do not hold the CLKC pin at high level when initial power on.

13. Typical Application



⋆1) Connect the capacitance of the oscillation circuit to the VSS pin.

⋆2) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C317.

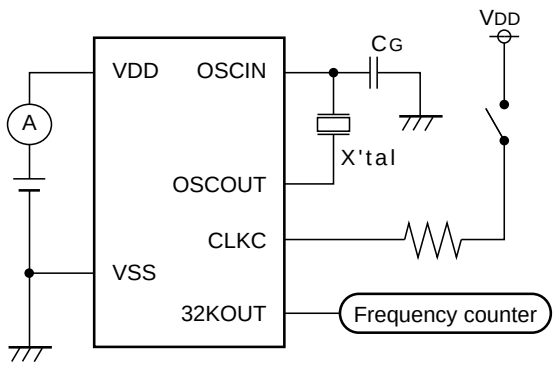
⋆3) Connect the pull-up resistor of the $\overline{\text{INTR}}$ pin or $\overline{\text{ALRM}}$ pin to two different positions depending on whether the resistor is in use during battery back-up:

(I) When not in use during battery back-up.....Position A in the above figure

(II) When in use during battery back-up.....Position B in the above figure

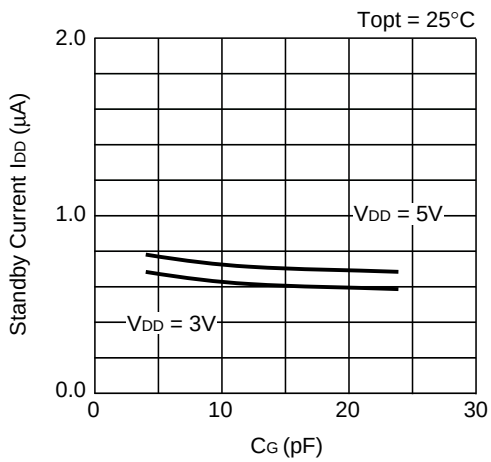
⋆4) When using a "D" circuit in place of "C", note that forward voltage of diode should be minimized to eliminate applying excess voltage to input pins. (Take the utmost care on system powering-ON and-OFF).

14. Typical Characteristic Measurements

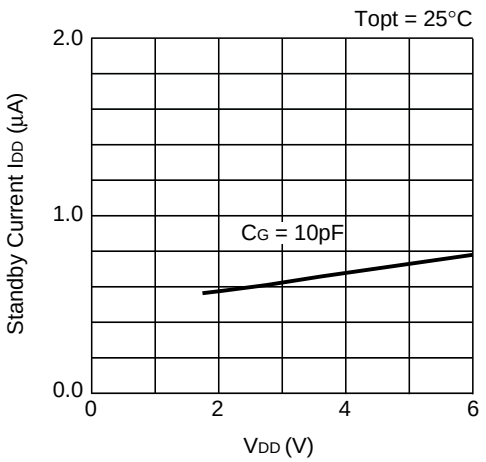


C_G=10pF
X'tal : R_1=30kΩ
Topt=25˚C
Input Pin : VDD or VSS
Output Pin : Open

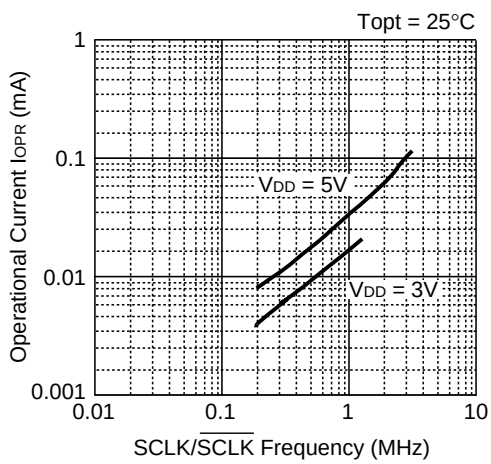
14.1 Standby Current vs. C_G



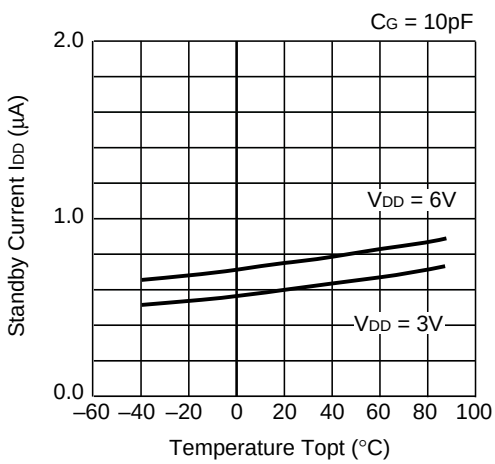
14.2 Standby Current vs. V_{DD}



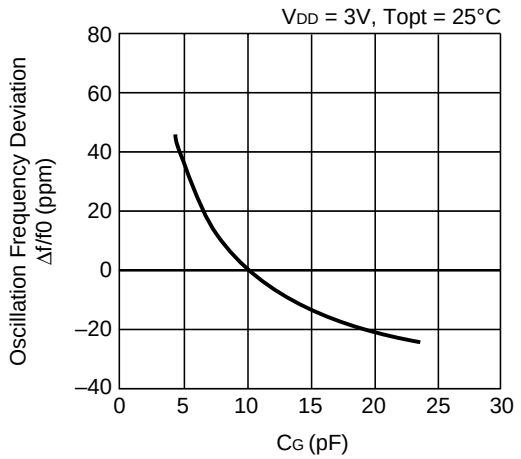
14.3 Operational Current vs. SCLK/$\overline{\text{SCLK}}$ Frequency



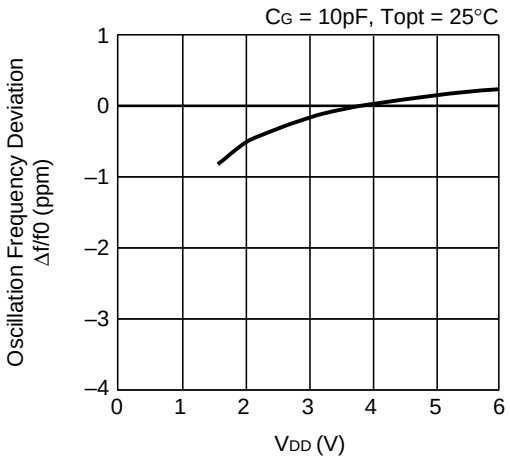
14.4 Standby Current vs. Temperature



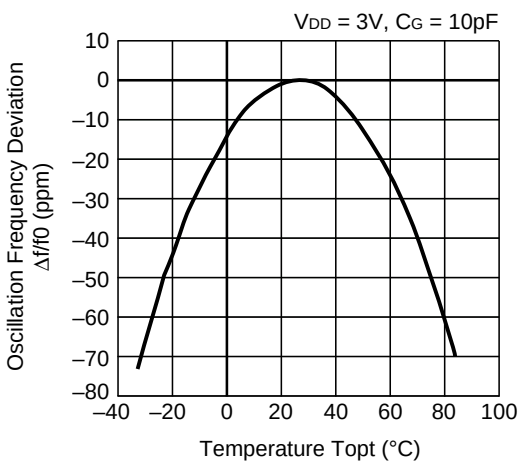
14.5 Oscillation Frequency Deviation vs. C_G (f0: C_G=10pF reference)



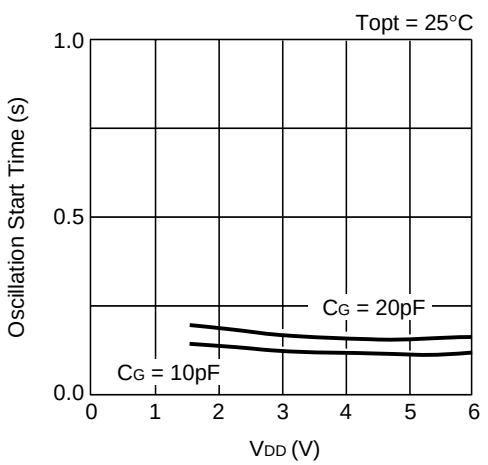
14.6 Oscillation Frequency Deviation vs. V_{DD} (f0: V_{DD}=4V reference)



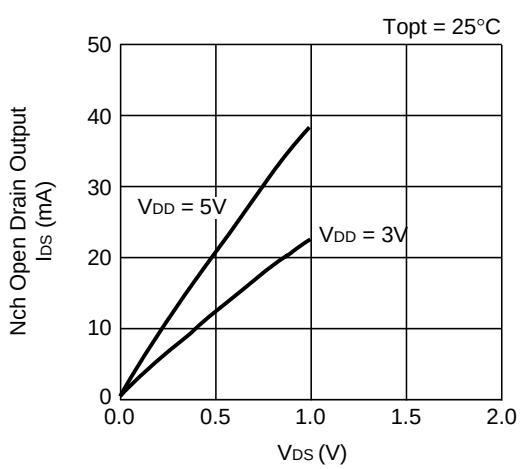
14.7 Oscillation Frequency Deviation vs. Temperature (f0: Topt=25°C reference)



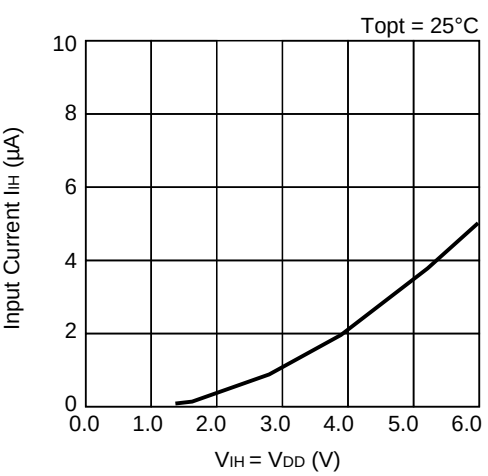
14.8 Oscillation Start Time vs. V_{DD}



14.9 V_{DS} vs. I_{DS} for Nch Open Drain Output

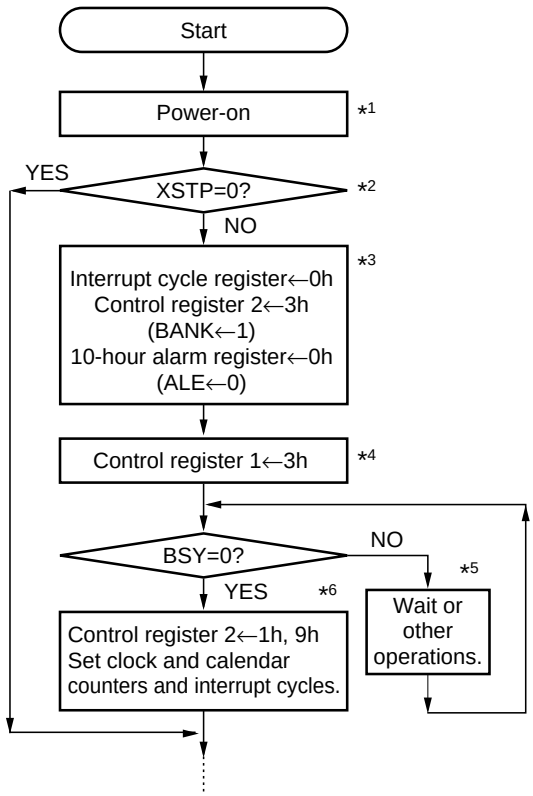


14.10 I_{IH} vs. V_{IH} for CLKC pin



15. Typical Software-based Operations

15.1 Initialization upon Power-on



*1) Switch the CE pin to the low level immediately after power-on.

*2) When not making oscillation halt sensing (data validity), the XSTP bit need not be checked.

*3) Turn off the $\overline{\text{INTR}}$ pin, whose output is uncertain at power-on.

*4) Set the ADJ bit to 1. When writing control register 1, if the oscillator has operated, the XSTP bit is changed from 1 to 0.

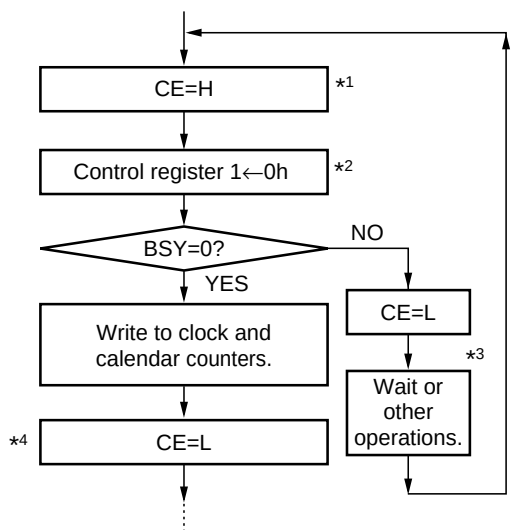
*5) It takes about 0.1 to 2 seconds to be set the BSY bit to 0 from oscillation starting upon power-on from 0V. Provide an exit from an oscillation start loop to prepare for oscillation failure.

*6) Set the XSTP bit to 0 by writing data to the control register 1, and set to the control register 2,
1h for the 12-hour time display system.
9h for the 24-hour time display system.

When Using the XSTP Bit

Ensure stable oscillation by preventing the following:
1) Condensation on the crystal oscillator
2) Instantaneous disconnection of power
3) Generation of clock noises, etc, in the crystal oscillator
4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

15.2 Write Operation to Clock and Calendar Counters



*1) After switching the CE pin to the high level, hold it at the high level until any subsequent operation requires switching it to the low level. (Note that switching the CE pin to the low level sets the WTEN bit to 1.)

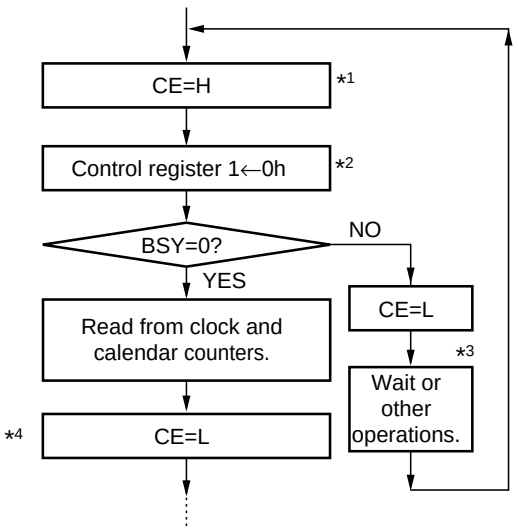
*2) WTEN bit is set to 0.

*3) The BSY bit is held at 1 for a maximum duration of 122.1µs.

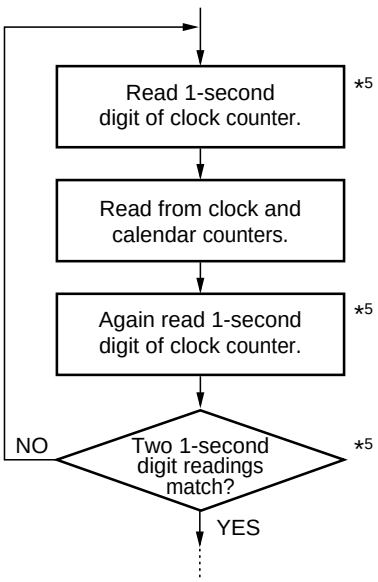
*4) Switch the CE pin to the low level to set the WTEN bit to 1. During write operation to the clock and calendar counters, one 1-second digit carry causes a 1-second increment while two 1-second digit carries also cause only a 1-seconds increment, which, in turn, causes a time delay.

15.3 Read Operation from Clock and Calendar Counters

15.3-1



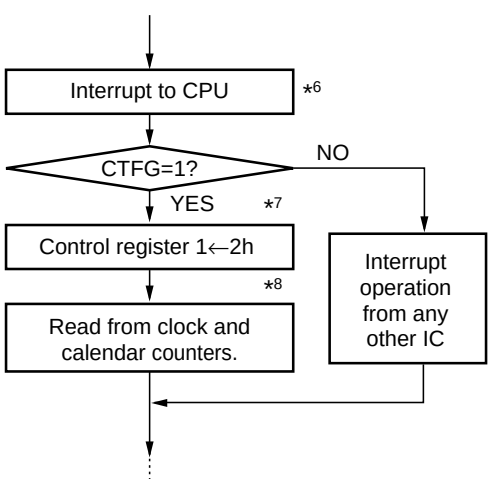
15.3-2



Note

Read data as described in 15.3-2 or 15.3-3 when it takes (1/1024) sec or more to set the WTEN bit from 0 to 1 (CE=L), the read operation described in 15.3-1 is prohibited as such a case.

15.3-3



*1) to *4) These notes are the same as 15.2 notes *1) to *4).

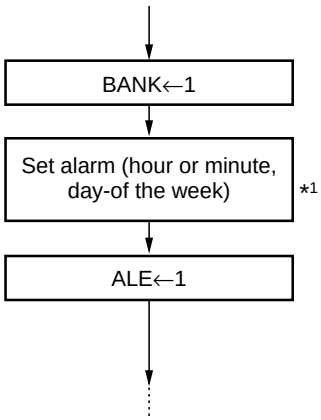
*5) When needing any higher-order digits than the minute digits, replace second digits with minute digits. (Reading LSD one of the required digits twice.)

*6) Select the level mode as an interrupt mode by setting the CT_3 bit to 1.

*7) Write 0 to CTFG bit for turning off $\overline{INTR}$ pin.

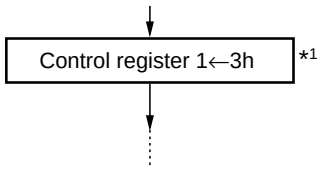
*8) Complete read operation within an interrupt cycle after interrupt generation. (e.g. within 1 second)

15.4 Write Operation to Alarm time



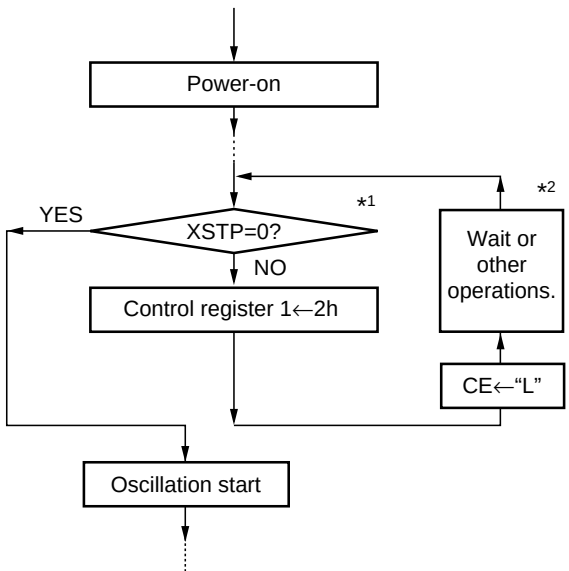
*1) Non-existent alarm time can set in the alarm registers, but when it sets, an alarm interrupt is disabled. To enable an alarm interrupt, existent alarm time must be set in the alarm registers.

15.5 Second-digit Adjustment by ±30 seconds



*1) Set the ADJ bit to 1.
(The BSY bit is held at 1 for a maximum duration of 122.1µs after the ADJ bit is set to 1.)

15.6 Oscillation Start Judgment



*1) The XSTP bit is set to 1 upon power-on from 0V.

*2) It takes approximately 0.1 to 2 seconds to start oscillation. Provide an exit from an oscillation start loop to prepare for oscillation failure.

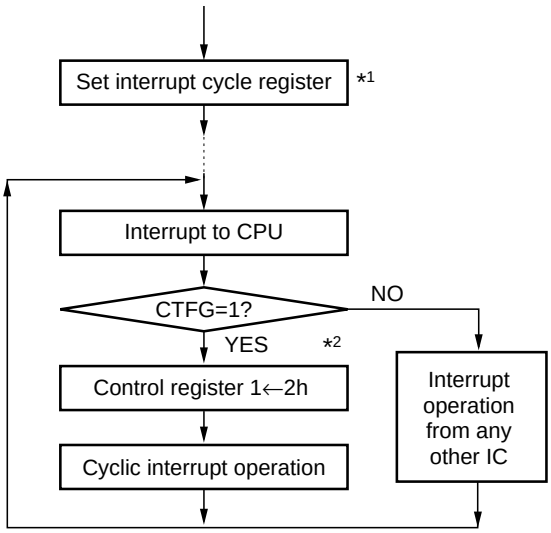
When Using the XSTP Bit

Ensure stable oscillation by preventing the following:

1) Condensation on the crystal oscillator
2) Instantaneous disconnection of power
3) Generation of clock noises, etc, in the crystal oscillator
4) Charge of voltage exceeding prescribed maximum ratings to the individual pins of the IC

15.7 Interrupt Operation

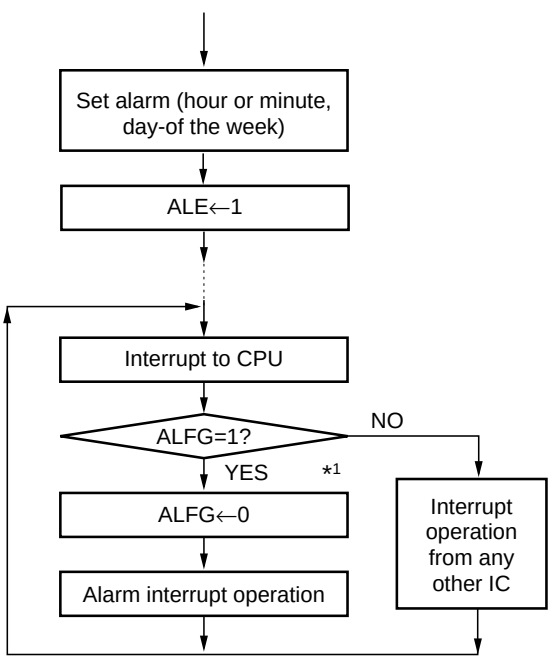
15.7-1 Cyclic Interrupt Operation



*1) Set the interrupt cycle register to the level mode by setting the CT_3 bit to 1.

*2) Write 0 to CTFG bit for turning off $\overline{INTR}$ pin.

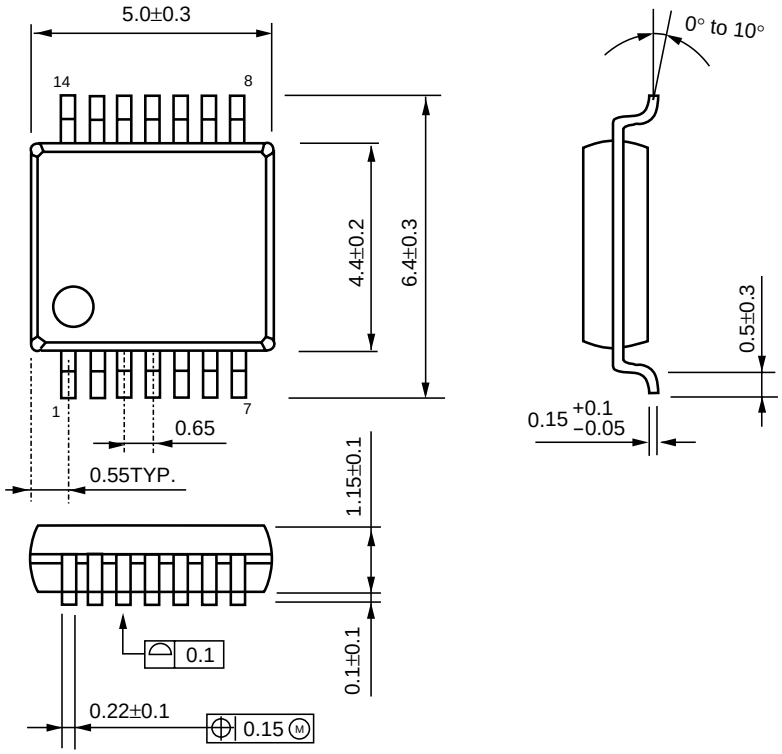
15.7-2 Alarm Interrupt Operation



*1) Write 0 to ALFG bit for turning off $\overline{ALRM}$ pin.

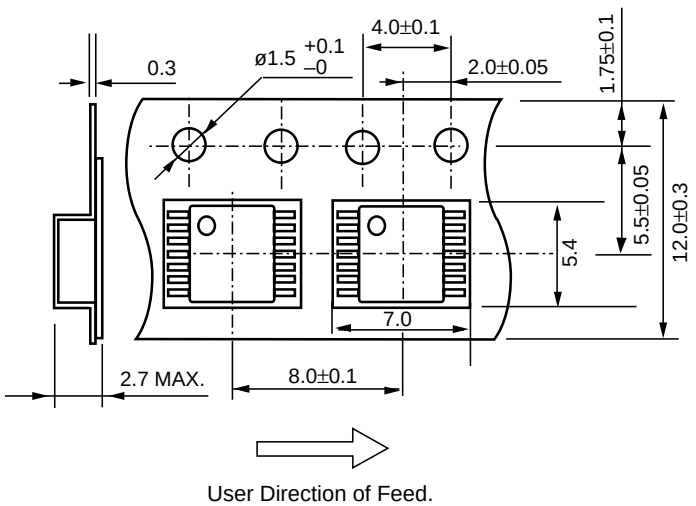
PACKAGE DIMENSIONS (Unit: mm)

• RS5C317A/B (14pin SSOP)



TAPING SPECIFICATION (Unit: mm)

The RS5C317A/B have one designated taping direction. The product designations for the taping components are "RS5C317A-E2" are "RS5C317B-E2".



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