RF AMP & SERVO SIGNAL PROCESSOR   S1L9223B02
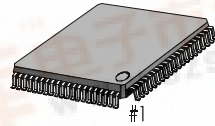
INTORDUCTION

80-TQFP-1212

The S1L9223B02 is a 1-chip BICMOS integrated circuit to perform the function of RF amp and servo signal processor for compact disc player applications.

It consist of blocks for RF signal processing, focus, tracking, sled and spindle servo. Also this IC has adjustment free function and embedded OP-AMP for audio post filter.

FEATURES

- RF amplifier & RF equalizer

- Focus error amplifier & servo control

- Tracking error amplifier & servo control

- Mirror & defect detector circuit

- Focus OK detector circuit

- APC (Auto Laser Power Control) circuit for constant laser power

- FE bias & focus servo offset adjustment free

- EF balance & tracking error gain adjustment free

- Embedded audio post filter

- The circuit for Interruption countermeasure

- Double speed play available

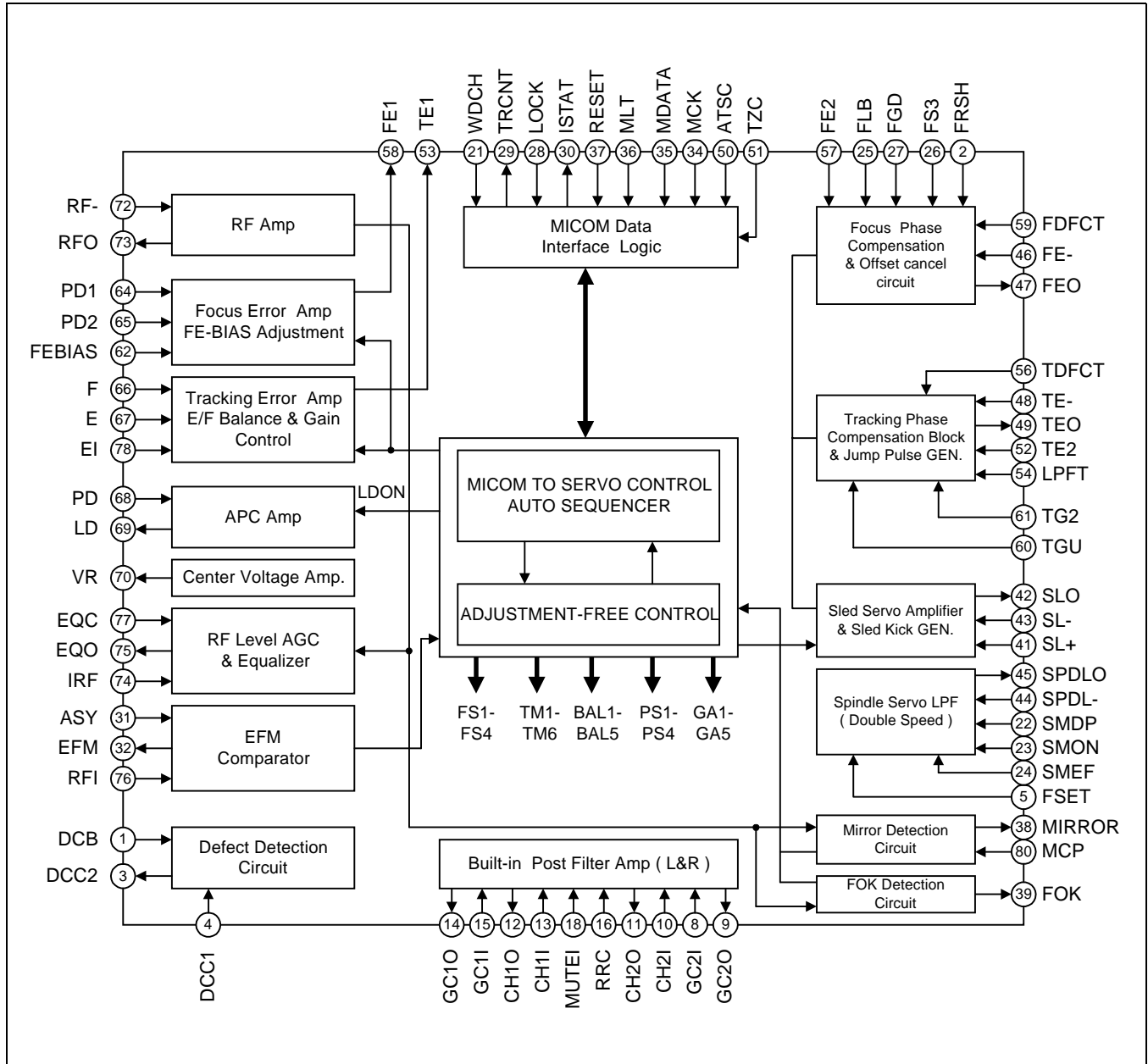- Operating voltage range: S1L9223B02: 3.4V

ORDERING INFORMATION

Device	Package	Temperature Range
S1L9223B02-T0R0	80-TQFP-1212	−20 to +70 °C

RELATED PRODUCT

- S5L9286F02 Data Processor

BLOCK DIAGRAM

PIN CONFIGURATION
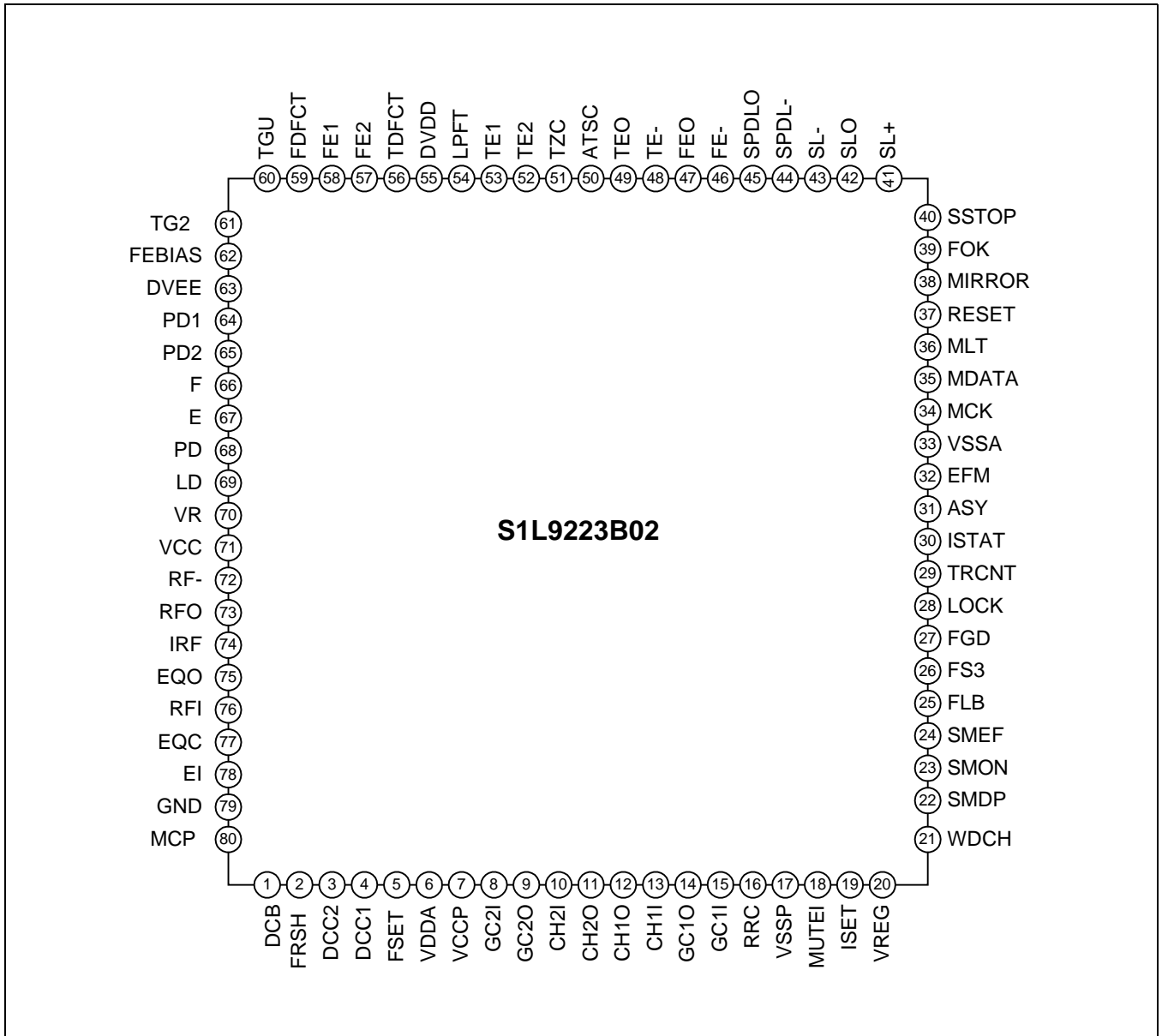
PIN DESCRIPTION

Pin No.	Symbol	Description
1	DCB	Capacitor connection pin for defect Bottom hold
2	FRSH	Capacitor connection pin for time constant to generate focus search waveform
3	DCC2	The input pin through capacitor of defect bottom hold output
4	DCC1	The output pin of defect bottom hold
5	FSET	The peak frequency setting pin for focus, tracking servo and cut off frequency of CLV LPF
6	VDDA	Analog VCC for servo part
7	VCCP	VCC for post filter
8	GC2I	Amplifier negative input pin for gain and low pass filtering of DAC output CH2
9	GC2O	Amplifier output pin for gain and low pass filtering of DAC output CH2
10	CH2I	The input pin for post filter channel2
11	CH2O	The output pin for post filter channel2
12	CH1O	The output pin for post filter channel1
13	CH1I	The input pin for post filter channel1
14	GC1O	Amplifier output pin for gain and low pass filtering of DAC output CH1
15	GC1I	Amplifier negative input pin for gain and low pass filtering of DAC output CH1
16	RRC	The pin for noise reduction of post filter bias
17	VSSP	VSS for post filter
18	MUTEI	The input pin for post filter muting control
19	ISET	The input pin for current setting of focus search, track jump and sled kick voltage
20	VREG	The output pin of regulator
21	WDCK	The clock input pin for auto sequence
22	SMDP	The input pin of CLV control output pin SMDP of DSP
23	SMON	The input pin for spindle servo ON through SMON of DSP
24	SMEF	The input pin of provide for an external LPF time constant
25	FLB	Capacitor connection pin to perform rising low bandwidth of focus loop
26	FS3	The pin for high frequency gain change of focus loop with internal FS3 switch
27	FGD	Reducing high frequency gain with capacitor between FS3 pin
28	LOCK	Sled runaway prevention pin
29	TRCNT	Track count output pin
30	ISTAT	Internal status output pin

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PIN DESCRIPTION (Continued)

Pin No.	Symbol	Description
31	ASY	The input pin for asymmetry control
32	EFM	EFM comparator output pin
33	VSSA	Analog VSS for servo part
34	MCK	MICOM clock input pin
35	MDATA	MICOM data input pin
36	MLT	MICOM data latch input pin
37	RESET	Reset input pin
38	MIRROR	The mirror output for test
39	FOK	The output pin of focus OK comparator
40	SSTOP	The pin for detection whether pick_up position is innermost or not
41	SL+	The noninverting input pin of sled servo amplifier
42	SLO	The output pin of sled servo amplifier
43	SL-	The inverting input pin of sled servo amplifier
44	SPDL-	The noninverting input pin of spindle servo amplifier
45	SPDLO	The output pin of spindle servo amplifier
46	FE-	The inverting input pin of focus servo amplifier
47	FEO	The output pin of focus servo amplifier
48	TE-	The inverting input pin of tracking servo amplifier
49	TEO	The output pin of tracking servo amplifier
50	ATSC	The input pin for Anti-shock detection
51	TZC	The comaparator input pin for tracking zero crossing detection
52	TE2	Tracking servo input pin
53	TE1	Tracking error amplifier output pin
54	LPFT	The input pin of tracking error low pass filtering signal
55	DVDD	The power supply pin for logic circuit
56	TDFCT	The capacitor connection pin for tracking defect compensation
57	FE2	Focus servo input pin
58	FE1	Focus error amplifier output pin
59	FDFCT	The capacitor connection pin for focus defect compensation
60	TGU	The capacitor connection pin for high frequency tracking gain switch
61	TG2	The pin for high frequency gain change of tracking servo loop with internal TG2 switch

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Description
62	FEBIAS	Focus error bias voltage control pin
63	DVEE	The DVEE pin for logic circuit
64	PD1	The negative input pin of RF I/V amplifier1(A+C signal)
65	PD2	The negative input pin of RF I/V amplifier2(B+D signal)
66	F	The negative input pin of F I/V amplifier (F signal)
67	E	The negative input pin of E I/V amplifier (E signal)
68	PD	The input pin for APC
69	LD	The output pin for APC
70	VR	The output pin of (AVEE+AVCC)/2 voltage
71	VCC	VCC for RF part
72	RF-	RF summing amplifier inverting input pin
73	RFO	RF summing amplifier output pin
74	IRF	The input pin for AGC
75	EQO	The output pin for AGC
76	RFI	The input pin for EFM comparison
77	EQC	The capacitor connection pin for AGC
78	EI	Feedback input pin of E I/V amplifier for EF Balance control
79	GND	GND for RF part
80	MCP	Capacitor connection pin for mirror hold

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{MAX}	6	V
Power Dissipation	P_D	150	mW
Operating Temperature	T_{OPR}	−20 to + 70	°C
Storage temperature	T_{STG}	−55 to + 150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, $V_{DD} = D_{VDD} = V_{CC}$ = +3.2V, $V_{SS} = D_{VSS}$ = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Supply Current High	ICCHI	V_{CC} = 3.6V, No load	−	12	27	42	mA
Supply Current Typ	ICCTY	V_{CC} = 3.2V, No Load	−	8	23	38	mA
RF Amp Offset Voltage	Vrfo	Input open	pin 73	−80	0	+80	mV
RF Amp Voltage Gain	Grf	SG3 f = 10kHz, 40mVp-p, sine		25.1	28.1	31.1	dB
RF THD	Rfthd	SG3 f =1kHz, 40mVp-p,sine		−	−	5	%
RF Amp Max. Output Voltage	Vrfpp1	SG3 DC 1.8V		2.8	−	−	V
RF Amp Min. Output Voltage	Vrfpp2	SG3 DC 1.4V		−	−	0.6	V
RF oscillation voltage	Rfosc1	Input open		0	50	100	mV
Focus Error Amp Offset Voltage	Vfeo1	input open	pin 58	−450	−250	−50	mV
Focus Error Amp Auto Offset Voltage	Vfeo2	WDCH=88.2kHz Pulse, $841		−35	0	35	mV
Focus Error Amp PD1 Voltage Gain	Gfe1	SG3 f=10kHz, 32mVp-p, sine		27	30	33	dB
Focus Error Amp PD2 Voltage Gain	Gfe2	SG3 f = 10kHz, 32mVp-p, sine		27	30	33	dB
Focus Error Amp Voltage Difference	GfeΔ	ΔGfe1-ΔGfe1		−3	0	+3	dB
Focus Error Amp Max. Output Voltage	Gfepp1	SG3 DC 2.7V		2.7	−	−	V
Focus Error Amp Min. Output Voltage	Gfepp2	SG3 DC2.3V		−	−	0.6	V
ISTAT output status	Vistat1	$878+$87F+$840	Pin 30	2.7	-	-	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
AGC Max Gain	Gagc	SG4 f = 500kHz, 20mVp-p, sine	pin 75	16	19	22	dB
AGC EQ Gain	Geq	Gain Difference of Gagc at f =1.5MHz		0	1	2	dB
AGC Gain2	Gagc2	SG4 f = 500kHz, 0.5Vp-p, sine		3.5	6	9	dB
AGC Compress Ratio	Cagc	Gain Difference of Gagc2 at 0.1Vp-p		0	2.5	5	dB
AGC Frequency	Fagc	Gain Difference SG4 f=1.5MHz,0.1Vp-p,sine and f=500kHz,0.1Vp-p,sine		−1.5	0	2.5	dB
RF& AGC oscillation voltage2	Rfosc2	Pin 74 IRF = 1.6V		0	25	50	mV
Tracking Error Offset Voltage	Vteo	$800, $830, input open	pin 53	−50	0	+50	mV
Tracking Error Amp Voltage Gain F	Gtef	$800, $820 SG3 0.3Vp-p, 10kHz, sine		2.1	5.1	8.1	dB
Tracking Error Amp Voltage Gain E	Gtee	SG3 0.3Vp-p, 40kHz, sine		−0.75	2.25	5.25	dB
Tracking Error Amp Voltage Gain Difference	GteΔ	Gtef-Gtee		−0.25	2.75	5.75	dB
Tracking Error Amp Maximum Output Voltage H	Vtepp1	DG3 DC 2.7V		2.2	–	–	V
Tracking Error Amp Minimum Output Voltage L	Vtepp2	SG3 DC 0.5V		–	–	1.2	V
Tracking Error Amp Gain up F	Tguf	$800,820 SG3 0.3Vp-p, 10kHz, sine		8.0	11.0	14.0	dB
Tracking Error Amp Gain up E	Tgue	$800, 820 SG3 0.3Vp-p, 10kHz, sine		5.3	8.3	11.3	dB
Tracking Gain Normal	Fgfn	SG3 0.3Vp-p, 1kHz, sine, $830		2.1	5.1	8.1	dB
Tracking F Gain 1	Fgf1	SG3 0.3Vp-p, 1kHz, sine, $831		0.1	3.1	6.1	dB
Tracking F Gain 2	Fgf2	SG3 0.3Vp-p,1kHz, sine, $832		−1.7	1.3	4.3	dB
Tracking F Gain 3	Fgf3	SG3 0.3Vp-p, 1kHz, sine, $833		−5.0	−2.0	1.0	dB
Tracking F Gain 4	Fgf4	SG3 0.3Vp-p, 1kHz, sine, $834		−9.2	−6.2	−3.2	dB

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ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Tracking E Balance Normal	Tben	SG3 0.3Vp-p, 1kHz, sine, $800	pin 53	−0.27	2.27	5.27	dB
Tracking E Balance 1	Tbe1	SG3 0.3Vp-p, 1kHz, sine, $801		−0.51	2.51	5.51	dB
Tracking E Balance 2	Tbe2	SG3 0.3Vp-p, 1kHz, sine, $802		−0.74	2.74	5.74	dB
Tracking E Balance 3	Tbe3	SG3 0.3Vp-p, 1kHz, sine, $804		0.17	3.17	6.17	dB
Tracking E Balance 4	Tbe4	SG3 0.3Vp-p, 1kHz, sine, $808		1.03	4.03	7.03	dB
Tracking E Balance 5	Tbe5	SG3 0.3Vp-p, 1kHz, sine, $810		2.63	5.63	8.63	dB
FGFN-FGF1	∆FG1	–	–	0	1.5	3	dB
FGFN-FGF2	∆FG2	–	–	0.5	2.0	3.5	dB
FGFN-FGF3	∆FG3	–	–	2.0	3.25	4.5	dB
FGFN-FGF4	∆FG4	–	–	3.0	4.25	5.5	dB
TBE5 – TBE4	∆TB1	–	–	0.6	1.6	2.6	dB
TBE4 – TBE3	∆TB2	–	–	−0.14	0.86	1.86	dB
TBE3 – TBE2	∆TB3	–	–	−0.57	0.43	1.43	dB
TBE2 – TBE1	∆TB4	–	–	−0.77	0.23	1.23	dB
APC PSUB Voltage 1	Vapc1	LDON, $854, SG4 GND+85mV	pin 69	–	–	1.2	V
APC PSUB Voltage 2	Vapc2	LDON, $854, SG4 GND+185mV		2.5	–	–	V
APC NSUB Voltage 1	Vapc3	LDON, $850, SG4 GND+95mV		2.5	–	–	V
APC NSUB Voltage 2	Vapc4	LDON, $850, SG4 GND+165mV		–	–	1.2	V
APC LD Off Voltage 1	Vapc5	LDOFF, $85C, SG4 1.6V		2.6	–	–	V
APC LD Off Voltage 2	Vapc6	LDOFF, $858, SG4 2.5V		–	–	1.1	V
APC Maximum Output Current H	Vapc7	LDON, $854, SG4 GND + 185mV		1.6	–	–	V
APC Minimum Output Current L	Vapc8	LDON, $854, SG4 GND + 85mV		–	–	1.6	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Mirror Maximum Output Voltage H	Vmirh	SG4 1.2V+0.8Vp-p, 1kHz,sine	pin 38	2.7	–	–	V
Mirror Minimum Output Voltage L	Vmirl	SG4 1.2V+0.8Vp-p, 1kHz,sine		–	–	0.5	V
Mirror Minimum Operating Frequency	Fmirh	SG4 1.2V + 0.8Vp-p, 900Hz,sine		–	550	900	Hz
Mirror Maximum Operating Frequency	Fmirb	SG4 1.2V+0.8Vp-p, 30kHz,sine		30	75	–	kHz
Mirror AM Frequency Characterstic	Fmir	SG4 1.2V+0.8Vp-p, 600Hz, fc=600kHz 55% modulation		-	400	600	Hz
Mirror Minimum Input Voltage	Vmir	SG4 1.2V + 0.2Vp-p, 10kHz,sine		–	0.1	0.2	V
Mirror Maximum Input Voltage	Vmih	SG4 1.2V+1.8Vp-p, 10kHz,sine	pin 39	1.8	–	–	V
FOK Threshold Voltage	Vfokt	SG4 1.35V - 1.1V, DCsweep, 5mV step		−420	−360	−300	mV
FOK Output Voltage H	Vfokh	SG4 DC 1.0V		2.7	–	–	V
FOK Output Voltage L	Vfokl	SG4 DC 1.6V		–	–	0.5	V
Defect Output Voltage H	Vdfcth	$863,SG3 1.615V+0.032Vp-p f = 1kHz,sine	pin 40	2.7	–	–	V
Defect Output Voltage L	Vdfcth	$863,SG3 1.615V+0.032Vp-p f = 1kHz,sine		–	–	0.5	V
Focus Loop Mute	Fmute	SG2 1.6V+0.1Vp-p 1kHz,sine	pin 47	−100	0	100	mV
Tracking Loop Mute	Tmute	SG2 1.6V+0.1Vp-p 1kHz,sine	pin 49	−100	0	120	mV
Loop mute offset voltage	Vteo1	No input		-100	0	100	mV
Interruption	Imute	$854 SG2 1.6V+0.1Vp-p 1kHz,sine		−100	0	120	mV
Interruption on 1	Imute1	$857 SG2 1.6V+0.1Vp-p 1kHz,sine		-100	0	100	mV
Interruption on 2	Imute2	$855 SG2 1.6V+0.1Vp-p 1kHz,sine		-100	0	100	mV

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ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Defect Bottom Voltage	Fdfct1	SG3 1.620V+0.04Vp-p, 1kHz,sine	pin 40	–	670	1000	Hz
Defect Max Freq. Voltage	Fdfct2	SG3 1.620V+0.04Vp-p, 2kHz,sine		2.0	4.7	–	kHz
Defect Minimum Input Voltage	Vdfct1	SG 3 1.610V+0.020Vp-p, 1kHz,sine		–	0.3	0.5	V
Defect Maximum Input Voltage	Vdfct2	SG3 1.635V+0.070Vp-p, 1kHz,sine		1.8	–	–	V
EFM Duty Voltage 1	Defm1	SG4 1.6V+0.75Vp-p, 750kHz,sine	pin 31	–50	0	50	mV
EFM Duty Voltage 2	Defm2	SG4 1.85V+0.75Vp-p, 750kHz,sine		0	50	100	mV
EFM Minimum input Voltage	Vefm1	SG4 1.6V+0.12Vp-p, 750kHz,sine	pin 32	–	–	0.12	V
EFM Maximum input Voltage	Vefm2	SG4 1.2V+1.8Vp-p 750kHz,sine		1.8	–	–	V
EFM Maximum Operating Frequency	Fefm	SG4 1.6V+0.75Vp-p 4MHz sine		4	–	–	MHz
EFM duty check	EFMduty	SG4 1.6V+0.75Vp-p 750kHz sine		45	50	55	%
FZC Threshold Voltage	Vfzc	DC 1.6V+34mV,100mV	pin 30	35	69	100	mV
ATSC Threshold Voltage 1	Vatsc1	$10,SG2 DC 1.6V-6mV –67mV		–67	–37	–7	mV
ATSC Threshold Voltage 2	Vatsc2	SG2 DC 1.6V+6mV,+67mV	pin 33	7	37	67	mV
TZC Threshold Voltage	Vtzc	$20,SG2 DC 1.6V-30mV +30mV	pin 30	–30	0	30	mV
SSTOP Threshold Voltage	Vsstop	$30,SG2 DC 1.6V-100mV –30mV		–100	–50	–30	mV
Tracking gain window voltage	VtGW	$840+$830 SG2 1.6V+ 199mV, 300mV DC sweep 5mV step	pin 29	200	250	300	mV
Tracking gain window range	VTGW2	$848+$830 SG2 1.6V+ 99mV, 200mV DC sweep 5mV step		100	150	200	mV

ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, $V_{DD} = D_{VDD} = V_{CC}$ = +3.2V, $V_{SS} = D_{VSS}$ = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Tracking balance window voltage	VTBW	$844+$810 SG2 1.6V + 99mV, -25mV 5mV DC sweep	pin 30	−25	15	55	mV
Tracking balance window range	VTBW2	$844+$810 SG2 1.6V + 99mV, -25mV 5mV DC sweep		−25	15	55	mV
Center Voltage	VCVO	1.6V Reference	pin 70	−100	0	100	mV
VREF Current Drive Voltage 1	VCVO1	1.6V Reference	pin 70	−100	0	100	mV
VREF Current Drive Voltage 2	VCVO2	1.6V Reference	pin 70	−100	0	100	mV
Post CH1 Freq. Characteristic	Fpos1	SG1 1.6V+1Vp-p 40kHz,sine	pin 12	−4.5	−3.0	−1.5	dB
Post CH2 Freq. Characteristic	Fpos2	SG1 1.6V+1Vp-p 40kHz,sine	pin 11	−4.5	−3.0	−1.5	dB
Post CH1 Mute	Mute1	Mute=3.2V SG1 1.6V+1Vp-p,1kHz,sine	pin12	−	−	-35	dB
Post CH2 Mute	Mute2	Mute=3.2V SG1 1.6V+1Vp-p,1kHz,sine	pin 11	−	−	-35	dB
Post CH1 offset	Vpos1	Mute=0V	pin 12	-50	0	50	mV
Post CH2 offset	Vpos2	Mute=0V	pin 11	-50	0	50	mV
Post CH1 Gain	Gpos1	Mute=0V, 1.6V+1Vp-p, 20kHz sine	pin 12	-1.5	0	1.5	dB
Post CH2 Gain	Gpos2	Mute=0V, 1.6V+1Vp-p, 20kHz sine	pin 11	-1.5	0	1.5	dB
Focus Loop DC Gain	Gf	$08, SG2 DC 1.7V, 1.5V average	pin 47	19.0	21.5	24.0	dB
Focus Off Offset	Vosf1	$00	pin 47	−100	0	100	mV
Focus On Offset	Vofs2	$08,DC 1.5V	pin 47	0	250	500	mV
Focus Auto Offset	Vaof	$842, WDCK, after 100ms	pin 47	−65	0	65	mV
ISTAT status after focus offset adjustment	Vistat2	$86F+842	pin 30	2.7	-	-	V

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ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
FE bias voltage after focus offset adjustment	Vteo3	after focus offset adjustment	pin 47	-50	0	50	mV
Focus Output Voltage H	Vfoh1	$08, DC 2.1V	pin 47	2.8	–	–	V
Focus Output Voltage L	Vfol1	$08, DC 1.1V	pin 47	–	–	0.60	V
Focus Oscillation Voltage	Vosc	$08, DC 1.6V	pin 47	0	100	200	mV
Focus Feed Through	Gff	Gain Difference at Servo on and off	pin 47	–	–	−35	dB
Focus AC Gain 1	Gfa1	$08, SG2 1.6V+0.1Vp-p 1.2kHz,sine	pin 47	19.0	23.0	27.0	dB
Focus AC Phase 1	Pfa1	$08, SG2 1.6V + 0.1Vp-p 1.2kHz,sine	pin 47	40	65	90	deg
Focus AC Gain 2	Gfa2	$08, SG2 1.6V + 0.1Vp-p 2.7kHz,sine	pin 47	14.0	18.5	23.0	dB
Focus AC Phase 2	Pfa2	$08, SG2 1.6V+0.1Vp-p 2.7kHz,sine	pin 47	40	65	90	deg
Focus Search Voltage1	Vfs1	$30+$02	pin 47	−0.65	−0.50	−0.35	V
Focus Search Voltage2	Vfs2	$30+$03	pin 47	0.35	0.50	0.65	V
Focus Loop Total Gain	Gftg	Focus PD gain + Focus loop DC gain	pin 47	49.5	51.5	53.5	dB
Tracking DC Gain	Gto	$25 SG2 DC 1.4V, 1.8V average gain	pin 49	13.5	15.5	17.5	dB
Tracking Off Offset	Vost1	$20	pin 49	−100	0	100	mV
Tracking On Offset	Vost2	SG2, DC 1.6V, $25	pin 49	−100	0	120	mV
Tracking Oscillation Voltage	Vosa1	$25, SG2 DC 1.6V	pin 49	0	100	200	mV
Tracking gain boost for ATSC	Gatsc	1.6V + 0.1Vp-p, 1kHz, sine	pin 49	17.5	20.5	23.5	dB
Tracking gain boost on LOCK (L)	Glock	1.6V + 0.1Vp-p,1kHz,sine	pin 49	17.5	20.5	23.5	dB
Tracking Output Voltage H	Vth1	$25,SG2 DC 0.6V	pin 49	2.8	–	–	V
Tracking Output Voltage L	Vtl1	$25, SG2 , DC 2.6V	pin 49	–	–	0.6	V
Tracking Jump Voltage 1	Vtj1	$2C	pin 49	−0.65	−0.5	−0.35	V
Tracking Jump Voltage 2	Vtj2	$28	pin 49	0.35	0.5	0.65	V
Direct 1 track jump 1	Vdir1	$28 + 877	pin 49	0.35	0.5	0.65	V
Direct 1 track jump 2	Vdir2	$2C + 877	pin 49	−0.65	−0.5	−0.35	V

ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Tracking Feed Through	Gtf	Gain Difference at Tracking servo on and off	pin 49	–	–	−39	dB
Tracking AC Gain 1	Gta1	$10,$25,SG2 1.6V + 0.1Vp-p, 1.2kHz,sine	pin 49	9.0	12.5	16.0	dB
Tracking AC Phase 1	Pta1	$10, $25, SG2 1.6V+ 0.1Vp-p, 1.2kHz,sine	pin 49	−140	−115	−90	deg
Tracking AC Gain 2	Gta2	$10, $25, SG2 1.6V+ 0.1Vp-p, 2.7kHz, sine	pin 49	17.5	21.5	25.5	dB
Tracking AC Phase 2	Pta2	$10,$25,SG2 1.6V + 0.1Vp-p, 2.7kHz,sine	pin 49	−195	−150	−100	deg
Tracking Loop Gain	Gtrt	tracking Amp F gain+ servo DC gain	-	18.5	20.5	22.5	dB
Sled DC Gain	Gsl	SG2 DC 1.8V, 1.4V	pin 42	20.5	22.5	24.5	dB
Sled Feed Through	Gslf	Gain Difference at sled servo on and off SG2 1.6V + 0.1Vp-p 1.2kHz,sine	pin 42	–	–	−34	dB
Sled Output Voltage H	Vslh1	$25, SG2 DC 2.0V	pin 42	2.8	–	–	V
Sled Output Voltage L	Vsll1	$25, SG2 DC 1.2V	pin 42	–	–	0.6	V
Sled Forward Kick Voltage	Vsk1	$22	pin 42	0.38	0.60	0.75	V
Sled Reverse Kick Voltage	Vsk2	$23	pin 42	−0.75	−0.6	−0.38	V
Spindle Normal Speed Gain	Gsp	$F0 SG1 DC 1.7V, 1.5V, average gain	pin 45	14.0	16.5	19.0	dB
Spindle Double Speed Gain	Gsp2	$F3 SG1 DC 1.7V, 1.5V, average gain	pin 45	19.0	23.0	27.0	dB
Spindle Output Voltage H	Gsph1	$F0, SG1 DC 2.5V	pin 45	2.8	–	–	V
Spindle Output Voltage L	Gspl1	$F0, SG1 DC 0.7V	pin 45	–	–	0.6	V
Spindle AC Gain	Gspa	$F0,SG1 1.6V + 0.2Vp-p, 2kHz,sine	pin 45	−7.0	−3.5	0	dB
Spindle AC Phase	Pspa	$F0,SG1 1.6V + 0.2Vp-p, 2kHz,sine	pin 45	−120	−90	−60	deg

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ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, $V_{DD} = D_{VDD} = V_{CC}$ = +3.2V, $V_{SS} = D_{VSS}$ = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Post filter output voltage mix.1L	Vpom1L	SG1 1.6V + 1.5Vp-p, 1kHz, within THD 1%	pin 12	0.5	0.55	–	Vrms
Post filter output voltage mix. 2L	Vpom2L	SG1 1.6V + 1.5Vp-p, 1kHz, within THD 1%	pin 11	0.5	0.55	–	Vrms
Total harmonic distortion 1L	THD11L	SG1 f = 100Hz, 0dBm	pin 12	–	0.01	0.05	%
Total harmonic distortion 1L	THD12L	SG1 f=1kHz,0dBm	pin 12	–	0.01	0.05	%
Total harmonic distortion 1L	THD13L	SG1 f = 10kHz, 0dBm	pin 12	–	0.05	0.1	%
Total harmonic distortion 1L	THD14L	SG1 f = 16kHz, 0dBm	pin 12	–	0.1	0.2	%
Total harmonic distortion 1L	THD15L	SG1 f = 20kHz, 0dBm	pin 12	–	0.1	0.2	%
Total harmonic distortion 2L	THD21L	SG1 f = 100Hz, 0dBm	pin 11	–	0.01	0.05	%
Total harmonic distortion 2L	THD22L	SG1 f = 1kHz, 0dBm	pin 11	–	0.01	0.05	%
Total harmonic distortion 2L	THD23L	SG1 f = 10kHz, 0dBm	pin 11	–	0.05	0.1	%
Total harmonic distortion 2L	THD24L	SG1 f = 16kHz, 0dBm	pin 11	–	0.1	0.2	%
Total harmonic distortion 2L	THD25L	SG1 f = 20kHz, 0dBm	pin 11	–	0.1	0.2	%
Frequency Characteristics 1L	fv11L	SG1 f = 100Hz, 0dBm	pin 12	–0.1	0	0.1	dB
Frequency Characteristics 1L	fv12L	SG1 f = 1kHz, 0dBm	pin 12	–0.25	0	+0.25	dB
Frequency Characteristics 1L	fv13L	SG1 f = 10kHz, 0dBm	pin 12	–0.5	0	0.5	dB
Frequency Characteristics 1L	fv14L	SG1 f = 16kHz, 0dBm	pin 12	–1.0	0	1.0	dB
Frequency Characteristics 1L	fv15L	SG1 f = 20kHz, 0dBm	pin 12	–1.5	0	1.5	dB
Frequency Characteristics 2L	fv21L	SG1 f = 100Hz, 0dBm	pin 11	–0.1	0	0.1	dB
Frequency Characteristics 2L	fv22L	SG1 f = 1kHz, 0dBm	pin 11	–0.25	0	+0.25	dB
Frequency Characteristics 2L	fv23L	SG1 f = 10kHz, 0dBm	pin 11	–0.5	0	0.5	dB
Frequency Characteristics 2L	fv24L	SG1 f = 16kHz, 0dBm	pin 11	–1.0	0	1.0	dB
Frequency Characteristics 2L	fv25L	SG1 f = 20kHz, 0dBm	pin 11	–1.5	0	1.5	dB

ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, V_{DD} = D_{VDD} = V_{CC} = +3.2V, V_{SS} = D_{VSS} = GND = V_{SSP} = 0V)

Characteristic	Symbol	Test Conditions	Output	Min.	Typ.	Max.	Unit
Cross talk 1L	CT11L	SG1 100Hz, 0dBm, ratio on Ch2	pin 12	67	80	–	dB
Cross talk 1L	CT12L	SG1 1kHz, 0dBm, ratio on Ch2	pin 12	62	75	–	dB
Cross talk 1L	CT13L	SG1 10kHz, 0dBm, ratio on Ch2	pin 12	57	65	–	dB
Cross talk 2L	CT21L	SG1 100Hz,0dBm,ratio on Ch1	pin 11	67	80	–	dB
Cross talk 2L	CT22L	SG1 1kHz,0dBm,ratio on Ch1	pin 11	62	75	–	dB
Cross talk 2L	CT23L	SG1 10kHz,0dBm, ratio on Ch1	pin 11	57	65	–	dB
Signal to noise ratio 1L	S/N1L	DC 2.5V 0dbm, ratio on Noise	pin 12	67	80	–	dB
Signal to noise ratio 2L	S/N2L	DC 2.5V 0dbm, ratio on Noise	pin 11	67	80	–	dB
Channel balance L	CBL	Gain Difference Ch1 and Ch2	-	–0.1	0	+0.1	dB

NOTE: The notation $ means hexa decimal of MICOM command, and Low voltage test items only refer to S1L9223B02-L

TEST CIRCUIT
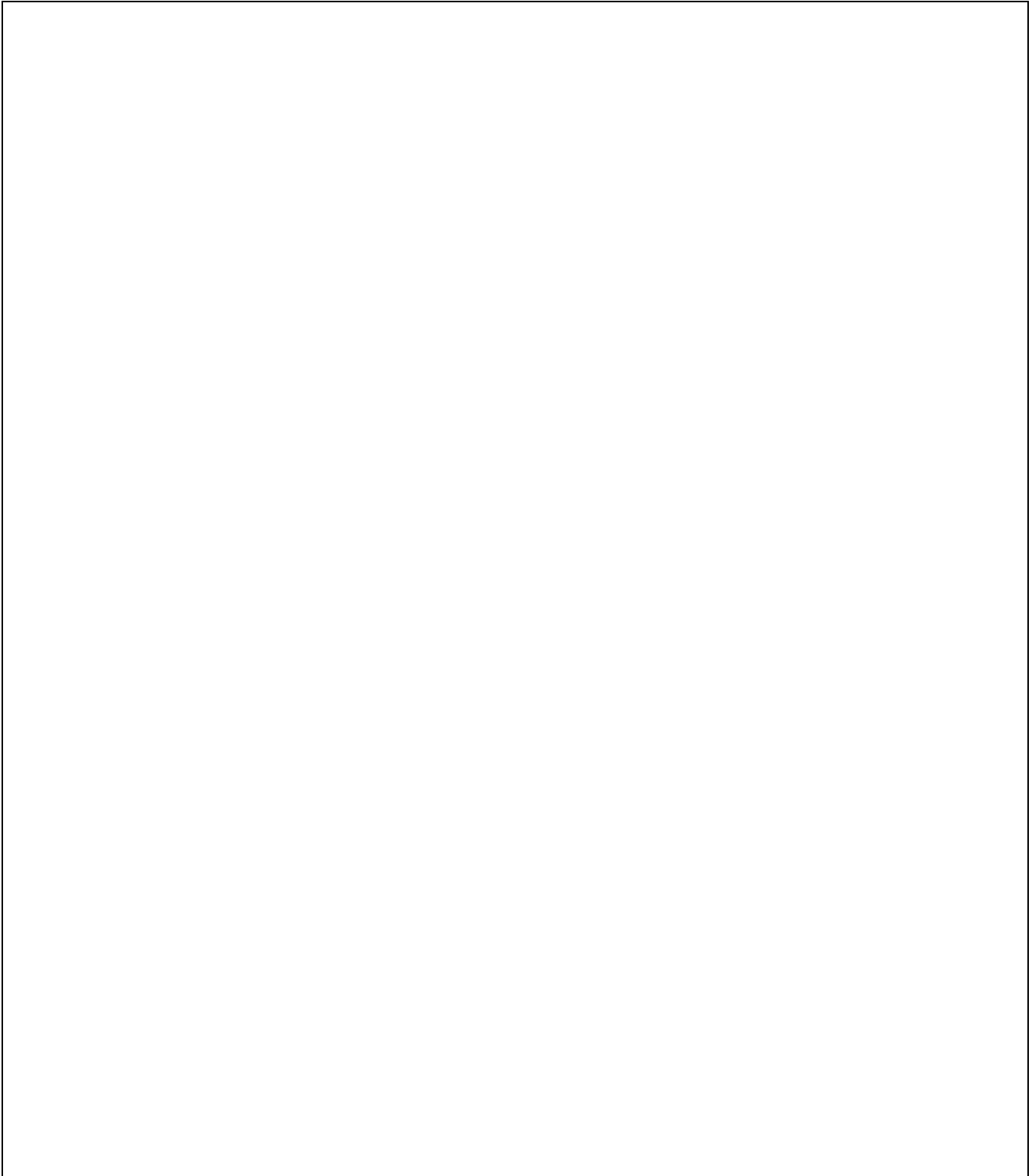
FUNCTIONAL DESCRIPTION

RF AMP BLOCK

RF AMPLIFIER

The optical currents input through pins PD1(A+C) and PD2(B+D) are converted into voltages through I-V amp, and they are added to RF summing amp. The voltage, converted from the photo diode (A+B+C+D) signal, is output through RFO (pin74) and the eye pattern can be checked at this pin.
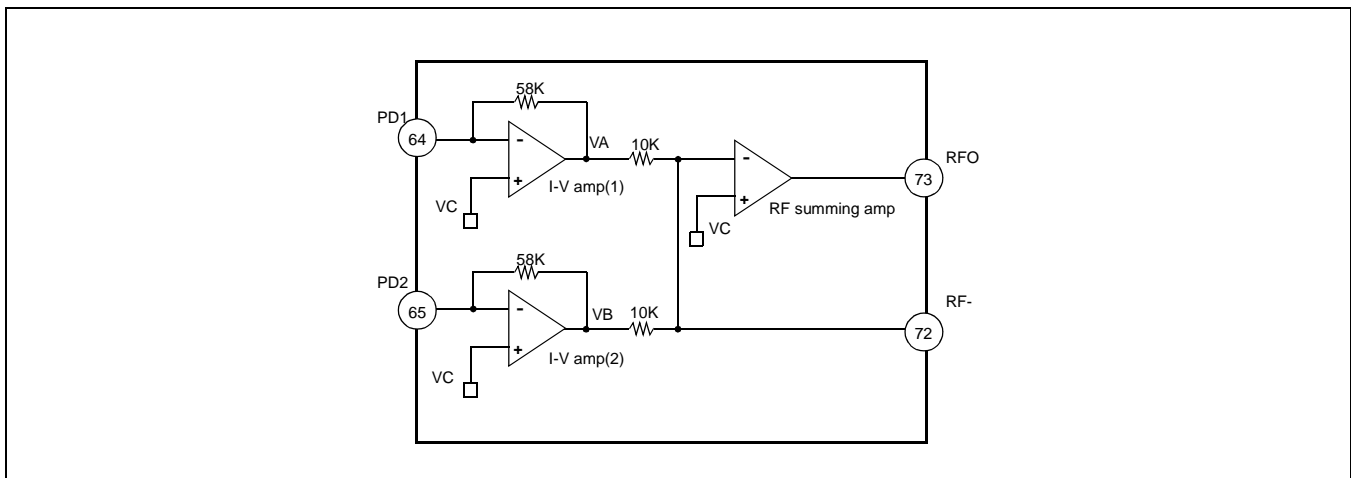
Figure 1. RF Amplifier Circuit

FOCUS ERROR AMP

The output of the focus error amp is the difference between I-V amp(1) output VA and

RF I-V amp(2) output VB. The focus error bias voltage applied to the (+) of focus error amp can be changed by output voltage of D/A converter as shown in diagram, so that the offset of focus error amp can be adjusted automatically by controlling 5 bits counter switches. Focus error bias can be adjusted from the range of +100mV — -100mV by connecting the resistor on pin 63 (FEBIAS).

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1. VA and VB refer to output signal of PD1 and PD2 I/V amp.
2. sev-stopb,sev-stop,fe-stopb and fcmpo are internal signals
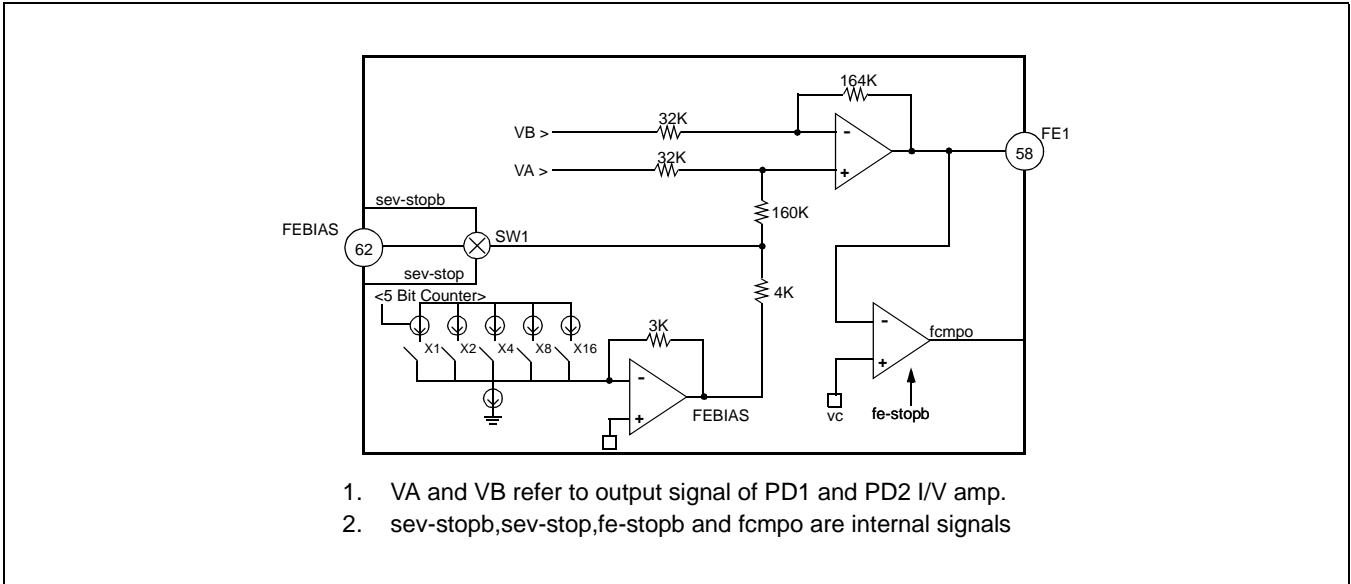
Figure 2. Focus Error Amplifier Circuit

TRACKING ERROR AMP

The optical currents detected from the side photo diode (E and F) pf pick-up are input to the E and F pin and converted into voltage signals by E I-V and F I-V amp. The output of tracking error amp generates the difference between E I-V AMP and F I-V AMP voltage output.

The E-F balance can be adjusted by modifying the gain of E I-V AMP, and the tracking gain can be adjusted automatically by controlling the peak voltage at pin TE2 by MICOM program.
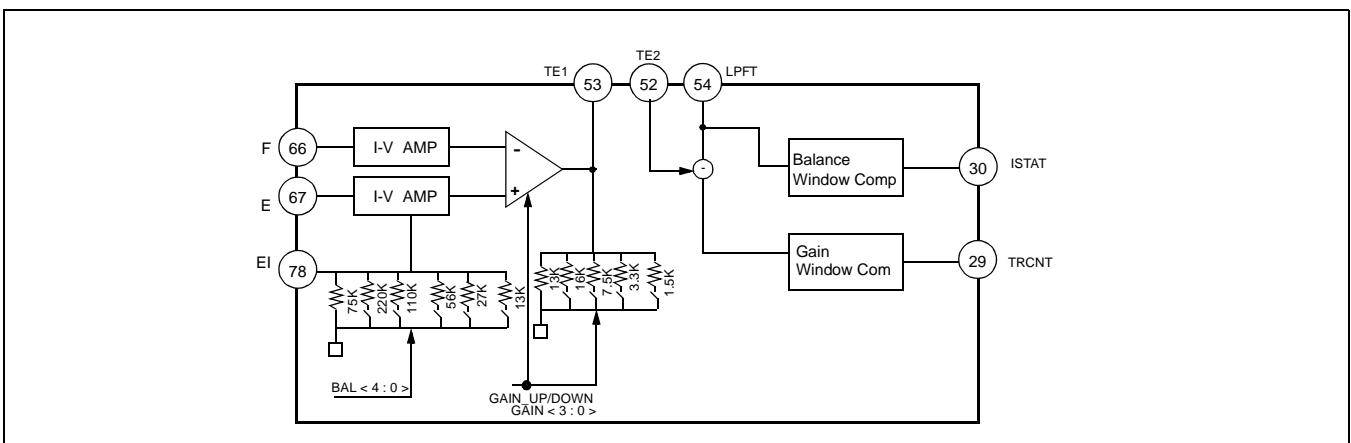
Figure 3. Tracking Error Amplifier Circuit

FOCUS OK CIRCUIT

The FOK is the output. The focus OK circuit generates a timing window to enable focus servo operation from focus search status. When the difference of the RFO (pin74) signal and DC coupled signal IRF (pin75) are above the predefined voltage the Focus OK circuit output (pin40) becomes active (High output). The predefined voltage is -0.39V
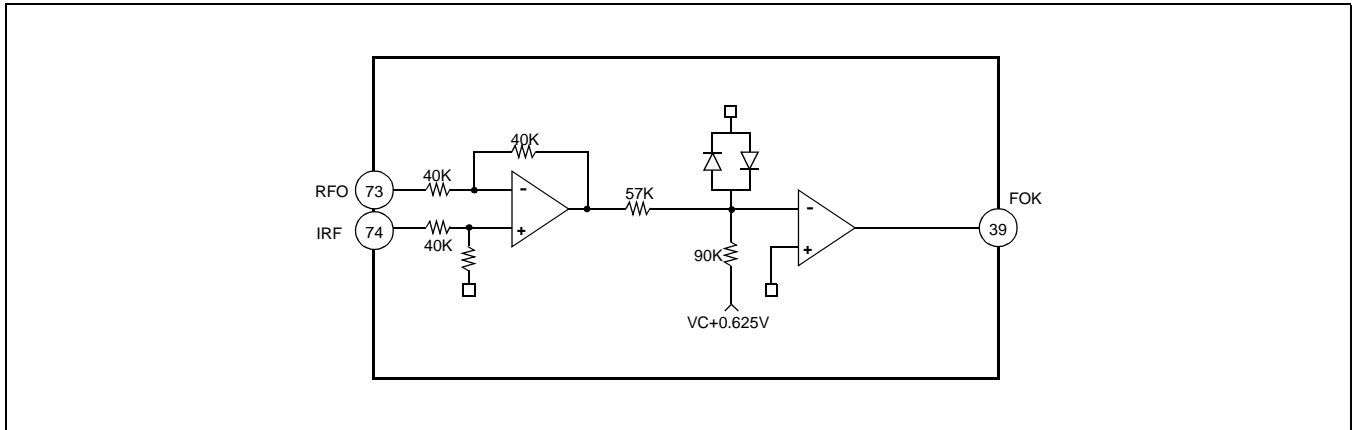
Figure 4. Focus OK Circuit

MIRROR CIRCUIT

IRF signal is amplified by the mirror amp, and the peak and bottom component of amplified signal are detected by peak and bottom hold circuit. The peak hold circuit covers traverse signal of up to 100KHz component and bottom hold circuit capable of covering the envelope frequency of disc rotation. The time constant for the mirror hold must be sufficiently larger than that of the traverse signal.
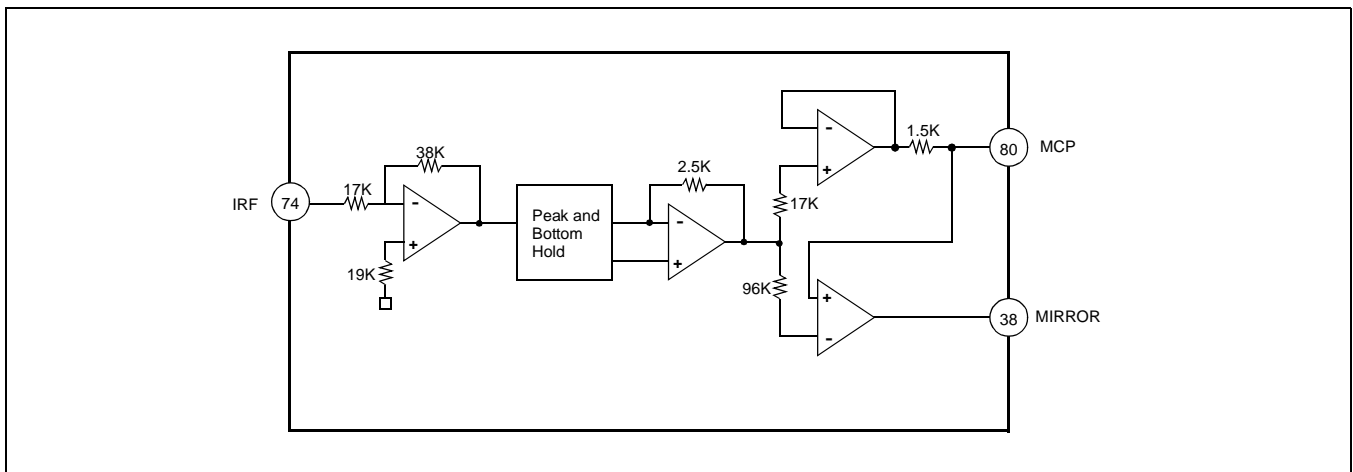
Figure 5. Mirror Circuit

EFM COMPARATOR

The EFM comparator converts a RF signal into a binary signal.

Because the asymmetry generated due to variations in disc manufacturing can not be eliminated by the AC coupling alone, this circuit uses to control reference voltage of EFM comparator for eliminating asymmetry.
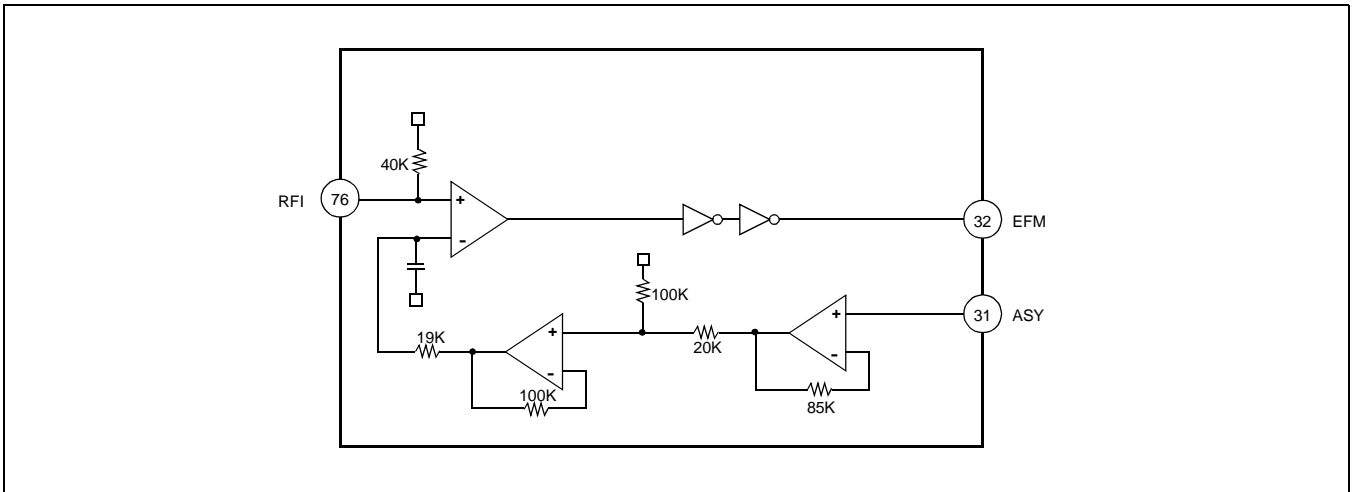
Figure 6. EFM Comparator & Asymmetry Circuit

DEFECT CIRCUIT

The RFO signal bottom, after being inverted, is held with two time constants of long and short.

The short time-constant bottom hold is done for a disc mirror defect more than 0.1msec, the long time-constant bottom hold is done with the mirror level prior to the defect. By differentiating this with a capacitor coupling and shifting the level, both signals are compared to generate the mirror defect detection signal.
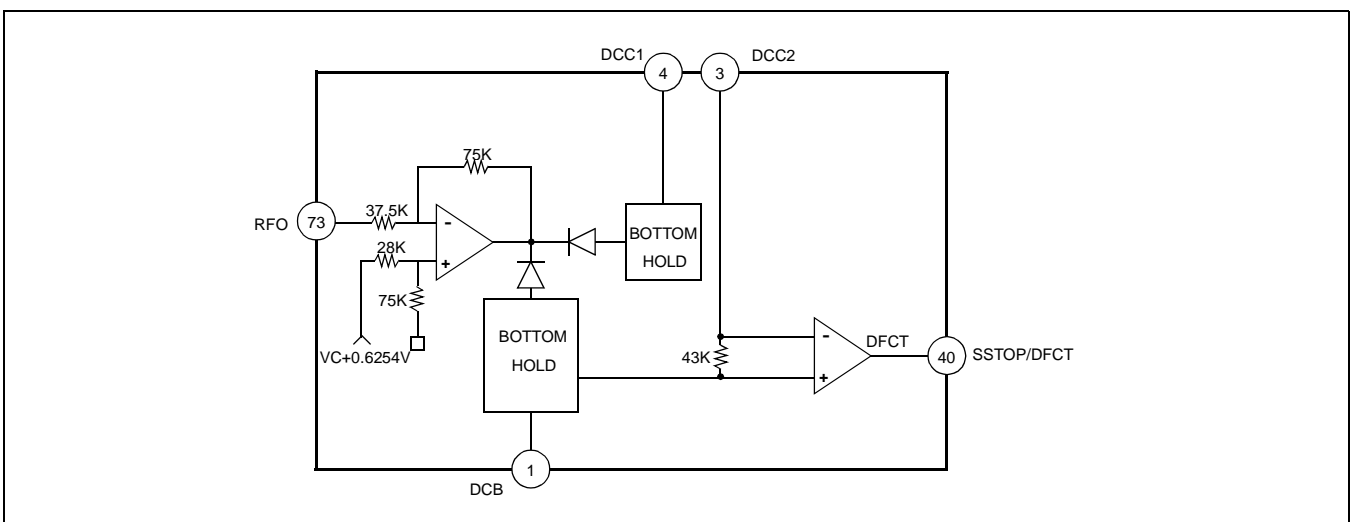
Figure 7. Defect Circuit

APC (AUTO POWER CONTROL) CIRCUIT

The laser diode has large negative temperature characteristic in its optical output when driven with a constant current on laser diode. Therefore, the output on processing monitor photo diode, must be a controlled current for getting regular output power, thus the APC (Auto Power Control) circuit is composed.
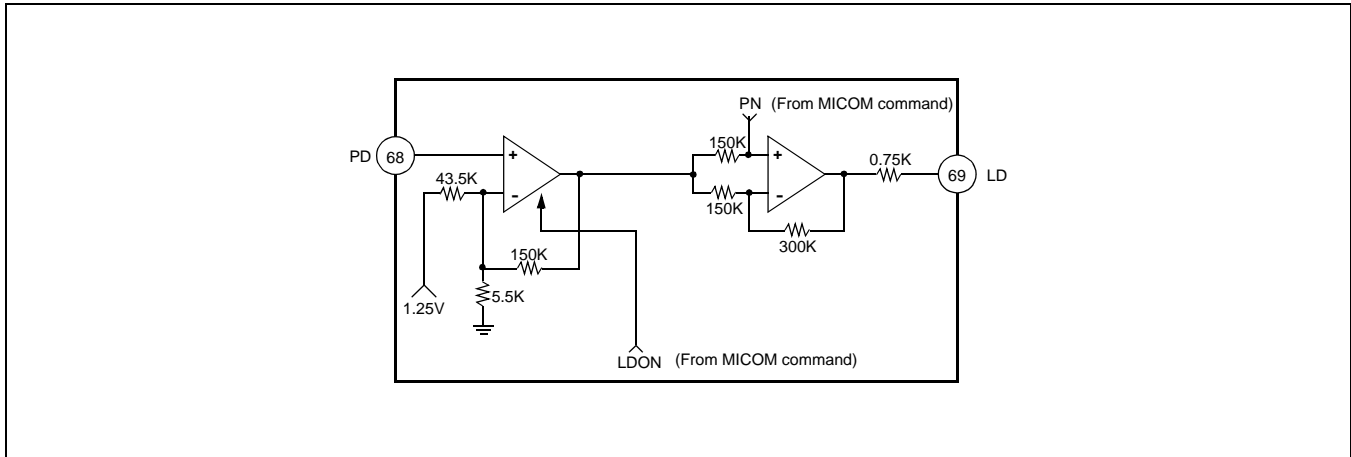
Figure 8. APC Circuit

AGC STABILITY CIRCUIT

The AGC block is the function used to maintain the constant level of RF peak to peak voltage. After the operation of RF envelop detection and comparing with reference voltage, RFO level is kept stable in 1Vp-p, and input to EFM Slice.

Figure 9. AGC Block

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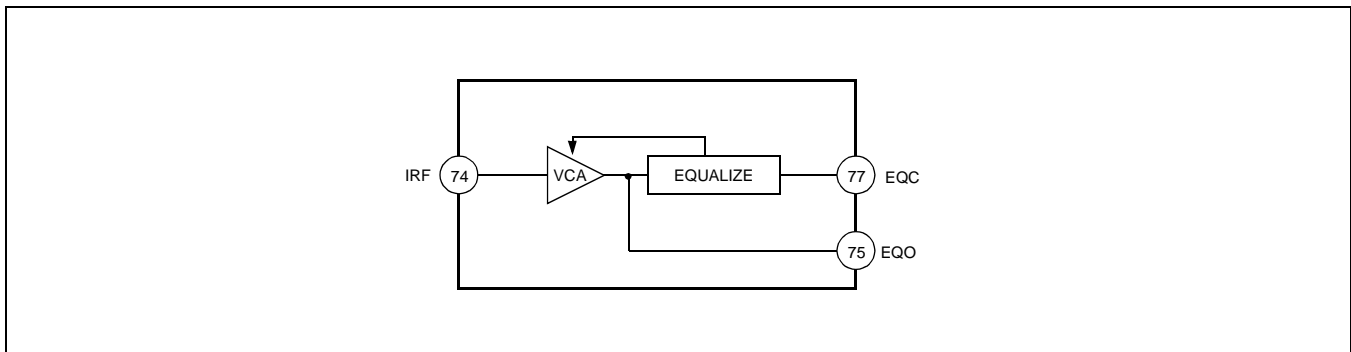
POST FILTER

The adjustment of audio output gain and the integration of possible de-emphasis output are executed by this circuit. This block has amps of 2 channel for gain and filter setting and mute pin for audio signal muting.
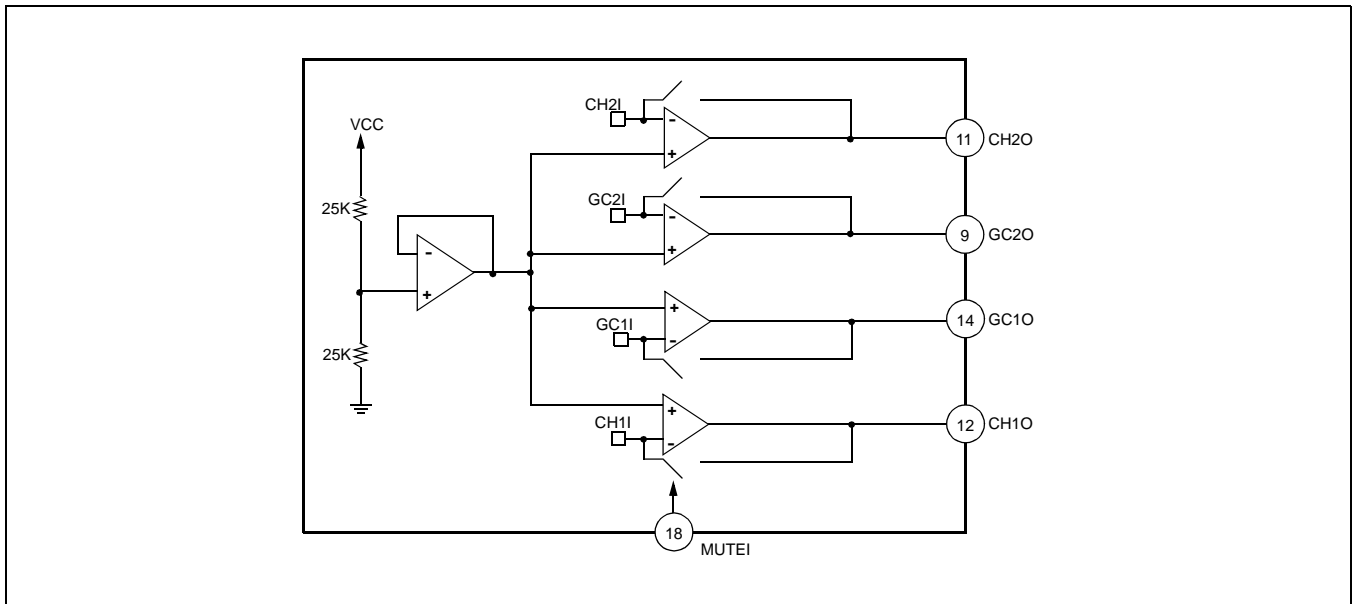
Figure 10. Post Filter Circuit

CENTER VOLTAGE GENERATION CIRCUIT

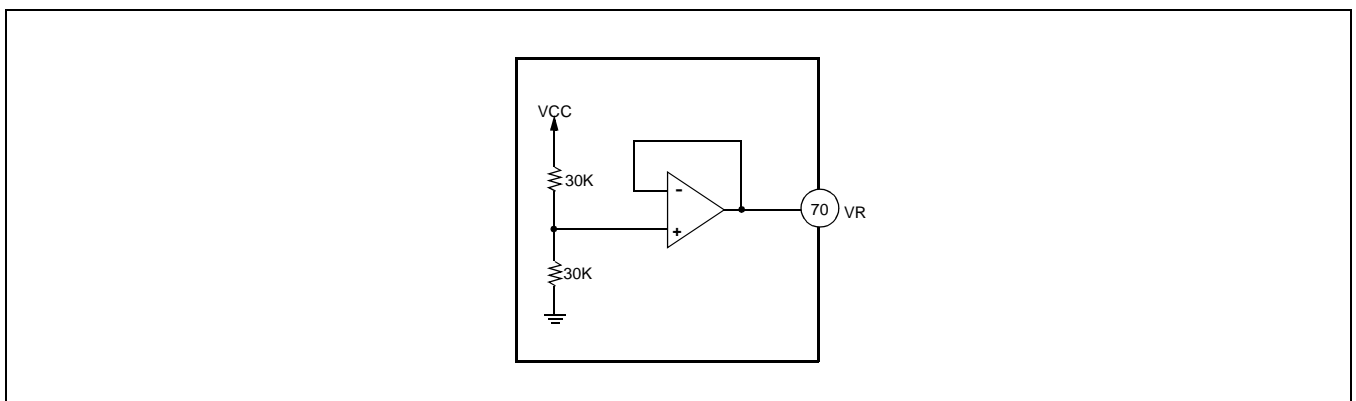The center voltage is generated by voltage divide using resistor.

Figure 11. Center Voltage Generation Circuit

SERVO BLOCK

FOCUS SERVO BLOCK

When defect is "H" (the defect signal is detected), the focus servo loop is muting in case of focus phase compensation. At this time, the focus error signal is output through the low pass filter formed by connecting a capacitor (0.1µF) and a built-in 470KΩ resistor to the FDFCT pin (pin 60). Accordingly, the focus error output is held at the error value just before defect error during defect occurring. The peak frequency of focus loop phase compensation is at about 1.2KHz when the resistor connected to FSET pin (pin 6) is 510KΩ, and it is inversely proportional to the resistor connected to the FSET pin. While the focus search is operating, the FS4 switch is on and then the focus error signal is isolated, accordingly the focus search signal is output by FEO pin (pin 48). When the FS2 switch is on (focus on), the focus servo loop is on and the focus error signal from FE2 pin (pin 58) is output through the focus servo loop.
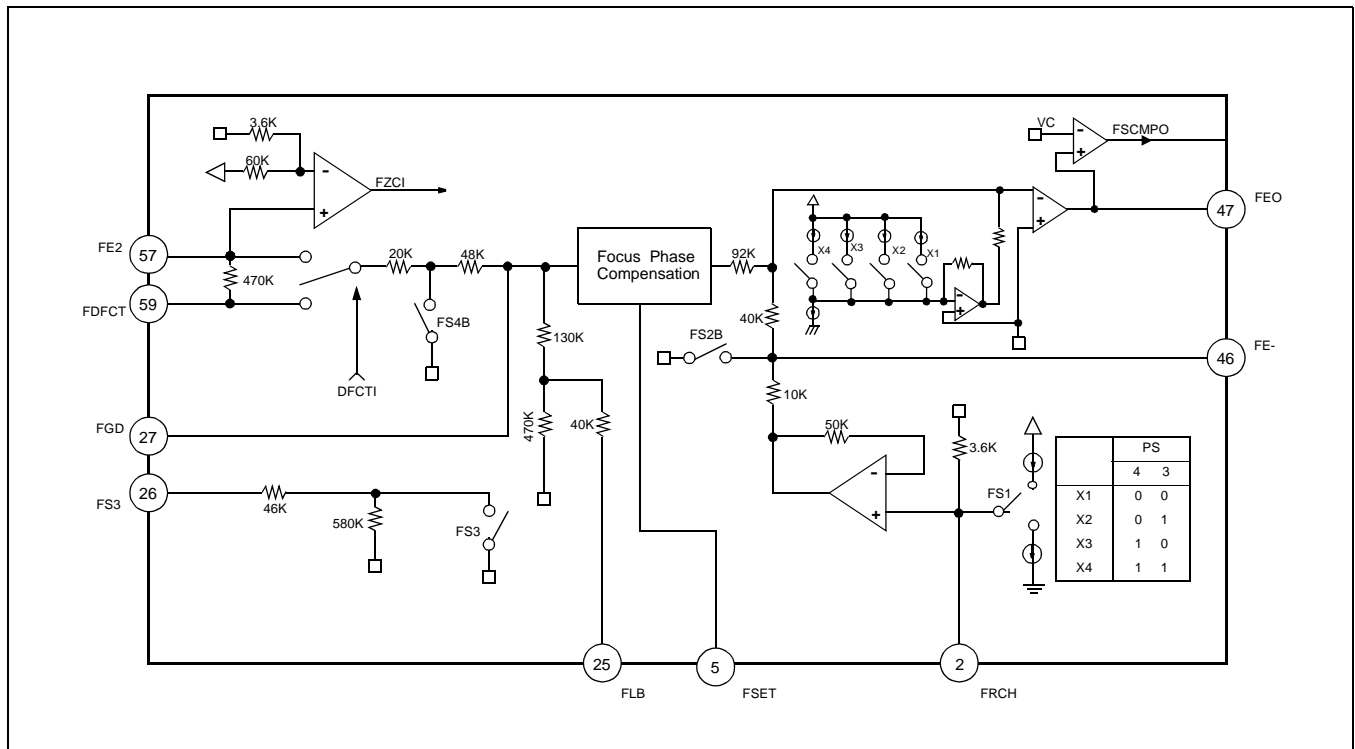
Figure 12. Focus Servo Block

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TRACKING SERVO BLOCK

During detection of defect, the tracking error signal is output through the tracking servo loop after passing the low pass filter formed by connecting a capacitor (0.1µF) and a built-in 470KΩ resistor to the TDFCT pin (pin57) in case of tracking phase compensation. The value of tracking gain up/down can be controlled by TGU and TG2 pin. The peak frequency of tracking loop phase compensation, the dynamic range and offset of OP AMP can be adjusted by changing the value of resistor connected to FSET pin same as focus loop. In case of unstable status of actuator after jumping, the ON/OFF of tracking loop is controlled by TM7 switch of break circuit.

After 10-track jumping, servo circuit gets out of the liner range and actuator's tracking becomes occasionally unstable. Hence unnecessary jumping with many tracking error should be prevented.
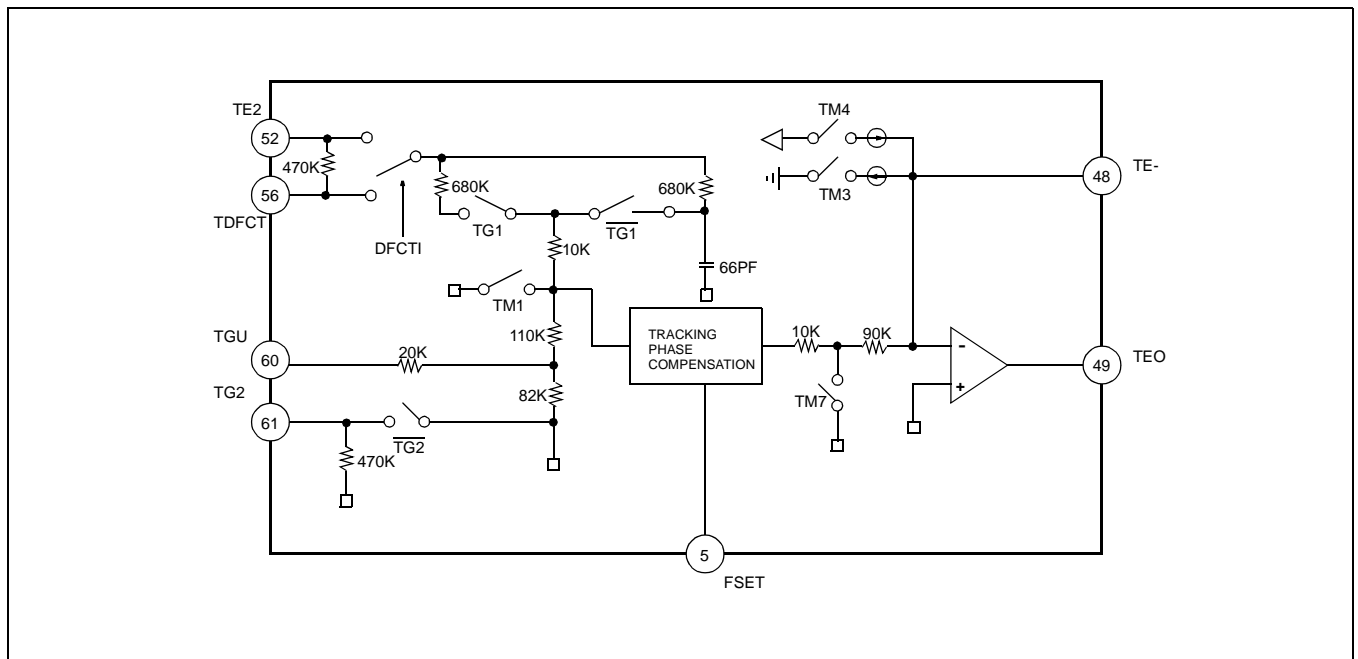

Figure 13. Tracking Servo Block

SLED SERVO BLOCK

The moving of pick-up is controlled by tracking servo output through a low pass filter.
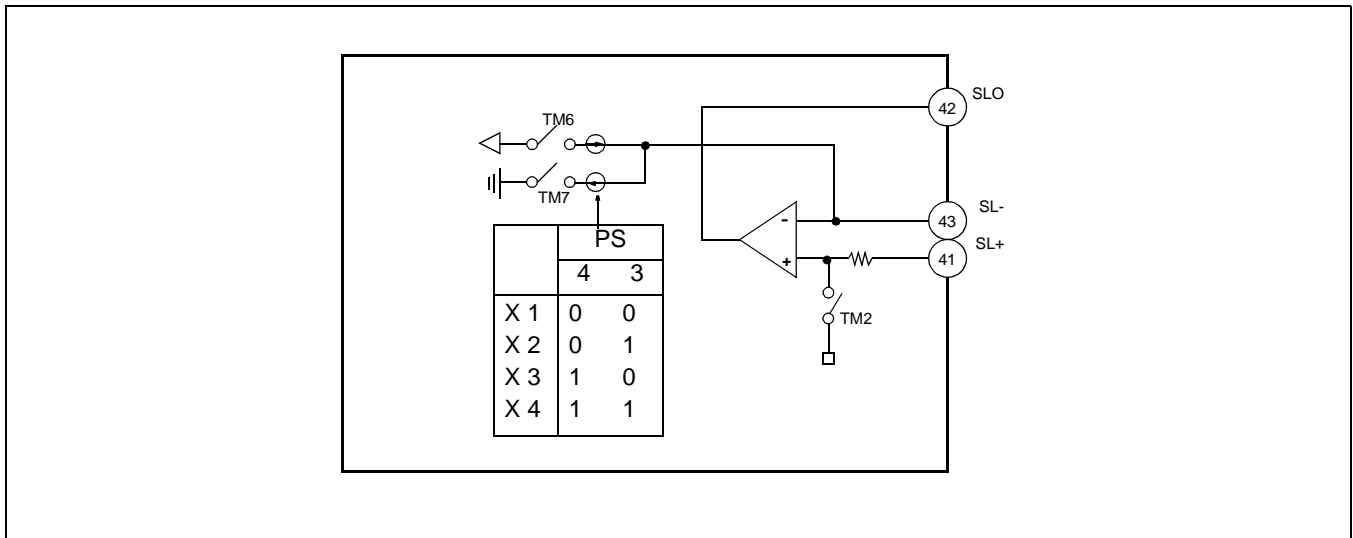The sled kick voltage is output for track jump operation.

Figure 14. Sled Servo Block

SPINDLE SERVO BLOCK

The 20KΩ resistor and 0.33uF capacitor form the 200Hz low pass filter, and the carrier component of spindle servo error signals is eliminated. In CLV-S mode, SMEF becomes "L" and pin 25 low pass filter fc lowers, strengthening the filter further. The characteristics of high frequency phase compensation in focus tracking servo and the characteristics of cut off frequency in CLV low pass filter are tested by FSET pin.
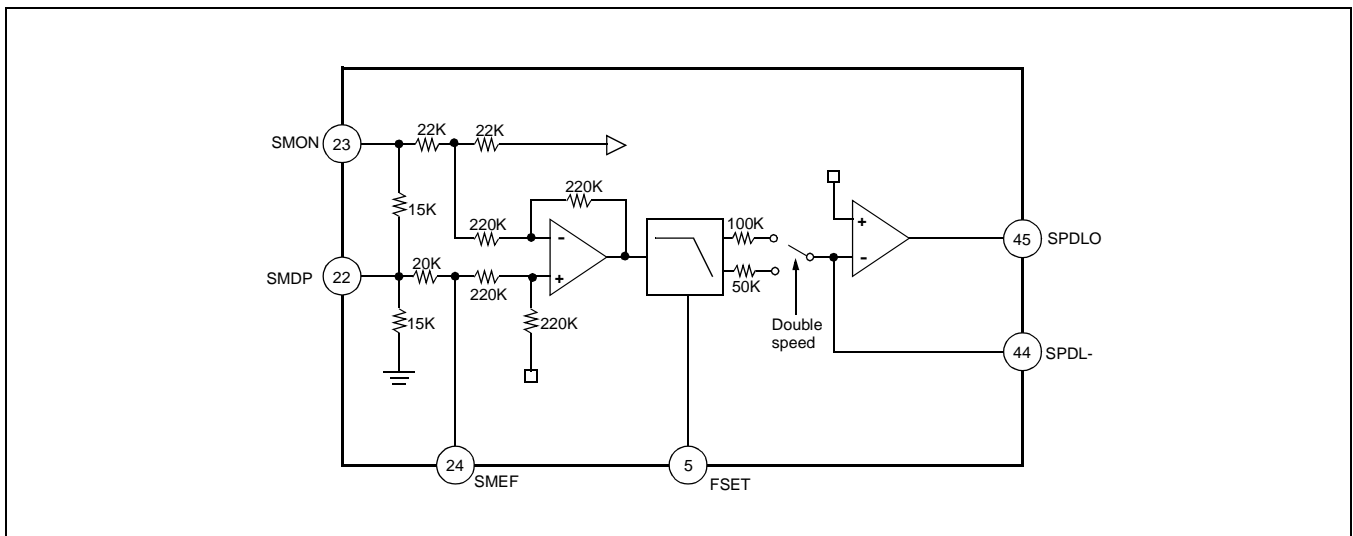

Figure 15. Spindle Servo Block

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DIGITAL BLOCK

DESCRIPTION

Digital block is transferred serial data by MICOM and 8-bit serial data is converted to parallel data by serial to parallel register. This data is decoded by latch signal. The status output of focus servo, tracking servo and sled servo system,etc. It is determined by each data. The auto-sequence function process 2 — 4 MICOM command by one auto-sequence command.
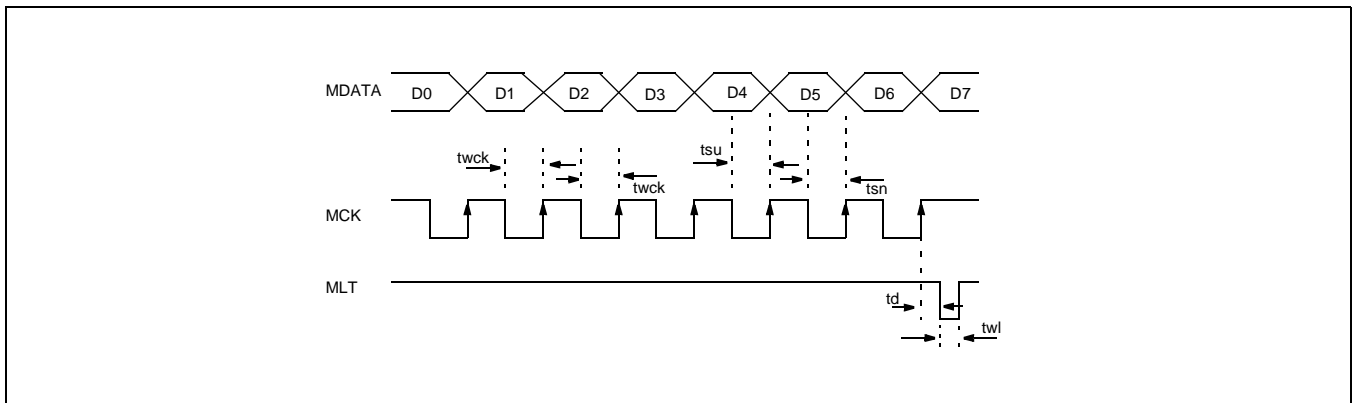

Figure 16. CPU Serial Interface Timing Chart

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	fck	–	–	1	MHz
Clock Pulse Width	fwck	500	–	–	ns
Hold Time	tsu	500	–	–	ns
Setup Time	tn	500	–	–	ns
Delay Time	td	500	–	–	ns
Latch Pulse Width	twl	1000	–	–	ns

MICOM COMMAND SET

Item		Hexa	Address				Data				ISTAT Out
			D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control		$0X	0	0	0	0	FS4 Focus On	FS3 Gain Down	FS2 Search On	FS1 Search Up	FZC
Tracking Control		$1X	0	0	0	1	Anti Shock	Brake On	TG2 Gain Set	TG1 Gain Set	A.S
Tracking Mode		$2X	0	0	1	0	Tracking Mode		Sled Mode		TZC
Select		$3X	0	0	1	1	PS4 Focus Search+2	PS3 Focus Search+2	PS2 Sled Kick+2	PS1 Sled Kick+1	STOP
Auto Sequence		$4X	0	1	0	0	AS3	AS2	AS1	AS0	/BUSY
R A M S E T	Blind/ overflow	$5X	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	Hi-Z
	Break						0.36ms	0.18ms	0.09ms	0.045ms	
	Kick	$6X	0	1	1	0	11.6ms	5.80ms	0.09ms	0.045ms	
	2N jump	$7X	0	1	1	1	64	32	16	8	
	move (M)						128	64	32	16	
Auto Adj.		$8XX	1	0	0	0	Offset, Balance, Gain, APC Control				–
Speed		$FX	1	1	1	1	$F0: Normal Speed $F3: Double Speed				–

Focus Control ($0X)

This command consists of 8 bits data and expressed by two hexa $0X.

D7	D6	D5	D4	D3	D2	D1	D0	ISTAT
0	**0**	**0**	**0**	**FS4**	**FS3**	**FS2**	**FS1**	**FZC**

FS4, FS3, FS2, FS1: internal switch for focus control

- Focus Search Operation (FS2,FS1)
  $02: FS2 switch become off and the value of servo output pin is as below.
  $(10\mu A-5\mu A)*50k*$(feedback Resistor/50k)
  $03: If FS1 switch is 1, the current supply is cut off and the discharge is performed.
  The waveform is as below and the time constant is determined by internal resistor 50K and external Cap.
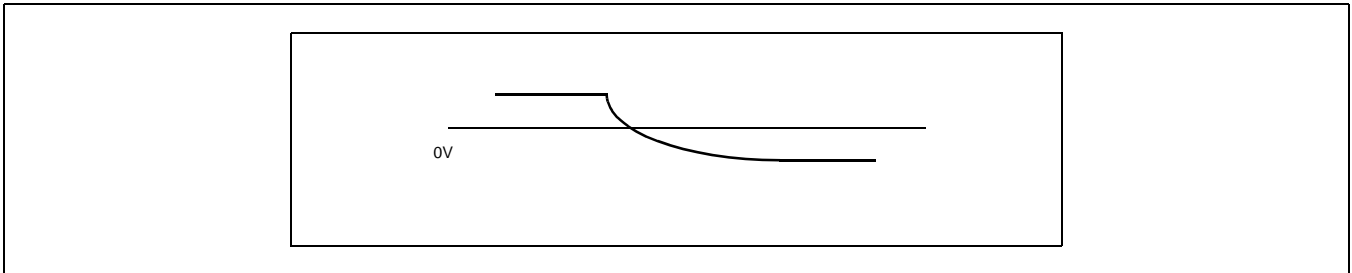
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Figure 17. Waveform at Pin 3 When FS1 Is Switched from 0 to 1

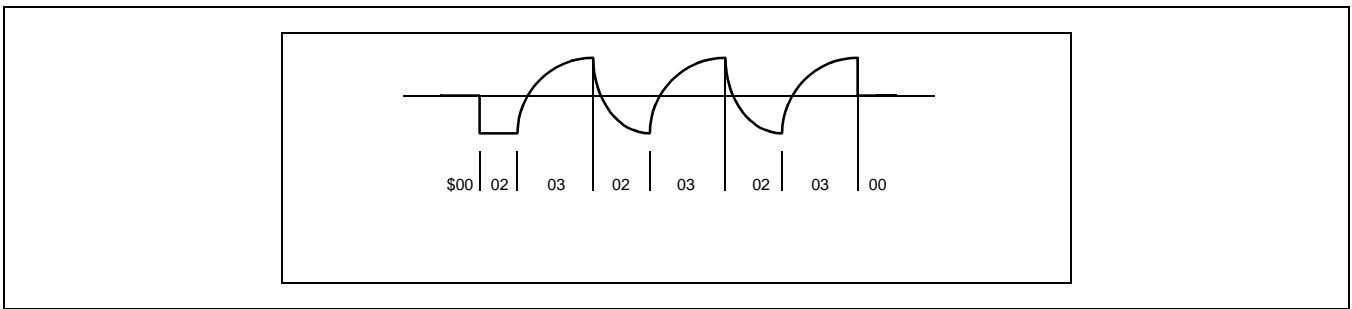The waveform of servo output pin according to FS1 and FS2 switches is as below.

Figure 18. Focus Search Waveform at Pin 48 by $02 and $03

FS4 is switch for on/off control of focus servo loop

$00: Focus servo off
$08: Focus servo on

Tracking Control ($1X)

This command is used for tracking loop gain control, break circuit and anti-shock on/off control.

D7	D6	D5	D4	D3	D2	D1	D0	ISTAT
0	0	0	1	Anti shock on/off	Break circuit on/off	TG2	TG1	Anti shock

TG2 and TG1 are internal switch for tracking gain set.

Tracking mode ($2X)

This command is used for tracking and sled servo on/off and jump for searching track.

D7	D6	D5	D4	D3	D2	D1	D0	ISTAT
0	0	1	0	Tracking control		Sled control		TZC

<Tracking control & Sled control>

D3	D2	Tracking mode	D1	D0	Sled mode
0	0	Tracking servo off	0	0	Sled servo off
0	1	servo on	0	1	servo on
1	0	Forward jump	1	0	Forward kick
1	1	Reverse jump	1	1	Reverse kick

Peak value set ($3X)

This command is used for the peak value setting of focus search and sled kick.

D0, D1: Sled kick
D2, D3: Focus search peak value

Auto Sequencer command ($4X)

This command is used for reducing control time and replacing several command by one auto- sequence command.

- Auto sequencer mode is performed from the first falling edge of WDCK clock after the falling of the latch pulse.

- Auto sequencer does not carry out tracking gain up, brake, anti-shock and focus gain down.

- MICOM checks ISTAT pin (/BUSY) and sends to $40 command to reset preceding auto sequencer status

	Hexa	AS3	AS2	AS1	AS0	Remark
Cancel	$40	0	0	0	0	Reset
Auto focus	$47	0	1	1	1	–
1 Track jump	$48	1	0	0	0	Forward
	$49	1	0	0	1	Reverse
10 Track jump	$4A	1	0	1	0	Forward
	$4B	1	0	1	1	Reverse
2N track jump	$4C	1	1	0	0	Forward
	$4D	1	1	0	1	Reverse
M track move	$4E	1	1	1	0	Forward
	$4F	1	1	1	1	Reverse

RAM Set ($5X — $7X)

The value of RAM set is somewhat different to the actual count and the initial value is like below

Item	Initial value	Actual Count Value
Blind	$55	Set value +4 — 5 WDCK clock
overflow, Brake		Set value +3 WDCK clock
Kick	$67	Set value +5 WDCK clock
2N, M Track jump	$7E	Set value +3 WDCK clock

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AUTO ADJUSTMENT COMMAND

This command is used for auto control of offset, balance, gain adjustment and reference voltage setting. This command is also in control of on/off and sub type of laser diode and test or set mode.

TRACKING BALANCE ($800 — $81F)

Item	Hexa	Data (5bits)	Initial value	ISTAT (pin31)	TRCNT (pin30)
Tracking balance	$800 — $81F	D4 — D0	$81F	BAL	TRCNT

TRACKING GAIN ($820 — $83F)

Item	Hexa	Data 5bits)	Initial value	ISTAT (pin31)	TRCNT (pin30)
Tracking gain	$820 — $83F	D4 — D0	$820	GAIN	TGL

TRACKING BALANCE & GAIN WINDOW LEVEL SETTING

Item	Hexa	D3	D2	D1	D0	Initial value
window level setting	$84X	gain	balance	0	0	$840

NOTE: The tracking balance and gain window level is set by D2,D3 data and the value has two kinds of window levels set

TRACKING BALANCE WINDOW LEVEL

D2 Data	0	1
Tracking balance window level	−10 to +15 mV	−20 to +20 mV

TRACKING GAIN WINDOW LEVEL

D3 Data	0	1
Tracking gain window level	250 to 400 mV	150 to 300 mV

FOCUS LOOP OFFSET ADJUSTMENT START COMMAND ($841, $842)

This command is used for adjusting focus error bias and removing focus servo offset.
It is executed during laser diode off.

Hexa command	meaning
$841	Focus error bias adjustment start command
$842	Focus servo offset cancel adjustment start command

APC CIRCUIT OPERATION AND INTERRUPTION ON/OFF SETTING CONDITION ($85X)

This command is used for setting of laser diode on/off, sub type (P_sub or N_sub) of laser diode and interruption countermeasure circuit on/off.

Item	Hexa	D3	D2	D1	D0	Initial value
APC & Interruption on/off condition	$85X	LD on/off 0: On 1: Off	Sub-type 0: N_sub 1: P_sub	Interruption ON/OFF and time setting		$858

Time setting for Interruption countermeasure circuit on/off

D1	D0	Meaning
0	0	Countermeasure circuit on for all mirror signal
0	1	Countermeasure circuit on up to 20KHz mirror signal
1	0	Countermeasure circuit off
1	1	Countermeasure circuit on up to 10KHz mirror signal

FOCUS SERVO OFFSET RESET COMMAND AND SET MODE COMMAND (86X)

This command is used for set and release before focus servo loop offset adjustment and mode change.

Item	Hexa	D3	D2	D1	D0
Set mode & Focus servo offset reset command	$86X	0: offset release 1: offset reset	option(Pin41 output) 0: Defect 1: SSTOP	1	1

NOTES:
1. The set mode command is sent by MICOM right after tracking gain is tuned.
2. The ISTAT pin is outputted the internal status of $00 ~ $7X command.

DIRECT COMMAND (DIRC) AND FOCUS BIAS RESET COMMAND ($87X)

This command is used for direct 1 track jump on/off setting and focus bias adjustment set and release

Item	Hexa	D3	D2	D1	D0
DIRC & focus bias reset	$87X	0: DIRC On 1:DIRC Off	0: reset 1: reset release	X	X

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THE EXAMPLE OF ADJUSTMENT FREE ALGORITHM

FOCUS ERROR BIAS & SERVO OFFSET CANCEL ADJUSTMENT
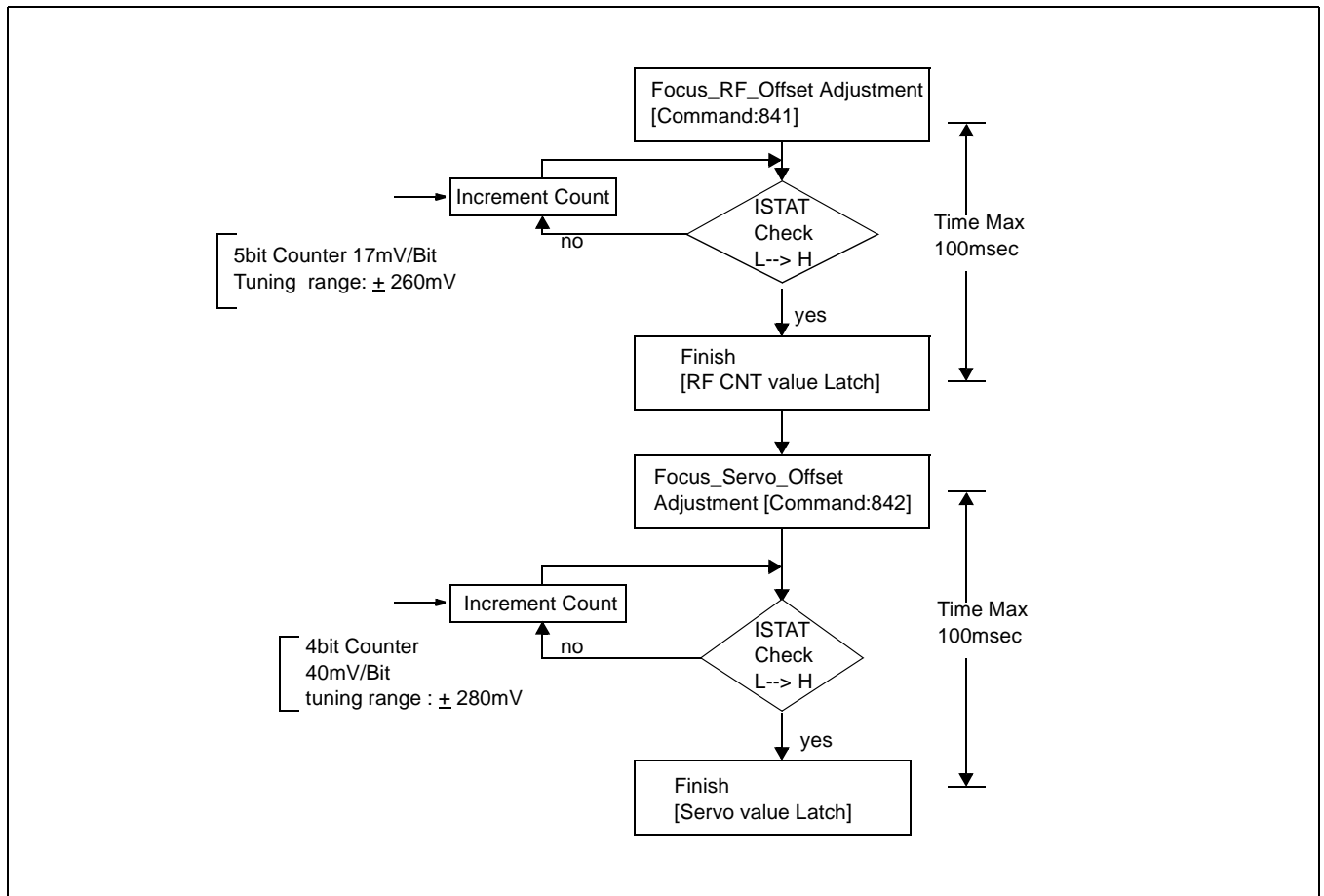

Figure 19. Focus Error Bias & Servo Offset Cancel Adjustment Flow Chart
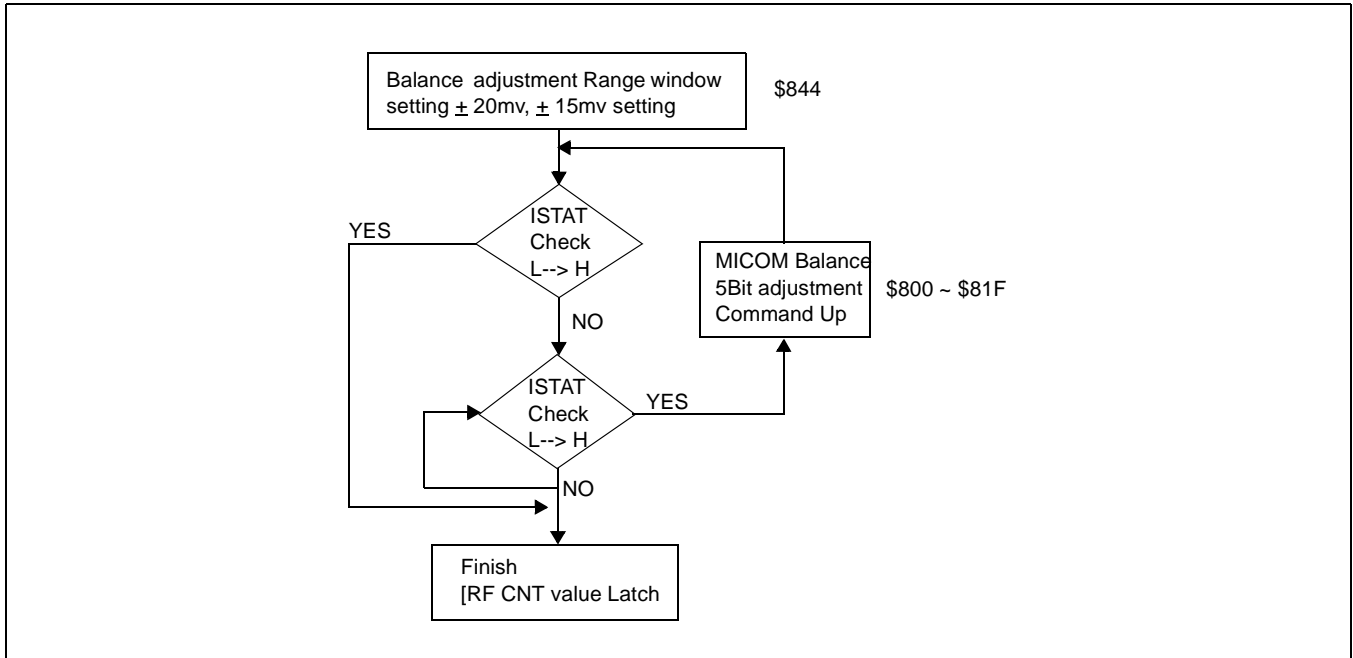
TRACKING BALANCE ADJUSTMENT

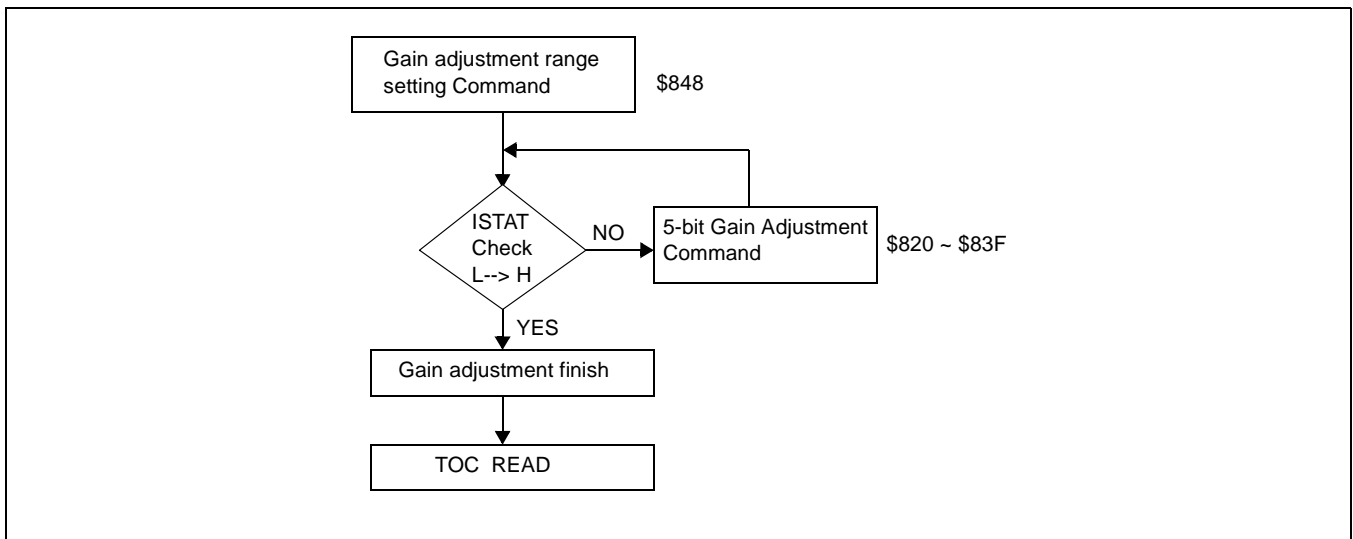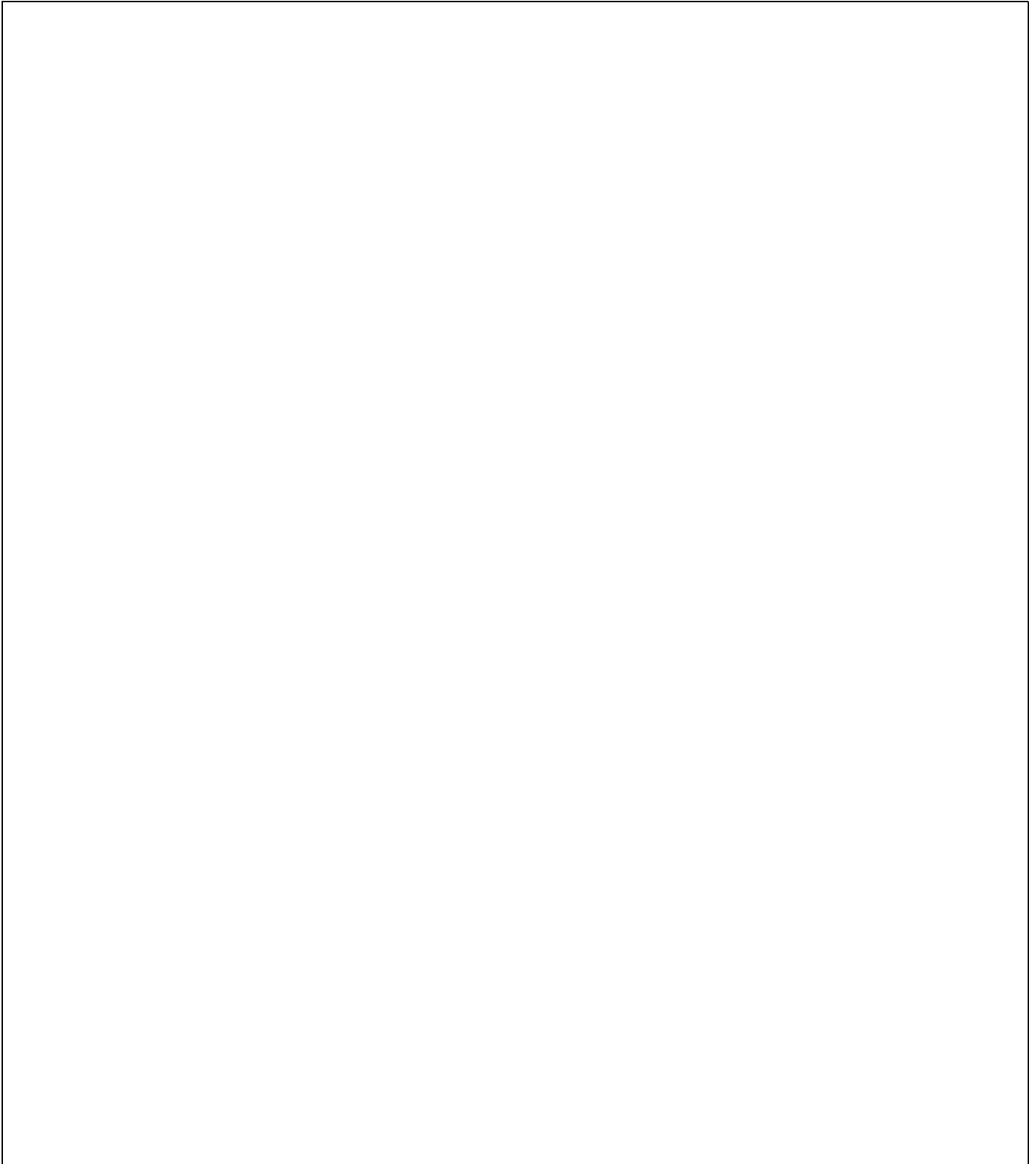**Figure 20. Tracking Balance Adjustment Flow Chart**

TRACKING GAIN ADJUSTMENT

Figure 21. Tracking Gain Adjustment Flow Chart

APPLICATION CIRCUIT

PACKATE DIMESTION

14.00 ± 0.20

12.00 ± 0.10

14.00 ± 0.20

12.00 ± 0.10

80-TQFP-1212

#80

#1

0.50

0.20 +0.07 / -0.03

(1.25)

0-7°

0.127 +0.073 / -0.037

0.08 MAX

0.45 - 0.75

0.05MIN

1.00 ± 0.05

1.20 MAX

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