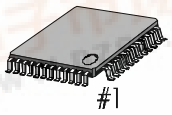
INTRODUCTION

48-LQFP-0707



As a pre-signal & servo signal processor for the DISC-MAN, S1L9226X is a low voltage, low consumption current IC that can read CD-RW, and CD-R discs and can be applied to various products, such as the CDP/VCD/CD-MP3 for the DISC-MAN. It is a hard-wired free-adjustment servo, which automatically controlled the control point of the pre-signal portion.

FEATURES

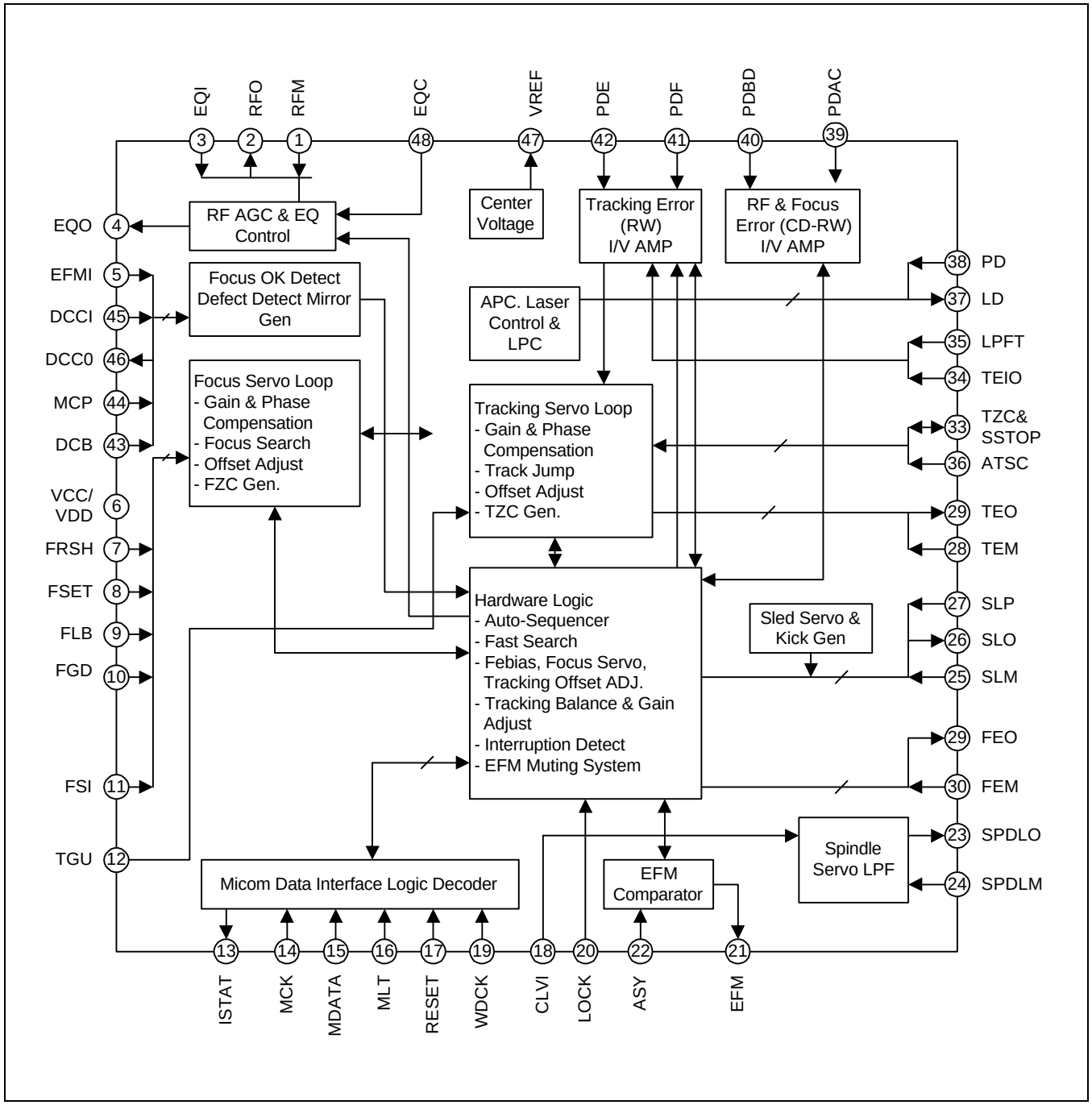
- RF amplifier (CD, CD-R, CD-RW applicable)
- Gain setting & monitoring for the CD-R, CD-RW DISC
- RFAMP offset adjustment
- Focus error amp & Febias adjustment
- Tracking error amp & balance, gain adjustment
- FOK, defect, mirror detect
- Center voltage amplifier
- APC (Automatic Power Control)
- RF AGC & EQ control (AGC Level Control Compatible)
- Enhanced EFM slice (Double Asymmetry Method)
- Focus servo loop & offset adjustment
- Tracking servo loop & offset adjustment
- Sled servo loop
- Spindle servo loop
- Auto-sequence
- Fast search mode (1 - 36000 track jump)
- Interruption countermeasure
- Focus & Tracking servo muting controlled by EFM duty check
- RF peaking prevention system by EFM duty check
- Focus, tracking, spindle loop pole move option
- Operating voltage 2.7V — 3.3V
- Power saving mode

<Notice> LPC Control used by side beam signal, it related to pick-up assurance.
When used pick-up, the specification is present extra.

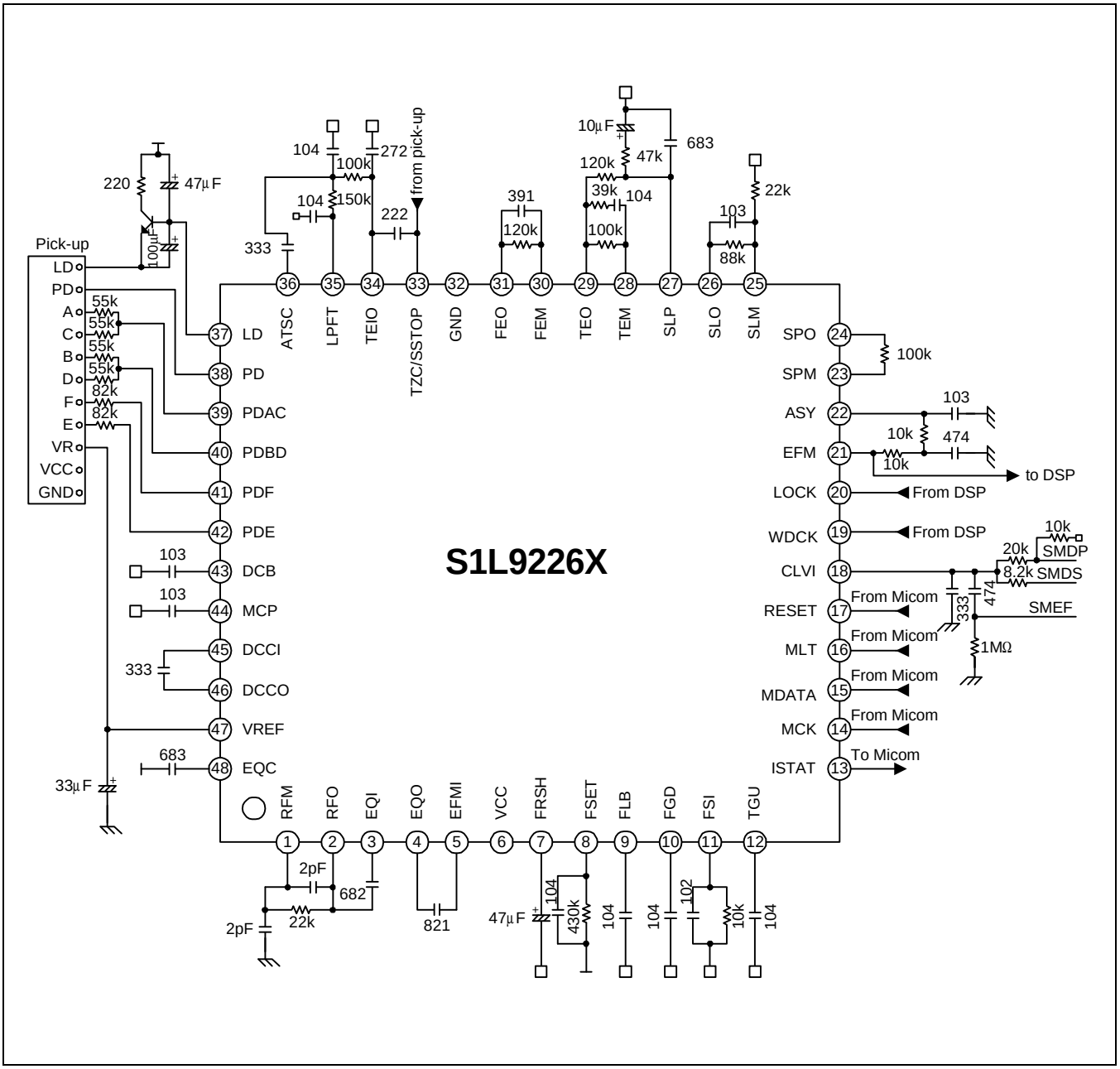
ORDERING INFORMATION

Device	Package	Supply Voltage	Operating Temperature
S1L9226X01—Q0R0	48-LQFP-0707	2.7V — 3.3V	-20°C — +75°C

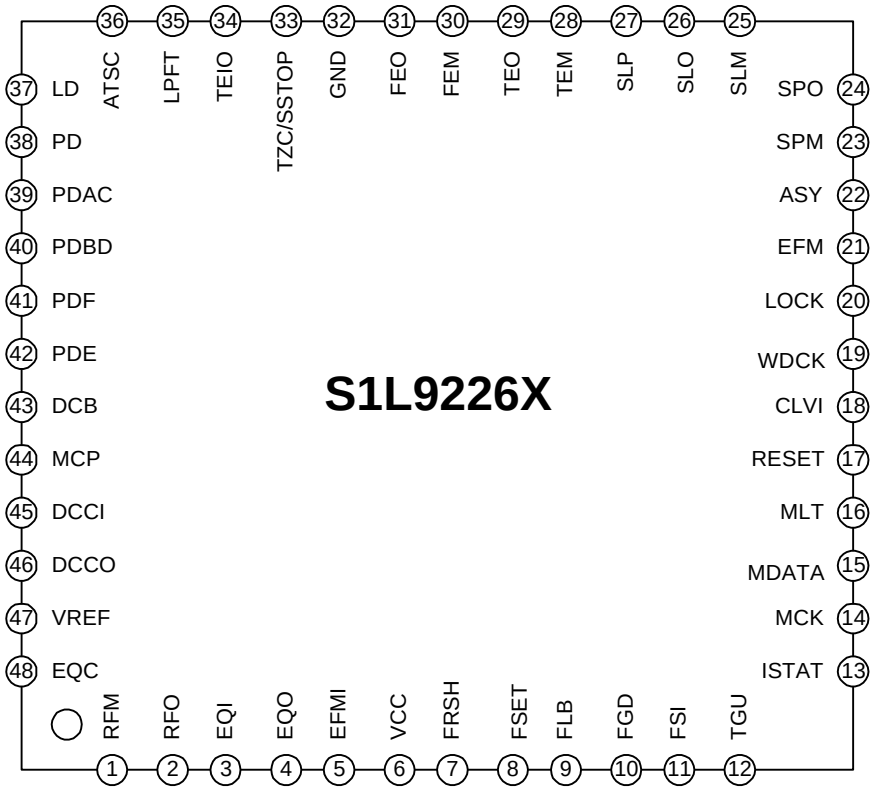
BLOCK DIAGRAM



APPLICATION DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Table 1. Pin Description

Pin No.	Symbol	I/O	Description
1	RFM	I	RF summing amp. inverting input
2	RFO	O	RF summing amp. output
3	EQI	I	RFO DC eliminating input(use by MIRROR, FOK ,AGC & EQ terminal)
4	EQO	O	RF equalizer output
5	EFMI	I	EFM slice input. (input impedance 47K)
6	VCC	P	Main power supply
7	FRSH	I	Capcitor connection to focus search
8	FSET	I	Filter bias for focus,tracking,spindle
9	FLB	I	Capacitor connection to make focus loop rising band
10	FGD	I	Terminal to change the hign frequency gain of focus loop
11	FSI	I	Focus servo input
12	TGU	I	Connect the component to change the high frequency of tracking Loop
13	ISTAT	O	Internal status output
14	MCK	I	Micom clock
15	MDATA	I	Data input
16	MLT	I	Data latch input
17	RESET	I	Reset input
18	CLVI	I	Input the spindle control output from DSP
19	WDCK	I	88.2KHz input terminal from DSP
20	LOCK	I	Sled run away inhibit pin (L: sled off & tracking gain up)
21	EFM	O	EFM output for RFO slice(to DSP)
22	ASY	I	Auto asymmetry control input
23	SPM	I	Spindle amp. inverting input
24	SPO	O	Spindle amp. output
25	SLM	I	Sled servo inverting input
26	SLO	O	Sled servo output
27	SLP	I	Sled servo noninverting input
28	TEM	I	Tracking servo amp.inverting input
29	TEO	O	Tracking servo amp. output
30	FEM	I	Focus servo amp. inverting input
31	FEO	O	Focus servo amp. output pin

Table 1. Pin Description (Continued)

Pin No.	Symbol	I/O	Description
32	GND	P	Main ground
33	TZC/ SSTOP	I	Tracking zero crossing input & Check the position of pick-up wherther inside or not
34	TEIO	B	Tracking error output & Tracking servo input
35	LPFT	I	Tracking error integration input (to automatic control)
36	ATSC	I	Anti-shock input
37	LD	O	APC amp. output
38	PD	I	APC amp. input
39	PDAC	I	Photo diode A & C RF I/V amp. inverting input
40	PDBD	I	Photo diode B & D RF I/V amp. inverting input
41	PDF	I	Photo diode F & tracking(F) I/V amp. inverting input
42	PDE	I	Photo diode E & tracking(E) I/V amp. inverting input
43	DCB	I	Capacitor connection to limit the defect detection
44	MCP	I	Capacitor connection to mirror hold
45	DCCI	O	Output pin to connect the component for defect detect
46	DCCO	I	Input pin to connect the component for defect detect
47	VREF	O	(VCC+GND)/2 Voltage reference output
48	EQC	I	AGC_equalize level control terminal & capacitor terminal to input in to VCA

MAXIMUM ABSOLUTE RATINGS

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	2.7 — 3.3	V
Absolute Ratings	V_I	4.5	V
Operating temperature	T_{OPR}	-20 — 75	°C
Storage temperature	T_{STG}	-40 — 125	°C

ELECTRICAL CHARACTERISTICS

Table 2. Electrical Characteristics

No.	Characteristics	Symbols	Test Block	Spec			Unit
				Min.	Typ.	Max.	
1	Supply current 2.7V	ICCTY		5	10	20	mA
2	RF AMP offset voltage	Vrfo	RF AMP	-100	0	100	mV
3	RF AMP offset voltage 2	Vrfo2		-300	-200	-100	mV
4	RF AMP oscillation voltage	Vrfosc		0	50	100	mV
5	RF AMP voltage gain AC	Grf		15.5	18.5	23.5	dB
6	RF THD characteristic	Rfthd		-	-	5	%
7	RF AMP maximum output voltage	Vrfh		2.35	-	-	V
8	RF AMP minimum output voltage	Vrfl		-	-	0.85	V
9	RF CDRW gain AC1	GRWAC1		1.05	1.30	1.55	-
10	RF CDRW gain AC2	GRWAC2		1.05	1.30	1.55	-
11	RF CDRW gain AC3	GRWAC3		1.05	1.30	1.55	-
12	Focus error offset voltage	VFEO1	Focus Error	-525	-250	0	mV
13	Focus error auto voltage	VFEO2		-50	0	50	mV
14	ISTAT state after FEBIAS control	VISTAT1		2.2	-	-	V
15	Focus positive offset 1	Vfep1		0	40	80	mV
16	Focus positive offset 2	Vfep2		10	60	100	mV
17	Focus positive offset 3	Vfep3		50	120	180	mV
18	Focus negative offset 1	Vfen1		-80	-40	0	mV
19	Focus negative offset 2	Vfen2		-100	-60	-10	mV
20	Focus negative offset 3	Vfen3		-180	-120	-50	mV
21	Focus Error voltage gain 1	GFEAC		19	23	27	dB
22	Focus Error voltage gain 2	GFEBD		19	23	27	dB
23	Focus Error voltage gain difference	ΔGFE		-3	0	3	dB
24	Focus Error RW down	GFERWD		0.4	0.7	1.0	-
25	Focus Error AC difference	VFEACP		0	50	100	mV
26	FERR maximum output voltage H	VFEPPH		2.3	-	-	V
27	FERR minimum output voltage L	VFEPPL		-	-	0.4	V
28	AGC max gain	GAGC	AGC_EQ	15	19	22	dB
29	AGC EQ gain	GEQ		-3	1	2.5	dB
30	AGC normal gain	GAGC2		3	6	9	dB
31	AGC compress ratio	CAGC		0	2.5	5	dB

Table 2. Electrical Characteristics (Continued)

No.	Characteristics	Symbols	Test Block	Spec			Unit
				Min.	Typ.	Max.	
32	AGC frequency	FAGC	AGC_EQ	-5.0	0	2.5	dB
33	AGC Level control	AGCL		0.95	1.125	1.25	-
34	AGC RF Sel	AGCS		15.5	19.5	23.5	dB
35	TERR gain voltage gain 1	GTEF1	Tracking Error	4.5	7.5	10.5	dB
36	TERR gain voltage gain 2	GTEF2		0.98	2.25	4.5	-
37	TERR gain voltage gain 3	GTEF3		0.98	1.3	1.6	-
38	TERR gain voltage gain 4	GTEF4		0.95	1.15	1.30	-
39	TERR gain voltage gain 5	GTEF5		0.90	1.075	1.15	-
40	TERR gain voltage gain 6	GTEF6		0.98	1.15	1.30	-
41	TERR gain voltage gain 7	GTEF7		0.98	1.35	1.70	-
42	TERR balance gain	GTEE		10.5	13.5	16.5	dB
43	TERR balance mode 1	TBE1		0.95	1.05	1.12	-
44	TERR balance mode 2	TBE2		0.95	1.05	1.12	-
45	TERR balance mode 3	TBE3		0.95	1.05	1.12	-
46	TERR balance mode 4	TBE4		1.0	1.25	1.5	-
47	TERR balance mode 5	TBE5		1.0	1.20	1.4	-
48	TERR balance mode 6	TBE6		1.0	1.3	1.75	-
49	TERR maximum output voltage H	VTPPH		1.9	-	-	V
50	TERR minimum output voltage L	VTPPL		-	-	0.8	V
51	TERR RW F gain 1	GRWTF1		1.05	1.75	2.50	-
52	TERR RW F gain 2	GRWTF2		1.05	1.35	1.80	-
53	TERR RW F gain 3	GRWTF3		1.00	1.30	1.65	-
54	TERR RW E gain 1	GRWTE1		1.05	1.35	1.65	-
55	TERR RW E gain 2	GRWTE2		1.05	1.35	2.00	-
56	TERR RW E gain 3	GRWTE3		1.00	1.30	1.65	-
57	APC PSUB voltage L	APSL	APC	-	-	1.0	V
58	APC PSUB voltage H	APSH	&	1.8	-	-	V
59	APC PSUB LDOFF	APSLOF	Laser	2.4	-	-	V
60	APC current drive H	ACDH	Control	1.35	-	-	V
61	APC current drive L	ACDL		-	-	1.35	V
62	MIRROR minimum operating frequency	FMIRB	MIRROR	-	550	900	HZ
63	MIRROR maximum operating frequency	FMIRP		30	75	-	kHz

Table 2. Electrical Characteristics (Continued)

No.	Characteristics	Symbols	Test Block	Spec			Unit
				Min.	Typ.	Max.	
64	MIRROR AM characteristic	FMIRA	MIRROR	-	400	600	HZ
65	MIRROR minimum input voltage	VMIRL		-	0.1	0.2	V
66	MIRROR gain option 1	MIRRO1		10	-	-	kHz
67	FOK threshold voltage	VFOKT	FOK	-450	-360	-300	mV
68	FOK threshold voltage 2	VFOKT2		-450	-560	-220	mV
69	FOK output voltage H	VFOHH		2.2	-	-	V
70	FOK output voltage L	VFOKL		-	-	0.5	V
71	FOK FEEQ. characteristic	FFOK		40	45	50	kHz
72	Defect bottom voltage	FDFCTB	Defect	-	670	1000	HZ
73	Defect CUTOFF voltage	FDFCTC		2.0	4.7	-	kHz
74	Defect minimum input voltage	VDFCTL		-	0.3	0.5	V
75	Defect maximum input voltage	VDFCTH		1.8	-	-	V
76	Defect option gain	FDFCTG		-	670	1000	Hz
77	Normal EFM duty voltage 1	NDEFMN	EFM Slice	-50	0	50	mV
78	Normal EFM duty symmetry	NDEFMA		45	50	55	%
79	Normal EFM duty voltage 3	NDEFMH		0	50	100	mV
80	Normal EFM duty voltage 4	NDEFML		-100	-50	0	mV
81	Normal EFM minimum input voltage	NDEFMV		-	-	0.12	V
82	Normal EFM duty difference 1	NDEFM1		20	50	80	mV
83	Normal EFM duty difference 2	NDEFM2		20	50	80	mV
84	EFM2 duty voltage 1	EDEFMN1	Enhanced	-50	0	50	mV
85	EFM2 duty symmetry	EDEFMA	EFM Slicer	45	50	55	%
86	Double ASY voltage 1	DEFM1		-375	-250	-125	mV
87	Double ASY voltage 2	DEFM2		125	250	375	mV
88	EFM2 minimum input voltage	EDEFMV		-	-	0.12	V
89	FZC threshold voltage	VFZC	Interface	30	69	105	mV
90	ANTI-shock detection H	VATSCH		20	60	100	mV
91	ANTI-shock detection L	VATSCL		-100	-60	-20	mV
92	TZC threshold voltage	VTZC		-150	0	150	mV
93	SSTOP threshold voltage	VSSTOP		-155	-90	-5	mV
94	Tracking gain win T1	VTGWT1		190	250	310	mV
95	Tracking gain win T2	VTGWT2		90	150	210	mV

Table 2. Electrical Characteristics (Continued)

No.	Characteristics	Symbols	Test Block	Spec			Unit
				Min.	Typ.	Max.	
96	Tracking gain win T3	VTGWT3	Interface	240	300	360	mV
97	Tracking gain win T4	VTGWT4		140	200	260	mV
98	Tracking gain win T5	VTGWT5		440	500	560	mV
99	Tracking gain win T6	VTGWT6		340	400	460	mV
100	Tracking BAL win T1	VTBWT1		-50	0	50	mV
101	Tracking BAL win T2	VTBWT2		-50	0	50	mV
102	Reference voltage	VREF	VREF	-100	0	100	mV
103	Reference current H	IREFH		-100	0	100	mV
104	Reference current L	IREFL		-100	0	100	mV
105	F. Servo off offset	VOSF1	Focus Servo	-100	0	100	mV
106	F. Servo DAC on offset	VOSF2		0	250	550	mV
107	F. Servo auto offset	VAOF		-65	0	65	mV
108	F. Servo auto ISTAT	VISTAT2		2.2	-	-	V
109	FERR FEBIAS status	VFEBIAS		-50	0	50	mV
110	F. Servo loop gain	GF		17	21.5	24	dB
111	F. Servo output voltage H	VFOH		2.2	-	-	V
112	F. Servo output voltage L	VFOL		-	-	0.5	V
113	F. Servo oscillation voltage	VFOSC		0	100	200	mV
114	F. Servo feed through	GFF		-	-	-35	dB
115	F. Servo search voltage H	VFSH		0.30	0.50	0.70	V
116	F. Servo search voltage L	VFSL		-0.70	-0.50	-0.30	V
117	Focus full gain	GFSFG		40.0	44.5	49.0	dB
118	F. Servo AC gain 1	GFA1		17.0	21.0	25.0	dB
119	F. Servo AC phase 1	PFA1		30	60	90	deg
120	F. Servo AC gain 2	GFA2		14.0	17.5	21.0	dB
121	F. Servo AC phase 2	PFA2		30	60	90	deg
122	F. Servo muting	GMUTT		-	-	-15	dB
123	F.Servo AC gain difference	GFAD		1.5	5	8	dB
124	F. Servo AC characteristic 1	GFAC1		1.75	2.25	2.80	
125	F. Servo AC characteristic 2	GFAC2		1.05	1.55	2.05	-
126	F. Servo AC characteristic 3	GFAC3		1.05	1.55	2.05	-

Table 2. Electrical Characteristics (Continued)

No.	Characteristics	Symbols	Test Block	Spec			Unit
				Min.	Typ.	Max.	
127	T. Servo DC gain	GTO	Tracking	13.0	15.5	18.0	dB
128	T. Servo off offset	VOST1	Servo	-100	0	100	mV
129	T. Servo DAC offset	VTDAC		150	320	700	mV
130	T. Servo auto offset	VTAOF		-55	0	70	mV
131	T.Servo STAT status	VTSTAT		2.2	-	-	V
132	T. Servo oscillation	VTOSC		0	100	185	mV
133	T. Servo ATSC gain	GATSC		17.5	20.5	23.5	dB
134	T. Servo lock gain	GLOCK		17.5	20.5	23.5	dB
135	T. Servo gain up	GTUP		17.5	20.5	23.5	dB
136	T. Servo output voltage H	VTSH		2.2	-	-	V
137	T. Servo output voltage L	VTSL		-	-	0.5	V
138	T. Servo jump H	VTJH		0.30	0.5	0.70	V
139	T. Servo jump L	VTJL		-0.70	-0.5	-0.30	V
140	T. Servo DIRC H	VDIRCH		0.30	0.5	0.70	V
141	T. Servo DIRC L	VDIRCL		-0.70	-0.5	-0.30	V
142	T. Servo output voltage L	GTFF		-	-	-39	dB
143	T. Servo AC gain 1	GTA1		10.5	14.5	17.5	dB
144	T. Servo AC phase 1	PTA1		-180	-135	-90	deg
145	T. Servo AC gain 1	GTA2		18.1	23.1	26.1	dB
146	T. Servo AC phase 1	PTA2		-180	-135	-90	deg
147	T. Servo full gain	GTFG		32	36	40	dB
148	T. Servo AC characteristic1	GTAC1		1.50	2.00	2.50	-
149	T. Servo AC characteristic2	GTAC2		0.40	0.80	1.30	-
150	T. Servo loop mutt AC	TSMTAC		0	50	100	mV
151	SL. Servo DC gain	GSL	Sled Servo	11.0	14.0	17.0	dB
152	SL. Servo feed through	GSLF		-	-	-34	dB
153	Sled forward kick	VSKH		0.40	0.60	0.80	V
154	Sled reverse kick	VSKL		-0.80	-0.60	-0.40	V
155	Sled output voltage H	VSLH		2.2	-	-	V
156	Sled output voltage L	VSLL		-	-	0.5	V
157	Sled lock off	VSLOCK		-100	0	100	mV

Table 2. Electrical Characteristics (Continued)

No.	Characteristics	Symbols	Test Block	Spec			Unit
				Min.	Typ.	Max.	
158	SP. Servo 1X gain	GSP	CLV Servo	13.5	16.5	19.5	dB
159	SP. Servo 2X gain	GSP2		19.0	23.0	27.0	dB
160	SP. Servo output voltage H	VSPH		2.2	-	-	V
161	SP. Servo output voltage L	VSPL		-	-	0.5	V
162	SP. Servo AC gain 1	GSPA1		-3.0	5.0	12.0	dB
163	SP. Servo AC phase 1	PSPA1		-120	-90	-50	deg
164	SP. Servo AC gain 2	GSPA2		3.0	10.0	17.0	dB
165	SP. Servo AC phase 2	PSPA2		-120	-80	-50	deg
166	SP.Servo AC gain 3	GSP3		0.85	3	5.0	-

OPERATION DESCRIPTION

MICOM COMMAND

$0X, $1X

Item	Address				Data				Istat Output
	D7	D6	D5	D4	D3	D2	D1	D0	
Focus control	0	0	0	0	FS4 Focus on	FS3 Gain down	FS2 Search on	FS1 Search up	FZC
Tracking control	0	0	0	1	Anti - shock	Brake - on	TG2 Gain set	TG1 Gain set	ATSC

Tracking Gain Setting According to Anti-Shock

D7	D6	D5	D4	D3		D2		D1		D0		Istat
0	0	0	1	ANTI - shock		Lens. Brake - on		TG2 (D3 = 1)		TG1		ATSC
				0	1	0	1	0	1	0	1	
				ANTI - shock off	ANTI - shock on	Lens brake off	Lens brake on	High - Freq. gain down	High - Freq. gain normal	Gain normal	Gain up	

Item	Hex	AS = 0		AS = 1	
		TG2	TG1	TG2	TG1
Tracking gain control TG1. TG2 = 1 → gain up	$10	0	0	0	0
	$11	0	1	0	1
	$12	1	0	1	0
	$13	1	1	1	1
	$14	0	0	0	0
	$15	0	1	0	1
	$16	1	0	1	0
	$17	1	1	1	1
$13, $17, $1B, $1F (AS0) $13, $17, $18, $1C (AS1) MIRROR muting turns off when the tracking gain goes up	$18	0	0	1	1
	$19	0	1	1	0
	$1A	1	0	0	1
	$1B	1	1	0	0
	$1C	0	0	1	1
	$1D	0	1	1	0
	$1E	1	0	0	1
	$1F	1	1	0	0

$2X

D7	D6	D5	D4	D3	D2		D1		D0	
0	0	1	0	Tracking Servo Mode			Sled Servo Mode			
Operation of mode (TM1-TM7)				MODE	TM7		TM5	TM4	TM3	TM2	TM1
TM1				$20	1	0	1	0	1	1	0
0	Track. servo off			$21	1	0	1	0	1	0	0
1	Track. servo on			$22	1	0	0	0	1	1	0
TM2				$23	1	1	1	0	1	1	0
0	Sled. servo on			$24	1	0	1	0	1	1	1
1	Sled. servo off			$25	1	0	1	0	1	0	1
TM4	TM3	Track. kick		$26	1	0	0	0	1	1	1
0	0	Fwd. jump		$27	1	1	1	0	1	1	1
0	1	Jump off		$28	1	0	1	0	0	1	0
1	1	Rev. jump		$29	1	0	1	0	0	0	0
TM6	TM5	Sled kick		$2A	1	0	0	0	0	1	0
0	0	Fwd kick		$2B	1	1	1	0	0	1	0
0	1	Kick off		$2C	1	0	1	1	1	1	0
1	1	Rev kick		$2D	1	0	1	1	1	0	0
TM7 (jump)				$2E	1	0	0	1	1	1	0
1	Lens brake on			$2F	1	0	0	1	1	1	0

DIRC (DIRECT 1 Track Jump) Tracking Condition

Item	Hex	DIRC = 1	DIRC = 0	DIRC = 1
		TM 654321	654321	654321
Tracking Mode	$20	000000	001000	000011
	$21	000010	001010	000011
	$22	010000	011000	100001
	$23	100000	101000	100001
	$24	000001	000100	000011
	$25	000011	000110	000011
	$26	010001	010100	100001
	$27	100001	100100	100001
	$28	000100	001000	000011
	$29	000110	001010	000011
	$2A	010100	011000	100001
	$2B	100100	101000	100001
	$2C	001000	000100	000011
	$2D	001010	000100	000011
	$2E	011000	000100	100001
	$2F	101000	100100	100001

Register $3X

Address	Focus & Sled	Focus search		SLED KICK		T.servo cpeak mutting	Tracking jump			
D15-D12		D11	D10	D9	D8	D7	D6		D5	D4
0011	Level value	PS4 search+2	PS3 serach+1	PS2 Kick+2	PS2 Kick+1	Mutting when above EFM11T	PS5 Jump +1		PS6 Jump 1/2	PS7 Jump 1/4
	1X	0	0	0	0	0: OFF 1: ON	0	0	0	0X (0u)
							0	0	1	0.25X (1.25u)
	2X	0	1	0	1		0	1	0	0.50X (2.50u)
							0	1	1	0.75X (3.75u)
	3X	1	0	1	0		1	0	0	1.00X (5.00u)
							1	0	1	1.25X (6.25u)
	4X	1	1	1	1		1	1	0	1.50X (7.50u)
							1	1	1	1.75X (8.75u)
INITIAL		0	0	0	0	0	1	0	0	

ADDRESS	INTC	FSET (Focus, tracking CVL Pole Freq. setting resistor)			
D15-D12	**D3**	**D2**	**D1**	**D0**	
0011	F.Servo Cpeak Mutt	FSETC	FSET2 24K	FSET1 12K	
	Mutting when above EFM11T	0	X	X	External resistor applied
		1 (104K)	0	0	140K (580K)
			0	1	116K (480K)
			1	0	128K (530K)
			1	1	104K (430K)
INITIAL	0	1	1	1	

Select (First 8 bits of 16 bits)

D15	D14	D13	D12	D11	D10	D9	D8	Istat
0	0	1	1	Focus Servo Search Level Control		Sled Servo Kick Level Control		SSTOP
				PS4	PS3	PS2	PS1	
				Search +2	Search +1	Kick +2	Kick +1	
Data Mode (level)				Search X1	$30XX-$33XX	Kick X1	$30XX, $34XX, $38XX, $3CXX	
				Search X2	$34XX-$37XX	Kick X2	$31XX, $35XX, $39XX, $3DXX	
				Search X3	$38XX-$3BXX	Kick X3	$32XX, $36XX, $3AXX, $3EXX	
				Search X4	$3CXX-$3FXX	Kick X4	$33XX, $37XX, $3BXX, $3FXX	
Data				S.X1, K.X1	S.X2, K.X2	S.X3, K.X3	S.X4, K.X4	
				$30XX	$35XX	$3AXX	$3FXX	

Auto-Sequence Mode

Address				Data			
0	**1**	**0**	**0**	**D3**	**D2**	**D1**	**D0**
Auto-sequence cancel				0	0	0	0
Auto-focus				0	1	1	1
1-track jump				1	0	0	0: FWD
10-track jump				1	0	1	1: REV
2N-track jump				1	1	0	
M-track jump				1	1	1	
Fast search				0	1	0	

Speed Related Command ($F00, F03)

Address								Data			
D11	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	1	1	0	0	0	0				
1X Speed ($F00, $F04, $08, $F0C)								x	x	0	0
2X Speed ($F03, $F07, $F0B, $F0F)								x	x	1	1

RAM Register Set

Item		Data							
Address		D7	D6	D5	D4	D3	D2	D1	D0
Blind A, E Overflow. C	$50XX	0.18ms	0.09ms	0.04ms	0.02ms				
BRAKE. B		0.36ms	0.18ms	0.09ms	0.04ms				
FAST F		23.2ms	11.6ms	5.80ms	2.90ms				
FAST K						0.72ms	0.36ms	0.18ms	0.09ms
INI.		1	0	0	0	1	0	0	0
Control Register	$51XX	PS3X	PSTZC	ATS	FZCOFF	TRSTS	TZCIC	MCC1	EQR
		SSTOP on/off	TZC on/off	ATSC on/off	FZC on/off	T.Bal & GainReset	TZC. Input	EQC output	AGC IN Level
	0	Off	Off(SSTOP)	T.BAL	Off	Reset	TERR	RFO	2/3 IN
	1	On	On (TZC)	ATSC	On	Set	FERR	EQO	Normal
INI.		1	1	1	1	1	0	1	1
Control Register	$52XX	FJTS	PEAKC	FEB5	FEB4	FEB3	FEB2	FEB1	FEB0
		TEO output when fast search	EFM Peaking	Ref posi-offset(3V) Ref voltage 3V depend on voltage		Febias offset FSIO offset control the option		RFO nega-offset fixed unrelated voltage	
				MSB	10mv/step	LSB	MSB	10mv/step	LSB
	0	T.Jump	off	00	0mV	off	on (-150mV)	00	-250mV
				01	+125mV			01	0mV
	1	T-off (TEO off)	on	10	0mV	on (+150mV)	off	10	-125mV
				11	+250mV			11	0mV
INI.		1	0	0	0	0	1	1	1
Febias offset regard on control	Before control the Febias offset $51xx TZCIC is set as the FERR 1'and monitored TZC output . The ISTAT output set + offset , Febias offset control in sequence. If ISTAT of TZC output set - offset, $52XX is set as the FEB2 0'. After get - offset, Febias offset control in sequence. * Remark : Phase of TZC output is opposite the input.								

Address	HEX	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
KICK D	$6XXX	11.6ms	5.80ms	2.90ms	1.45ms								
FAST R		23.2ms	11.6ms	5.80ms	2.90ms								
PWM DUTY PD						8	4	2	1				
PWM WIDTH PW										11.0ms	5.43ms	2.71ms	1.35ms
	INI.	0	1	1	1	1	0	1	0	0	0	1	0
2N TRA. N M TRA. M	$7XXX	4096	2048	1024	512	256	128	64	32	16	8	4	2
Fast searchT	$7XXX	16384	8192	4096	2048	1024	512	256	128	64	32	16	8
	INI.	0	0	0	0	0	0	1	1	1	1	1	1
Brake point P	$CXXX	16384	8192	4096	2048	1024	512	256	128	64	32	16	8
	INI.	0	0	0	0	0	0	1	1	1	0	0	0
CLV on/off register		CLV on, EFM on $99X1~$99XF				X	X	X	X	X	X	X	1
		CLV off, EFM off $99X0				X	X	X	X	0	0	0	0
	INI	1	0	0	1	X	X	X	X	0	0	0	0
Notice.		The actual value may be slightly different from the set value. A set value + 4 - 5 WDCK B, D, E set value + 3 WDCK C set value + 5 WDCK N, M, T, P set value + 3 TRCNT Caution - Among the 16 settings of PWM WIDTH 'PW' only one from D3, D2, D1, and D0 can be selected. (not 4bit combination) - More than 512 tracks are not recommended when 2N track and M track are used. (algorithm possesses problem generation) - Because PWM DUTY 'PD' can have 1 - 2 errors, should be set to "set value + 2"											

AUTOMATIC CONTROL COMMAND

Tracking Balance and Gain Control

Address	Address				Data			
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Tracking BAL. $800X - $801X	0	0	0	B4	B3	B2	B1	B0
Initial V.				0	1	1	1	1
Tracking Gain. $810X - $811X	0	0	0	G4	G3	G2	G1	G0
Initial V.				1	0	0	0	0

Tracking Balance and Gain Control Window & APC ON/OFF

ADDRESS	DATA								
	D7		**D6**	**D5**	**D4**		**D3**		
	STGW		STBW	F.S.O.C	F.E.O.C		LDON		
$84X	Tracking gain control windows		Tracking balance control windows	F.Servo offset control	FB.BIAS offset control	$85	LD ON/OFF		
	TGL	TGH	ISTAT						
	250mV	200mV	-20mV-20mV	OFF	OFF		OFF		
	150mV	300mV	-30mV-30mV	ON	ON		ON		
INITIAL	0		0	0	0		0		

Additional Register Set

	D3	D2	D1	D0		D3	D2	D1	D0
	RSTS	**EQOC**	**DFCT1**	**DFCT2**		**DIRC**	**RSTF**	**AGCL**	**EQB**
$86X	Focus servo offset DAC reset	EQ0 offset Vref(1) VCC follow(0)	Defect input gain	Input offset addition	&87X	Direct 1 track JUMP	Focus error DAC RESET	EQ0 output level UP	EQ respose GM
0	Reset	Normal	1.5X	VR+0.25V	0	ON	Reset	UP	12u
1	Set	Buffer	1X	VR+0.35V	1	OFF	Set	Normal	18u
INITIAL	1	1	1	1	INITIAL	1	1	1	1

$8EXX Focus & Tracking Servo Filter Control Command

Address	**Data**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
$8EXX	CLV Freq. movement 0: low frequency 1: high frequency		T. Servo Phase shift 0: low frequency 1: high frequency			Fcous freq. movement 0: low frequency 1: high frequency		
0	On	On	On	On	On	On	On	On
1	Off	Off	Off	Off	Off	Off	Off	Off
Initial V.	1	0	1	1	0	1	1	0

$8FXX Tracking Servo Offset Control Command

Address	Data							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
$8F00 — $8F1F	X	X	X	Tracking servo offset control command 8F(000XXXXX) $8F1F → $8F00 (-160mV → +160mV) Control window is used with the balance window and monitors the ISTAT output Because tracking offset of approximately +30mV - +50mV is ideal in the system, consider the control setting by raising to ($8F1F → $8F00) 3 - 5 steps after controlling the offset to 0mV. <Notice> Consider the measure setting by $8010 command of tracking switch and $811F command of tracking gain switch after $24 command.				
Initial V.	0	0	0	1	0	0	0	0

Photo-Diode I/V AMP Gain Setting for CD-R and CD-RW

Address	DATA									
	D7	**D6**	**D5**	**D4**	**RF & FERR GAIN**		**RFO ONLY GAIN**		**RFO TOTAL**	
	Focus gain down	RWC3 1.5X	RW2C 2.0X	RWC1 1.25X	I/V AMP Equivalence resistance	Input resistance 55K Gain	Summing Resistance	RFO Feed resistance ratio 22K	RFO LOOP TOTAL	
\$82XX	RFO Focus error			RFO only	1 stage gain		2 stage gain		RFO total	Compare to F
07(0F)	Focus gain down bit	1	1	1	58.5K	1.06	10K	22K/10K=2.2	9.33	1.00
06(0E)		1	1	0	91.5K	1.66	10K	22K/10K=2.2	14.61	1.56
05(0D)		1	0	1	121.75K	2.21	10K	22K/10K=2.2	19.45	2.08
04(0C)		1	0	0	154.75K	2.81	10K	22K/10K=2.2	24.73	2.65
03(0B)		0	1	1	154.75K	2.81	10K	22K/10K=2.2	24.73	2.65
02(0A)		0	1	0	187.75K	3.41	10K	22K/10K=2.2	30.00	3.21
01(09)		0	0	1	218.00K	3.96	10K	22K/10K=2.2	34.84	3.73
00(08)		0	0	0	251.00K	4.56	10K	22K/10K=2.2	40.33	4.32
0	down	up	up	up	Set the 8 when CD-RW mode					
1	normal	normal	normal	normal						
INITIAL	1	1	1	1						

Tracking Error CD-RW Mode Gain

Address	DATA									
	D3	D2	D1	D0	Tracking Error				Terr total	
	SPEAK	RWC8 1.5X	RWC7 2.0X	RWC6 1.5X	I/V AMP equivalence resistance	Input Resistance 82K gain	Resistance Difference	Tracking feed resistance ratio 22K	TERR LOOP TOTAL	
$82XX		Tracking error gain		TE difference	1 stage gain		2 stage gain		Terr total	compare to 7
07(0F)	EFM Duty Check Freq.	1	1	1	391K	1.06	30K	96K/30K=32	3.392	1.00
06(0E)		1	1	0	583K	1.66	30K	96K/30K=32	5.312	1.56
05(0D)		1	0	1	786K	2.21	30K	96K/30K=32	7.07	2.08
04(0C)		1	0	0	979K	2.81	30K	96K/30K=32	8.992	2.65
03(0B)		0	1	1	979K	2.81	30K	96K/30K=32	8.992	2.65
02(0A)		0	1	0	1171K	3.41	30K	96K/30K=32	10.91	3.21
01(09)		0	0	1	1374K	3.96	30K	96K/30K=32	12.67	3.73
00(08)		0	0	0	1567K	4.56	30K	96K/30K=32	14.592	4.32
0	88K	up	up	up	Set the 0 (4.01X) when CD-RW mode setting (because need long lead in time to check 8 setp)					
1	44K	Normal	Normal	Normal						
INITIAL	0	1	1	1						

ISTAT output Monitor Select Mode & RFO Offset Control.

Address	DATA							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	MGA1	**MGA2**	**RFOC**	**TOCD**	**EMODEC**	**CSTAT**	**RFBC**	**GSEL**
$83XX	Mirror input gain	Mirror bias addition	T.Gain win input select	Tracking offset comtrol on/off	EFM slice mode	ISTAT output option	RFO offset FOK select	T.Gain windows sel
0	2X	off	focus error	off	Double ASY	CSTAT	FOK	200/300mV
1	1.5X	on	T.Gain	on	Vref	CSTATB	RFO offset	400/500mV
INITIAL	1	0	1	1	1	1	0	0

Command.	Solution
CD-RW Detect Method focus error CD-RW distinction	The monitor output in the table above is set as the focus error output and the focus error output level comparison $81XX is sent to ISTAT1 and ISTAT2 to allow the micom to monitor the focus error output. After $81XX is sent, it possible to monitor because the tracking gain window comparator are used commonly. With search command ($47), if the intensity of radiation set its target, focus search level is 1Vp-p, and peak value is 0.5V. As the table below, windows level transmit $84CX $513X command, ISTAT1 monitored at 500mV

GSEL	ISTAT output mode	TGL	GSEL(TGH)		
			0	1	
	$844X	250mV	200mV	400mV	Use the 6 types tracking gain window to distinguish the CD and CD-RW disc.
	$84CX	150mV	300mV	500mV	

ISTAT	CSTAT	5X	6X	7X	1X	ISTAT output
	1	Cpeak	FZCB	TZCB	ATSC	Change the ISTAT output by CSTAT
	0	FSDFCT	MIRROR	DFCINT	FOK, LOCK or output	Change the ISTAT output by CSTAT
	INITIAL.	1	1	1	1	Change the ISTAT output by CSTAT
	0X	FOK				
	2X	TRCNT				
	3X	SSTOP				
	4X	Auto SEQ BUSY signal				
	$841	Focus Error Offset window				
	$842	Focus Servo Offset window				
	$CXXXX	Tracking gain window (TGL)				
	$80XX	Tracking Balance window				
	$81XX	Tracking Gain window (TGH)				
	$8FXX	Tracking Servo offset window				

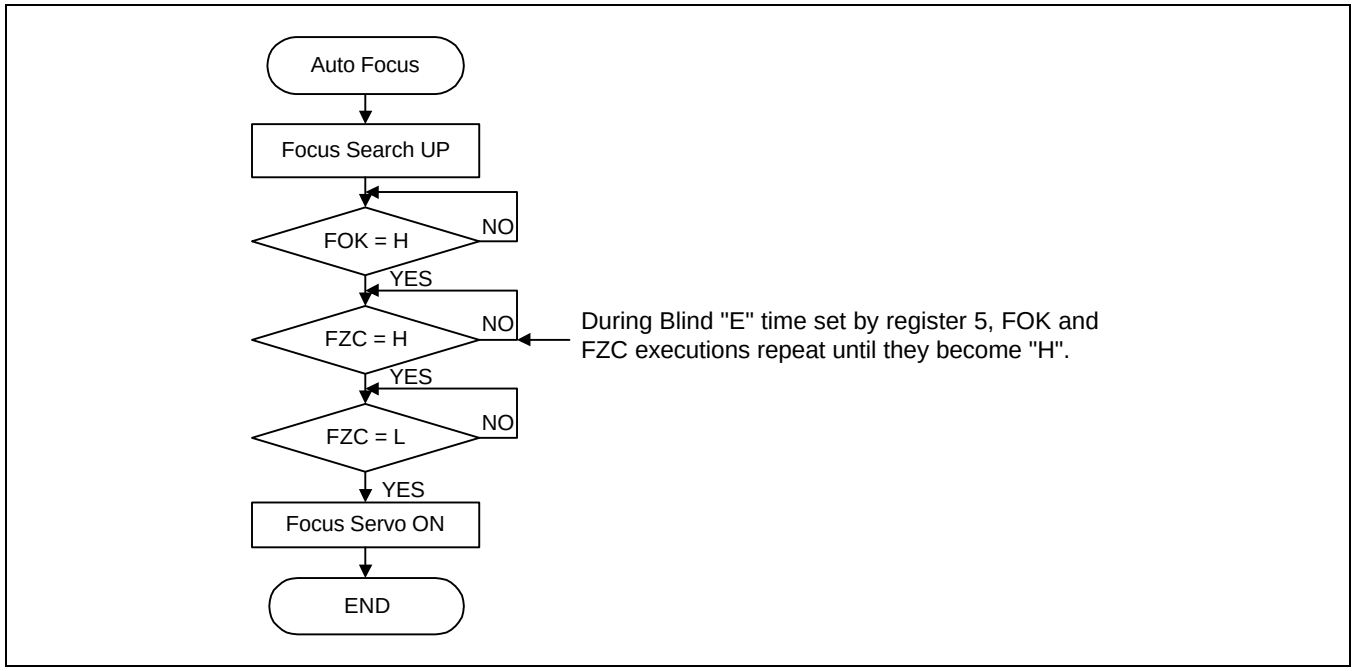
$99XX	$9900 CLV OFF	$9901 - $991F CLV ON	CLV Command decording

AUTO-SEQUENCE

This function executes the chain of commands that execute auto-focus, track jump, and move. MLT latches the data at time L, and ISTAT is L during auto-sequence. It output H upon.

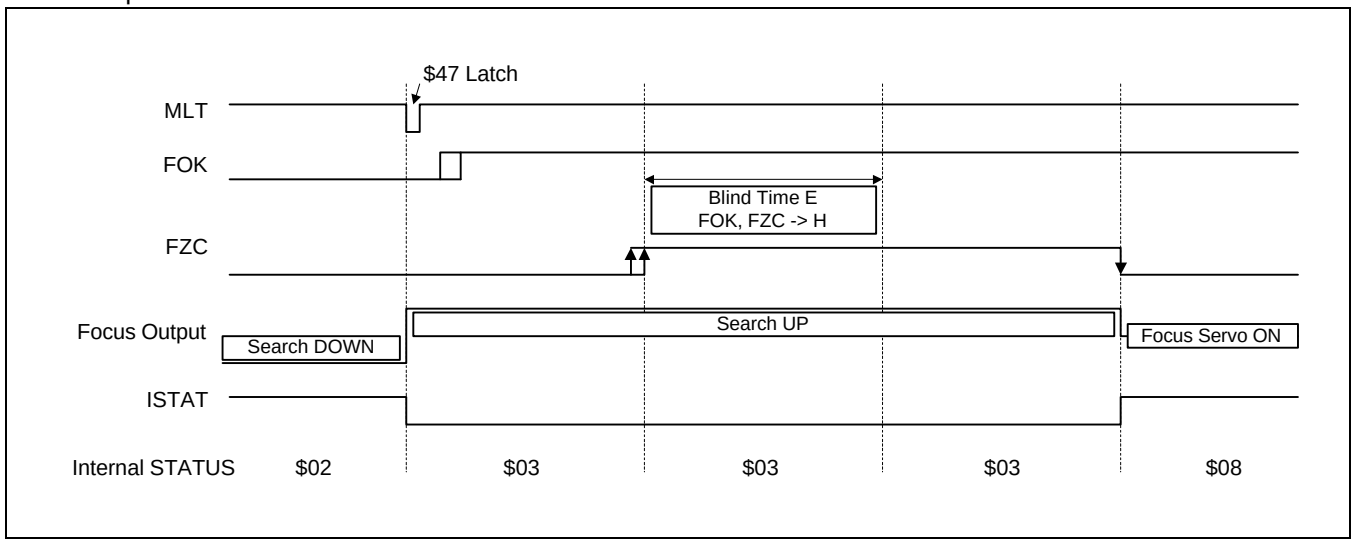
AUTO FOCUS

Flow-Chart



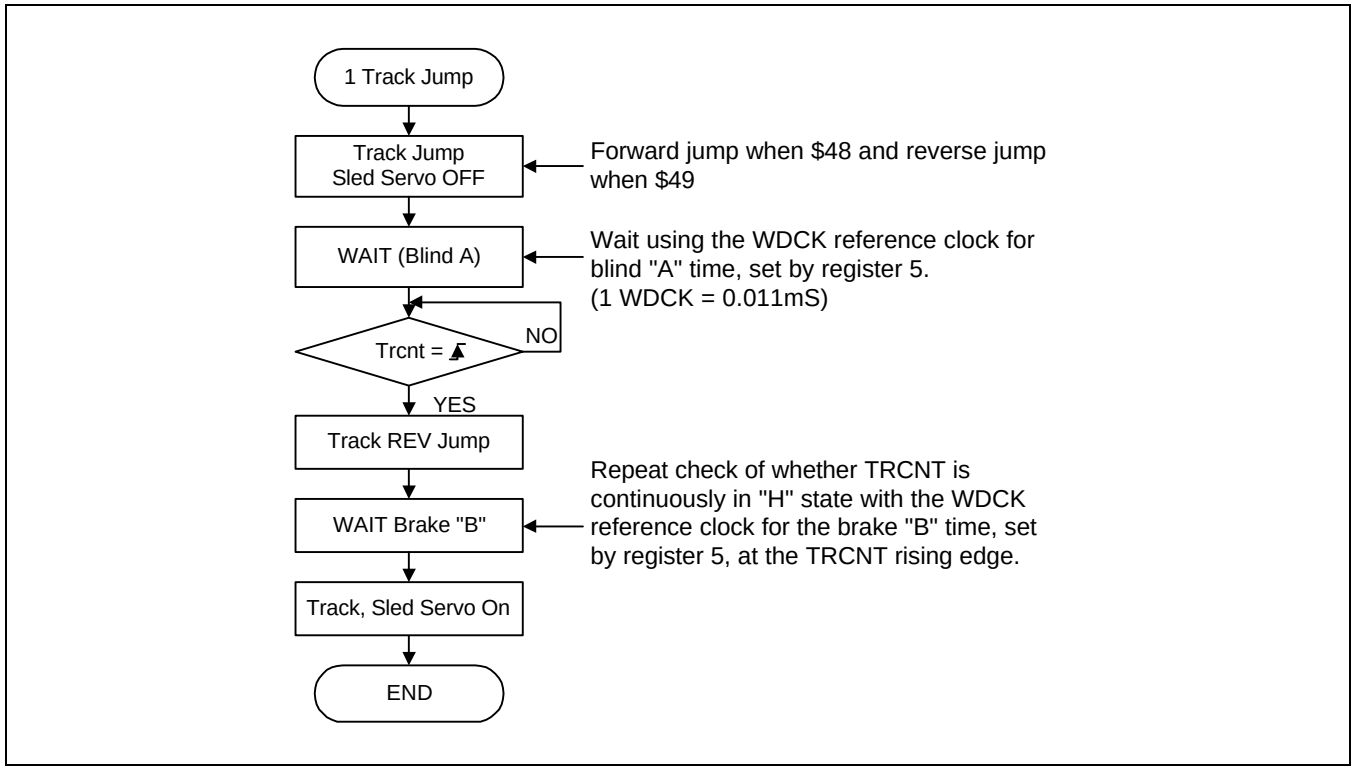
Timing Chart

Auto-focus receives the auto-focus command from the MICOM in the focus search down state and focus search up. The SSP becomes focus servo on when FZC changes to L after the internal FOK RZC satisfy 'H', all the time set blind 'E' (Register $5X). All the internal auto focus executes ended. And this status is sent to micom through the ISTAT output.

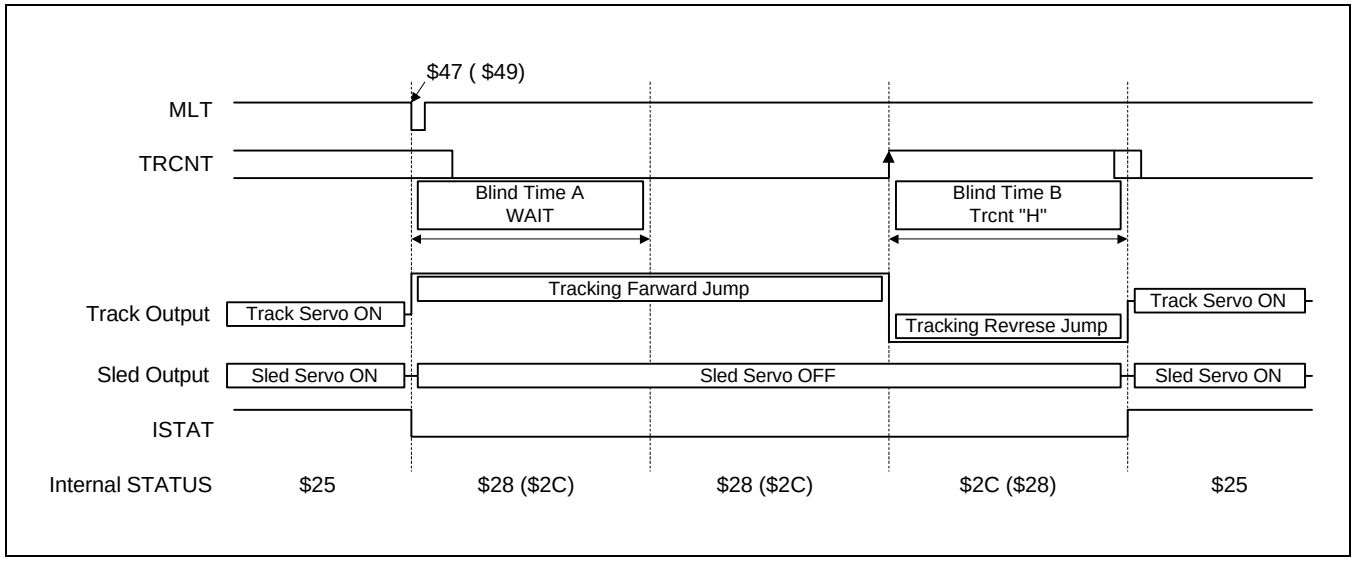


1 TRACK JUMP {$48(FWD), $49(REV)}

Flow-Chart



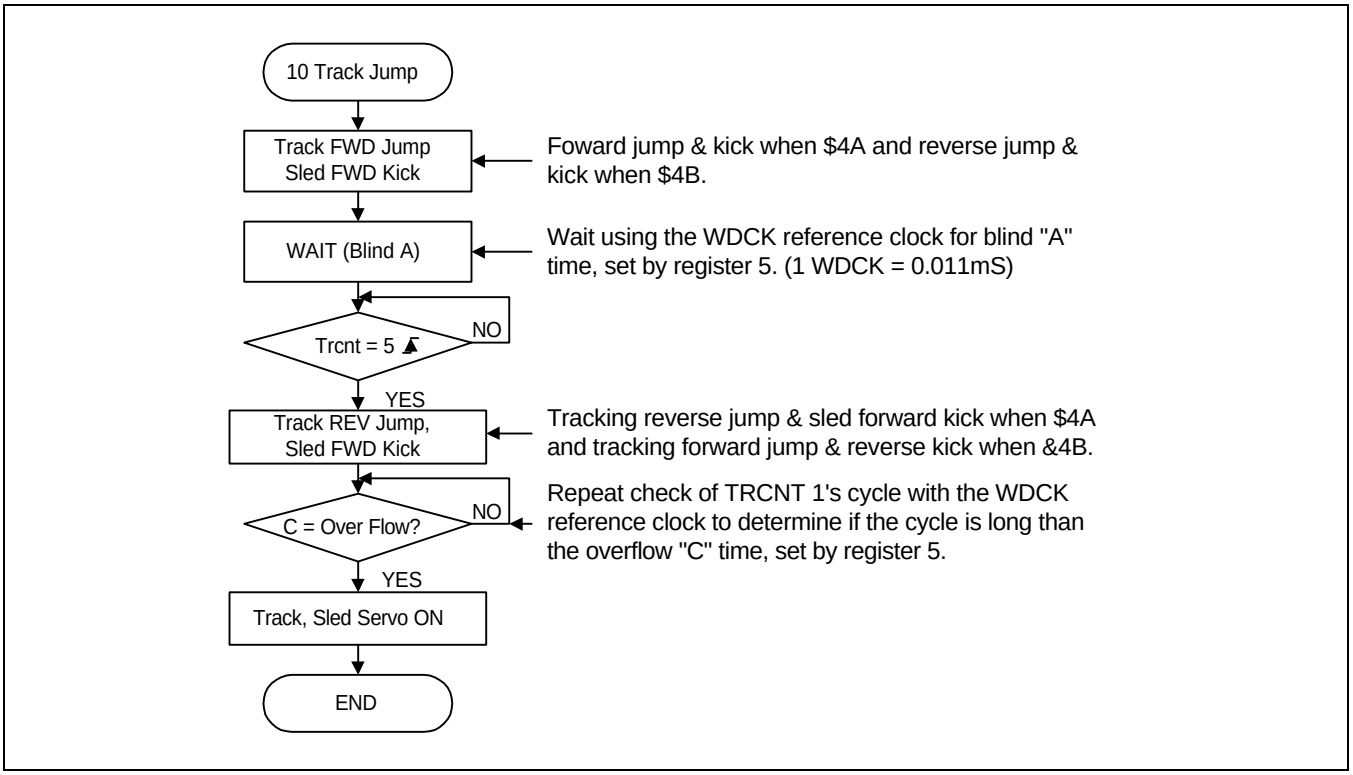
1 Track Jump Timing Chart {$48(FWD), $49(REV) inside ( ) Reverse}



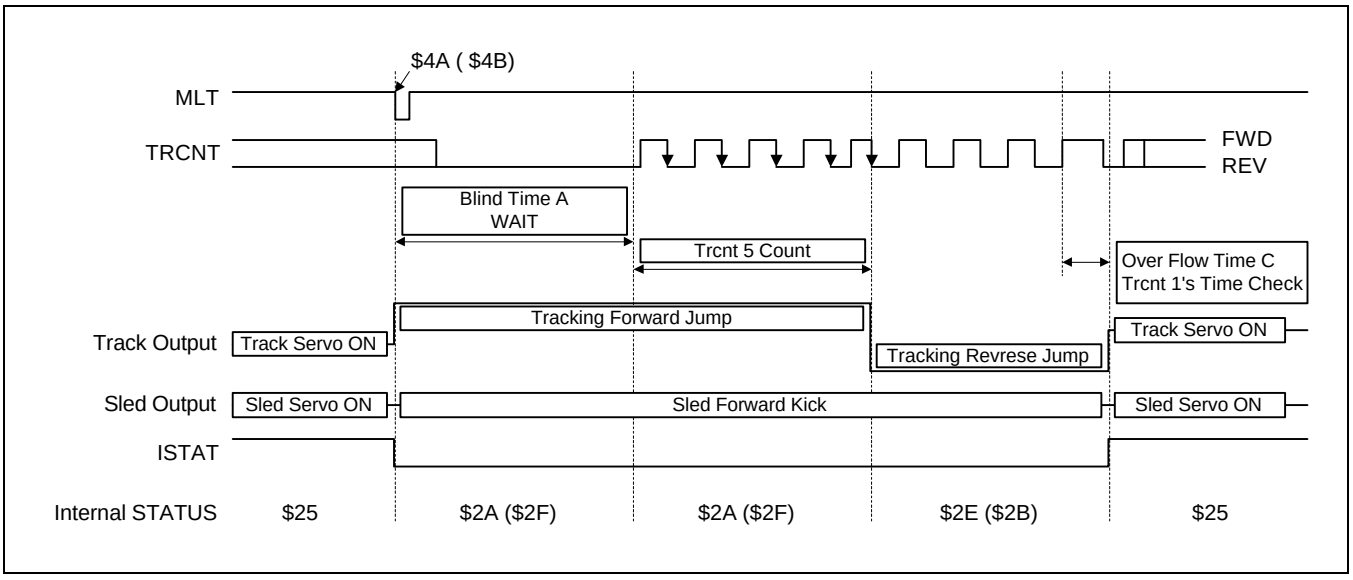
Receives $48 ($49) for 1 track jump and sets the blind and brake times through register $5X.

10 TRACK JUMP {$4A(FWD), $4B(REV)}

Flow-Chart



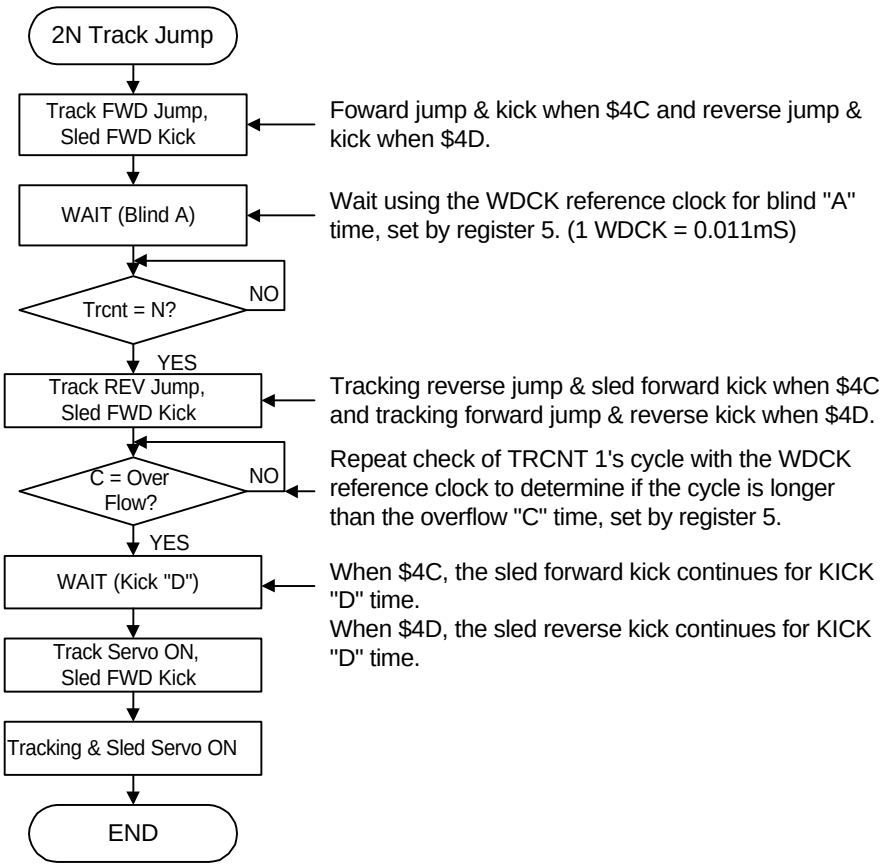
10 Track Jump Timing Chart {$4A(FWD), $4B(REV) inside ( )Reverse }



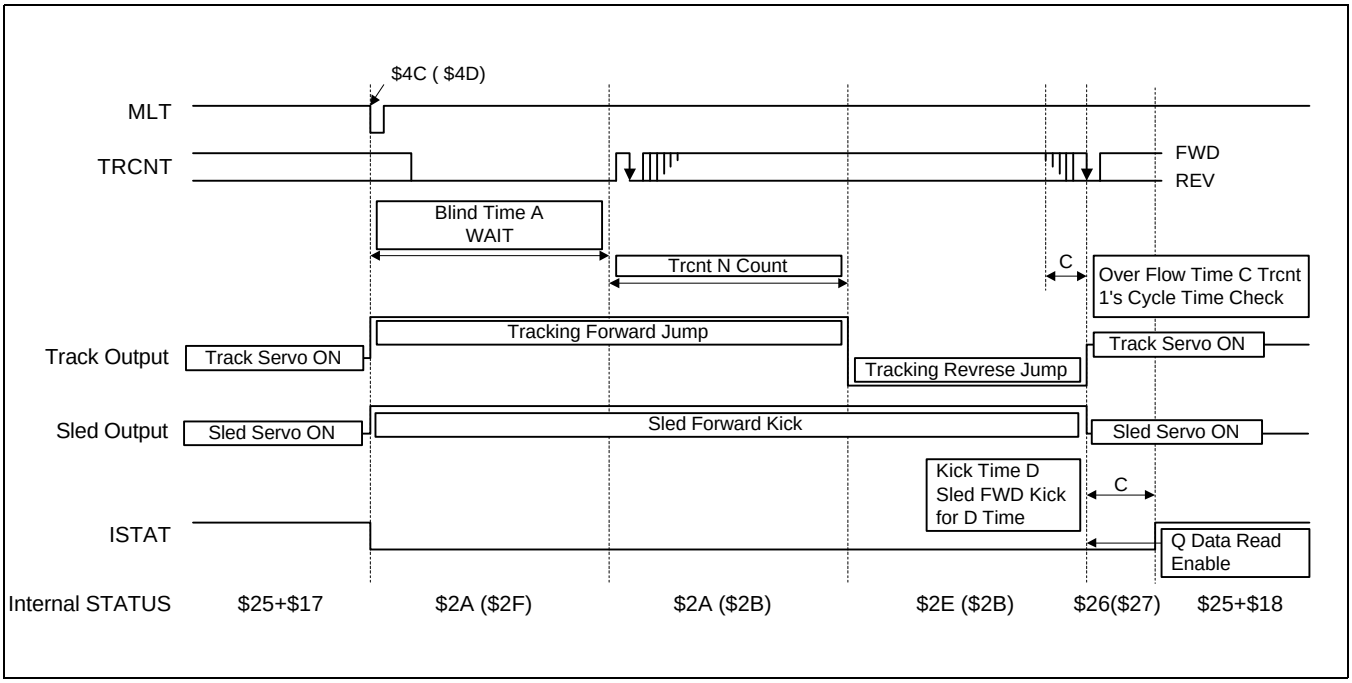
10 track jump executes the tracking forward jump up to trcnt 5track count and turns on the tracking and sled servos after a tracking reverse jump until trcnt 1's cycle is longer than the overflow 'C' time. This operation checks whether the actuator speed is sufficient to turn on the servo.

2N TRACK JUMP

Flow-Chart



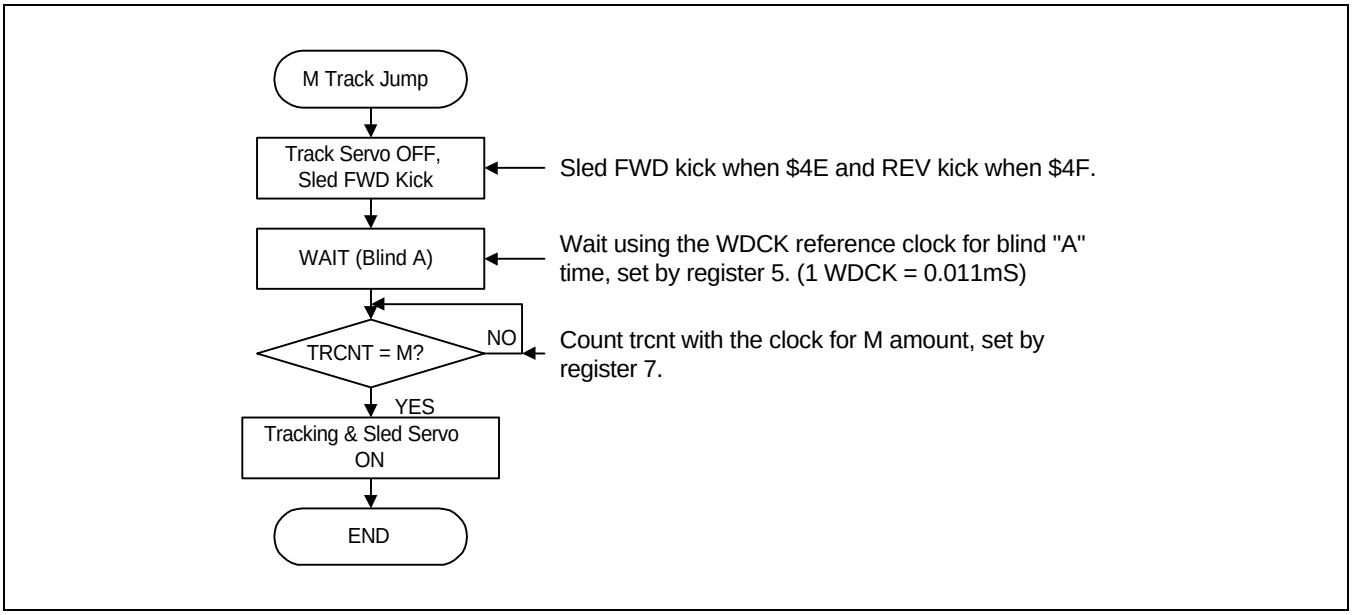
2N Track Jump Timing Chart {$4C(FWD), $4D(REV) inside ( ) Reverse }



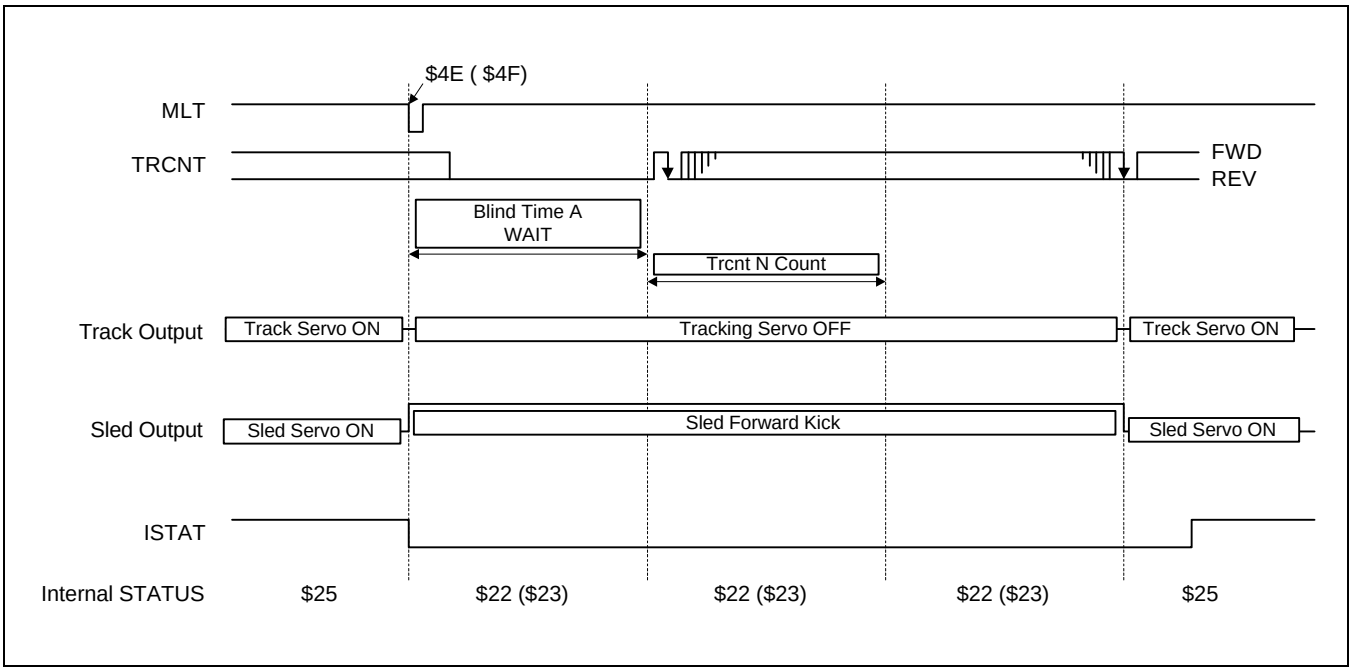
Similar to 10 tracks and executes by adding sled kick by the amount of kick 'D' time and the servo turns on after lens brake starts.

M TRACK JUMP {$4E(FWD), $4F(REV)}

Flow-Chart



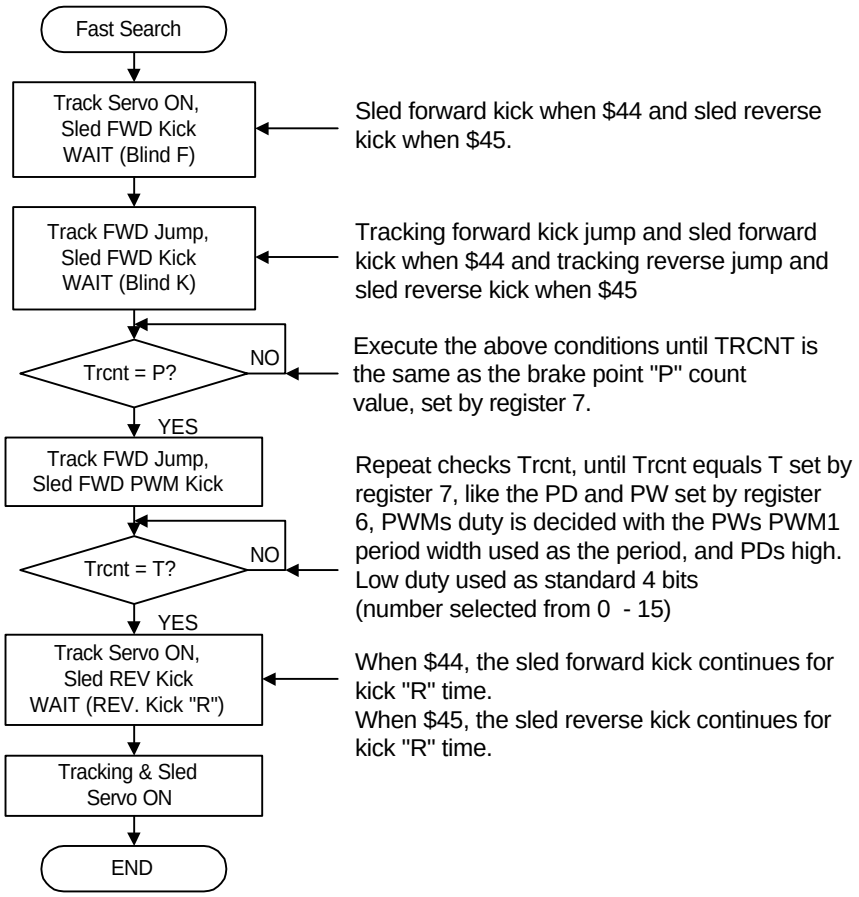
M TRACK JUMP TIMING CHART *{$4E(FWD), $4F(REV) INSIDE () REVERSE}*



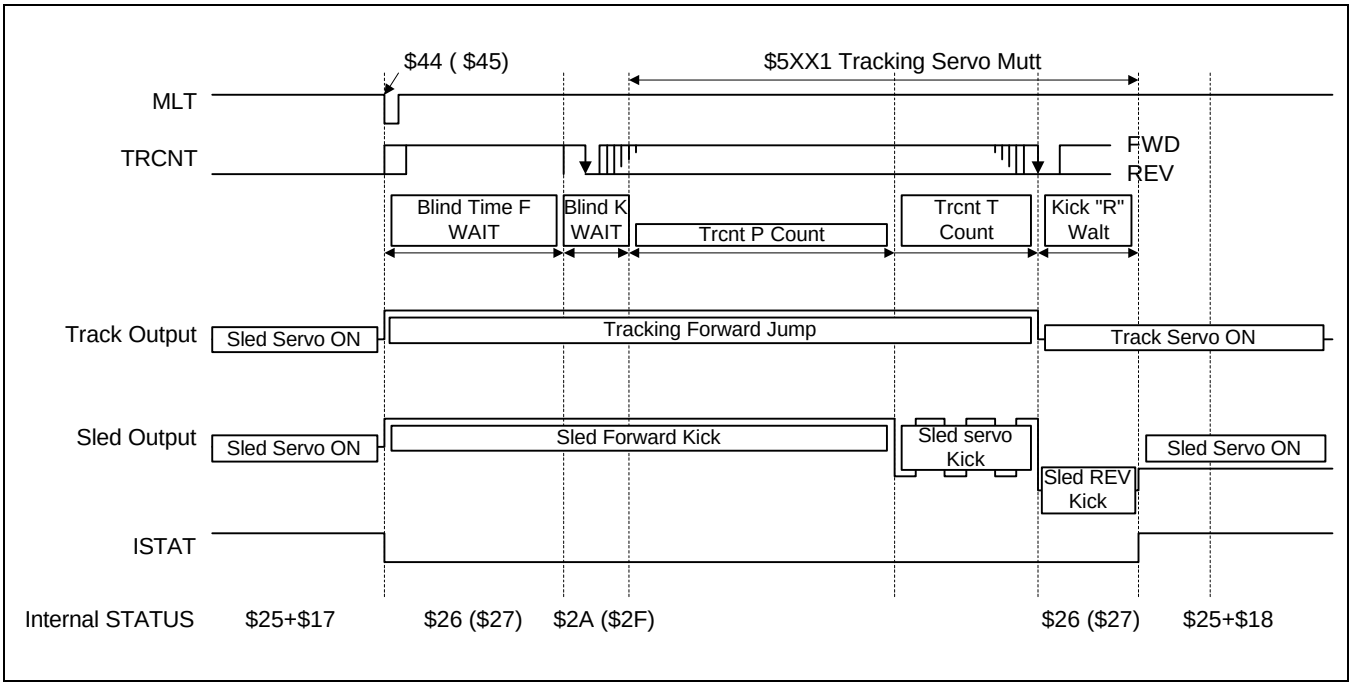
Makes Trcnt to clock and counts to the value of M count, set by register 7, to execute sled kick.

FAST SEARCH

Flow-Chart



FAST SEARCH TIMING CHART {$44(FWD), $45(REV) INSIDE () REVERSE}

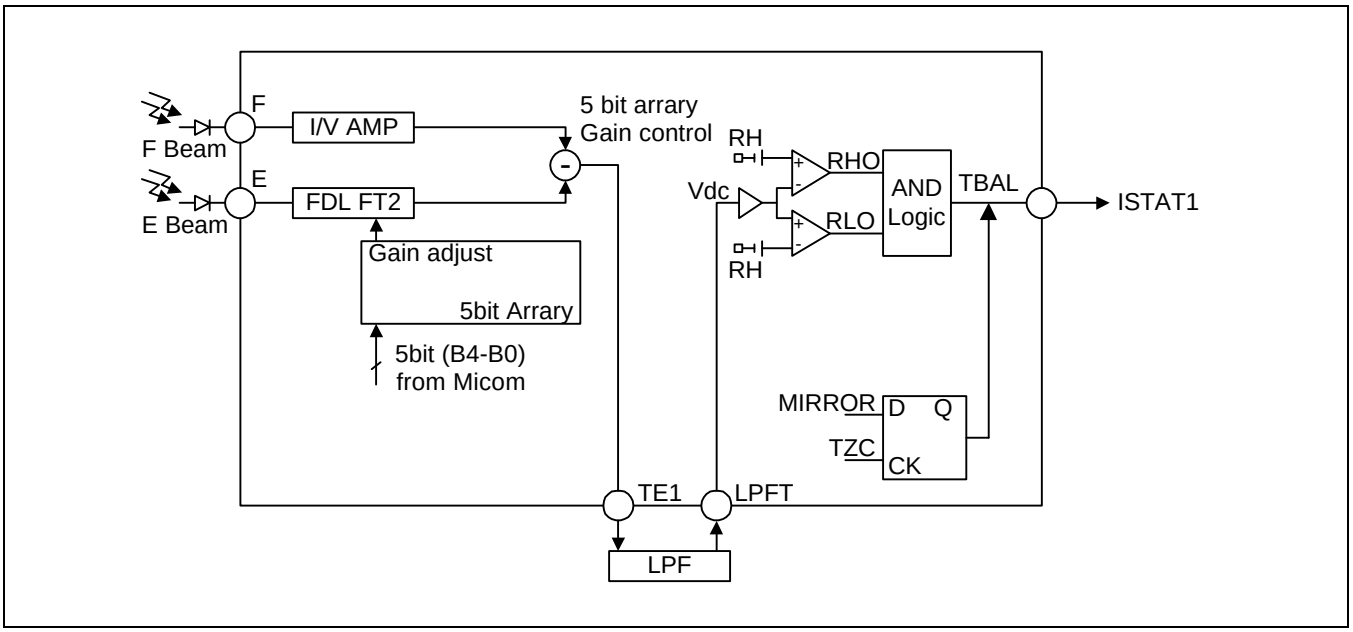


To Note During use of Auto-Sequence

1. Must send tracking gain up and brake on ($17) during 1, 10, 2N, track jump, and fast search.
2. Before the auto-sequence mode, MLT becomes 'L' and sequence operation executes at the initial WDCK falling edge after data latch.
3. During play, determine as FOK and GFS, not ISTAT.
4. Tracking gain up, brake, anti-shock and focus gain down are not executed in auto-sequence, and separate command must be provided.
5. If the Auto-sequence does not operate as Istat Max time over, apply $40 and use after clearing the SSP internal state.
6. The above indicated WDCK receives 88.2kHz from DSP. (2x → 176kHz)
7. The auto-sequence internal trcnt and the actual trcnt are slightly different.
8. Problems can be generated in the algorithm for 2N and M tracks if jump of more than 512 tracks are attempted; therefore, use them for less than 512 track jumps, if at all possible.
9. Use the fast-search algorithm for more than 512 tracks, if possible.

TRACKING BALANCE CONTROL CONCEPT

In tracking balance control, the micom compares and monitors the previously set DC voltage window and the tracking error DC offset, extracted from the external LPF for automatic control.



Summary of Operation

When the focus and spindle servos are on, tracking balance control turns off the tracking and servo loops to open the tracking loop, extracts the DC offset by sending the error signal, passed through the optical pick-up and tracking error amp, through the external LPF, then this offset to the previously set window comparator level, and then informs of the completion the balance control to the micom through the ISTAT, when the dc offset of the tracking error amp in window is extracted. At this time, Tracking E beam-side I/V amps gain is selected by MICOM, and the 5-bit resistance arrays resistance value is selected by the 5-bit control signal.

The values that MICOM applies are 00000 $\rightarrow$ 11111. If you select the switch, TESO DC offset increases the (2.5V-ΔV) $\rightarrow$ (2.5V + ΔV) one step at a time, to enter the pre-selected DC window level. When it enters that level, the balance adjust is completed, and the switch condition is latched at this time

Because the TESO signal frequency is distributed up to 2kHz, the DC offset that passed through the LPF is not a correct value, if a DC component exists, and therefore, micom monitors the window output when the TESO signal frequency is above 1kHz. At this time, the frequency check the ISTAT pin. When TBAL output is H, balance control is complete.

	Vdc < RLI <RHI	**RLI < Vdc < RHI**	**RLI < RHI < Vdc**
RHO	H	H	L
RLO	L	H	H
TBAL (AND gate)	L	H	L

— RHI: High level threshold value

— RLI: Low level threshold value

— Vdc: Window comparator input voltage

— TBAL: And gate output value of the window comparator output

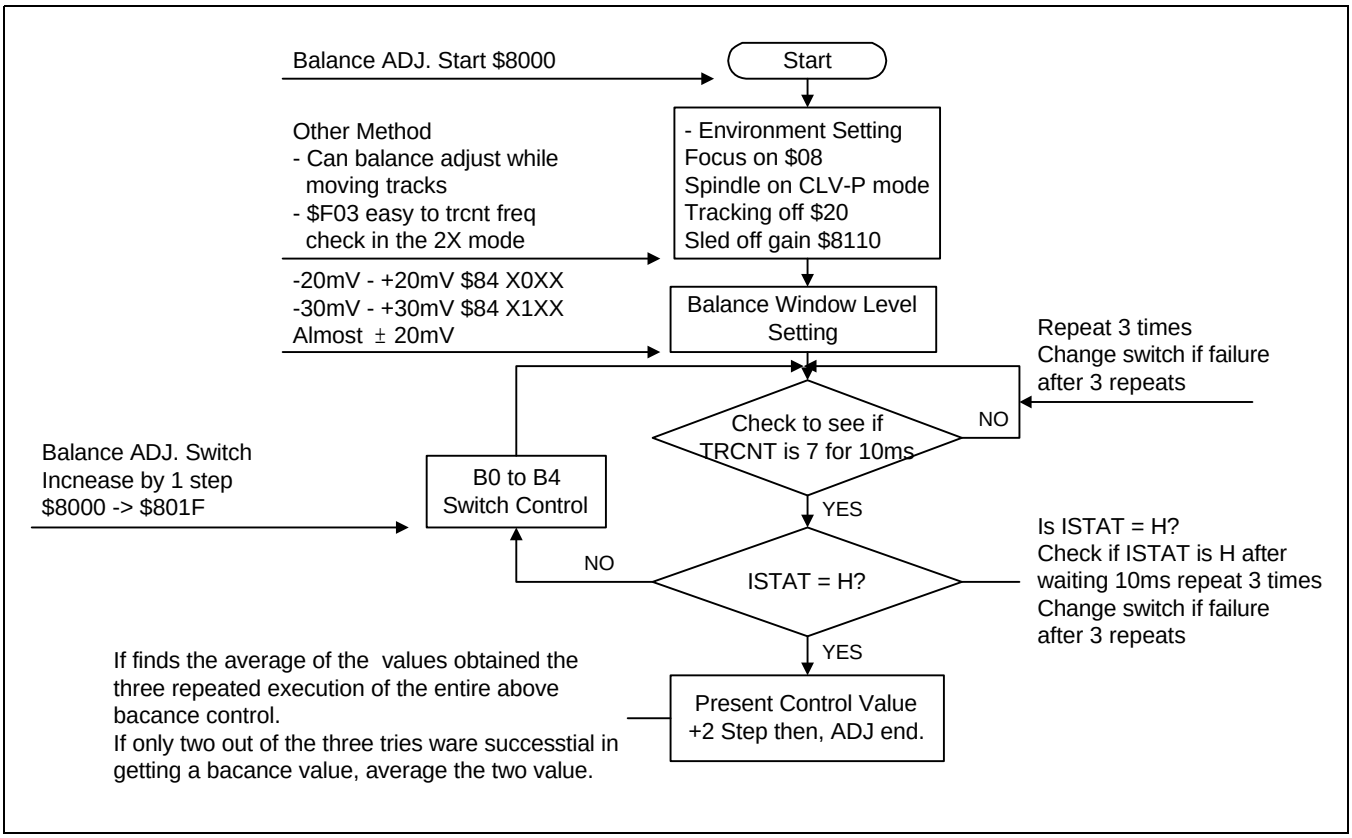
An Example of Tracking Balance Control

Out of $8000 → $801F 32 steps, the upper and lower 32 steps are used and recommand the CLV to CLV-P mode. After receiving $8110 as the gain when the focus and tracking are on, the control flow checks TRCNT frequency in ISTAT to see if the more than 7 TRCNT entered during 10ms. If yes, it checks the ISTAT, if no, it checks the number of TRCNT three times and goes on to the ISTAT check.

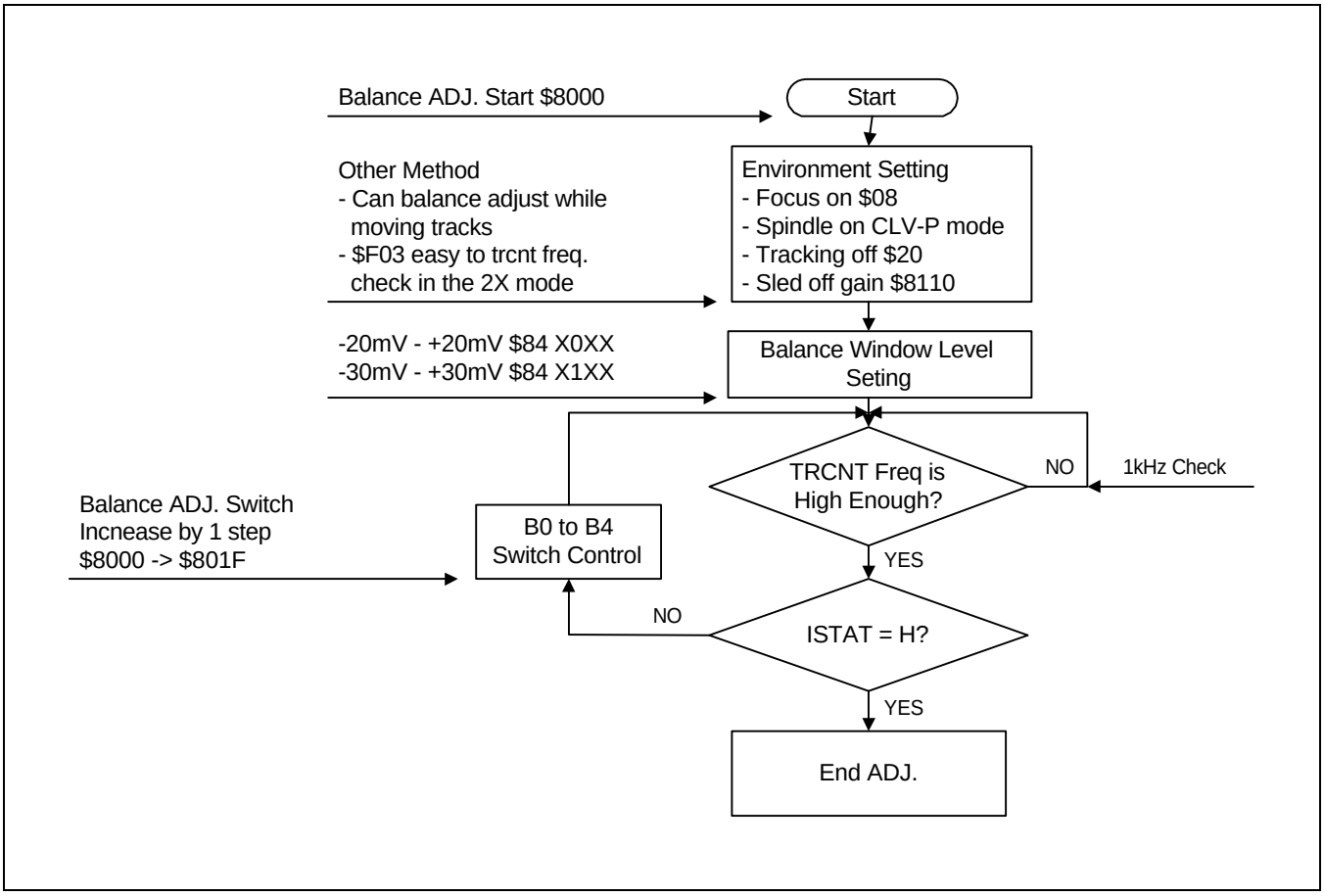
Repeats fail, it raises the balance switch by 1 step. If ISTAT does not immediately go to H, it for 10 ms during ISTAT check after which it check whether ISTAT is H continuously for 10ms, is repeated three times. If the three repeats fail, it raises the balance switch by 1 step.

The above wait 10 ms while running the system. It finds the average of the values obtained the three repeated execution of the entire above balance control. If only the balance values are from two of the three repeats, these values are averaged. If only two out of the three tries were successful in getting a balance value, average the two values. Set as balance switch, this average value +2. This is because the balance for the system and the minus value for the DC is stable in the system. Precision is important in balance adjust, and about 1+2 sec is spent as adjust time, which is accounted for.

Balance Control Flowchart 1



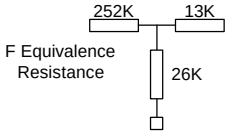
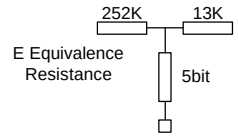
Balance Control Flowchart 2



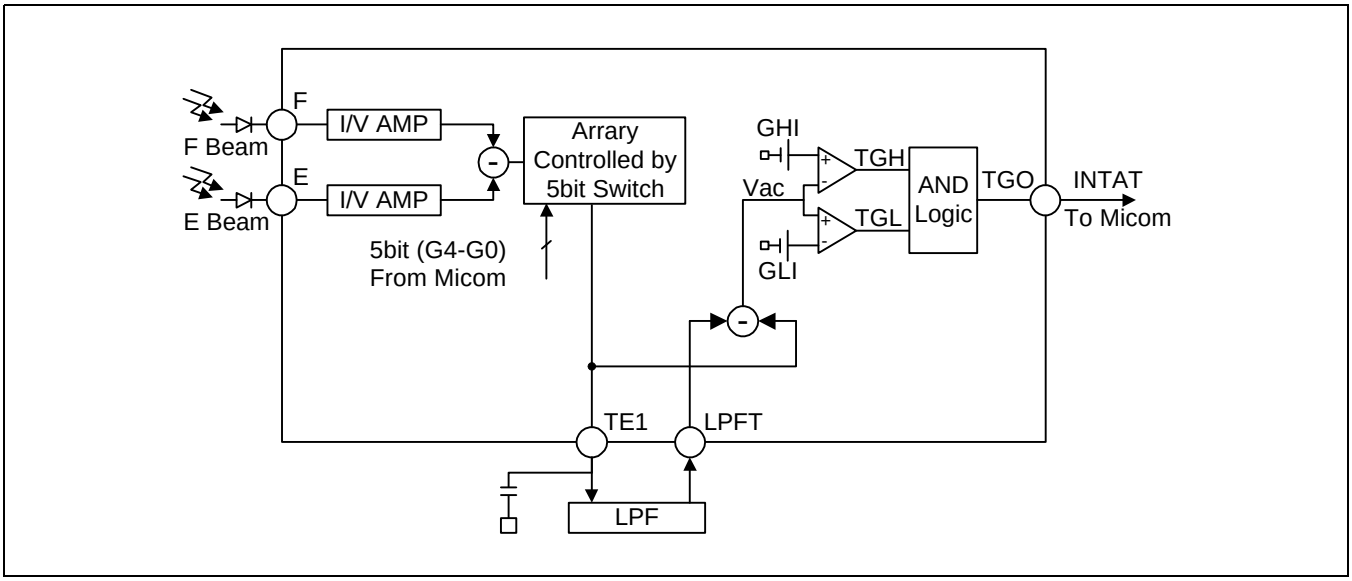
When Tracking Balance

- The balance adjust is from $8000 to $801F, and the switch mode is changed one step at a time by 16-bit data transmission. After adjustment, a separate latch pulse is not necessary.
- If the Trcnt freq. is not high enough, the balance control can be adjusted at $F03 applied 2x mode .
- Here, we have suggested tracking off status for the balance adjust, but the same amount of flow can be balance adjusted while in track move.
- Among the 16 bit data, the tracking balance window setting level can be selected from 0: -20 mV — +20mV 1: -30mV — +30mV through the D6 bit.
- When the tracking balance adjust is complete, the tracking gain control starts.

Tracking Balance Equivalent Resistance

	Tracking Balance			Fixed Resistance and Parallel Resistance		Variable Resistance (5bit)						
Data	**TSIO offset**	**F equivalent Res.**	**E equivalent Res.**	**100K/ 5bit R**	**5bit equivalence**	**35K**	**70K**	**140K**	**280K**	**560K**	**Comments**	
\$8000		391K	480K	15.22K	17.9K	1	1	1	1	1		
\$8001		391K	475K	15.6K	18.6K	1	1	1	1	0		
\$8002	+	391K	468K	16.1K	19.3K	1	1	1	0	1		
\$8003		391K	463K	16.5K	19.7K	1	1	1	0	0		
\$8004		391K	455K	17.2K	20.8K	1	1	0	1	1		
\$8005		391K	451K	17.6K	21.5K	1	1	0	1	0		
\$8006		391K	444K	18.3K	22.4K	1	1	0	0	1		
\$8007		391K	439K	18.9K	23.3K	1	1	0	0	0		
\$8008		391K	433K	19.5K	24.3K	1	0	1	1	1		
\$8009		391K	426K	20.4K	25.5K	1	0	1	1	0		
\$800A	-	391K	421K	21.0K	26.6K	1	0	1	0	1	70K//35K = 23.3K	1
\$800B		391K	415K	21.9K	28.0K	1	0	1	0	0	280K//140K = 93.3K	2
\$800C		391K	409K	22.7K	29.4K	1	0	0	1	1	560K//280K = 186.6K	3
\$800D		391K	403K	23.7K	31.1K	1	0	0	1	0	140K//35K = 28K	4
\$800E		391K	397K	24.7K	32.9K	1	0	0	0	1	280K//35K = 31.1K	5
\$800F		391K	391K	25.9K	35K	1	0	0	0	0	560K//35K = 32.9K	6
\$8010		391K	385K	27.1K	37.2K	0	1	1	1	1	140K//70K = 46.6K	7
\$8011		391K	380K	28.5K	39.9K	0	1	1	1	0	280K//70K = 56K	8
\$8012		391K	374K	30.0K	43.0K	0	1	1	0	1	560K//70K = 62.2K	9
\$8013		391K	368K	31.7K	46.6K	0	1	1	0	0	1//2 = 18.56K	10
\$8014		391K	361K	33.9K	51.4K	0	1	0	1	1	10//560K = 17.96K	
\$8015		391K	357K	35.8K	56K	0	1	0	1	0		
\$8016		391K	350K	38.3K	62.2K	0	1	0	0	1		
\$8017		391K	344K	41.1K	70K	0	1	0	0	0		
\$8018		391K	336K	44.5K	80.4K	0	0	1	1	1		
\$8019		391K	332K	48.4K	93.9K	0	0	1	1	0		
\$801A		391K	327K	52.8K	112K	0	0	1	0	1		
\$801B		391K	321K	58.3K	140K	0	0	1	0	0		
\$801C		391K	315K	65.1K	187K	0	0	0	1	1		
\$801D		391K	309K	73.6K	280K	0	0	0	1	0		
\$801E		391K	303K	84.8K	560K	0	0	0	0	1		
\$801F		391K	298K	100K	0K	0	0	0	0	0		

TRACKING GAIN CONTROL CONCEPT



Operation Summary

Tracking gain control is executed by comparing the previously set gain set value of the window with the only the pure AC component of the signal TEIO (DC+AC) , which was extracted the resistance divide of the tracking error amp output, passed through the LPF and DC offset .

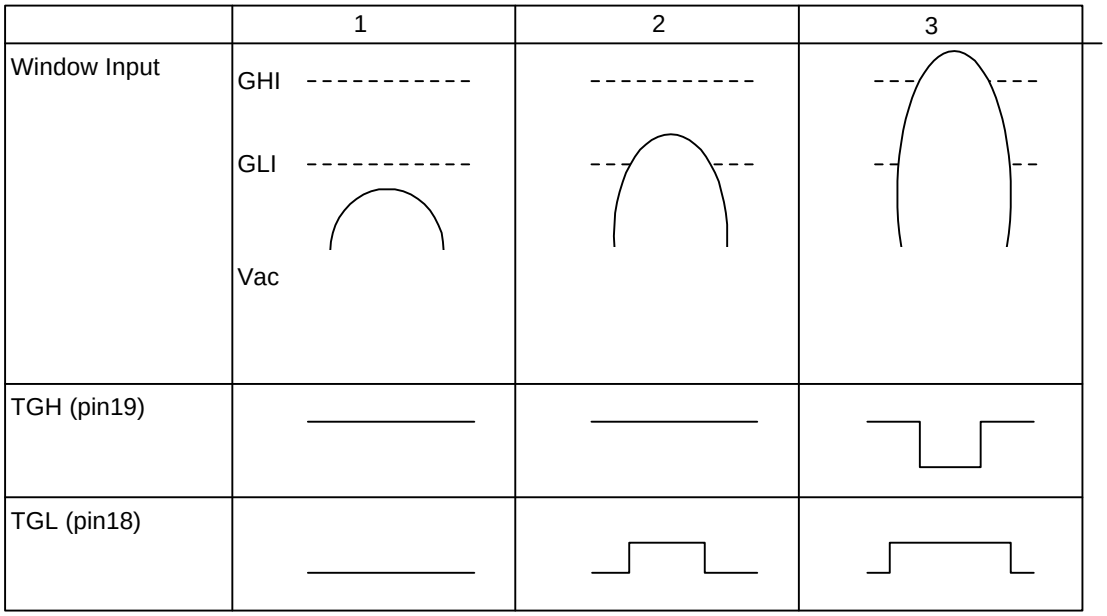
The resistance divide regulates the gain by changing the 5 bit resistance combination with micom command. The tracking gain control is executed under the balance control, the same of focus loop on, spindle servo on, tracking servo off and sled servo off and controls amount of optical pick-up reflection and tracking error amp gain. External LPF cut-off freq. Is 1o 10Hz - 100Hz. The window comparator comparison level can be selected between +150mV - +300mV and +250mV - 200mV using the micom command.

TGL outputs the +150mV and +250mV comparator outputs to TRCNT.

TGH outputs the +300mV and +200mV comparator outputs to ISTAT.

	Vac < GLI <GHI	**GLI < Vac < GHI**	**GLI < GHI < Vac**
TGH (ISTAT output)	H	H	L
TGL (TRCNT output)	L	H	H

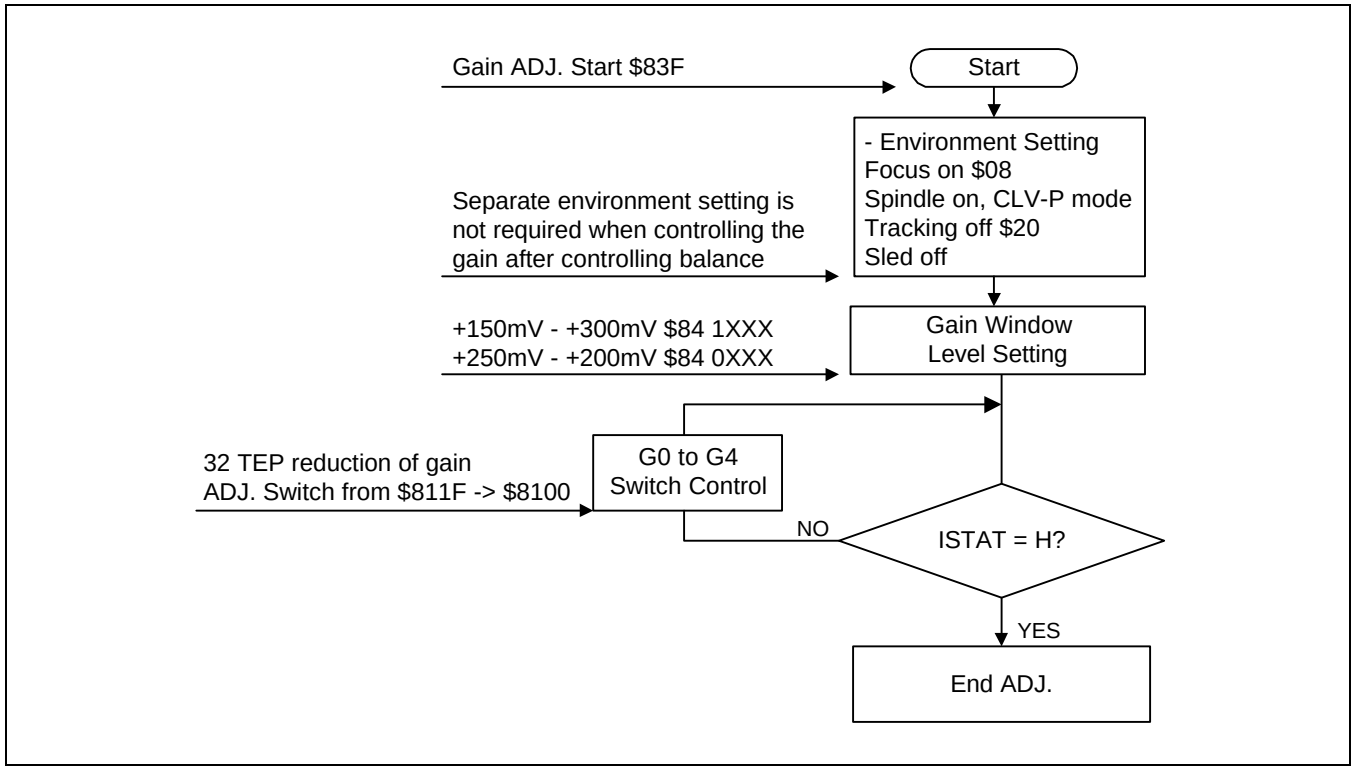
Gain control completes control when TGL output is H.



Tracking Gain Control

- In balance control, 16 bit data transmission changes the switch mode by 1step from $811F → $8100, and , after adjustment, a separate latch pulse is not needed.
- The H duty check reference of TGL output of Trcnt output is above 0.1ms.
- The most appropriate method is chosen among the 4 control modes listed besides the ones above for control.
- Among the 12 bit data, the tracking balance window setting level can be selected from 0: +250mV (TGL) - +200mV (TGH), 1: +150mV (TGL) - +300mV (TGH) through the D3 bit.
- When the tracking gain adjust is complete, it enters the tracking & sled servo loop and TOC read.

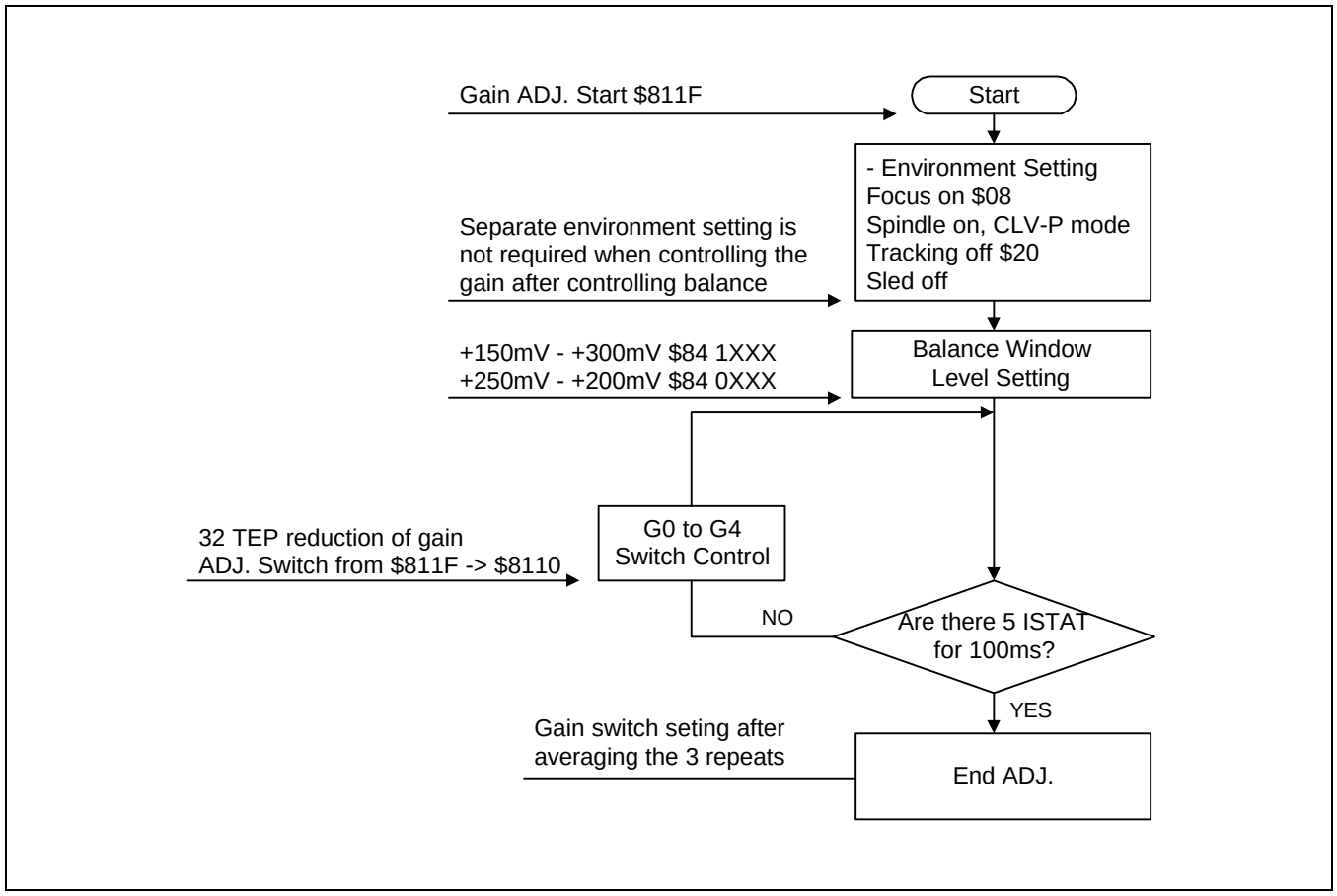
Gain Control Flowchart 1



In gain control, the micom command from $811F → $8100 successively executes the down command and goes status 1 to 2 → 3. If it reaches status 2, control ends.

- Gain Control Method 1
  The micom monitors the TGL output of ISTAT and, when it detects the output's H duty (0.1ms), ends. The window comparator level at this time is +150mV - +300mV.
- Gain Control Method 2
  The micom monitors the TGH output of ISTAT and, when it detects the output's H duty (0.1ms), ends. The window comparator level at this time is +150mV - +300mV.
- Gain Control Method 3
  The micom monitors the TGL output of ISTAT and, when it detects the output's H duty (0.1ms), ends. It changes the window comparator level at this time from +150mV - +300mV to +250mV - +200mV. Then it re-monitors the TGL output of ISTAT, and, if it detects the output's H duty (0.1ms), control ends. If it latches the middle command between the previous micom command value and latter command value, +200mV gain control becomes possible.
- Gain Control Method 4
  The micom monitors the TGL output of ISTAT and, when it detects the output's H duty (0.1ms), it down the micom command by 1 and control ends. The window comparator level at this time is +150mV - +300mV.
- Gain Control Method 5
  Gain control is set to 32 steps in total and gain window is set to +250mV.
  (That is, start from $811F and head toward $8110) after setting $811F, it monitors the ISTAT to check whether five ISTAT were detected for 10ms. If yes, control ends, and, if not, it as gain switch is lowered by 1 step.
  The above process is repeated three times and the average value obtained from this repetition set as the gain control switch.

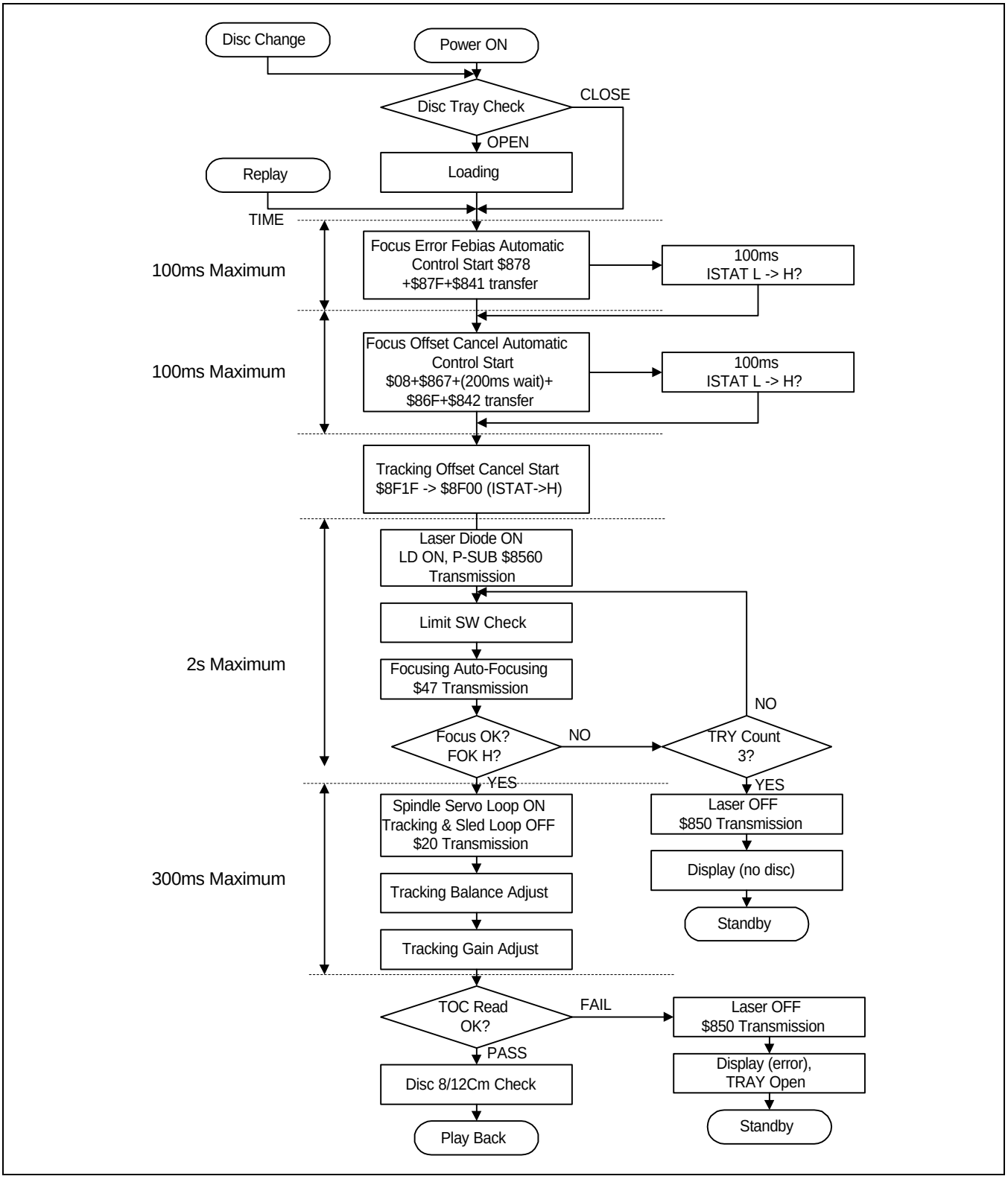
Gain Control Flowchart 2



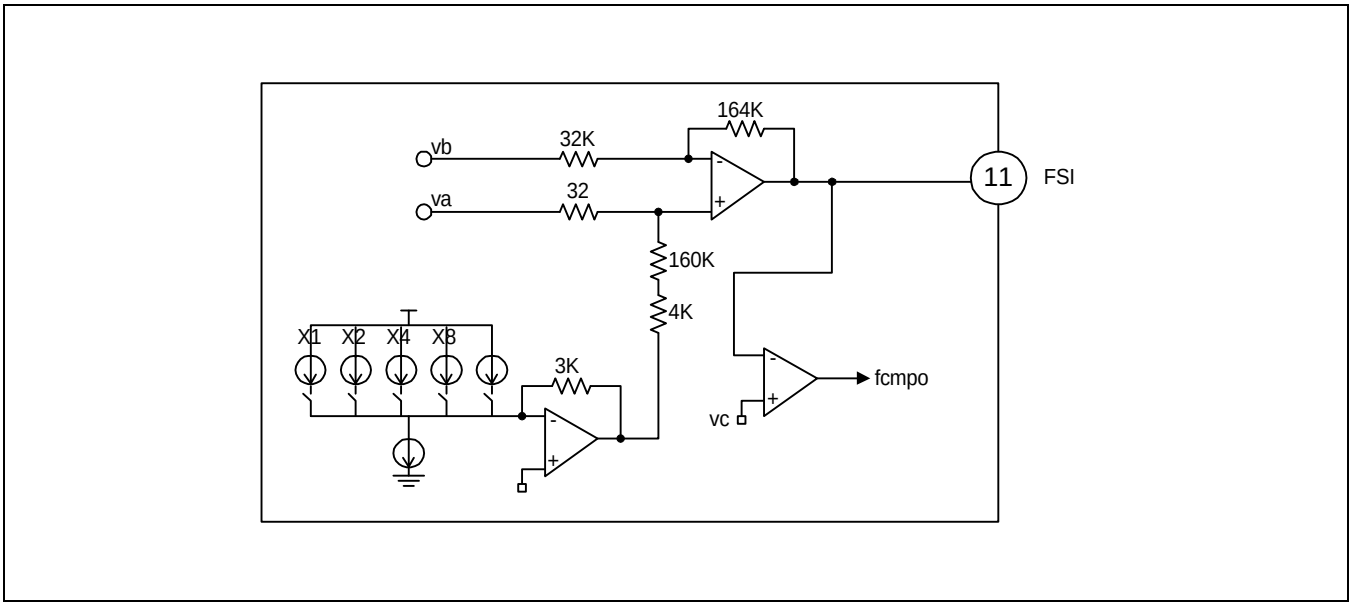
Tracking Gain Equivalent Resistance

	Tracking Gain										
Data	**TERR Gain**	**TERR Gain**	**5Bit Gain Ratio**	**Proportional Resistance**	**Combined Resistance**	**7.5K**	**7.5K**	**3.75K**	**2.0K**	**1K**	**Comments**
$811F	0.096	96K/32K	0.032	15.0K	0.5K	1	1	1	1	1	The gain at
$811E	0.272	→ x 3.0	0.090	15.0K	1.5K	1	1	1	1	0	ratio is
$811D	0.428		0.142	15.0K	2.5K	1	1	1	0	1	calculated in
$811C	0.567		0.189	15.0K	3.5K	1	1	1	0	0	the TSIO
$811B	0.662		0.220	15.0K	4.25K	1	1	0	1	1	terminal.
$811A	0.777		0.259	15.0K	5.25K	1	1	0	1	0	
$8119	0.882		0.294	15.0K	6.25K	1	1	0	0	1	
$8118	0.977		0.325	15.0K	7.25K	1	1	0	0	0	
$8117	1.043		0.347	15.0K	8.0K	1	0	1	1	1	
$8116	1.144		0.381	15.0K	9.25K	1	0	1	1	0	
$8115	1.200		0.400	15.0K	10.0K	1	0	1	0	1	
$8114	1.269		0.423	15.0K	11.0K	1	0	1	0	0	
$8113	1.317		0.439	15.0K	11.75K	1	0	0	1	1	
$8112	1.378		0.459	15.0K	12.75K	1	0	0	1	0	
$8111	1.434		0.478	15.0K	13.75K	1	0	0	0	1	
$8110	1.487		0.495	15.0K	14.75K	1	0	0	0	0	
$810F	1.548		0.516	7.5K	8.0K	0	1	1	1	1	
$810E	1.636		0.545	7.5K	9.0K	0	1	1	1	0	
$810D	1.714		0.571	7.5K	10.0K	0	1	1	0	1	
$810C	1.783		0.594	7.5K	11.0K	0	1	1	0	0	
$810B	1.860		0.620	7.5K	12.25K	0	1	0	1	1	
$810A	1.888		0.629	7.5K	12.75K	0	1	0	1	0	
$8109	1.941		0.647	7.5K	13.75K	0	1	0	0	1	
$8108	1.988		0.662	7.5K	14.75K	0	1	0	0	0	
$8107	2.021		0.673	7.5K	15.50K	0	0	1	1	1	
$8106	2.0625		0.6875	7.5K	16.50K	0	0	1	1	0	
$8105	2.100		0.700	7.5K	17.50K	0	0	1	0	1	
$8104	2.134		0.711	7.5K	18.50K	0	0	1	0	0	
$8103	2.158		0.719	7.5K	19.25K	0	0	0	1	1	
$8102	2.189		0.729	7.5K	20.25K	0	0	0	1	0	
$8101	2.217		0.739	7.5K	21.25K	0	0	0	0	1	
$8100	2.243		0.747	7.5K	22.25K	0	0	0	0	0	

EXAMPLE OF SYSTAM CONTROL



FEBIAS OFFSET CONTROL

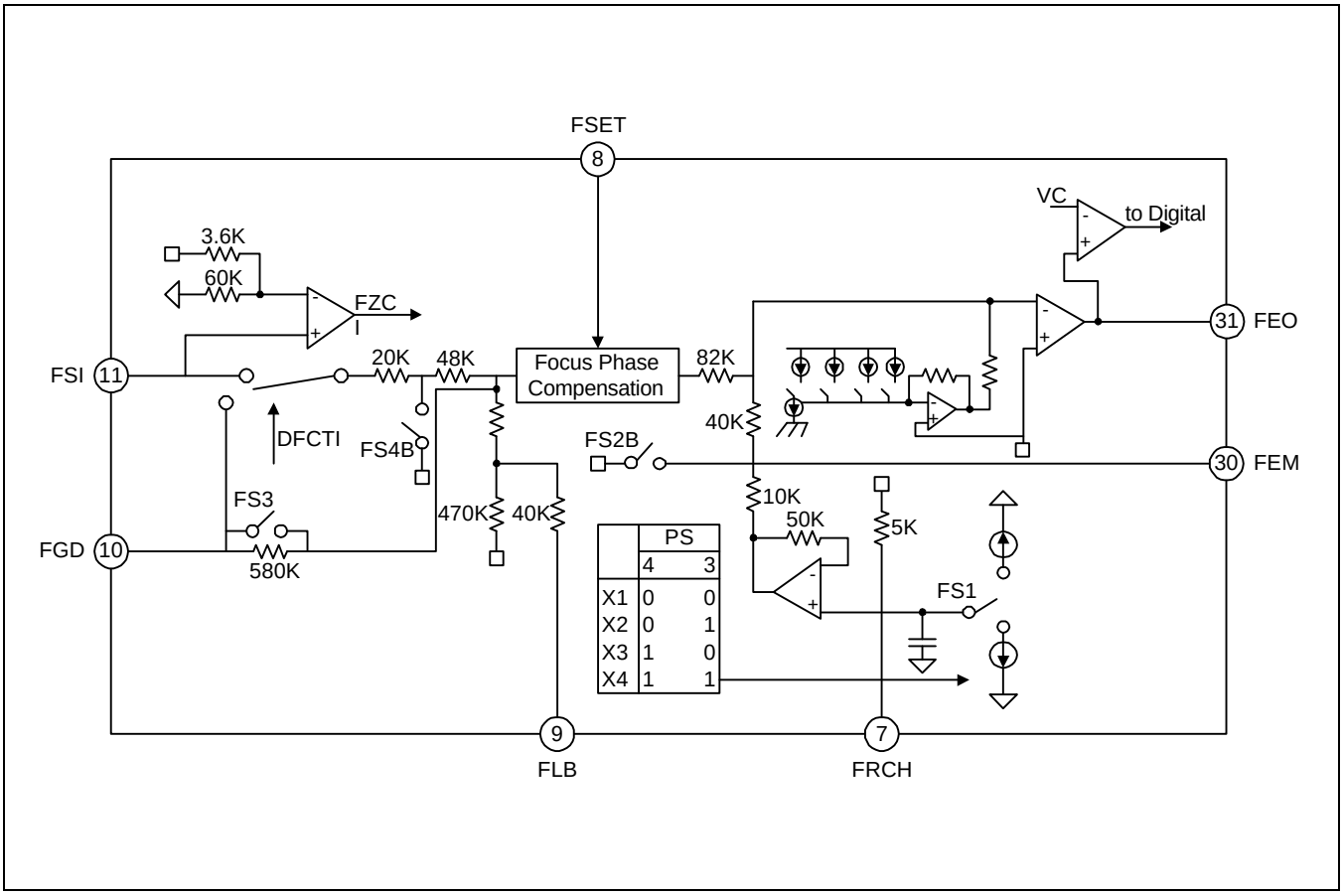


Febias offset control starts when it receives the febias offset control start command $841X from the micom. Febias offset control ends when the focus error amp output above 1/2 VCC after the focus output with 1/2 VCC at the focus error amp final output terminal. The voltage per 1 step of the focus offset control is approximately 17mV. The 5bit resistance DAC changes from 112mV up to - 112mV in 1 step, after which 1/2 step, approximately -8mV offset, is applied.

The offset dispersion after febias offset control exists between -8mV - +8mV. The time per 1 step is 2.5ms; for 5 bits and total of 32 steps, the maximum required time is 128ms.

Hardware performs the control from minus offset to plus offset. The febias offset re-control is when 4bit DAC is reset by $878. And Reset can be canceled only when the $87F applied D2 bit is changed from 0 $\rightarrow$ 1. The Febias DAC latch block reset for electrostatics and system operation is reset by Micom DATA and not by RESET terminal, the system reset.

FOCUS OFFSET CONTROL



Focus Offset control starts when it receives the Focus Offset control start command $842X from micom. Focus Offset control ends when the focus error amp output below 1/2VCC after the focus output with 1/2 VCC at the focus error amp final output terminal. The voltage per 1 step of the focus offset control is approximately 40mV. The 4 bit resistance DAC changes from 320mV up to -320mV in 1 step, after which 1/2 step, approximately -20ms offset, is applied. The offset dispersion after Focus offset control exists between -20mV - +20mV. The Febias Offset can be changed in 10mV step within the micom's ± 100mV range after focus offset control. The required per 1 step is 2.5ms; for 4 bits and total of 16 steps, the maximum required time is 128ms.

For focus offset readjust, 4-bit DAC is reset by $867, and reset can be canceled only when the $86FX applied D3 bit is changed from 0 → 1. The Febias DAC latch block reset for electrostatics and operation error is reset by micom DATA and not by RESET terminal, the system reset.

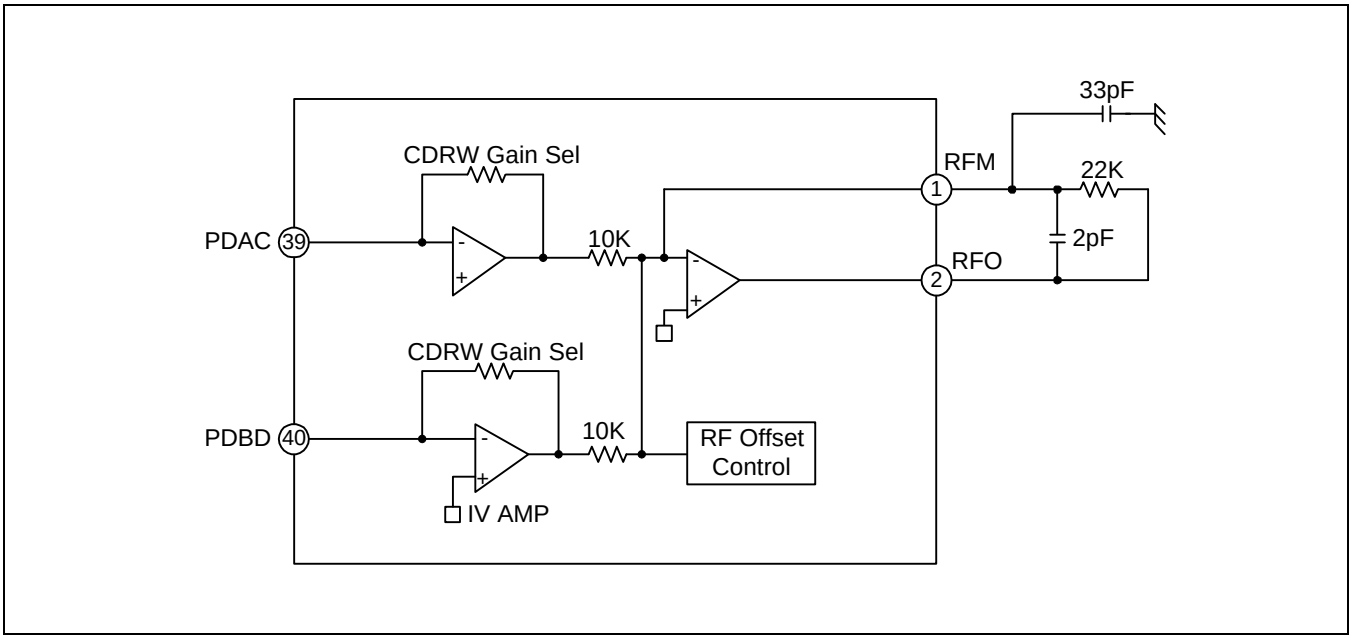
FEBIAS OFFSET SETTING

Febias Control

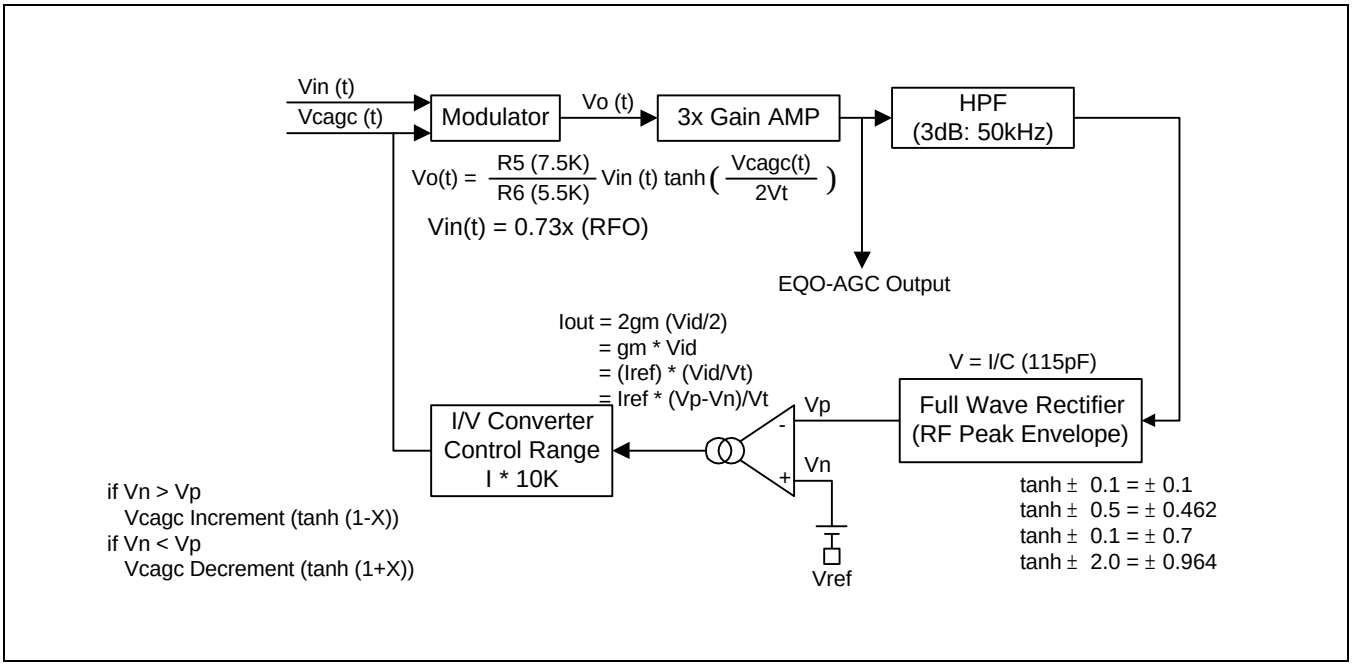
The FEBIAS offset control is automatically controlled to 0mV and can be controlled to ± 200mV. After the focus offset automatic control ends after FEBIAS offset automatic control, the command sets the internal positive and negative offsets in 20mV units to the micom.

RF SUMMING AMPLIFIER APPICATION

The RF I/V AMP can be controlled to 0.5X 8Step up to 1X - 4X CD-R and CDRW. The information related to CDR, CDRW disc detector is output as RFO level through the ISTAT. The RFO offset control is installed to prevent RF level clipping during low RFO voltage.



RF EQUALIZE & AGC



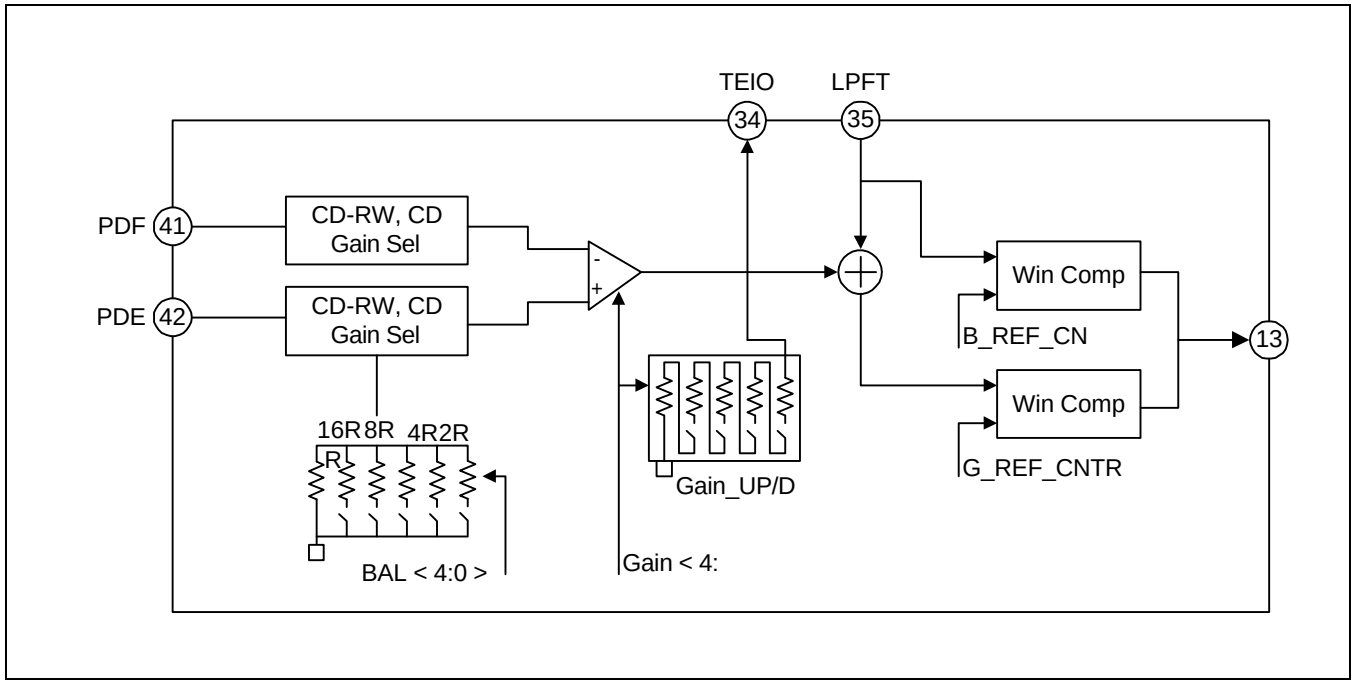
The modulator output, which had the Veqc's Tanh term multiplied at the input, passes through the approximately 3X gain terminal to the ARF pad. On the one hand, the output is - rectified as it passes through the HPF having 50kHz pole frequency and follows the peak envelope the RF level. At this time, the pole frequency of the HPF is set to 50kHz so that the 3T - 11T component can pass through without attenuation. The RF level peak value is integrated at the 's CAP node after wave rectification. If this peak value is less than the already set voltage comparison, sinking current is output and, if not, sourcing current is output. The maximum peak value at this time is 10uA, which is I/V converted and applied as the modulator control voltage. Under the sinking condition, the Vcagc increases to 1outx10K and multiplied by Tanh (1-X); the sourcing condition, Vcagc decreases to Iout x10K and multiplied by Tanh (1+X), where X is (Veqc/2Vt).

Overall, after detecting the 3T and 11T levels by full-wave rectification, it is compared to Tanh using the modulator and multiplied to the gain to realize the wave-form equalize. The above is related to the AGC concept, which means that a specific RF level is always taken

OTHER BLOCK

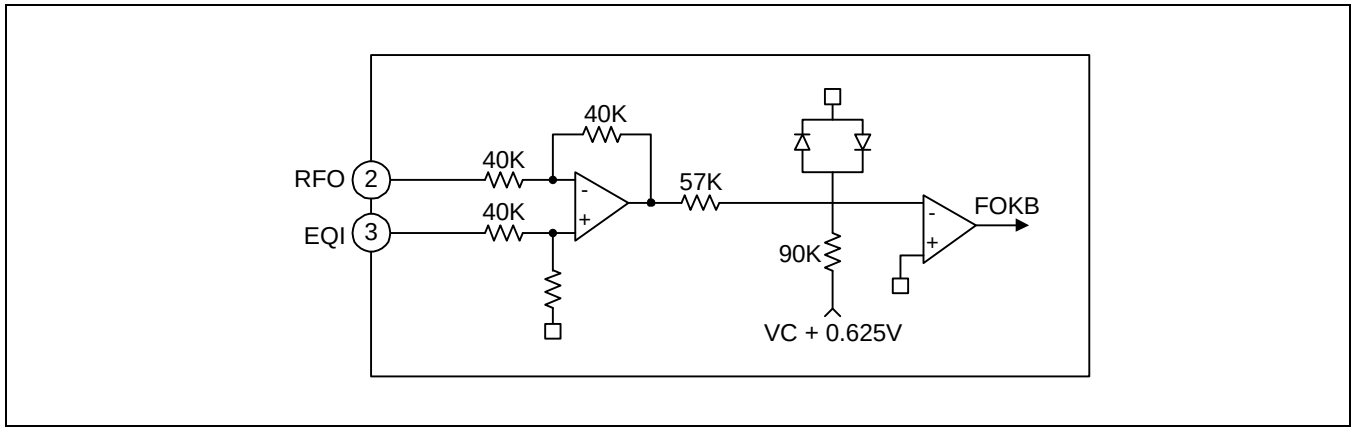
Tracking Error Amplifier

The side spot photo diode current input to terminals E and F passes through the E Loop I-V and F Loop I-V Amps. It is then converted into voltage, in order to gain the difference signal in the Tracking Error Amp. This portion can perform 0.5X 8 step gain control up to 1X-4X for CD-R and CD-RW. Has the micom programming, which controls the balance by controlling gain at the E terminal and controls the gain at TEIO.



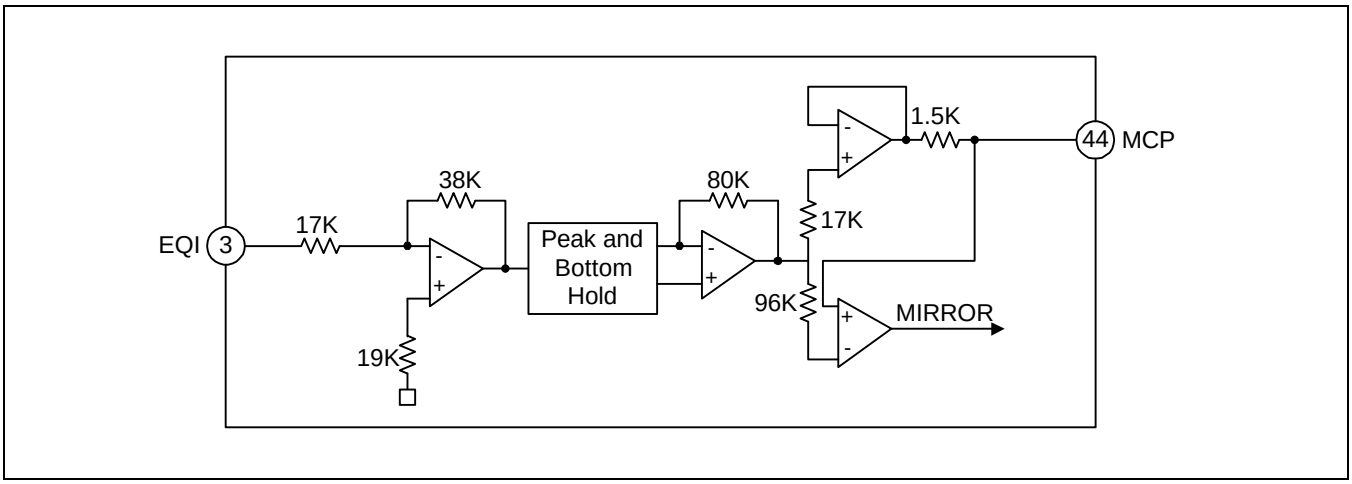
Focus OK circuit

Focus Ok circuit makes the timing window, which turns on the focus in the focus search state by "output" FOK as L $\rightarrow$ H if the RF level is above the reference after the difference in DC between and RFO terminals extracted and compared to the reference DC value.



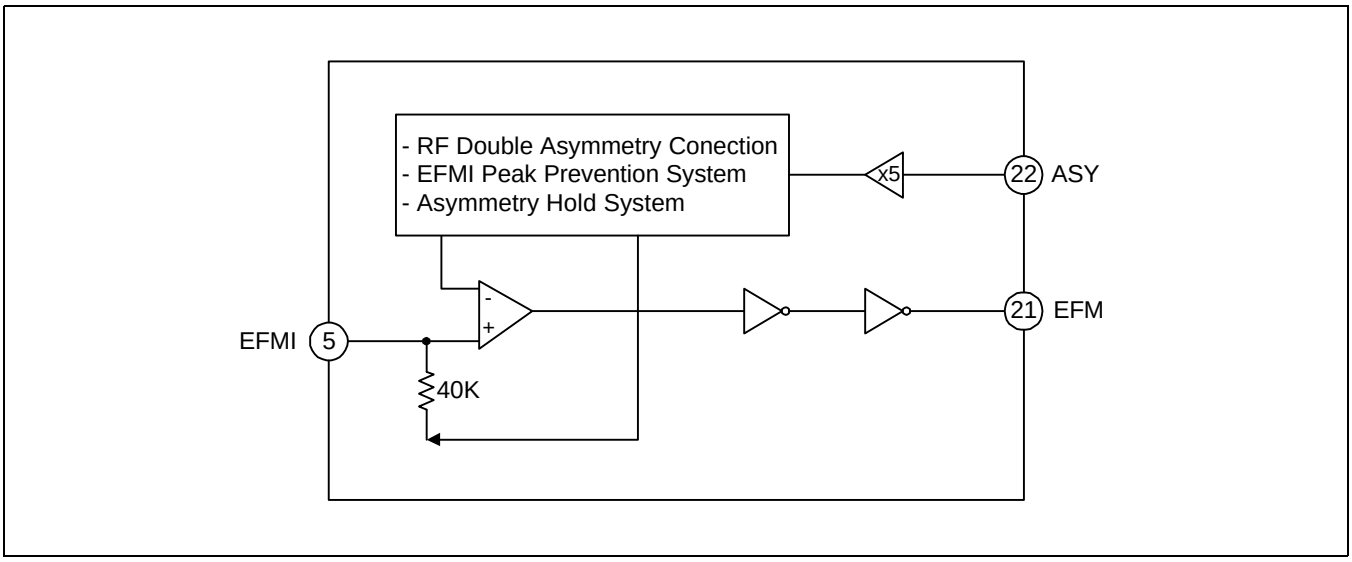
MIRROR CIRCUIT

After amplifying the RFI signal, the mirror signal peak and bottom holds.
Peak hold can follow even at defect type traverse and bottom hold counts the tracks by following RF envelop at a jump. The mirror output is "L" on the disc track and "H" between tracks. Even if above 1.4 ms is detected, it outputs "H".



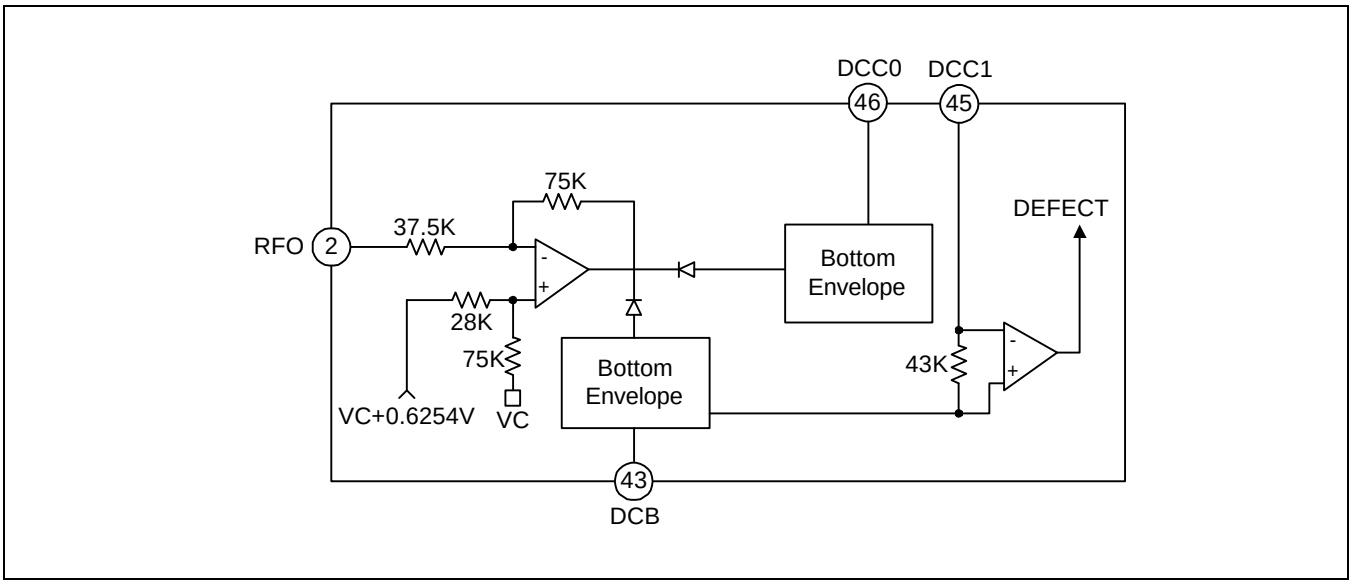
EFM Comparator

The EFM Comparator makes the Rf signal into a secondary signal. The Asymmetry generated by a fault during Disc production cannot be eliminated by only AC coupling, so control the standard voltage of the EFM Comparator to eliminate it.



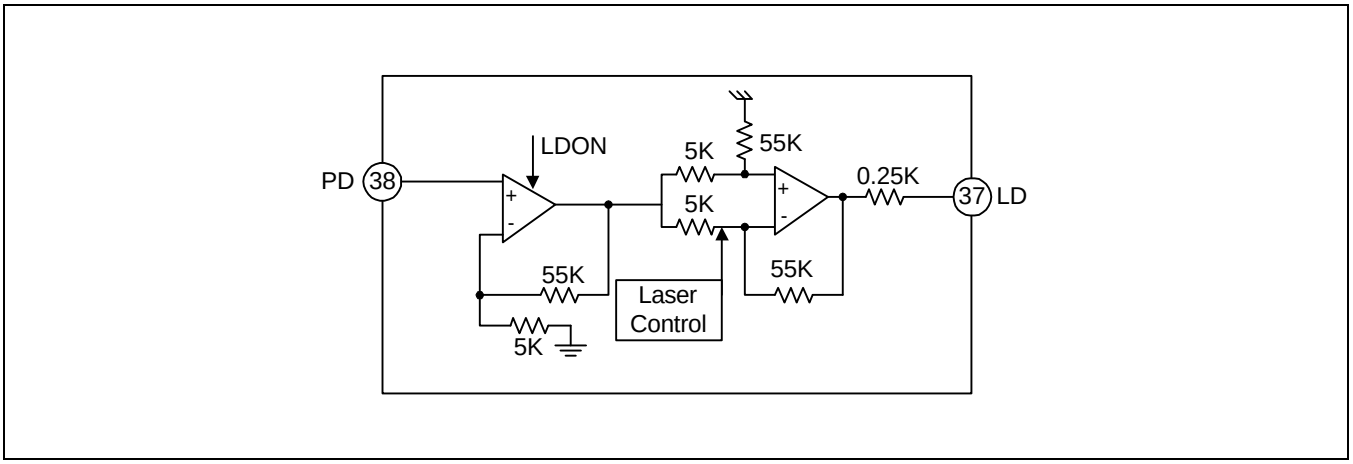
Defect Circuit

After RFO signal inversion, bottom hold is carried out using only 2. Except, the bottom hold of holds the coupling level just before the coupling. Differentiate this with the coupling, then level shift it. Compare the signals to either direction to generate the defect detect signal.



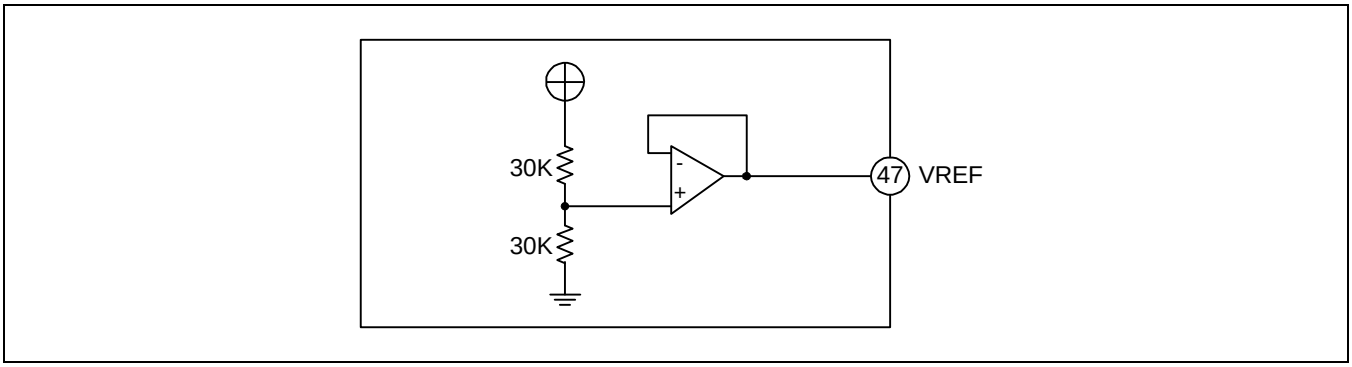
APC Circuit

When the laser diode operates in electrostatic field, the laser output temperature highly negative so the monitor photo diode controls the laser output at a fixed level. The laser control system is installed to absorb the deviation of the disc reflection. System controls the laser power using the tracking summing signal of the side beam to a fixed laser output.



Center Voltage Generation Circuit

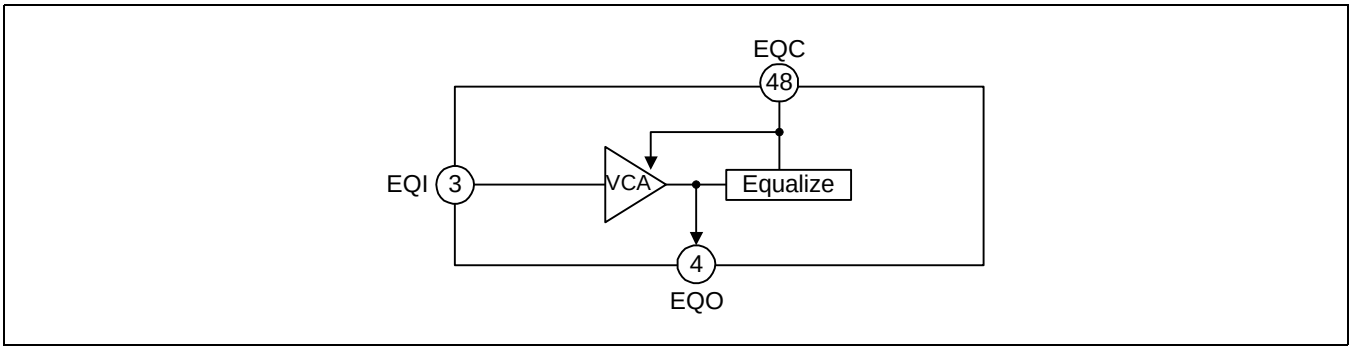
The center voltage is made by using the resistance divide.



RF Equalize Circuit

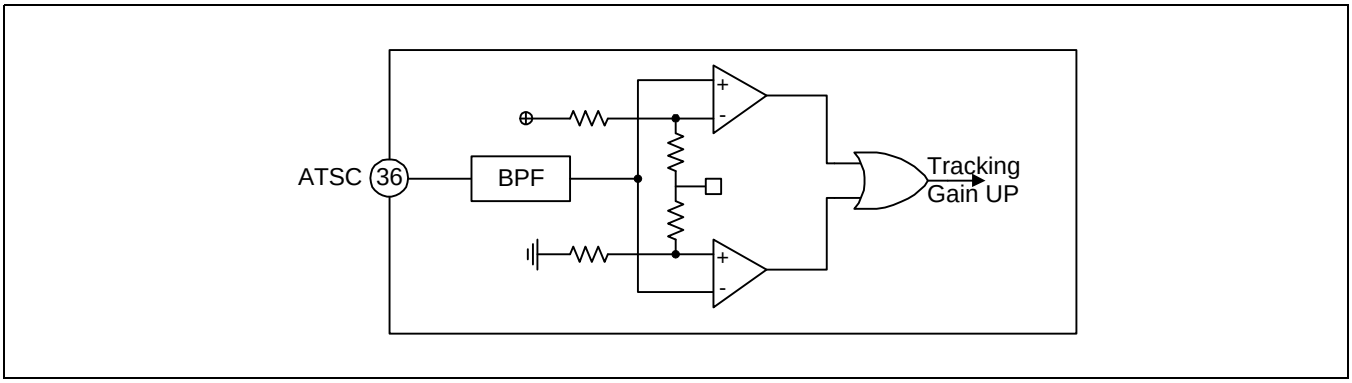
The AGC block, which maintains the RF peak to peak level, possess the 3T gain boost. It detects the RF envelop and compares it to the reference voltage to control the gain.

Receives the RF output to stabilize the RF level to 1Vpeak-peak, which is applied to the EFM slice input.



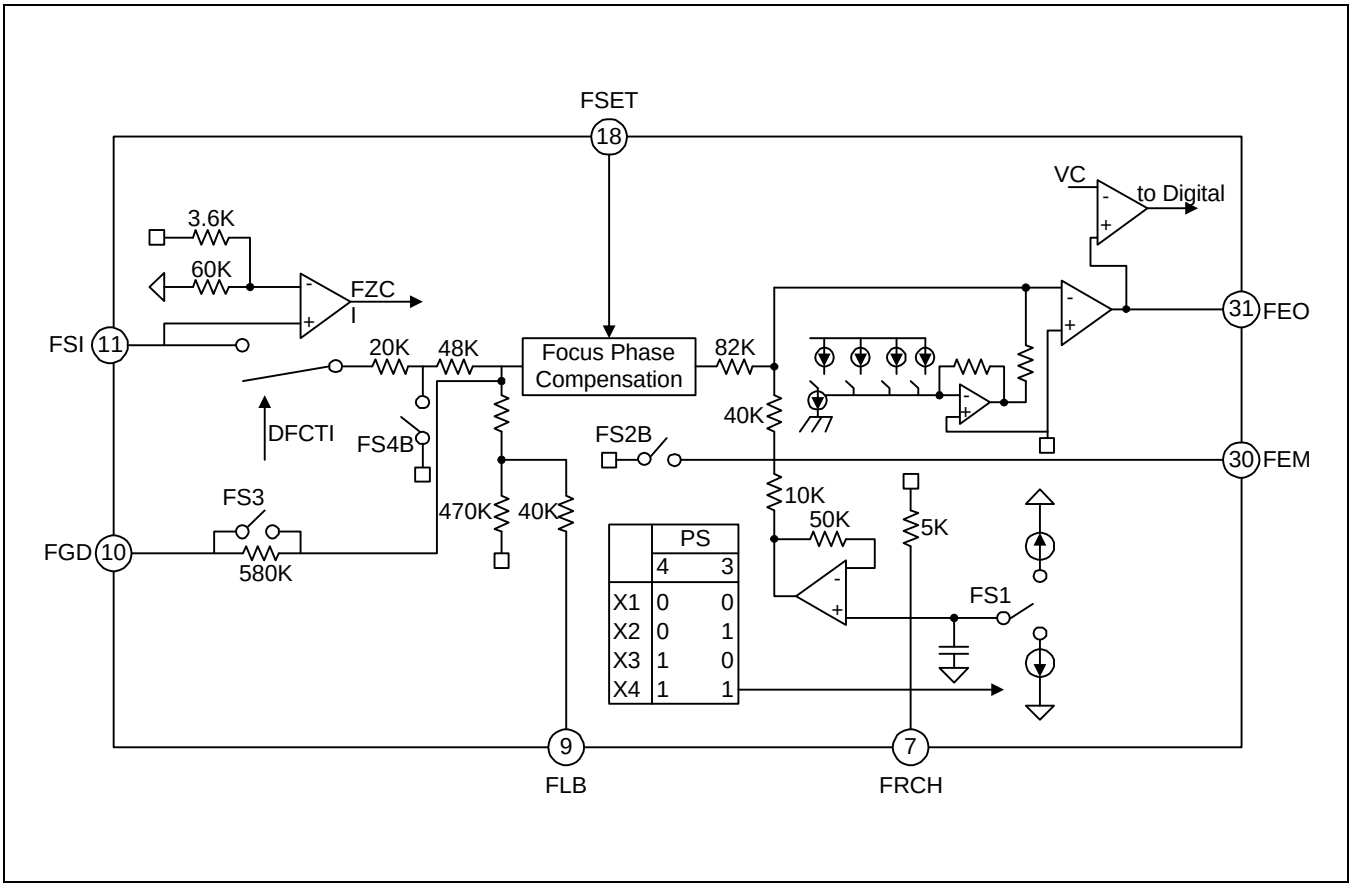
ATSC

The detection circuit for shock tracking gain up is composed of the window comparator.



Focus Servo

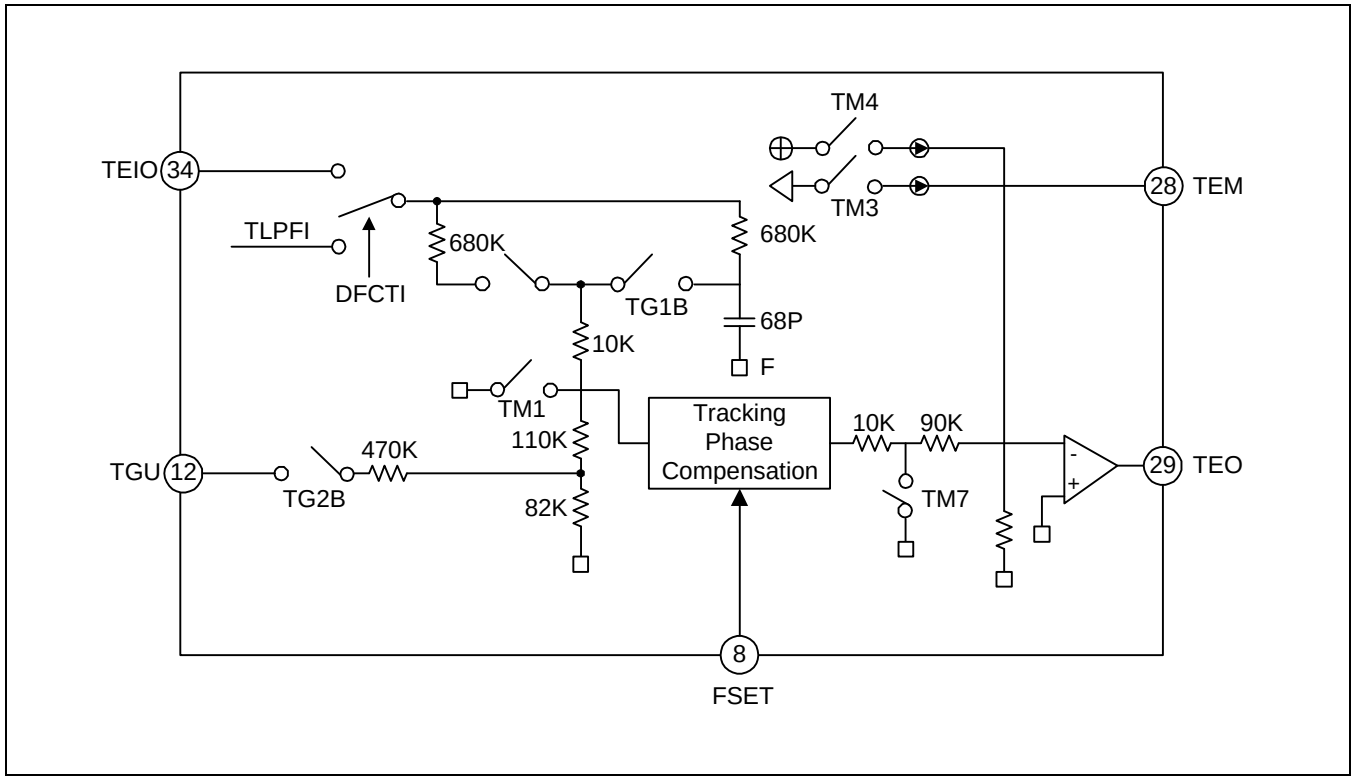
If the focus servo loop phase has been compensated, the focus servo loop mutts if the defect is. The focus error signal at this time is differentiated by the 0.1uF capacitor to be connected to the terminal and the 470kohms resistance and is output es through the servo loop. Therefore, the focus output is held to value before the defect error during defect. The FSET terminal changes the at which the focus loop compensation is at its maximum.
If the resistance to VDDA connected to the terminal, the phase compensation frequency is changed 1.2kHz below, and GND connected to the terminal, the frequency is changed 1.2kHz above.
During focus search, Fs4 turns on to cutoff the error signal and to output the focus search signal through the FEO. When the focus is on, FS2 turns on, and the focus error signal input through the FSI is output through the loop to the output pin.



Tracking Servo

The tracking servo phase compensate the tracking servo loop and differentiates the tracking error signal, after which it outputs the signal through the servo loop. TGU exchanges the tracking gain up/down time constant.

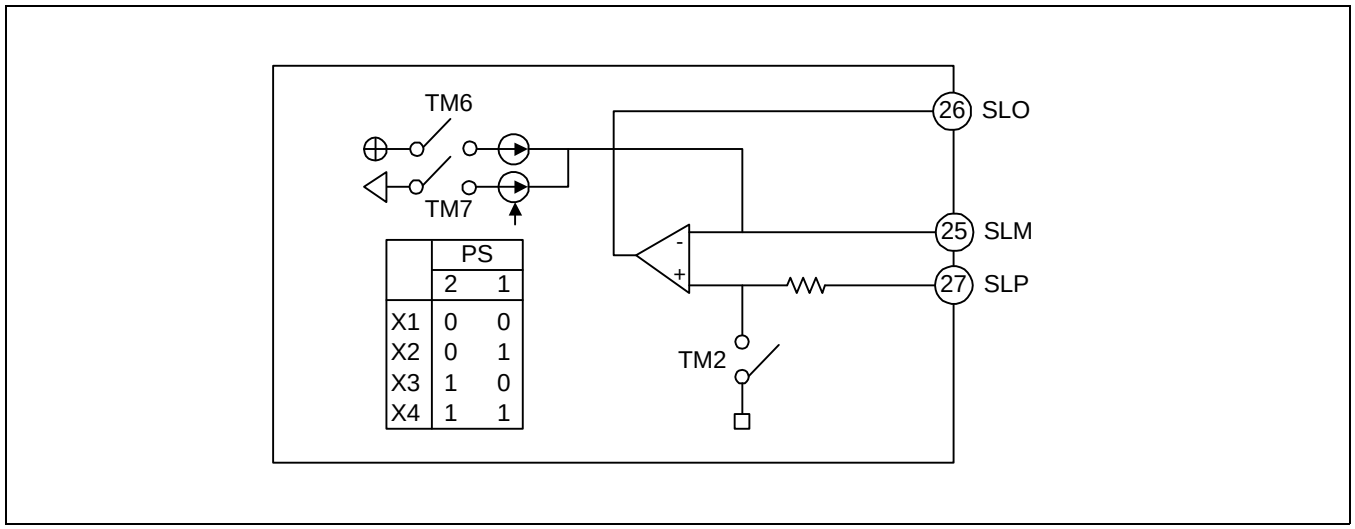
As in the focus loop, the phase compensation peak frequency is varied by the Fset terminal. If the resistance connected to the FSET terminal changes, the OP Amp dynamic range offeset changes also.



The TM7 switch is a brake switch which turns the tracking loop on/off when the actuator is unstable after a jump. After the servo jumps 10 tracks, the servo circuit leaves the linear range and the actuator sometimes pursues the unstable track, preventing unnecessary jumps from undesired tracking errors. As the terminal which controls the tracking servo loop's high frequency gain, the Tgu terminal controls the desired frequency range of the gain through the external cap.

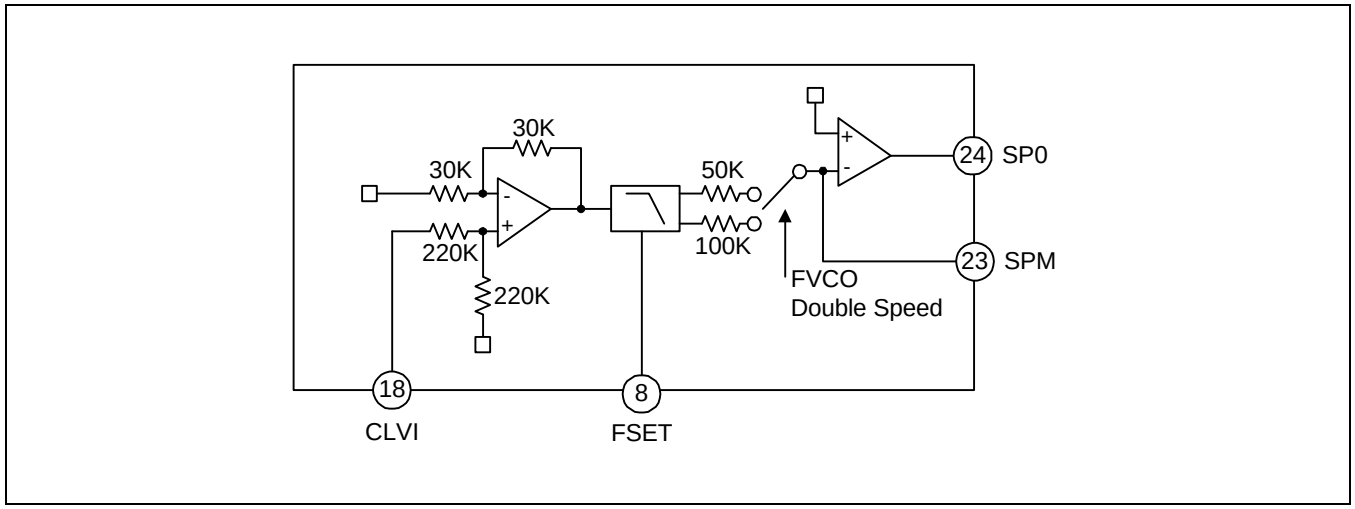
Sled Servo

This servo differentiates the tracking servo and moves the pick-up. It also outputs the sled kick voltage to make a track jump in the sled axis during track movement.



Spindle Servo & Low Pass Filter

The 200Hz LPF, composed of an external 20kohms resistance and 0.33uF cap, eliminiates the high frequency carrier component.



Mirror & Cpeak Mute (use only for tracking mute)

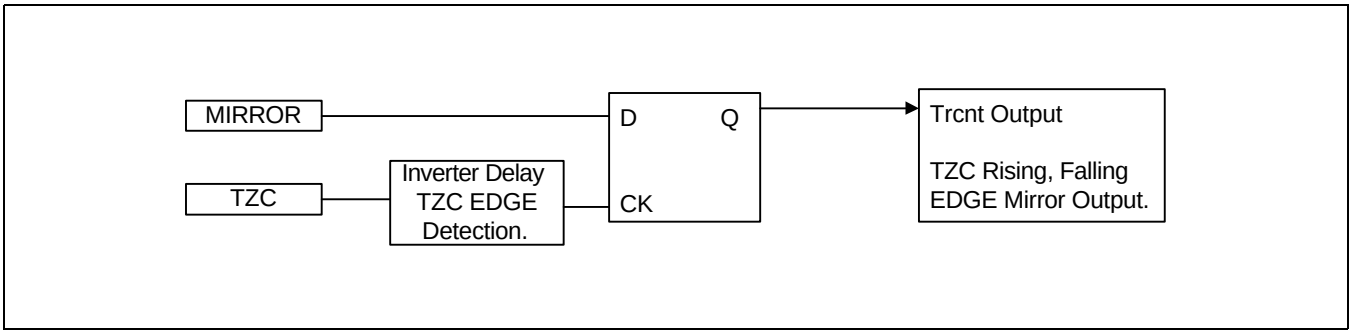
Used against ABEX-725A, this circuit processes the tracking mutting when mirror is detected.
(No recommend) the tracking mutting when EFM duty is above 22T after it is checked.

Mute does not operate in the following four cases.

- Micom tracking gain up command transmission (TG1, TG2 = 1)
- Anti-shock detection (ATSC)
- Lock falls to L
- Defect detection

TRCNT Output

TRCNT is output of mirror and TZC.
Mirror is the track movement detection output of the main beam; TZC is the track movement detection output of the side beam. TRCNT receives these two inputs to determine whether the present pick-up is moving from the inside to the outside or from the outside to the inside. It is used at $17 tracking brake operation.



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