

- Contains Eight Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

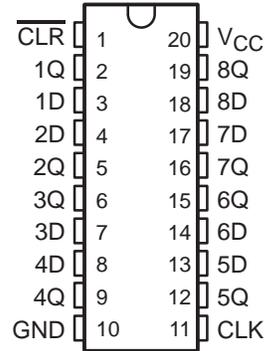
**description**

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

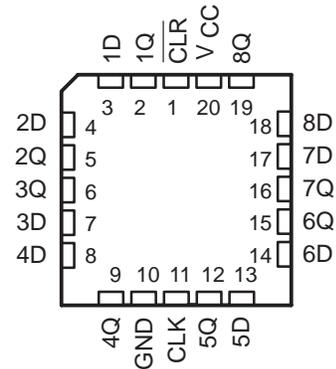
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

SN54273, SN74LS273 . . . J OR W PACKAGE  
SN74273 . . . N PACKAGE  
SN74LS273 . . . DW OR N PACKAGE  
(TOP VIEW)



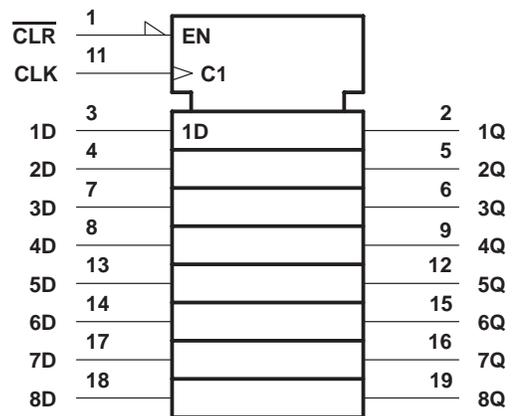
SN54LS273 . . . FK PACKAGE  
(TOP VIEW)



**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT Q
CLEAR	CLOCK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

**logic symbol†**

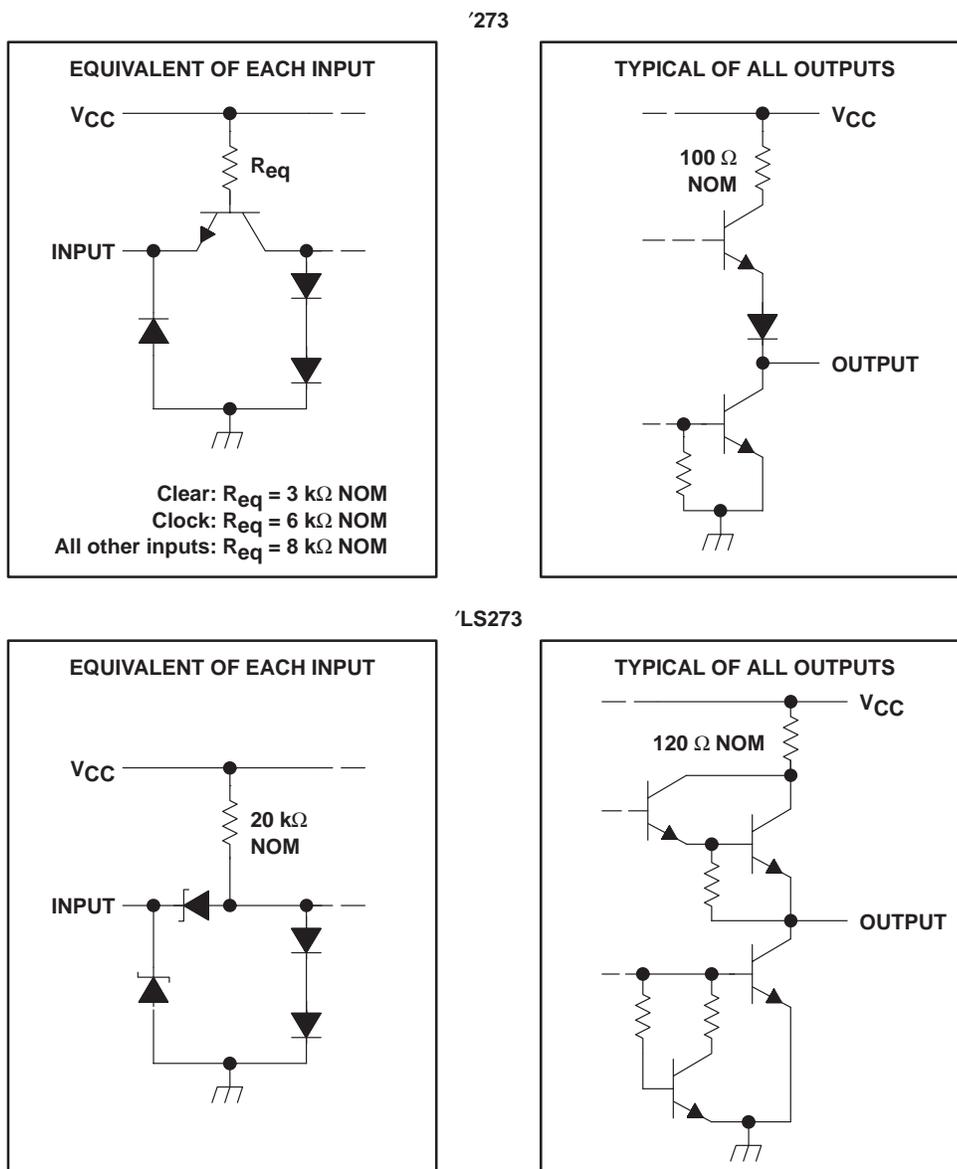


† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, J, N, and W packages.

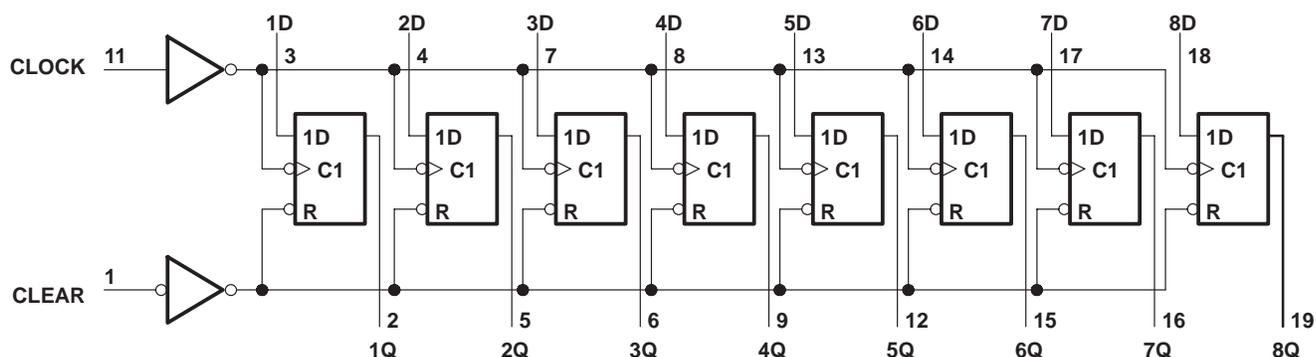
# SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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## schematics of inputs and outputs



## logic diagram (positive logic)



Pin numbers shown are for the DW, J, N, and W packages.



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# SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage . . . . .	5.5 V
Operating free-air temperature range, $T_A$ : SN54273 .....	-55°C to 125°C
SN74273 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54273			SN74273			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Clock frequency, $f_{clock}$	0		30	0		30	MHz
Width of clock or clear pulse, $t_w$	16.5			16.5			ns
Setup time, $t_{su}$	Data input		20 $\uparrow$	Data input		20 $\uparrow$	ns
	Clear inactive state		25 $\uparrow$	Clear inactive state		25 $\uparrow$	
Data hold time, $t_h$	5 $\uparrow$			5 $\uparrow$			ns
Operating free-air temperature, $T_A$	-55		125	0		70	°C

$\uparrow$  The arrow indicates that the rising edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS $\dagger$	MIN	TYP $\ddagger$	MAX	UNIT
$V_{IH}$	High-level input voltage		2			V
$V_{IL}$	Low-level input voltage				0.8	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = 16 \text{ mA}$			0.4	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	Clear			80	$\mu$ A
		Clock or D	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		40	
$I_{IL}$	Low-level input current	Clear	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$		-3.2	mA
		Clock or D			-1.6	
$I_{OS}$	Short-circuit output current $\S$	$V_{CC} = \text{MAX}$	-18		-57	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ , See Note 2		62	94	mA

$\dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

$\ddagger$  All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

$\S$  Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to clock.

# SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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## switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$	Maximum clock frequency	$C_L = 15\text{ pF}$ , $R_L = 400\ \Omega$ , See Note 3	30	40		MHz
$t_{PHL}$	Propagation delay time, high-to-low-level output from clear			18	27	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from clock			17	27	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range, $T_A$ : SN54LS273	$-55^\circ\text{C}$ to $125^\circ\text{C}$
SN74LS273	$0^\circ\text{C}$ to $70^\circ\text{C}$
Storage temperature range	$-65^\circ\text{C}$ to $150^\circ\text{C}$

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54LS273			SN74LS273			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu\text{A}$
Low-level output current, $I_{OL}$			4			8	mA
Clock frequency, $f_{\text{clock}}$	0		30	0		30	MHz
Width of clock or clear pulse, $t_w$	20			20			ns
Setup time, $t_{su}$	Data input			20 $\uparrow$			ns
	Clear inactive state			25 $\uparrow$			
Data hold time, $t_h$	5 $\uparrow$			5 $\uparrow$			ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^\circ\text{C}$

$\uparrow$  The arrow indicates that the rising edge of the clock pulse is used for reference.

# SN54273, SN54LS273, SN74273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONST	SN54LS273			SN74LS273			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.7			0.8	V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OH</sub> = -400 μA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
					0.35	0.5		
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX	-20		-100	-20		-100	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 2		17	27		17	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I<sub>CC</sub> is measured after a momentary ground, then 4.5 V, is applied to clock.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub> Maximum clock frequency	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 3	30	40		MHz
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from clear			18	27	ns
t <sub>PLH</sub> Propagation delay time, low-to-high-level output from clock			17	27	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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