1 PRODUCT OVERVIEW

1.1 OVERVIEW

Samsung's S3C2510A 16/32-bit RISC micro-controller is a cost-effective, high-performance micro-controller solution for Ethernet-based systems, for example, SOHO router, internet gateway, WLAN AP, etc.

To efficiently support those network applications, S3C2510A provides the followings: 16/32-bit ARM940T RISC embedded with 4K-byte I-cache and 4K-byte D-cache, memory controller with 24-bit external address pins, one external bus master with bus request/acknowledge pins, two 10/100 Mbps Ethernet controllers, PCI & PC Card host/agent controller, AAL5 SAR and UTOPIA L1/L2, two port full/low speed USB host with root hub, one port USB function device with transceiver, six general-purpose DMAs, two high-speed UARTs, one console UART, DES and 3DES for IP security, IIC serial interface, interrupt controller, six 32-bit programmable timers, 30-bit watchdog timer, 64 programmable I/O ports, and four PLLs for clock generation.

The S3C2510A is developed using an ARM940T core, 0.18um CMOS standard cells and a memory compiler. Its powerful, elegant and fully static design is suitable for various network applications. Also S3C2510A adopts a new bus architecture, AMBA (Advanced Microcontroller Bus Architecture).

1.2 FEATURES

The following integrated on-chip functions are described in detail in this user's manual:

- 16/32-bit ARM940T RISC Embedded
- 4K-byte I-Cache and 4K-byte D-Cache
- Memory Controller with 24-bit External Address Pins
  - — 2 Banks of SDRAM for 16/32-bit Bus
  - — 8 Banks of Flash/ROM/SRAM/External I/O for 8/16/32-bit Bus
  - — One External Bus Master with Bus Request/Acknowledge Pins
- Two 10/100 Mbps Ethernet Controllers
- PCI Host/Agent Controller or CardBus (PCMCIA) Host/Agent Controller
  - — PCI Host mode: 5 (or more) PCI Slots Interface for PCI Cards
  - — PC Card Host mode: 1 PC Card Socket Interface for 16-bit PC Card or CardBus PC Card
- AAL5 SAR and UTOPIA L1/L2
- 2 Port Full/Low Speed USB HOST with Root Hub.
- 1 Port Full Speed USB Function with Transceiver Spec. 1.1
- Six General-Purpose DMAs
- Two High-Speed UARTs
- One Console UART
- DES and 3DES for IP Security
- IIC Serial Interface
- Interrupt Controller
- Six 32-bit Programmable Timers
- 30-bit Watchdog Timer
- 64 Programmable I/O Ports
  - — 8 General-Purpose I/O
  - — 6 External Interrupt Request
  - — 6 Timer Output
  - — 4 External DMA Request
  - — 4 External DMA Acknowledge
  - — 21 SAR Signals
  - — 15 UART Signals
- Four PLLs for each ARM940T (166MHz), System (133MHz), PCI & PC Card Controller Clock (33/66MHz), USB Host/Device Clock (48MHz), and Ethernet PHY (20/25MHz).
- CPU Operating Frequency: Up to 166MHz
- AHB Bus Operating Frequency: Up to 133MHz
- Package Type: 416 PBGA
- Core Operating at 1.8V ±5 %, -40~85 ^{o}C
- I/O Operating at 3.3V ±5 %, -40~85 ^{o}C
- 3.3V input/output levels, 5V tolerant only for PCI.

1.3 BLOCK DIAGRAM

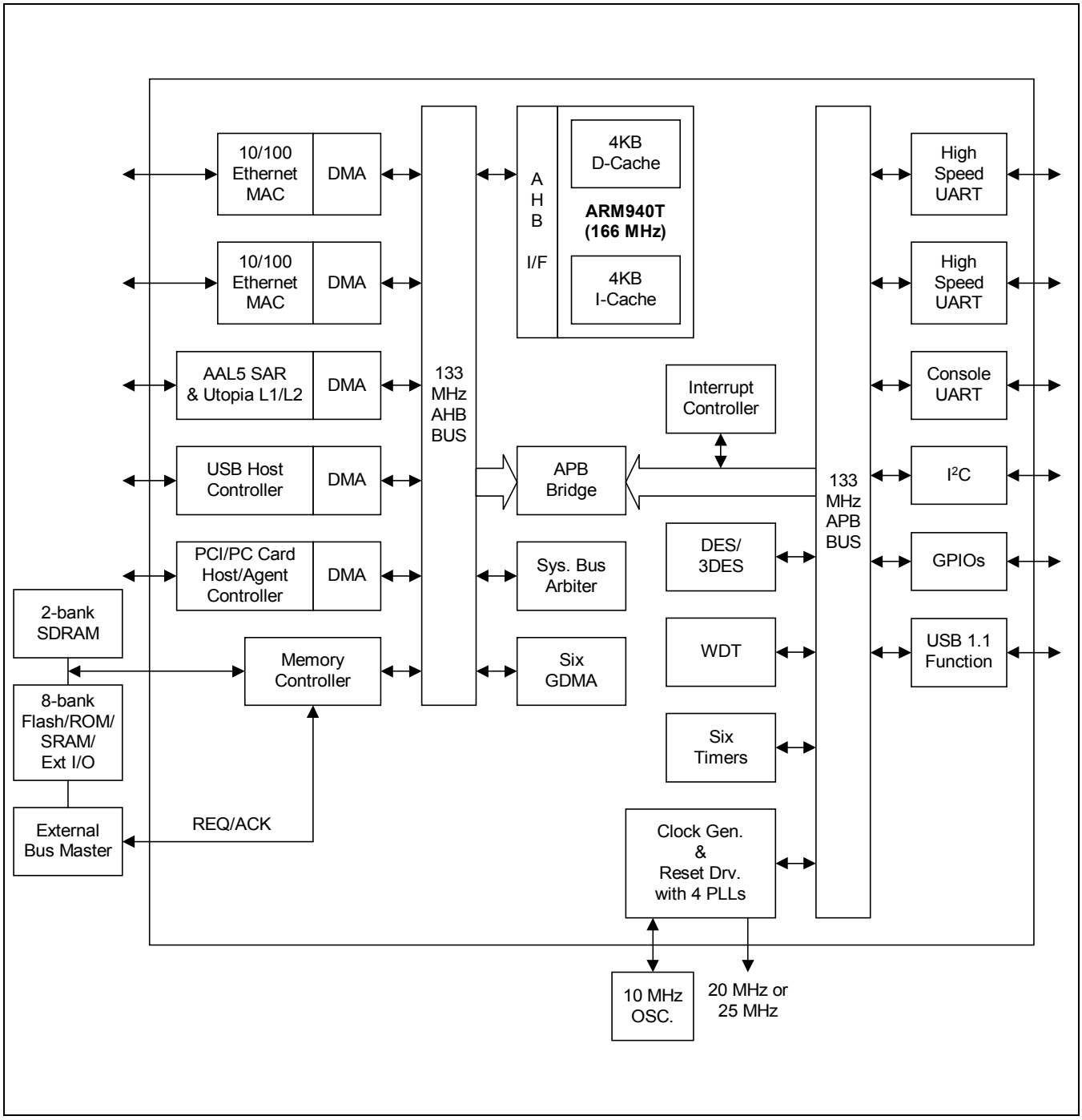


Figure 1-1. Block Diagram

ARM940T

The ARM940T cached processor is a member of the ARM9 Thumb family of high-performance 32-bit system-on-a-chip processor solutions. It provides a complete high performance CPU subsystem, including ARM9TDMI RISC integer CPU, 4KB instruction/data caches, write buffer, and protection unit, with an AMBA bus interface. The ARM9TDMI core within the ARM940T executes both the 32-bit ARM and 16-bit Thumb instruction sets, allowing the user to trade off between high performance and high code density. It is binary compatible with ARM7TDMI, ARM10TDMI, and StrongARM processors, and is supported by a wide range of tools, operating systems, and application software.

Memory organization

Memory system is composed of 8 ROM/SRAM/Flash/Ext I/O banks and 2 SDRAM banks. Each ROM bank is fixed with 16M-byte address range and is supported with multiplexed and non-multiplexed address/data bus capability. Each SDRAM bank is supported with 128 MByte.

Two Ethernet Controllers

The S3C2510A includes two Ethernet controllers, which enables the user to configure SOHO router, internet gateway, etc. The main features are as follows.

— Buffered DMA (BDMA) engine using burst mode
— BDMA Tx/Rx buffers (256-byte/256-byte)
— MAC Tx/Rx FIFOs (80-byte/16-byte) to support re-transmit after collision without DMA request
— Data alignment logic
— Support for old and new media (compatible with existing 10M-bit/s networks)
— 10/100 Mbps operation to increase price/performance options and to support phased conversions
— Full IEEE 802.3 compatibility for existing applications
— Media Independent interface (MII) or 7-wire interface
— Station management (STA) signaling for external physical layer configuration and link negotiation
— On-chip CAM (21 addresses)
— Full-duplex mode for doubled bandwidth
— Pause operation hardware support for full-duplex flow control
— Long packet mode for specialized environments
— Short packet mode for fast testing
— PAD generation for ease of processing and reduced processing time

PCI & PC Card Host/Agent Controller

S3C2510A's PCI & PC Card Host/Agent Controller complies with the PCI Local Bus Specification rev. 2.2, PC Card Standard Release 7.2, and various design guides. PCI & PC Card Controller connects the ARM940T processor core and local system memory to the PCI bus or CardBus socket. The PCI bus or CardBus uses a 32-bit multiplexed, address/data bus, and various control and error signals. Mis-aligned transfers are supported as well as burst transfers at the maximum data rate of 264MB/s @66MHz (132MB/s @33MHz). S3C2510A can function as a PCI(or CardBus) master(initiator) or target(slave), and function as PCI host bridge(or CardBus host bus adapter) referred to as "host mode" or PCI device(or CardBus PC Card) referred to as "agent mode". In host mode, it can be used as host/PCI bridge (or CardBus socket controller) on main board . But in agent mode, it can be used as PCI device on PCI card or CardBus device on CardBus PC Card. The PCI & PC Card Host Controller provides PCI bus arbitration for the S3C2510A and up to five other PCI bus masters (except PCI target-only devices). It can be disabled to allow for external PCI arbiter (if more than five PCI bus masters will be connected).

The PCI & PC Card Host Controller has one integrated block for PCI interface and CardBus interface (common silicon) and it supports only one interface as defined by PCI_PCCDM(PC Card Mode) pin. And PCI_HOSTM pin signal forces PCI & PC Card Controller to operate in host mode or agent mode. Each modes can be set as followings.

PCI Host Mode	PCI_PCCDM = 0, PCI_HOSTM=1
PCI Agent Mode	PCI_PCCDM = 0, PCI_HOSTM=0
CardBus PC Card Host Mode	PCI_PCCDM = 1, PCI_HOSTM=1, CardBus PC Card is inserted
16-bit PC Card (PCMCIA) Host Mode	PCI_PCCDM = 1, PCI_HOSTM=1, 16-bit PC Card is inserted
CardBus PC Card Agent Mode	PCI_PCCDM = 1, PCI_HOSTM=0

NOTE: Each mode is selected by PCI_PCCDM & PCI_HOSTM pin input and inserted card type

The PCI & PC Card Host/Agent Controller provides an address translation mechanism to map inbound PCI to local memory or peripherals and outbound processor core or peripherals to PCI. Four independent 8-word deep FIFOs are implemented for flow-through operation of PCI & PC Card read/write burst operation. And doorbell and mailbox registers, CLKRUN# central resource control logic, integrated pull-up resistors are also implemented.

As a CardBus host mode, it supports only single PC Card slot and generates interface signals to PC Card power-switch. CardBus Host Controller supports 16-bit PC Card (PCMCIA card) or CardBus PC Card. CardBus Host Controller provides an address translation mechanism to map inbound PCI to local memory or peripherals and outbound processor core or peripherals to PCI. Four independent 8-word deep FIFOs are implemented.

As a PCI/CardBus agent mode, it supports independent three address decoders and provides address translation mechanism to map AHB local memory from PCI bus through three address bars and vice-versa. To support power management, it complies with PCI Bus Power Management Interface Specification Rev. 1.1 and PCI Mobile Design Guide Ver. 1.1. And also it supports DMA operation with two-channel dedicated DMA to enhance the performance.

PCI Host/Agent Controller Features are as Follows

— 32-bit, 33/66 MHz, 5V tolerant, Up to 264M-byte/sec @66MHz
— PCI Local Bus Specification Rev.2.2 compliant
— PCI Bus Power Management Interface Specification Rev.1.1 compliant
— PCI Mobile Design Guide Ver.1.1 compliant
— Mini PCI Specification Rev.1.0 compliant
— Advanced Configuration and Power Interface (ACPI) Specification Rev.2.0 compliant
— Supports PCI PME# pin and wake-up by software
— Round-robin PCI bus arbiter supports five external REQ#, GNT# pins
— Two-channel dedicated DMA
— Integrated pull-up resistors

CardBus PC Card Host/Agent Controller Features (Common Silicon with PCI) are as Follows

— 32-bit, 33 MHz, 3.3V, Up to 132M-byte/sec
— PC Card Standard Release 7.1 compliant
— PCI Bus Power Management Interface Specification Rev.1.1 compliant
— PCI Mobile Design Guide Ver.1.1 compliant
— Advanced Configuration and Power Interface (ACPI) Specification Rev.2.0 compliant
— Single PC Card slot interface with hot insertion and removal
— Interface to 16-bit PC Card (PCMCIA card) or CardBus PC Card
— Interface to PC Card power-switch like TI™ TPS2211A and MAXIM™ MAX1602
— Integrated slew-rate controlled buffers for the difference between PCI and CardBus
— Advanced filtering on card detect lines provide 60 microseconds of noise immunity
— Supports CardBus CSTSCHG pin and Socket Event (Status Changed registers) registers
— Two-channel dedicated DMA
— Integrated pull-up resistors
— Common memory, attribute memory and I/O interface supported for 16-bit PC Card

16-bit PC Card Host Controller Features (Common Silicon with PCI) are as Follows

— PC Card Standard Release 7.1 compliant
— Advanced filtering on card detect lines provide 60 microseconds of noise immunity
— Two-channel dedicated DMA

AAL5 SAR and UTOPIA L1/L2

The S3C2510A SAR is a powerful, cost-effective solution for providing packet-to-ATM connectivity. Once a data packet is given to the S3C2510A SAR, the packet is translated into cells using either the AAL5 protocol or the null AAL protocol. Then, without further host intervention, the cells are transmitted using selected scheduling algorithms. The host is notified upon completion of the packet transmission. The S3C2510A SAR also receives cells from the PHY devices, reassembles them into packets, and notifies the host when a packet has arrived.

All packets are queued in system memory. Misaligned transfers are supported for ease of implementing LANE and MPOA protocols without requiring any packet data movement. VP scheduling is supported, as well as the more common VC scheduling, allowing a mix of Permanent Virtual Path (PVP), Switched Virtual Path (SVP), Permanent Virtual Channel (PVC), and Switched Virtual Channel (SVC) connections.

Some key features are as follow:

— CBR, UBR, rt-VBR and nrt-VBR traffic with rates set on a per-VC or per-VP basis

— AAL0 (raw cells) and AAL5 segmentation and reassembly

— Segments and reassembles data up to about 70Mbps via UTOPIA interface

— Generates and verifies CRC-10 for OAM cells and AAL-3/4 cells

— Concurrent OAM cells and AAL5 cells on each active connection

— Simultaneous segmentation and reassembly of up to 32 connection with internal memory and up to 4K connection with external memory

— On chip 8K-byte SRAM for internal connection memory

— CAM for connection number mapping (up to 32 connections)

— Packet sizes up to 64K-byte

— Scatter and gather packet capability for large packets

— Starts of Packet offset available for ease of implementing bridging and routing between different protocols

— Big/little endian mode for packet payload

— Glue-less UTOPIA level 2 interface (up to 7 PHYs).

USB Host Controller

S3C2510A supports 2 port USB host interface as follows; Open HCI Rev 1.0 compatible, USB Rev1.1 compatible, 2 down stream ports. Support for Full/Low Speed USB devices. The S3C2510A USB Host controller complies with OPEN HCI Rev 1.0. Please refer to Open Host Controller Interface Rev 1.0 specification for detail information. The main features are as follows

— USB specification 1.0 compliant

— Full/Low speed operation support.

— Root hub built in with 2 downstream ports.

Universal Serial Bus (USB) Function Device

The S3C2510A includes a USB controller that enables the customers to implement USB devices for telephony, audio, and other applications. The USB controller is intended for the full-speed signaling rate of 12Mbit/s. Additionally, the S3C2510A USB controller has following features:

— A total of 5 endpoints: 1 control endpoint and 4 data endpoints that can support control, interrupt, bulk transaction.

— Two data endpoints have 32-byte FIFO, two data endpoints have 64-byte FIFO.

— General DMA supported

Universal Asynchronous Receiver Transmitter (UART)

The S3C2510A has one console-UART and two high-speed UART. Consol UART can be used as system configuration or debug port. Each high-speed UART can be used as modem interface or other high-speed applications.

The most important features of high-speed UART are as follows

— Programmable baud rates

— 32-byte Transmit FIFO and 32-byte Receive FIFO

— UART source clock selectable (Internal clock: MCLK2, External clock : EUCLK)

— Auto baud rate detection

— Infra-red (IR) transmit/receive

— Insertion of one or two Stop bits per frame

— Selectable 5-bit, 6-bit, 7-bit, or 8-bit data transfers

— Parity checking

DES/3DES Accelerator

The DES Accelerator is a hardware accelerator for execution of the Data Encryption Standard(DES) algorithms as defined in FIPS PUB 46-1, which is equivalent to the Data Encryption Algorithm(DEA) provided in ANSI x3.92-1981. The main features are as follows

— DES or Triple DES mode

— ECB or CBC mode

— Encryption or decryption support

— General DMA support

Six General DMA Channels

The S3C2510A has six general DMA channels, which can be used for data transfer between memory and peripherals (memory to peripherals, peripherals to memory) or within memory space (memory to memory). On-chip peripherals with general DMA service are the two high-speed UART, the DES and the USB controller. General DMA can also support four external DMA requests from DMA request pins (xGDMA_Req0 – xGDMA_Req3). General DMA can also support the programmable cycle counts of the external DMA acknowledge signals (xGDMA_Ack0 – xGDMA_Ack3).

Six Programmable Timer

The S3C2510A has six programmable timers. Each timer has its related pin, which is shared with programmable I/O function. Each timer can be programmed two operation mode. One is interval mode and the other is toggle mode. In interval mode, the initial timer output is set to low and it is set to high for 1 cycle time when timeout is reached. therefore the timer output is shaped like pulse wave. In toggle mode, the timer output is toggled when timeout is reached.

Hardware Watchdog Timer

The S3C2510A includes a watchdog timer, which is capable of generating system reset when the timeout value is reached. The time value is ranged up to 2^30 system clock cycles. The watchdog timer is used to reset and restart the system when a system has failed due to software error or to wrong response of external device.

Programmable Interrupt Controller

The S3C2510A has one programmable interrupt controller, which arranges the 36 programmable interrupt sources by the programmable priority. The interrupt controller supports 36 maskable interrupt sources, where 30 interrupts are from internal interrupts and 6 interrupts are from external interrupts. The interrupt with the highest priority is reported to the CPU.

Programmable I/O Port Controller

The S3C2510A has 64 programmable I/O ports, which can be used for another function. If another function is enabled, its I/O functionality is disabled. Six external interrupt request, four external DMA request, four external DMA acknowledge, six timer outputs, 21 SAR signals, and 15 UART signals are multiplexed with I/O function. Each I/O port can be programmed as Input or Output.

I^2C Controller

The S3C2510A has IIC controller, which enables the customer to implement a simple and cost effective inter-IC connection. The IIC bus is a two-wire synchronous serial interface consisting of one data (SDA) and one clock (SCL) line. The S3C2510A IIC controller operates in only single master mode.

1.4 S3C2510A PIN LIST AND PAD TYPE

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
System Configurations (21)	XCLK	T3	I	phic	S3C2510A PLL Clock Source. If CLKSEL is Low, PLL output clock is used as the system clock. If CLKSEL is high, XCLK is used as the system clock.
	HCLKO	M23	O	phbst24	System clock output. The internal system clock is monitored via HCLKO. If SDRAM is used, this clock should be used SDRAM clock
	CLKSEL	U1	I	phic	Clock Select for CPU PLL. If CLKSEL is low, CPU PLL clock is used as ARM940T source clock. If high, XCLK (External clock) is used.
	FILTER	R2	AO	poar50_abb	PLL filter pin for System PLL. If the PLL is used, 320pF capacitor should be connected between the pin and ground.
	PHY_FREQ	Y2	I	phic	PHY clock frequency select for PHY PLL. 0 = 20MHz 1 = 25MHz
	PHY_CLKSEL	U3	I	phic	Clock Select for PHY PLL If this pin is set to Low, the PHY PLL generates clock depending on PHY_FREQ state. The PHY PLL goes into power down mode with PHY_CLKSEL set to High.
	PHY_FILTER	T2	AO	poar50_abb	PLL filter pin for PHY PLL. If the PLL is used, 320pF capacitor should be connected between the pin and ground.
	PHY_CLKO	AD12	O	phob8	PHY clock Out PHY PLL clock output can be monitored by PHY_CLKO. This clock is used as the external PHY source clock.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
System Configurations (21)	CLKMOD[1] CLKMOD[0]	AB4 AC2	I	phic	The CLKMOD pin determines internal clock scheme of S3C2510A. When CLKMOD is “00”, the nfast clock mode is defined. In this mode, the same clock is used as CPU clock and system clock. When CLKMOD is “01” or “10”, the sync mode is defined. In this mode, the system clock is half frequency of the CPU clock. When CLKMOD is "11", the async clock mode is defined. In this mode, the CPU clock and system clock can operate independently as long as the CPU clock is faster than system clock. In this case, BUS_FREQ[2:0] pins should be 3b’000 to select PCI PLL, 3b’001 to select USB PLL for programmable setting.
	CPU_FREQ[2] CPU_FREQ[1] CPU_FREQ[0]	AE1 AD1 AC3	I	phic	CPU Clock Frequency Selection.
	BUS_FREQ[2] BUS_FREQ[1] BUS_FREQ[0]	AD2 AB3 AC1	I	phic	System Bus Clock Frequency Selection.
	nRESET	AB2	I	phis	Not Reset. NRESET is the global reset input for the S3C2510A and nRESET must be held to "low" for at least 64 clock cycles for digital filtering.
	TMODE	AF3	I	phicd	Test Mode. The TMODE pin setting is interpreted as follows: 0 = normal operating mode 1 = chip test mode.
	BIG	W3	I	phicd	BIG endian mode select pin. When this pin is set to “0”, the S3C2510A operates in litte endian mode. When this pin is set to “1”, the S3C2510A operates in big endian mode.
	PCI_PCCDM	AA2	I	phic	PCI(1'b0) or PC Card(1'b1) Mode Select of PCI & PC Card Controller
	PCI_HOSTM	Y3	I	phic	Host (1'b1) or Agent (1'b0) Mode Select of PCI & PC Card Controller

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Memory Interface (80)	ADDR[23:0] ADDR[10]	B14	O	phot20	Address bus. The 24-bit address bus covers the full 16 M word address range of each ROM/SRAM /FLASH and external I/O bank. In the SDRAM interface, ADDR[14:13] is always used as bank address of SDRAM devices. If SDRAM devices with 2 internal bank is used, ADDR[13] should be connected to the BA of SDRAM. If SDRAM devices with 4 internal bank is used, ADDR[14:13] should be connected to the BA[1:0] of SDRAM. ADDR[10]/AP is the auto precharge control pin. The auto precharge command is issued at the same time as burst read or burst write by asserting high on ADDR[10]/AP.
	XDATA[31:0]		B	phbsut20	External bi-directional 32bit data bus. The S3C2510A supports 8 bit, 16bit, 32bit bus with ROM/SRAM/Flash/Ext IO bank, but supports 16 bit or 32 bit bus with SDRAM bank.
	nSDCS[1] nSDCS[0]	G24 F26	O	phot20	Not chip select strobe for SDRAM. Two SDRAM banks are supported.
	nSDRAS	E25	O	phot20	Not row address strobe for SDRAM. NSDRAS signal is used for both SDRAM banks.
	nSDCAS	E26	O	phot20	Not column address strobe for SDRAM. NSDCAS signal is used for both SDRAM banks.
	CKE	L24	O	phob12	Clock Enable for SDRAM CKE is clock enable signal for SDRAM.
	nSDWE/nWE16	F23	O	phot20	Not Write Enable for SDRAM or 16 bit ROM/SRAM. This signal is always used as write enable of SDRAM and is used as write enable of only 16-bit ROM/SRAM/Flash. (That is, It is not enabled for 8 bit Memory)

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Memory Interface (80)	nEWAIT	K25	I	phicu	Not External wait signal. This signal is activated when an external I/O device or ROM/SRAM/Flash banks need more access cycles than those defined in the corresponding control register.
	nMCS[7] nMCS[6] nMCS[5] nMCS[4] nMCS[3] nMCS[2] nMCS[1] nMCS[0]	J24 H26 H25 J26 K24 J25 K23 K26	O	phot20	Not ROM/SRAM/Flash/ External I/O Chip select. The S3C2510A supports upt to 8 banks of ROM/SRAM/Flash/ External I/O. By controlling the nRCS signals, you can map CPU address into the physical memory banks.
	B0SIZE[1] B0SIZE[0]	AE3 AF2	I	phic	Bank 0 Data Bus Access Size. Bank0 is used for the boot program. You use these pins to set the size of the bank 0 data bus as follows: “01” = Byte, “10” = Half word, “11” = Word, and “00” = reserved.
	nOE	G25	O	phot20	Not output enable. Whenever a memory read access occurs, the nOE output controls the output enable port of the specific memory device.
	nWBE[3]/nBE/ DQM[3] nWBE[2]/nBE/ DQM[2] nWBE[1]/nBE/ DQM[1] nWBE[0]/nBE/ DQM[0]	F25 H24 G26 H23	O	phot20	Not write byte enable or DQM for SDRAM Whenever a memory write access occurs, the nWBE output controls the write enable port of the specific memory device. DQM is data input/output mask signal for SDRAM.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Memory Interface (80)	XBMREQ	M24	I	phicd	External Bus Master request. An external bus master uses this pin to request the external bus. When it activates the XBMREQ, the S3C2510A drives the state of external bus pins to high impedance. This lets the external bus master take control of the external bus. When it has control, the external bus master assumes responsibity for SDRAM refresh operation. The XBMREQ is deactivated when the external bus master releases the external bus. When this occurs, the S3C2510A can get the control of the bus and the XBMACK goes “low”.
	XBMACK	L26	O	phob8	External bus Acknowledge.
TAP Control (5)	TCK	AC5	I	phic	JTAG Test Clock. The JTAG test clock shifts state information and test data into, and out of, the S3C2510A during JTAG test operations.
	TMS	AE4	I	phicu	JTAG Test Mode Select. This pin controls JTAG test operations in the S3C2510A. This pin is internally connected pull-up.
	TDI	AF4	I	phicu	JTAG Test Data In. The TDI level is used to serially shift test data and instructions into the S3C2510A during JTAG test operations. This pin is internally connected pull-up.
	TDO	AD4	O	phot12	JTAG Test Data Out. The TDO level is used to serially shift test data and instructions out of the S3C2510A during JTAG test operations.
	nTRST	AE5	I	phicu	JTAG Not Reset. Asynchronous reset of the JTAG logic. This pin is internally connected pull-up.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Ethernet Controller (2)	MDC	B1	O	phob12	Management Data Clock. The signal level at the MDC pin is used as a timing reference for data transfers that are controlled by the MDIO signal.
	MDIO	C2	B	phbcut12	Management Data I/O. When a read command is being executed, data that is clocked out of the PHY is presented on this pin. When a write command is being executed, data that is clocked out of the controller is presented on this pin for the Physical Layer Entity, PHY.
Ethernet Controller0 (16)	COL_0	C1	I	phis	Collision Detected/Collision Detected for 10M. COL is asserted asynchronously with minimum delay from the start of a collision on the medium in MII mode. COL_10M is asserted when a 10-Mbit/s PHY detects a collision.
	TX_CLK_0	D2	I	phis	Transmit Clock/Transmit Clock for 10M. The controller drives TXD[3:0] and TX_EN from the rising edge of TX_CLK. In MII mode, the PHY samples TXD[3:0] and TX_EN on the rising edge of TX_CLK. For data transfers, TXCLK_10M is provided by the 10M-bit/s PHY.
	TXD0[3] TXD0[2] TXD0[1]/ LOOP_10M TXD0[0]/ TXD_10M	E4 E2 D1 D3	O	phob12	Transmit Data/Transmit Data for 10M. Transmit data is aligned on nibble boundaries. TXD[0] corresponds to the first bit to be transmitted on the physical medium, which is the LSB of the first byte and the fifth bit of that byte during the next clock. TXD_10M is shared with TXD[0] and is a data line for transmitting to the 10M-bit/s PHY. LOOP_10M is shared with TXD[1] and is driven by the loop-back bit in the control register.
	TX_EN_0	E3	O	phob4	Transmit Enable/Transmit Enable for 10M. TX_EN provides precise framing for the data carried on TXD[3:0]. This pin is active during the clock periods in which TXD[3:0] contains valid data to be transmitted from the preamble stage through CRC. When the controller is ready to transfer data, it asserts TXEN_10M.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Ethernet Controller0 (16)	TX_ERR_0/ PCOMP_10M	E1	O	phob4	Transmit Error/Packet Compression Enable for 10M. TX_ERR is driven synchronously to TX_CLK and sampled continuously by the Physical Layer Entity, PHY. If asserted for one or more TX_CLK periods, TX_ERR causes the PHY to emit one or more symbols which are not part of the valid data, or delimiter set located somewhere in the frame that is being transmitted. PCOMP_10M is asserted immediately after the packet's DA field is received. PCOMP_10M is used with the Management Bus of the DP83950 Repeater Interface Controller (from National Semiconductor). The MAC can be programmed to assert PCOMP if there is a CAM match, or if there is not a match. The RIC (Repeater Interface Controller) uses this signal to compress (shorten) the packet received for management purposes and to reduce memory usage. (See the DP83950 Data Sheet, published by National Semiconductor, for details on the RIC Management Bus.) This pin is controlled by a special register, with which you can define the polarity and assertion method (CAM match active or not match active) of the PCOMP signal.
	CRS_0	F2	I	phis	Carrier Sense/Carrier Sense for 10M. CRS is asserted asynchronously with minimum delay from the detection of a non-idle medium in MII mode. CRS_10M is asserted when a 10-Mbit/s PHY has data to transfer. A 10-Mbit/s transmission also uses this signal.
	RX_CLK_0	F4	I	phis	Receive Clock/Receive Clock for 10M. RX_CLK is a continuous clock signal. Its frequency is 25 MHz for 100-Mbit/s operation, and 2.5 MHz for 10-Mbit/s. RXD[3:0], RX_DV, and RX_ERR are driven by the PHY off the falling edge of RX_CLK, and sampled on the rising edge of RX_CLK. To receive data, the RXCLK_10 M clock comes from the 10Mbit/s PHY.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Ethernet Controller0 (16)	RXD0[3] RXD0[2] RXD0[1] RXD0[0]/ RXD_10M	G1 G2 F1 F3	I	phis	Receive Data/Receive Data for 10M. RXD is aligned on nibble boundaries. RXD[0] corresponds to the first bit received on the physical medium, which is the LSB of the byte in one clock period and the fifth bit of that byte in the next clock. RXD_10M is shared with RXD[0] and it is a line for receiving data from the 10M-bit/s PHY.
	RX_DV_0/ LINK_10M	G3	I	phis	Receive Data Valid. PHY asserts RX_DV synchronously, holding it active during the clock periods in which RXD[3:0] contains valid data received. PHY asserts RX_DV no later than the clock period when it places the first nibble of the start frame delimiter (SFD) on RXD[3:0]. If PHY asserts RX_DV prior to the first nibble of the SFD, then RXD[3:0] carries valid preamble symbols. LINK_10M is shared with RX_DV and used to convey the link status of the 10M-bit/s endec. The value is stored in a status register.
	RX_ERR_0	H2	I	phisd	Receive Error. PHY asserts RX_ERR synchronously whenever it detects a physical medium error (e.g., a coding violation). PHY asserts RX_ERR only when it asserts RX_DV.
Ethernet Controller1 (16)	COL_1	H4	I	phis	Collision Detected/Collision Detected for 10M.
	TX_CLK_1	H1	I	phis	Transmit Clock/Transmit Clock for 10M.
	TXD1[3] TXD1[2] TXD1[1]/ LOOP_10M TXD1[0]/ TXD_10M	K2 J1 J2 H3	O	phob12	Transmit Data/Transmit Data for 10M.
	TX_EN_1	J3	O	phob4	Transmit Enable/Transmit Enable for 10M.
	TX_ERR_1/ PCOMP_10M	K1	O	phob4	Transmit Error/Packet Compression Enable for 10M.
	CRS_1	K4	I	phis	Carrier Sense/Carrier Sense for 10M.
	RX_CLK_1	L2	I	phis	Receive Clock/Receive Clock for 10M.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
Ethernet Controller1 (16)	RXD1[3] RXD1[2] RXD1[1] RXD1[0]/ RXD_10M	M1 M2 L1 K3	I	phis	Receive Data/Receive Data for 10M.
	RX_DV_1/ LINK_10M	L3	I	phis	Receive Data Valid.
	RX_ERR_1	N2	I	phisd	Receive Error.
PCI & PC Card Controller – PCI Host Mode (65)	PCICLK1	AA23	O	phopcicb	PCI clock output signal 1
	PCICLK2	AE24	O	phopcicb	PCI clock output signal 2
	PCICLK3/ EXT_PCICLK	AD18	B	phtbpcicb	PCI clock output signal 3 or external PCI clock input
	PCIRST#/ EXT_PCIRST#	AE19	B	phtbpcicb	PCI reset signal
	REQ#/REQ#[1]	AF22	B	phtbpcicbu	PCI bus request signal
	REQ#[2]	AD21	I	phtipcicbu	PCI bus request signals
	REQ#[5] REQ#[4] REQ#[3]	AC19 AE20 AF21	I (B)	phtbpcicbu	PCI bus request signals
	GNT#/GNT#[1]	AC21	B	phtbpcicbu	PCI bus grant signal
	GNT#[3] GNT#[2]	AD20 AE21	O(B)	phtbpcicb	PCI bus grant signals
	GNT#[5] GNT#[4]	AD19 AF20	O	photcicb	PCI bus grant signals

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
PCI & PC Card Controller – PCI Host Mode (65)	AD[31:0]		B	phtbpcicb	PCI address / data 32-bit lines
	C/BE#[3] C/BE#[2] C/BE#[1] C/BE#[0]	AD26 AA26 V26 T24	B	phtbpcicb	Command / byte enable 4-bit lines
	PAR	W23	B	phtbpcicb	Even parity signal
	FRAME#	AA25	B	phtbpcicbu	Signal indicating duration of access
	IRDY#	AA24	B	phtbpcicbu	Signal indicating the master is ready
	TRDY#	Y26	B	phtbpcicbu	Signal indicating the target is ready
	DEVSEL#	Y25	B	phtbpcicbu	Target device selected signal
	STOP#	Y24	B	phtbpcicbu	Stop signal for disconnect or retry
	LOCK#	W26	O(B)	phtbpcicbu	Lock signal (always pull-up)
	PERR#	W25	B	phtbpcicbu	Parity error report signal
	SERR#	W24	I(BD)	phtbdpcicbu	System error report signal
	INTA#	AF19	I(BD)	phtbdpcicbu	Level-sensitive Interrupt signal
	PME#	AE22	I (B)	phtbpcicbu	PCI Power Management Event signal
	CLKRUN#	L25	B	phtbpcicbu	PCI clock speed control signal
	PCI_XCLK	AA3	I	phic	S3C2510A PCI PLL Clock Source. It can be system bus clock if BUS_FREQ[2:0] select PCI clock.
	PCI_CLKSEL	AB1	I	phic	Clock Select for PCI PLL. If this pin is low, PCI PLL on. If high, PCI PLL off.
	PCI_FILTER	R4	AO	poar50_abb	PLL filter pin for PCI PLL.

- PCI & PC Card controller pins are 69 pins (66 interface signals + 3 PLL signals).
- When in PCI host mode (PCI_PCCDM=0, PCI_HOSTM=1), PCI & PC Card controller pins are mapped to PCI host signals as above. Extra 4 pins (PCICVS[2:1], PCICCD[2:1]) are not used in this mode.
- These pins in above table are shared with other pins according to PCI & PC Card controller mode. Refer to “S3C2510A PCI / PC Card Signals Reference Table”.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
PCI & PC Card Controller – PCI Agent Mode (53)	EXT_PCICLK	AD18	I (B)	phtbpcicb	External PCI clock input
	EXT_PCIRST#	AE19	B	phtbpcicb	PCI reset signal
	REQ#	AF22	O(B)	phtbpcicbu	PCI bus request signal
	GNT#	AC21	I (B)	phtbpcicbu	PCI bus grant signal
	IDSEL	AD21	I	phtipcicbu	PCI Initialization Device Select signal
	AD[31:0]		B	phtbpcicb	PCI address / data 32-bit lines
	C/BE#[3] C/BE#[2] C/BE#[1] C/BE#[0]	AD26 AA26 V26 T24	B	phtbpcicb	Command / byte enable 4-bit lines
	PAR	W23	B	phtbpcicb	Even parity signal
	FRAME#	AA25	B	phtbpcicbu	Signal indicating duration of access
	IRDY#	AA24	B	phtbpcicbu	Signal indicating the master is ready
	TRDY#	Y26	B	phtbpcicbu	Signal indicating the target is ready
	DEVSEL#	Y25	B	phtbpcicbu	Target device selected signal
	STOP#	Y24	B	phtbpcicbu	Stop signal for disconnect or retry
	LOCK#	W26	I (B)	phtbpcicbu	Lock signal
	PERR#	W25	B	phtbpcicbu	Parity error report signal
	SERR#	W24	OD (BD)	phtbdpcicbu	System error report signal
	INTA#	AF19	OD (BD)	phtbdpcicbu	Level-sensitive Interrupt signal
	PME#	AE22	O(B)	phtbpcicbu	PCI Power Management Event signal
	CLKRUN#	L25	O(B)	phtbpcicbu	PCI clock speed control signal

- PCI & PC Card controller pins are 69 pins (66 interface signals + 3 PLL signals).
- When in PCI agent mode (PCI_PCCDM=0, PCI_HOSTM=0), PCI & PC Card controller pins are mapped to PCI agent (general PCI device) signals as above. Extra 16 pins (PCICLK[2:1], PCIREQ[5:3], PCIGNT[5:2], PCICVS[2:1], PCICCD[2:1], PCI_XCLK, PCI_CLK_SEL, PCI_FILTER) are not used in this mode.
- These pins in above table are shared with other pins according to PCI & PC Card controller mode. Refer to “S3C2510A PCI / PC Card Signals Reference Table”.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
PCI & PC Card Controller – CardBus PC Card Host Mode (63)	CCLK / EXT_CCLK	AD18	B	phtbpcicb	CardBus clock output or external clock input
	CRST# / EXT_CRST#	AE19	B	phtbpcicb	CardBus reset signal
	CREQ#	AF22	I (B)	phtbpcicbu	CardBus bus request signal
	CGNT#	AC21	O (B)	phtbpcicbu	CardBus bus grant signal
	CAD[31:0]		B	phtbpcicb	CardBus address / data 32-bit lines
	C/BE#[3] C/BE#[2] C/BE#[1] C/BE#[0]	AD26 AA26 V26 T24	B	phtbpcicb	Command / byte enable 4-bit lines
	CPAR	W23	B	phtbpcicb	Even parity signal
	CFRAME#	AA25	B	phtbpcicbu	Signal indicating duration of access
	CIRDY#	AA24	B	phtbpcicbu	Signal indicating the master is ready
	CTRDY#	Y26	B	phtbpcicbu	Signal indicating the target is ready
	CDEVSEL#	Y25	B	phtbpcicbu	Target device selected signal
	CSTOP#	Y24	B	phtbpcicbu	Stop signal for disconnect or retry
	CBLOCK#	W26	O (B)	phtbpcicbu	Lock signal (always pull-up)
	CPERR#	W25	B	phtbpcicbu	Parity error report signal
	CSERR#	W24	I (BD)	phtbdpcicbu	System error report signal
	CINT#	AF19	I (BD)	phtbdpcicbu	Level-sensitive Interrupt signal
	CSTSCHG	AE22	I (B)	phtbpcicbu	CardBus Status Changed signal
	CLKRUN#	L25	B	phtbpcicbu	CardBus clock speed control signal
	CVS[2] CVS[1]	N25 N24	B	phbcbcvs	CardBus Voltage Sense signal lines
	CCD#[2] CCD#[1]	M26 M25	I	phicbccd	CardBus Card Detect signal lines
	VCCD[0]	AE20	O (B)	phtbpcicbu	CardBus Power-Switch VCC control signal
	VCCD[1]	AF20	O	phopcicb	CardBus Power-Switch VCC control signal
	VPPD_VCC	AC19	O (B)	phtbpcicbu	CardBus Power-Switch VPP control signal VCC Voltage (5V/3.3V)
	VPPD_PGM	AD19	O	phopcicb	CardBus Power-Switch VPP control signal Higher Voltage (12V)
	PCI_XCLK	AA3	I	phic	S3C2510A PCI PLL Clock Source.
	PCI_CLKSEL	AB1	I	phic	Clock Select for PCI PLL.
	PCI_FILTER	R4	AO	poar50_abb	PLL filter pin for PCI PLL.

- PCI & PC Card controller pins are 69 pins (66 interface signals + 3 PLL signals).
- When CardBus PC Card is inserted in CardBus PC Card host mode (PCI_PCCDM=1, PCI_HOSTM=1), PCI & PC Card controller pins are mapped to CardBus PC Card host signals as above. Extra 6 pins (PCICLK1, PCICLK2, PCIREQ2, PCIREQ3, PCIGNT2, PCIGNT3) are not used in this mode.
- These pins in above table are shared with other pins according to PCI & PC Card controller mode. Refer to "S3C2510A PCI / PC Card Signals Reference Table".

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
PCI & PC Card Controller – CardBus PC Card Agent Mode (53)	EXT_CCLK	AD18	I (B)	phtbpcicb	External CardBus clock
	EXT_CRST#	AE19	B	phtbpcicb	CardBus reset signal
	CREQ#	AF22	O (B)	phtbpcicbu	CardBus bus request signal
	CGNT#	AC21	I (B)	phtbpcicbu	CardBus bus grant signal
	CAD[31:0]		B	phtbpcicb	CardBus address / data 32-bit lines
	CC/BE#[3] CC/BE#[2] CC/BE#[1] CC/BE#[0]	AD26 AA26 V26 T24	B	phtbpcicb	Command / byte enable 4-bit lines
	CPAR	W23	B	phtbpcicb	Even parity signal
	CFRAME#	AA25	B	phtbpcicbu	Signal indicating duration of access
	CIRDY#	AA24	B	phtbpcicbu	Signal indicating the master is ready
	CTRDY#	Y26	B	phtbpcicbu	Signal indicating the target is ready
	CDEVSEL#	Y25	B	phtbpcicbu	Target device selected signal
	CSTOP#	Y24	B	phtbpcicbu	Stop signal for disconnect or retry
	CBLOCK#	W26	I (B)	phtbpcicbu	Lock signal
	CPERR#	W25	B	phtbpcicbu	Parity error report signal
	CSERR#	W24	OD (BD)	phtbdpcicbu	System error report signal
	CINT#	AF19	OD (BD)	phtbdpcicbu	Level-sensitive Interrupt signal
	CSTSCHG	AE22	O (B)	phtbpcicbu	CardBus Status Changed signal
	CLKRUN#	L25	O (B)	phtbpcicbu	CardBus clock speed control signal
	GWA_EVENT	AD21	I	phtipcicbu	External General Wakeup Event signal

- PCI & PC Card controller pins are 69 pins (66 interface signals + 3 PLL signals).
- When CardBus PC Card is inserted in CardBus PC Card agent mode (PCI_PCCDM=1, PCI_HOSTM=0), PCI & PC Card controller pins are mapped to CardBus PC Card agent signals as above. Extra 16 pins (PCICLK[2:1], PCIREQ[5:3], PCIGNT[5:2], PCICVS[2:1], PCICCD[2:1], PCI_XCLK, PCI_CLK_SEL, PCI_FILTER) are not used in this mode.
- These pins in above table are shared with other pins according to PCI & PC Card controller mode. Refer to "S3C2510A PCI / PC Card Signals Reference Table".

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
PCI & PC Card Controller – 16-bit PC Card (PCMCIA) Host Mode (64)	PCRESET	AE19	O(B)	phtbpcicb	16-bit PC Card reset signal
	PCADDR[25:0]		O(B)	phtbpcicb	16-bit PC Card address lines
	PCDATA[15:0]		B	phtbpcicb	16-bit PC Card data lines
	CE#[2] CE#[1]	U23 T24	O(B)	phtbpcicb	Card enable signals (even and odd address)
	REG#	AD26	O(B)	phtbpcicb	Attribute memory select signal
	OE#	U24	O(B)	phtbpcicb	Output enable signal of memory read cycles.
	WE#	AC21	O(B)	phtbpcicb	Write enable signal of memory write cycles
	IORD#	U26	O(B)	phtbpcicb	I/O read signal of I/O read cycles
	IOWR#	V25	O(B)	phtbpcicb	I/O write signal of I/O write cycles
	WAIT#	W24	I(BD)	phtbdpcicbu	16-bit PC Card bus cycle wait signal
	READY (IREQ#)	AF19	I(BD)	phtbdpcicbu	Ready signal of memory interface or Interrupt request signal of I/O interface
	INPACK#	AF22	I (B)	phtbpcicbu	Input acknowledge signal of I/O read cycles
	WP(IOIS16#)	L25	I (B)	phtbpcicbu	Write protect signal of memory interface or 16bit I/O indicating signal of I/O interface
	BVD[1] (STSCHG#)	AE22	I (B)	phtbpcicbu	Battery voltage detect 1 signal or Status change interrupt signal
	BVD[2] (SPKR#)	AD21	I	phtipcicbu	Battery voltage detect 2 signal
	VS#[2] VS#[1]	N25 N24	B	phbcbcvs	PC Card Voltage Sense signal lines
	CD#[2] CD#[1]	M26 M25	I	phicbccd	PC Card Card Detect signal lines
	VCCD[0]	AE20	O(B)	phtbpcicbu	PC Card Power-Switch VCC control signal
	VCCD[1]	AF20	O	phopcicb	PC Card Power-Switch VCC control signal
	VPPD_VCC	AC19	O(B)	phtbpcicbu	PC Card Power-Switch VPP control signals VCC Voltage (5V/3.3V)
	VPPD_PGM	AD19	O	phopcicb	PC Card Power-Switch VPP control signals Higher Voltage (12V)

- PCI & PC Card controller pins are 69 pins (66 interface signals + 3 PLL signals).
- When 16-bit PC Card (PCMCIA card) is inserted in PC Card host mode (PCI_PCCDM=1, PCI_HOSTM=1), PCI & PC Card controller pins are mapped to 16-bit PC Card host (PCMCIA host) signals as above. Extra 5 pins (PCICLK[3:2], PCI_XCLK, PCI_CLK_SEL, PCI_FILTER) are not used in this mode.
- These pins in above table are shared with other pins according to PCI & PC Card controller mode. Refer to "S3C2510A PCI / PC Card Signals Reference Table".
- PCI & PC Card controller doesn't support 16-bit PC Card agent (PCMCIA card) mode.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
SAR & UTOPIA L1/L2 (29)	UTO_TXAD[2]/GPIO[45] UTO_TXAD[1]/GPIO[44] UTO_TXAD[0]/GPIO[43]	A10 C11 B10	O/B	phbst8	TX Address Bus to the ATM PHY / General I/O Ports.
	UTO_RXAD[2] UTO_RXAD[1] UTO_RXAD[0]	C10 B9 D10	O	phob12	RX Address Bus to the ATM PHY
	UTO_TXD[7]/GPIO[53] UTO_TXD[6]/GPIO[52] UTO_TXD[5]/GPIO[51] UTO_TXD[4]/GPIO[50] UTO_TXD[3]/GPIO[49] UTO_TXD[2]/GPIO[48] UTO_TXD[1]/GPIO[47] UTO_TXD[0]/GPIO[46]	C8 A7 D8 B7 C9 A8 B8 A9	O/B	phbst8	Transmit Data Bus to the ATM PHY / General I/O Ports
	UTO_TXSOC/GPIO[54]	B6	O/B	phbst8	Start Of Cell Indicator for Transmit Data / General I/O Ports
	UTO_TXENB/GPIO[55]	A6	O/B	phbst8	Transmit Data Transfer Enable, Low Active / General I/O Ports
	UTO_TXCLAV	C7	I	phis	Cell Buffer Available for Transmit Data.
	UTO_RXD[7]/GPIO[63] UTO_RXD[6]/GPIO[62] UTO_RXD[5]/GPIO[61] UTO_RXD[4]/GPIO[60] UTO_RXD[3]/GPIO[59] UTO_RXD[2]/GPIO[58] UTO_RXD[1]/GPIO[57] UTO_RXD[0]/GPIO[56]	B3 C5 A4 D5 B4 C6 A5 B5	I/B	phbst8	Receive Data Bus from the ATM PHY / General I/O Ports
	UTO_RXSOC	C4	I	phis	Start Of Cell Indicator for Receive Data.
	UTO_RXENB	A3	O	phob8	Receive Data Transfer Enable, Low Active.
	UTO_RXCLAV	A2	I	phis	Cell Buffer Available for Receive Data.
	UTO_CLK	D6	O	phob8	Transfer/Receive Interface Byte Clock.

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
USB Host/Device (11)	HUSB_DP[1] HUSB_DP[0]	AA4 W4	B	pbusb	Internal USB HOST transceiver Full/Low Speed differential I/O
	HUSB_DN[1] HUSB_DN[0]	AA1 Y1	B	pbusb	Internal USB HOST transceiver Full/Low Speed differential I/O
	USB_DP	W2	B	pbusbfs	Internal USB Function Device transceiver Full Speed differential I/O
	USB_DN	W1	B	pbusbfs	Internal USB Function Device transceiver Full Speed differential I/O
	HUSB_OvrCurrent[1] HUSB_OvrCurrent[0]	V3 V1	I	phic	USB HOST Over Current
	USB_XCLK	N1	I	phic	S3C2510A USB PLL Clock Source.
	USB_CLKSEL	M4	I	phic	USB Clock Select. When USB_CLKSEL is '0', USB PLL output is used as the USB clock. When USB_CLKSEL is '1', the USB_XCLK is used as the USB clock.
	USB_FILTER	P2	AO	poar50_abb	Filter for USB PLL If the PLL is used, 320pF capacitor should be connected between the pin and ground.
CUART (2)	CURXD/GPIO[42]	AD17	I/B	phbst8	Console UART Receive Data/General I/O Ports
	CUTXD	AF18	O	phob12	Console UART Transmit Data.
UART (1)	UCLK	AD15	I	phis	UART External Clock for UART0/UART1
HUART0 (7)	HURXD0/GPIO[28]	AE14	I/B	phbst8	HUART0 Receive Data. HURXD0 is the HUART0 input signal for receiving serial data. General I/O Port
	HUTXD0/GPIO[29]	AF14	O/B	phbst8	HUART0 Transmit Data. HUTXD0 is the HUART0 output signal for transmitting serial data. General I/O Port
	HUnDTR0/GPIO[30]	AD13	O/B	phbst8	Not HUART0 Data Terminal Ready.. This output signals the host (or peripheral) that HUART0 is ready to transmit or receive serial data. General I/O Port

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
HUART0 (7)	HUnDSR0/GPIO[31]	AE15	I/B	phbst8	Not HUART0 Data Set Ready. This input signals in the UART0 that the peripheral (or host) is ready to transmit or receive serial data General I/O Port
	HUnRTS0/GPIO[32]	AD14	O/B	phbst8	Not request to send. This pin output state goes Low or High according to the transmit data is in Tx buffer or Tx FIFO when hardware flow control bit value set to one in HUART0 control register. If Tx buffer or Tx FIFO has data to send, this pin state goes low. If hardware flow control bit is zero, this pin output can be controlled directly by HUART0 control register. General I/O Port
	HUnCTS0/GPIO[33]	AF15	I/B	phbst8	Not Clear to send. This input pin function controlled by hardware flow control bit value in HUART0 control register. If hardware flow control bit set to one, HUART0 can transmit the transmitting data only when this pin state is active. General I/O Port
	HUnDCD0/GPIO[34]	AE16	I/B	phbst8	Not Data Carrier Detect. This input pin function is determined by hardware flow control bit value in HUART control register. If hardware flow control bit set to one, HUART0 can receive the receiving data only when this pin state is active. General I/O Port
HUART1 (7)	HURXD1/GPIO[35]	AF16	I/B	phbst8	UART1 Receive Data / General I/O Port
	HUTXD1/GPIO[36]	AC15	O/B	phbst8	UART1 Transmit Data / General I/O Port
	HUnDTR1/GPIO[37]	AE17	O/B	phbst8	Not UART1 Data Terminal Ready/General I/O Port
	HUnDSR1/GPIO[38]	AD16	I/B	phbst8	Not UART1 Data Set Ready/General I/O Port
	HUnRTS1/GPIO[39]	AF17	O/B	phbst8	Not UART1 Request To Send/General I/O Port

Table 1-1. S3C2510A Pin List and PAD Type S3C2510A Pin List and PAD Type (Continued)

Group	Pin Name	Pin No.	I/O Type	Pad Type	Description
HUART1 (7)	HUnCTS1/GPIO[40]	AC17	I/B	phbst8	Not UART1 Clear To Send/General I/O Port.
	HUnDCD1/GPIO[41]	AE18	I/B	phbst8	Not UART1 Data Carrier Detected/General I/O Port.
General Purpose In/Out Ports (including xINT xGDMA_Req xGDMA_Ack TIMER) (28)	GPIO[7] GPIO[6] GPIO[5] GPIO[4] GPIO[3] GPIO[2] GPIO[1] GPIO[0]	AF7 AE7 AF6 AD6 AC6 AE6 AF5 AD5	B	phbst8	General I/O Ports.
	xINT[5]/GPIO[13] xINT[4]/GPIO[12] xINT[3]/GPIO[11] xINT[2]/GPIO[10] xINT[1]/GPIO[9] xINT[0]/GPIO[8]	AE9 AD8 AF8 AC8 AE8 AD7	I/B	phbst8	External interrupt requests/General I/O Ports.
	xGDMA_Req[3]/GPIO[17] xGDMA_Req[2]/GPIO[16] xGDMA_Req[1]/GPIO[15] xGDMA_Req[0]/GPIO[14]	AF10 AD9 AE10 AF9	I/B	phbst8	External DMA requests for GDMA/General I/O Ports.
	xGDMA_Ack[3]/GPIO[21] xGDMA_Ack[2]/GPIO[20] xGDMA_Ack[1]/GPIO[19] xGDMA_Ack[0]/GPIO[18]	AF11 AD10 AE11 AC10	O/B	phbst8	External DMA acknowledge from GDMA/General I/O Ports.
	TIMER[5]/GPIO[27] TIMER[4]/GPIO[26] TIMER[3]/GPIO[25] TIMER[2]/GPIO[24] TIMER[1]/GPIO[23] TIMER[0]/GPIO[22]	AF13 AC12 AE13 AD11 AF12 AE12	O/B	phbst8	TIMER[5:0] Out/General I/O Ports.
I^2C (2)	SCL	U4	B	phbcd8	I^2C serial clock.
	SDA	V2	B	phbcd8	I^2C serial data.

- Total Number of Signal Pins = 296

1.5 S3C2510A PAD TYPE

Table 1-2. S3C2510A PAD Type and Feature

Pad Type	I/O Type	Current Drive	Cell Type	Feature	Slew-Rate Control
phic	I	–	LVCMOS Level	3.3V	–
phicd	I	–	LVCMOS Level	3.3V Pull-down resistor	–
phicu	I	–	LVCMOS Level	3.3V Pull-up resistor	–
phis	I	–	LVCMOS Schmitt Trigger Level	3.3V	–
phisd	I	–	LVCMOS Schmitt Trigger Level	3.3V Pull-down resistor	–
poar50_abb	AO	–	Analog output with separate bulk bias	–	–
phob4	O	4mA	Normal Buffer	3.3V	–
phob8	O	8mA	Normal Buffer	3.3V	
phob12	O	12mA	Normal Buffer	3.3V	
phot12	O	12mA	Tri-State Buffer	3.3V	–
phot20	O	20mA	Tri-State Buffer	3.3V	
phbcut12	B	12mA	LVCMOS Level Tri-State Buffer	3.3V Pull-up resistor	
phbsut20	B	20mA	LVCMOS Schmit trigger level Tri-State Buffer	3.3V Pull-up resistor	
phbcd8	B	8mA	LVCMOS Level Open drain buffer	3.3V	–
phbst8	B	8mA	LVCMOS Schmit trigger level Tri-State Buffer	3.3V	
phbst24	B	24mA	LVCMOS Schmit trigger level Tri-State Buffer	3.3V	
pbusb	B	6mA	USB Host Full/Low Speed Buffer		–
pbusbfs	B	6mA	USB Function Full Speed Buffer		–
phopcicb	O		PCI & PC Card output	3.3V	

Table 1-2. S3C2510A PAD Type and Feature (Continued)

Pad Type	I/O Type	Current Drive	Cell Type	Feature	Slew-Rate Control
phtbpcicb	B		PCI & PC Card Bi-directional	5V tolerant	
phtbpcicbu	B		PCI & PC Card Bi-directional	5V tolerant Pull-up resistor	
phtbdpcicbu	BD		PCI & PC Card Bi-directional Open-Drain	5V tolerant Pull-up resistor	
phtipcicbu	I		PCI & PC Card input	5V tolerant Pull-up resistor	
phbcbcvs	B		CardBus PC Card CVS	3.3V	
phicbccd	I		CardBus PC Card CCD#	3.3V	

NOTE: For the detail information about the pad type, see Input/Output Cells of the "STD130/MDL130 0.18um 3.3V Standard Cell Library Data Book" which is produced by Samsung Electronics Co., Ltd, ASIC Team.

1.6 S3C2510A PCI / PC CARD SIGNALS REFERENCE TABLE

Table 1-3. S3C2510A PCI / PC Card Signals Reference Table

Pin Name	Ball Grid	I/O cell	PCI Host Mode	PCI Agent Mode	CardBus PC Card Host Mode	CardBus PC Card Agent Mode	PCMCIA Host Mode
PCI_PCCDM	AA2	phic	0	0	1	1	1
PCI_HOSTM	Y3	phic	1	0	1	0	1
PCICLK3	AD18	phtbpcicb	PCICLK3 / EXT_PCICLK	EXT_PCICLK	CCLK / EXT_CCLK	EXT_CCLK	-
PCIINTA	AF19	phtbdpcicbu	INTA#	INTA#	CINT#	CINT#	READY(IREQ#)
PCIRST	AE19	phtbpcicb	PCIRST# / EXT_PCIRST#	EXT_PCIRST#	CRST# / EXT_CRST#	EXT_CRST#	PCRESET
PCIGNT5	AD19	phopcicb	GNT#[5]	–	VPPD_PGM	–	VPPD_PGM
PCIREQ5	AC19	phtbpcicbu	REQ#[5]	–	VPPD_VCC	–	VPPD_VCC
PCIGNT4	AF20	phopcicb	GNT#[4]	–	VCCD[1]	–	VCCD[1]
PCIREQ4	AE20	phtbpcicbu	REQ#[4]	–	VCCD[0]	–	VCCD[0]
PCIGNT3	AD20	phtbpcicb	GNT#[3]	–	–	–	PCDATA[14]
PCIREQ3	AF21	phtbpcicbu	REQ#[3]	–	–	–	PCADDR[18]
PCIGNT2	AE21	phtbpcicb	GNT#[2]	–	–	–	PCDATA[2]
PCIREQ2	AD21	phtipcicbu	REQ#[2]	IDSEL	–	GWA_EVENT	BVD[2](SPKR#)
PCIGNT1	AC21	phtbpcicb	GNT# / GNT#[1]	GNT#	CGNT#	CGNT#	WE#
PCIREQ1	AF22	phtbpcicbu	REQ# / REQ#[1]	REQ#	CREQ#	CREQ#	INPACK#
PCIPME	AE22	phtbpcicbu	PME#	PME#	CSTSCHG	CSTSCHG	BVD[1] (STSCHG#)
PCIAD31	AD22	phtbpcicb	AD[31]	AD[31]	CAD[31]	CAD[31]	PCDATA[10]
PCIAD30	AC22	phtbpcicb	AD[30]	AD[30]	CAD[30]	CAD[30]	PCDATA[9]
PCIAD29	AF23	phtbpcicb	AD[29]	AD[29]	CAD[29]	CAD[29]	PCDATA[1]
PCIAD28	AE23	phtbpcicb	AD[28]	AD[28]	CAD[28]	CAD[28]	PCDATA[8]
PCIAD27	AD23	phtbpcicb	AD[27]	AD[27]	CAD[27]	CAD[27]	PCDATA[0]
PCICLK2	AE24	phopcicb	PCICLK2	–	–	–	–
PCIAD26	AF24	phtbpcicb	AD[26]	AD[26]	CAD[26]	CAD[26]	PCADDR[0]
PCIAD25	AF25	phtbpcicb	AD[25]	AD[25]	CAD[25]	CAD[25]	PCADDR[1]
PCIAD24	AE26	phtbpcicb	AD[24]	AD[24]	CAD[24]	CAD[24]	PCADDR[2]

Table 1-3. S3C2510A PCI / PC Card Signals Reference Table (Continued)

Pin Name	Ball Grid	I/O cell	PCI Host Mode	PCI Agent Mode	CardBus PC Card Host Mode	CardBus PC Card Agent Mode	PCMCIA Host Mode
PCICBE3	AD26	phtbpcicb	C/BE#[3]	C/BE#[3]	CC/BE#[3]	CC/BE#[3]	REG#
PCIAD23	AD25	phtbpcicb	AD[23]	AD[23]	CAD[23]	CAD[23]	PCADDR[3]
PCIAD22	AC26	phtbpcicb	AD[22]	AD[22]	CAD[22]	CAD[22]	PCADDR[4]
PCIAD21	AC25	phtbpcicb	AD[21]	AD[21]	CAD[21]	CAD[21]	PCADDR[5]
PCIAD20	AC24	phtbpcicb	AD[20]	AD[20]	CAD[20]	CAD[20]	PCADDR[6]
PCIAD19	AB26	phtbpcicb	AD[19]	AD[19]	CAD[19]	CAD[19]	PCADDR[25]
PCIAD18	AB25	phtbpcicb	AD[18]	AD[18]	CAD[18]	CAD[18]	PCADDR[7]
PCIAD17	AB24	phtbpcicb	AD[17]	AD[17]	CAD[17]	CAD[17]	PCADDR[24]
PCIAD16	AB23	phtbpcicb	AD[16]	AD[16]	CAD[16]	CAD[16]	PCADDR[17]
PCICBE2	AA26	phtbpcicb	C/BE#[2]	C/BE#[2]	CC/BE#[2]	CC/BE#[2]	PCADDR[12]
PCIFRAME	AA25	phtbpcicbu	FRAME#	FRAME#	CFRAME#	CFRAME#	PCADDR[23]
PCIIRDY	AA24	phtbpcicbu	IRDY#	IRDY#	CIRDY#	CIRDY#	PCADDR[15]
PCICLK1	AA23	phopcicb	PCICLK1	–	CCLK	–	PCADDR[16]
PCITRDY	Y26	phtbpcicbu	TRDY#	TRDY#	CTRDY#	CTRDY#	PCADDR[22]
PCIDEVSEL	Y25	phtbpcicbu	DEVSEL#	DEVSEL#	CDEVSEL#	CDEVSEL#	PCADDR[21]
PCISTOP	Y24	phtbpcicbu	STOP#	STOP#	CSTOP#	CSTOP#	PCADDR[20]
PCILOCK	W26	phtbpcicbu	(Pull-up)	LOCK#	(Pull-up)	CBLOCK#	PCADDR[19]
PCIPERR	W25	phtbpcicbu	PERR#	PERR#	CPERR#	CPERR#	PCADDR[14]
PCISERR	W24	phtbdpcicbu	SERR#	SERR#	CSERR#	CSERR#	WAIT#
PCIPAR	W23	phtbpcicb	PAR	PAR	CPAR#	CPAR#	PCADDR[13]
PCICBE1	V26	phtbpcicb	C/BE#[1]	C/BE#[1]	CC/BE#[1]	CC/BE#[1]	PCADDR[8]
PCIAD15	V25	phtbpcicb	AD[15]	AD[15]	CAD[15]	CAD[15]	IOWR#
PCIAD14	V24	phtbpcicb	AD[14]	AD[14]	CAD[14]	CAD[14]	PCADDR[9]
PCIAD13	U26	phtbpcicb	AD[13]	AD[13]	CAD[13]	CAD[13]	IORD#
PCIAD12	U25	phtbpcicb	AD[12]	AD[12]	CAD[12]	CAD[12]	PCADDR[11]
PCIAD11	U24	phtbpcicb	AD[11]	AD[11]	CAD[11]	CAD[11]	OE#
PCIAD10	U23	phtbpcicb	AD[10]	AD[10]	CAD[10]	CAD[10]	CE#[2]
PCIAD9	T26	phtbpcicb	AD[9]	AD[9]	CAD[9]	CAD[9]	PCADDR[10]

Table 1-3. S3C2510A PCI / PC Card Signals Reference Table (Continued)

Pin Name	Ball Grid	I/O cell	PCI Host Mode	PCI Agent Mode	CardBus PC Card Host Mode	CardBus PC Card Agent Mode	PCMCIA Host Mode
PCIAD8	T25	phtbpcicb	AD[8]	AD[8]	CAD[8]	CAD[8]	PCDATA[15]
PCICBE0	T24	phtbpcicb	C/BE#[0]	C/BE#[0]	CC/BE#[0]	CC/BE#[0]	CE#[1]
PCIAD7	R26	phtbpcicb	AD[7]	AD[7]	CAD[7]	CAD[7]	PCDATA[7]
PCIAD6	R25	phtbpcicb	AD[6]	AD[6]	CAD[6]	CAD[6]	PCDATA[13]
PCIAD5	R24	phtbpcicb	AD[5]	AD[5]	CAD[5]	CAD[5]	PCDATA[6]
PCIAD4	R23	phtbpcicb	AD[4]	AD[4]	CAD[4]	CAD[4]	PCDATA[12]
PCIAD3	P26	phtbpcicb	AD[3]	AD[3]	CAD[3]	CAD[3]	PCDATA[5]
PCIAD2	P25	phtbpcicb	AD[2]	AD[2]	CAD[2]	CAD[2]	PCDATA[11]
PCIAD1	P24	phtbpcicb	AD[1]	AD[1]	CAD[1]	CAD[1]	PCDATA[4]
PCIAD0	N26	phtbpcicb	AD[0]	AD[0]	CAD[0]	CAD[0]	PCDATA[3]
PCICVS2	N25	phbcbcvs	–	–	CVS[2]	–	VS#[2]
PCICVS1	N24	phbcbcvs	–	–	CVS[1]	–	VS#[1]
PCICCD2	M26	phicbccd	–	–	CCD#[2]	–	CD#[2]
PCICCD1	M25	phicbccd	–	–	CCD#[1]	–	CD#[1]
PCICLKRUN	L25	phtbpcicbu	CLKRUN#	CLKRUN#	CCLKRUN#	CCLKRUN#	WP(IOIS16#)

PCI Host Mode	PCI_PCCDM = 0, PCI_HOSTM=1
PCI Agent Mode	PCI_PCCDM = 0, PCI_HOSTM=0
CardBus PC Card Host Mode	PCI_PCCDM = 1, PCI_HOSTM=1, CardBus PC Card is inserted
CardBus PC Card Agent Mode	PCI_PCCDM = 1, PCI_HOSTM=0
16-bit PC Card (PCMCIA) Host Mode	PCI_PCCDM = 1, PCI_HOSTM=1, 16-bit PC Card is inserted

NOTE: Each mode is selected by PCI_PCCDM & PCI_HOSTM pin input signal and inserted card type

1.7 S3C2510A PCI & PC CARD I/O

Table 1-4. Cell Description

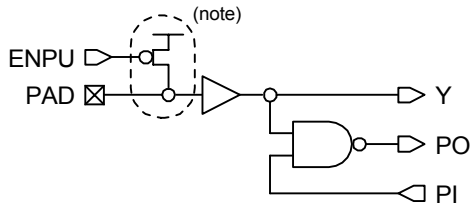
Cell Name	Type (I/O/B/OD)	Mode		Operating Frequency
		Description	Condition	
phtipcicbuc	I	CardBus PC Card (16-bit PC Card)	ENCB ="1"	33MHz
phopcicbc	O			
phtbpcicbuc	B			
phtbpcicbc	B			
phtbdpcicbuc	B(OD)			
phtipcicbup	I	PCI	ENCB ="0"	66MHz
phopcicbp	O			
phtbpcicbup	B			
phtbpcicbp	B			
phtbdpcicbup	B(OD)			
phbcbcvs	B	for CVS[2:1]		
phicbccd	I	for CCD#[2:1]		

Table 1-5. PCI & PC Card Pull-up Description

Pin Name	I/O cell	Ball Grid	PCI Host Mode		PCI Agent Mode	CardBus Host Mode		CardBus Agent Mode	PCMCIA Host Mode
PCI_PCCDM mode		AA1	"0"		"0"	"1"		"1"	"1"
PCI_HOSTM mode		Y3	"1"		"0"	"1"		"0"	"1"
Arbiter mode (PCICON[ARB])			Int. Arb.	Ext. Arb.		Int. Arb.	Ext. Arb.		
PCIREQ1	phtbpcicbu	AE22	Pull-up	No	No	Pull-up	No	No	Pull-up
PCIREQ2	phtipcicbu	AC21	Pull-up	No	No	Pull-up	No	No	Pull-up
PCIREQ3	phtbpcicbu	AE21	Pull-up	No	No	Pull-up	No	No	No
PCIREQ4	phtbpcicbu	AD20	Pull-up	No	No	Pull-up	No	No	No
PCIREQ5	phtbpcicbu	AF20	Pull-up	No	No	Pull-up	No	No	No
PCIGNT1	phtbpcicbu	AF22	No	No	No	No	No	Pull-up	No
PCIFRAME	phtbpcicbu	AA25	Pull-up	Pull-up	No	No	No	Pull-up	No
PCIIRDY	phtbpcicbu	AA24	Pull-up	Pull-up	No	Pull-up	Pull-up	No	No
PCITRDY	phtbpcicbu	Y26	Pull-up	Pull-up	No	Pull-up	Pull-up	No	No
PCIDEVSEL	phtbpcicbu	Y25	Pull-up	Pull-up	No	Pull-up	Pull-up	No	No
PCISTOP	phtbpcicbu	Y24	Pull-up	Pull-up	No	Pull-up	Pull-up	No	No
PCILOCK	phtbpcicbu	W26	Pull-up	Pull-up	No	Pull-up	Pull-up	No	No
PCIPERR	phtbpcicbu	W25	Pull-up	Pull-up	No	Pull-up	Pull-up	No	No
PCISERR	phtbdpcicbu	W24	Pull-up	Pull-up	No	Pull-up	Pull-up	No	Pull-up
PCIINTA	phtbdpcicbu	AE19	Pull-up	Pull-up	No	Pull-up	Pull-up	No	Pull-up
PCIPME	phtbpcicbu	AF19	Pull-up	Pull-up	No	No	No	No	Pull-up
PCICLKRUN	phtbpcicbu	L25	Pull-up*	Pull-up*	No	Pull-up*	Pull-up*	No	Pull-up

NOTE: * pull-up is enabled only during clock stop mode.

SYMBOL AND TRUTH TABLE



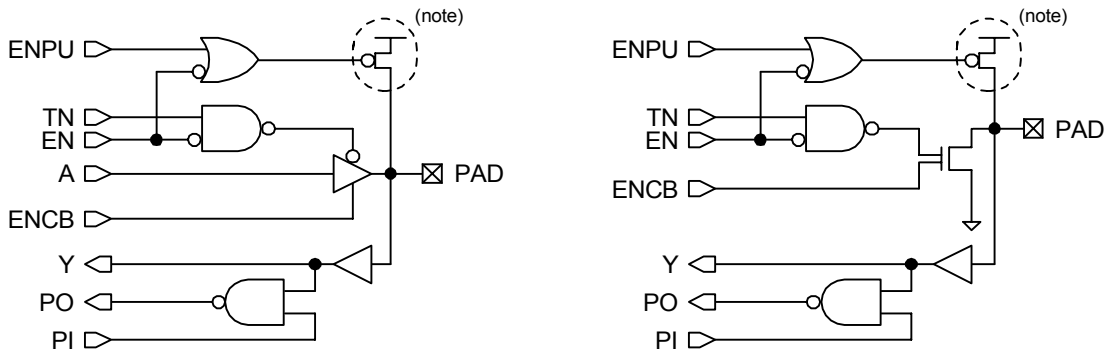
<phtipcicbu(c/p) symbol>

NOTE: ENPU = 'low' Pull-up Enabled, ENPU = 'high' Pull-up Disabled.
phtipcicb cell has a current path from VDD to PAD as following application.
ENPU = low and PAD = low.
The value of pull-up resistor is 35K[Ω] in typical condition
(Voltage: 3.3V, Process: NN, Temp: 25° C)

Figure 1-2. Symbol of phtipcicbu(c/p)

Table 1-6. Truth Table of phtipcicbu(c/p)

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1



<phtbpcicbu(c/p) symbol> **<phtbdpcicb(c/p) symbol>**

NOTE: ENPU = 'low' & EN = 'high' Pull-up Enabled.
Those cell have a current path from VDD to PAD as following application.
(ENPU = low & EN = high) and PAD = low.
The value of pull-up resistor is 35K[Ω] in typical condition
(Voltage: 3.3V, Process: NN, Temp: 25° C)

Figure 1-3. Symbol of phtbpcicbu(c/p) and phtbdpcicb(c/p)

Table 1-7. Truth Table (Input) of phtbpcicbu(c/p) and phtbdpcicb(c/p)

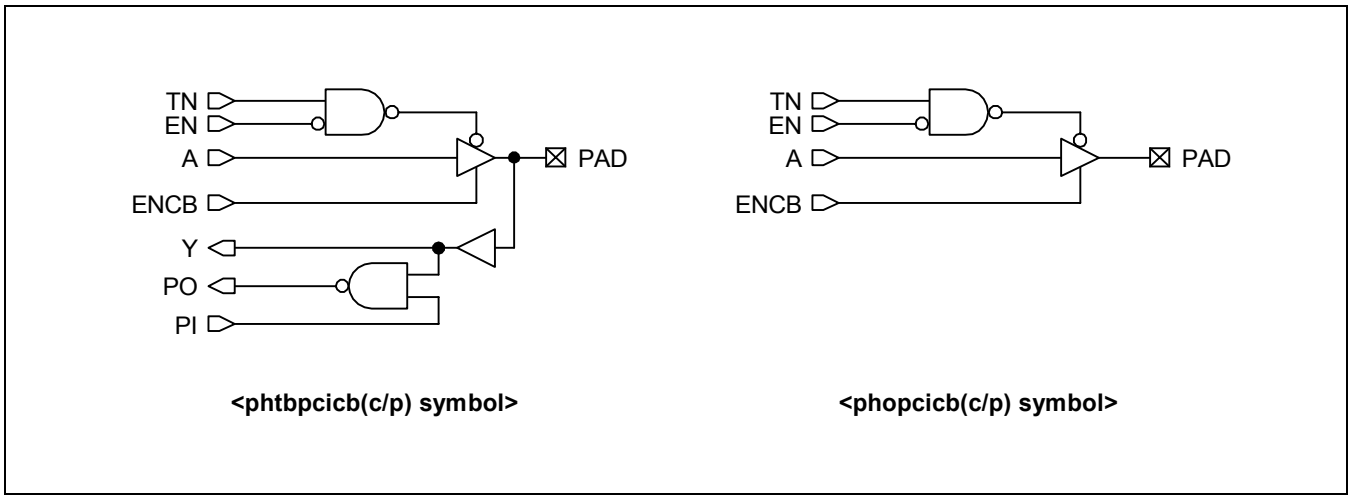
PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Table 1-8. Truth Table (Output) of phtbpcicbu(c/p)

A	EN	TN	ENPU	PAD
0	0	1	x	0
1	0	1	x	1
x	1	x	0	1
			1	Hi-Z
x	0	0	x	Hi-Z
x	1	0	0	1
			1	Hi-Z

Table 1-9. Truth Table (Open Drain) of phtbdpcicb(c/p)

EN	TN	ENPU	PAD
0	1	x	0
1	x	0	1
		1	Hi-Z
0	0	x	Hi-Z
1	0	0	1
		1	Hi-Z



<phtbpcicb(c/p) symbol> <phopcicb(c/p) symbol>

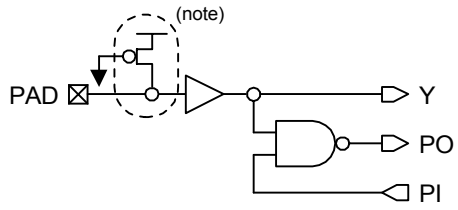
Figure 1-4. Symbol of phtbpcicb(c/p) and phopcicb(c/p)

Table 1-10. Truth Table (Input) of phtbpcicb(c/p)

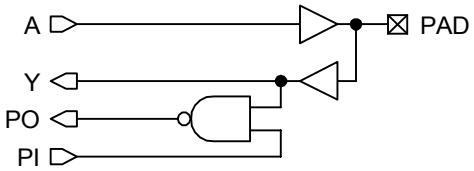
PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Table 1-11. Truth Table (Output) of phtbpcicb(c/p) and phopcicb(c/p)

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z



<phicbccd symbol>



<phbcbcvs symbol>

NOTE: Those cell have a current path from VDD to PAD when PAD is Low.
The value of pull-up resistor is 130K[Ω] in typical condition
(Voltage: 3.3V, Process: NN, Temp: 25° C)

Figure 1-5. Symbol of phicbccd and phbcbcvs

1.8 PIN ASSIGNMENT

Table 1-12. Pin Assignment

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
B1	MDC	O	M2	RXD2_1	I
C2	MDIO	B	M1	RXD3_1	I
C1	COL_0	I	L3	RX_DV_LINK10_1	I
D2	TX_CLK_0	I	N2	RX_ERR_1	I
D3	TXD0_0	O	M4	USB_CLKSEL	I
D1	TXD1_LOOP10_0	O	N1	USB_XCLK	I
E2	TXD2_0	O	M3	1.8VDD_A	
E4	TXD3_0	O	P2	USB_FILTER	O
E3	TX_EN_0	O	P1	GND_A	
E1	TX_ERR_PCOMP_10M_0	O	N3	1.8VDD_A	
F2	CRS_0	I	R2	FILTER	O
F4	RX_CLK_0	I	P3	GND_A	
F3	RXD0_0	I	R1	1.8VDD_A	
F1	RXD1_0	I	T2	PHY_FILTER	O
G2	RXD2_0	I	R3	GND_A	
G1	RXD3_0	I	T1	1.8VDD_A	
G3	RX_DV_LINK10_0	I	R4	PCI_FILTER	O
H2	RX_ERR_0	I	U2	GND_A	
H4	COL_1	I	T3	XCLK	I
H1	TX_CLK_1	I	U1	CLKSEL	I
H3	TXD0_1	O	U4	SCL	B
J2	TXD1_LOOP10_1	O	V2	SDA	B
J1	TXD2_1	O	U3	PHY_CLKSEL	I
K2	TXD3_1	O	V1	HUSB_OVRCURRENT0	I
J3	TX_EN_1	O	W2	USB_DP	B
K1	TX_ERR_PCOMP_10M_1	O	W1	USB_DN	B
K4	CRS_1	I	V3	HUSB_OVRCURRENT1	I
L2	RX_CLK_1	I	Y2	PHY_FREQ	I
K3	RXD0_1	I	W4	HUSB_DP0	B
L1	RXD1_1	I	Y1	HUSB_DN0	B

Table 1-12. Pin Assignment (Continued)

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
W3	BIG	I	AE7	GPIO6	B
AA2	PCI_PCCDM	I	AF7	GPIO7	B
AA4	HUSB_DP1	B	AD7	GPIO8_xINT0	B
AA1	HUSB_DN1	B	AE8	GPIO9_xINT1	B
Y3	PCI_HOSTM	I	AC8	GPIO10_xINT2	B
AB2	nRESET	I	AF8	GPIO11_xINT3	B
AB1	PCI_CLKSEL	I	AD8	GPIO12_xINT4	B
AA3	PCI_XCLK	I	AE9	GPIO13_xINT5	B
AC2	CLK_MOD0	I	AF9	GPIO14_xGDMA_Req0	B
AB4	CLK_MOD1	I	AE10	GPIO15_xGDMA_Req1	B
AC1	BUS_FREQ0	I	AD9	GPIO16_xGDMA_Req2	B
AB3	BUS_FREQ1	I	AF10	GPIO17_xGDMA_Req3	B
AD2	BUS_FREQ2	I	AC10	GPIO18_xGDMA_Ack0	B
AC3	CPU_FREQ0	I	AE11	GPIO19_xGDMA_Ack1	B
AD1	CPU_FREQ1	I	AD10	GPIO20_xGDMA_Ack2	B
AE1	CPU_FREQ2	I	AF11	GPIO21_xGDMA_Ack3	B
AF2	B0SIZE0	I	AE12	GPIO22_TIMER0	B
AE3	B0SIZE1	I	AF12	GPIO23_TIMER1	B
AF3	TMODE	I	AD11	GPIO24_TIMER2	B
AE4	TMS	I	AE13	GPIO25_TIMER3	B
AD4	TDO	O	AC12	GPIO26_TIMER4	B
AF4	TDI	I	AF13	GPIO27_TIMER5	B
AE5	nTRST	I	AD12	PHY_CLKO	O
AC5	TCK	I	AE14	GPIO28_HURXD0	B
AD5	GPIO0	B	AF14	GPIO29_HUTXD0	B
AF5	GPIO1	B	AD13	GPIO30_HUnDTR0	B
AE6	GPIO2	B	AE15	GPIO31_HUnDSR0	B
AC6	GPIO3	B	AD14	GPIO32_HUnRTS0	B
AD6	GPIO4	B	AF15	GPIO33_HUnCTS0	B
AF6	GPIO5	B	AE16	GPIO34_HUnDCD0	B

Table 1-12. Pin Assignment (Continued)

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
AD15	UCLK	I	AF24	PCIAD26	B
AF16	GPIO35_HURXD1	B	AF25	PCIAD25	B
AC15	GPIO36_HUTXD1	B	AE26	PCIAD24	B
AE17	GPIO37_HUnDTR1	B	AD25	PCIAD23	B
AD16	GPIO38_HUnDSR1	B	AD26	PCICBE3	B
AF17	GPIO39_HUnRTS1	B	AC25	PCIAD21	B
AC17	GPIO40_HUnCTS1	B	AC24	PCIAD20	B
AE18	GPIO41_HUnDCD1	B	AC26	PCIAD22	B
AD17	GPIO42_CURXD	B	AB25	PCIAD18	B
AF18	CUTXD	O	AB23	PCIAD16	B
AE19	PCIRST	B	AB24	PCIAD17	B
AF19	PCIINTA	B	AB26	PCIAD19	B
AD18	PCICLK3	B	AA25	PCIFRAME	B
AE20	PCIREQ4	B	AA23	PCICLK1	O
AC19	PCIREQ5	B	AA24	PCIIRDY	B
AF20	PCIGNT4	O	AA26	PCICBE2	B
AD19	PCIGNT5	O	Y25	PCIDEVSEL	B
AE21	PCIGNT2	B	Y26	PCITRDY	B
AC21	PCIGNT1	B	Y24	PCISTOP	B
AF21	PCIREQ3	B	W25	PCIPERR	B
AD20	PCIGNT3	B	W23	PCIPAR	B
AE22	PCIPME	B	W26	PCILOCK	B
AF22	PCIREQ1	B	W24	PCISERR	B
AD21	PCIREQ2	I	V25	PCIAD15	B
AE23	PCIAD28	B	V26	PCICBE1	B
AC22	PCIAD30	B	U25	PCIAD12	B
AF23	PCIAD29	B	V24	PCIAD14	B
AD22	PCIAD31	B	U26	PCIAD13	B
AE24	PCICLK2	O	U23	PCIAD10	B
AD23	PCIAD27	B	T25	PCIAD8	B

Table 1-12. Pin Assignment (Continued)

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
U24	PCIAD11	B	H23	nWBE0/DQM0	O
T26	PCIAD9	B	G26	nWBE1/DQM1	O
R25	PCIAD6	B	H24	nWBE2/DQM2	O
R26	PCIAD7	B	F25	nWBE3/DQM3	O
T24	PCICBE0	B	F23	nSDWE	O
P25	PCIAD2	B	F26	nSDCS0	O
R23	PCIAD4	B	G24	nSDCS1	O
P26	PCIAD3	B	E25	nSDRAS	O
R24	PCIAD5	B	E26	nSDCAS	O
N25	PCICVS2	B	F24	XDATA0	B
N26	PCIAD0	B	D25	XDATA1	B
P24	PCIAD1	B	E23	XDATA2	B
M25	PCICCD1	I	D26	XDATA3	B
N24	PCICVS1	B	E24	XDATA4	B
M26	PCICCD2	I	C25	XDATA5	B
L25	PCICLKRUN	B	D24	XDATA6	B
M24	XBMREQ	I	C26	XDATA7	B
L26	XBMACK	O	B26	XDATA8	B
M23	HCLKO	B	A25	XDATA9	B
K25	nEWAIT	I	B24	XDATA10	B
L24	CKE	O	A24	XDATA11	B
K26	nMCS0	O	B23	XDATA12	B
K23	nMCS1	O	C23	XDATA13	B
J25	nMCS2	O	A23	XDATA14	B
K24	nMCS3	O	B22	XDATA15	B
J26	nMCS4	O	D22	XDATA16	B
H25	nMCS5	O	C22	XDATA17	B
H26	nMCS6	O	A22	XDATA18	B
J24	nMCS7	O	B21	XDATA19	B
G25	nOE	O	D21	XDATA20	B

Table 1-12. Pin Assignment (Continued)

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
C21	XDATA21	B	A12	ADDR19	O
A21	XDATA22	B	B11	ADDR20	O
B20	XDATA23	B	C12	ADDR21	O
A20	XDATA24	B	A11	ADDR22	O
C20	XDATA25	B	D12	ADDR23	O
B19	XDATA26	B	B10	GPIO43_UTO_TXAD0	B
D19	XDATA27	B	C11	GPIO44_UTO_TXAD1	B
A19	XDATA28	B	A10	GPIO45_UTO_TXAD2	B
C19	XDATA29	B	D10	UTO_RXAD0	O
B18	XDATA30	B	B9	UTO_RXAD1	O
A18	XDATA31	B	C10	UTO_RXAD2	O
B17	ADDR0	O	A9	GPIO46_UTO_TXD0	B
C18	ADDR1	O	B8	GPIO47_UTO_TXD1	B
A17	ADDR2	O	A8	GPIO48_UTO_TXD2	B
D17	ADDR3	O	C9	GPIO49_UTO_TXD3	B
B16	ADDR4	O	B7	GPIO50_UTO_TXD4	B
C17	ADDR5	O	D8	GPIO51_UTO_TXD5	B
A16	ADDR6	O	A7	GPIO52_UTO_TXD6	B
B15	ADDR7	O	C8	GPIO53_UTO_TXD7	B
A15	ADDR8	O	B6	GPIO54_UTO_TXSOC	B
C16	ADDR9	O	D6	UTO_CLK	O
B14	ADDR10	O	A6	GPIO55_UTO_TXENB	B
D15	ADDR11	O	C7	UTO_TXCLAV	I
A14	ADDR12	O	B5	GPIO56_UTO_RXD0	B
C15	ADDR13	O	A5	GPIO57_UTO_RXD1	B
B13	ADDR14	O	C6	GPIO58_UTO_RXD2	B
A13	ADDR15	O	B4	GPIO59_UTO_RXD3	B
C14	ADDR16	O	D5	GPIO60_UTO_RXD4	B
B12	ADDR17	O	A4	GPIO61_UTO_RXD5	B
C13	ADDR18	O	C5	GPIO62_UTO_RXD6	B

Table 1-12. Pin Assignment (Continued)

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
B3	GPIO63_UTO_RXD7	B	AE2	GND	
C4	UTO_RXSOC	I	AC13	GND	
A3	UTO_RXENB	O	AD24	GND	
A2	UTO_RXCLAV	I	P23	GND	
G4	3.3VDD		C24	GND	
T4	3.3VDD		D14	GND	
AC7	3.3VDD		C3	GND	
AC16	3.3VDD		P4	GND	
Y23	3.3VDD		AD3	GND	
L23	3.3VDD		AC14	GND	
D20	3.3VDD		AE25	GND	
D11	3.3VDD		N23	GND	
L4	1.8VDD		B25	GND	
Y4	1.8VDD		D13	GND	
AC11	1.8VDD		D4	GND	
AC20	1.8VDD		V4	GND	
T23	1.8VDD		AC4	GND	
G23	1.8VDD		AC18	GND	
D16	1.8VDD		AF26	GND	
D7	1.8VDD		J23	GND	
A1	GND		A26	GND	
J4	GND		D9	GND	
AF1	GND		K10	GND	
AC9	GND		L10	GND	
AC23	GND		M10	GND	
V23	GND		N10	GND	
D23	GND		P10	GND	
D18	GND		R10	GND	
B2	GND		T10	GND	
N4	GND		U10	GND	

Table 1-12. Pin Assignment (Continued)

Pin #	Pin Name	Direction	Pin #	Pin Name	Direction
K11	GND		T14	GND	
L11	GND		U14	GND	
M11	GND		K15	GND	
N11	GND		L15	GND	
P11	GND		M15	GND	
R11	GND		N15	GND	
T11	GND		P15	GND	
U11	GND		R15	GND	
K12	GND		T15	GND	
L12	GND		U15	GND	
M12	GND		K16	GND	
N12	GND		L16	GND	
P12	GND		M16	GND	
R12	GND		N16	GND	
T12	GND		P16	GND	
U12	GND		R16	GND	
K13	GND		T16	GND	
L13	GND		U16	GND	
M13	GND		K17	GND	
N13	GND		L17	GND	
P13	GND		M17	GND	
R13	GND		N17	GND	
T13	GND		P17	GND	
U13	GND		R17	GND	
K14	GND		T17	GND	
L14	GND		U17	GND	
M14	GND				
N14	GND				
P14	GND				
R14	GND				

1.9 PIN ASSIGNMENT FIGURE

S3C2510 416PBGA2727
TOP VIEW

A1 CORNER

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	UTO_RX CLAV	UTO_RX ENB	GPIO61 _UTO _RXD5	GPIO57 _UTO _RXD1	GPIO55 _UTO _TXENB	GPIO52 _UTO _TXD6	GPIO48 _UTO _TXD2	GPIO46 _UTO _TXD0	GPIO45 _UTO _TXAD2	ADDR22	ADDR19	ADDR15	ADDR12	ADDR8	ADDR6	ADDR2	XDATA3 1	XDATA2 8	XDATA2 4	XDATA2 2	XDATA1 8	XDATA1 4	XDATA1 1	XDATA9	GND	A
B	MDC	GND	GPIO63 _UTO _RXD7	GPIO59 _UTO _RXD3	GPIO56 _UTO _RXD0	GPIO54 _UTO _TXSOC	GPIO50 _UTO _TXD4	GPIO47 _UTO _TXD1	UTO _RXAD1	GPIO43 _UTO _TXAD0	ADDR20	ADDR17	ADDR14	ADDR10	ADDR7	ADDR4	ADDR0	XDATA3 0	XDATA2 6	XDATA2 3	XDATA1 9	XDATA1 5	XDATA1 2	XDATA1 0	GND	XDATA8	B
C	COL_0	MDIO	GND	UTO _RXSOC	GPIO62 _UTO _RXD6	GPIO58 _UTO _RXD2	UTO_TX CLAV	GPIO53 _UTO _TXD7	GPIO49 _UTO _TXD3	UTO _RXAD2	GPIO44 _UTO _TXAD1	ADDR21	ADDR18	ADDR16	ADDR13	ADDR9	ADDR5	ADDR1	XDATA2 9	XDATA2 5	XDATA2 1	XDATA1 7	XDATA1 3	GND	XDATA5	XDATA7	C
D	TXD1_L OOP10_ 0	TX_CLK _0	TXDO_0	GND	GPIO60 _UTO _RXD4	UTO _CLK	1.8VDD	GPIO51 _UTO _TXD5	GND	UTO _RXAD0	3.3VDD	ADDR23	GND	GND	ADDR11	1.8VDD	ADDR3	GND	XDATA2 7	3.3VDD	XDATA2 0	XDATA1 6	GND	XDATA6	XDATA1	XDATA3	D
E	TX_ERR _PCOM P_10M_ 0	TXD2_0	TX_EN_ 0	TXD3_0																			XDATA2	XDATA4	nSDRAS	nSDCAS	E
F	RXD1_0	CRS_0	RXD0_0	RX_CLK _0																			nSDWE	XDATA0	nWBE3/ DQM3	nSDCS0	F
G	RXD3_0	RXD2_0	RX_DV_ LINK10_ 0	3.3VDD																			1.8VDD	nSDCS1	n0E	nWBE1/ DQM1	G
H	TX_CLK _1	RX_ERR _0	TXD0_1	COL_1																			nWBE0/ DQM0	nWBE2/ DQM2	nMCS5	nMCS6	H
J	TXD2_1	TXD1_L OOP10_ 1	TX_EN_ 1	GND																			GND	nMCS7	nMCS2	nMCS4	J
K	TX_ERR _PCOM P_10M_ 1	TXD3_1	RXD0_1	CRS_1						GND	GND	GND	GND	GND	GND	GND	GND						nMCS1	nMCS3	nEWAIT	nMCS0	K
L	RXD1_1	RX_CLK _1	RX_DV_ LINK10_ 1	1.8VDD						GND	GND	GND	GND	GND	GND	GND	GND						3.3VDD	CKE	PCICLK RUN	XBMAC K	L
M	RXD3_1	RXD2_1	1.8VDD_ A	USB_CL KSEL						GND	GND	GND	GND	GND	GND	GND	GND						HCLKO	XBMRE Q	PCICCD 1	PCICCD 2	M
N	USB_XC LK	RX_ERR _1	1.8VDD_ A	GND						GND	GND	GND	GND	GND	GND	GND	GND						GND	PCICVS 1	PCICVS 2	PCIAD0	N
P	GND_A	USB_FIL TER	GND_A	GND						GND	GND	GND	GND	GND	GND	GND	GND						GND	PCIAD1	PCIAD2	PCIAD3	P
R	1.8VDD_ A	FILTER	GND_A	PCI_ FILTER						GND	GND	GND	GND	GND	GND	GND	GND						PCIAD4	PCIAD5	PCIAD6	PCIAD7	R
T	1.8VDD_ A	PHY_FIL TER	XCLK	3.3VDD						GND	GND	GND	GND	GND	GND	GND	GND						1.8VDD	PCICBE 0	PCIAD8	PCIAD9	T
U	CLKSEL	GND_A	PHY_CL KSEL	SCL						GND	GND	GND	GND	GND	GND	GND	GND						PCIAD1 0	PCIAD1 1	PCIAD1 2	PCIAD1 3	U
V	HUSB_O VRCUR RENT0	SDA	HUSB_O VRCUR RENT1	GND																			GND	PCIAD1 4	PCIAD1 5	PCICBE 1	V
W	USB_DN	USB_DP	BIG	HUSB_D P0																			PCIPAR	PCISER R	PCIPER R	PCILOC K	W
Y	HUSB_D N0	PHY_FR EQ	PCI_HO STM	1.8VDD																			3.3VDD	PCISTO P	PCIDEV SEL	PCITRD Y	Y
AA	HUSB_D N1	PCI_PC CDM	PCI_XC LK	HUSB_D P1																			PCICLK 1	PCIIRDY	PCIFRA ME	PCICBE 2	AA
AB	PCI_CL KSEL	nRESET	BUS_FR EQ1	CLK_MO D1																			PCIAD1 6	PCIAD1 7	PCIAD1 8	PCIAD1 9	AB
AC	BUS_FR EQ0	CLK_MO D0	CPU_FR EQ0	GND	TCK	GPIO3	3.3VDD	GPIO10 _xINT2	GND	GPIO18 _xGDMA _Ack0	1.8VDD	GPIO26 _TIMER 4	GND	GND	GPIO36 _HUTXD 1	3.3VDD	GPIO40 _HUnCT S1	GND	PCIREQ 5	1.8VDD	PCIGNT 1	PCIAD3 0	GND	PCIAD2 0	PCIAD2 1	PCIAD2 2	AC
AD	CPU_FR EQ1	BUS_FR EQ2	GND	TD0	GPIO0	GPIO4	GPIO8_x INT0	GPIO12 _xINT4	GPIO16 _xGDMA _Req2	GPIO20 _xGDMA _Ack2	GPIO24 _TIMER 2	PHY _CLK0	GPIO30 _HUnDT R0	GPIO32 _HUnRT S0	UCLK	GPIO38 _HUnDS R1	GPIO42 _CURXD	PCICLK 3	PCIGNT 5	PCIGNT 3	PCIREQ 2	PCIAD3 1	PCIAD2 7	GND	PCIAD2 3	PCICBE 3	AD
AE	CPU_FR EQ2	GND	BOSIZE 1	TMS	nTRST	GPIO2	GPIO6	GPIO9 _xINT1	GPIO13 _xINT5	GPIO15 _xGDMA _Req1	GPIO19 _xGDMA _Ack1	GPIO22 _TIMER 0	GPIO25 _TIMER 3	GPIO28 _HURXD 0	GPIO31 _HUnDS R0	GPIO34 _HUnDC D0	GPIO37 _HUnDT R1	GPIO41 _HUnDC D1	PCIRST	PCIREQ 4	PCIGNT 2	PCIPME	PCIAD2 8	PCICLK 2	GND	PCIAD2 4	AE
AF	GND	BOSIZE 0	TMODE	TD1	GPIO1	GPIO5	GPIO7	GPIO11 _xINT3	GPIO14 _xGDMA _Req0	GPIO17 _xGDMA _Req3	GPIO21 _xGDMA _Ack3	GPIO23 _TIMER 1	GPIO27 _TIMER 5	GPIO29 _HUTXD 0	GPIO33 _HUnCT S0	GPIO35 _HURXD 1	GPIO39 _HUnRT S1	CUTXD	PCIINTA	PCIGNT 4	PCIREQ 3	PCIREQ 1	PCIAD2 9	PCIAD2 6	PCIAD2 5	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 1-6. Pin Assignment Figure

SAMSUNG ELECTRONICS