



PD- 94080

IRFB4710

IRFS4710

IRFSL4710

HEXFET® Power MOSFET

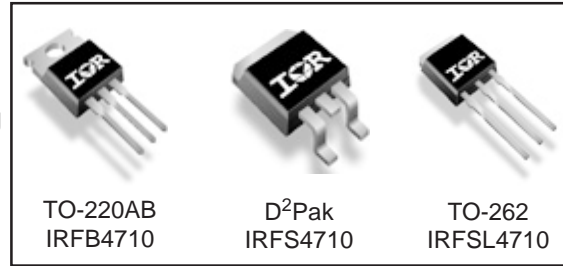
Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies

V_{DSS}	R_{DS(on)} max	I_D
100V	0.014Ω	75A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	75	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	53	
I _{DM}	Pulsed Drain Current ①	300	
P _D @ T _A = 25°C	Power Dissipation ②	3.8	W
P _D @ T _C = 25°C	Power Dissipation	200	W/°C
	Linear Derating Factor	1.4	
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	8.2	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.74	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
R _{θJA}	Junction-to-Ambient⑤	—	62	
R _{θJA}	Junction-to-Ambient⑦	—	40	

Notes ① through ⑦ are on page 11

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International
IR Rectifier

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.011	0.014	Ω	V _{GS} = 10V, I _D = 45A ④
V _{GS(th)}	Gate Threshold Voltage	3.5	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 95V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

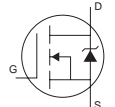
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	35	—	—	S	V _{DS} = 50V, I _D = 45A
Q _g	Total Gate Charge	—	110	170	nC	I _D = 45A
Q _{gs}	Gate-to-Source Charge	—	43	—		V _{DS} = 50V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	40	—		V _{GS} = 10V,
t _{d(on)}	Turn-On Delay Time	—	35	—	ns	V _{DD} = 50V
t _r	Rise Time	—	130	—		I _D = 45A
t _{d(off)}	Turn-Off Delay Time	—	41	—		R _G = 4.5Ω
t _f	Fall Time	—	38	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	6160	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	440	—		V _{DS} = 25V
C _{riss}	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	1580	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	280	—		V _{GS} = 0V, V _{DS} = 80V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	430	—		V _{GS} = 0V, V _{DS} = 0V to 80V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	190	mJ
I _{AR}	Avalanche Current①	—	45	A
E _{AR}	Repetitive Avalanche Energy①	—	20	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	300		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 45A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	74	110	ns	T _J = 25°C, I _F = 45A
Q _{rr}	Reverse Recovery Charge	—	180	260	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

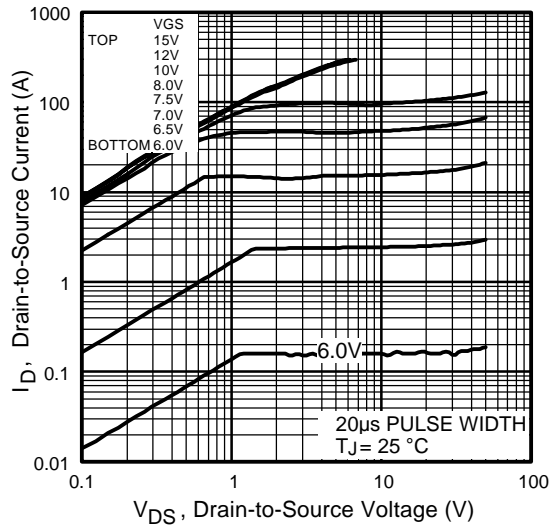


Fig 1. Typical Output Characteristics

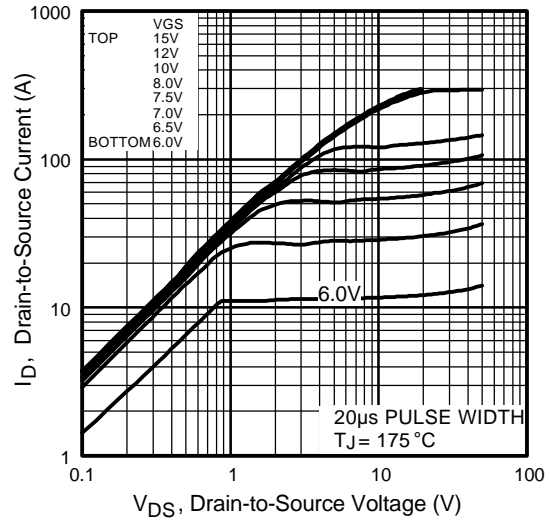


Fig 2. Typical Output Characteristics

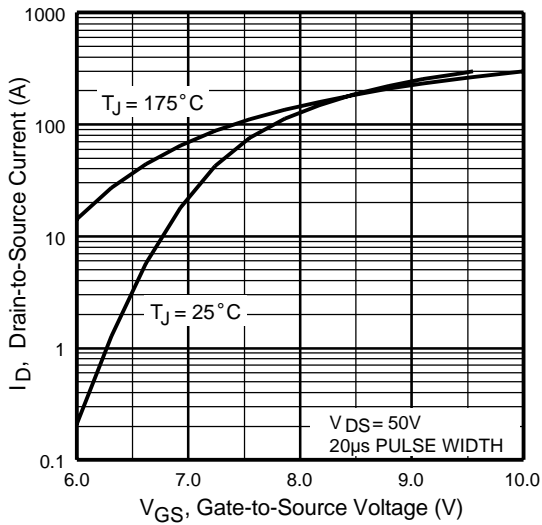


Fig 3. Typical Transfer Characteristics

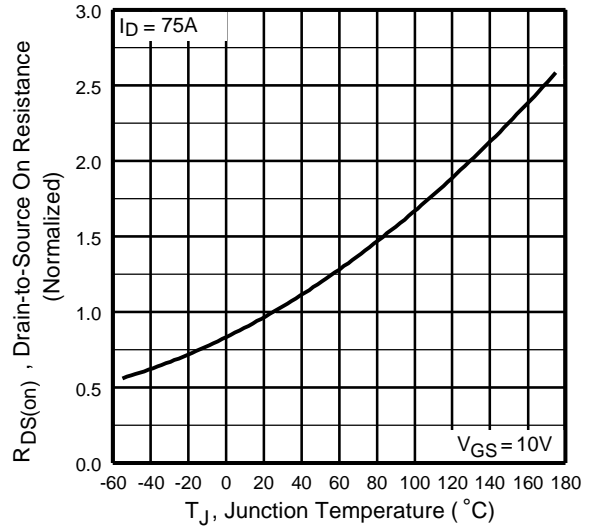


Fig 4. Normalized On-Resistance Vs. Temperature

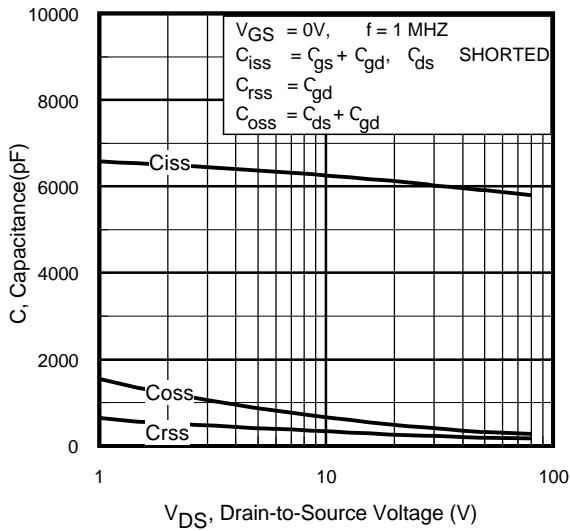


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

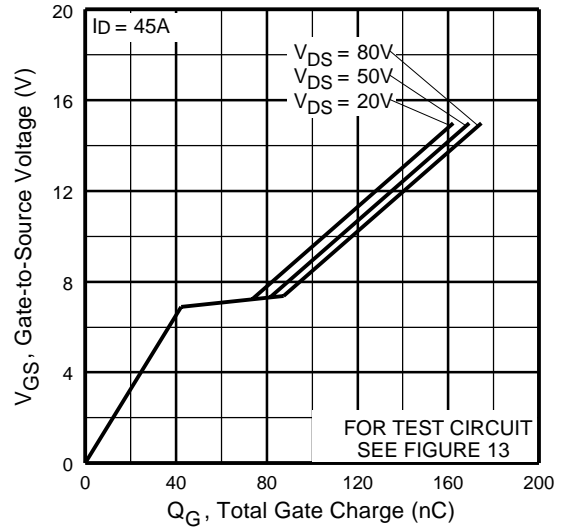


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

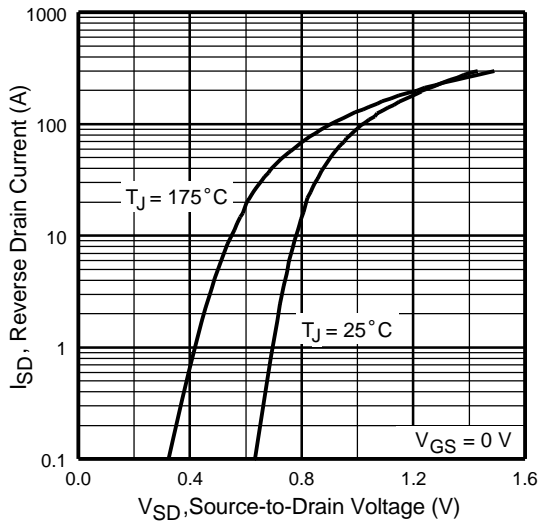


Fig 7. Typical Source-Drain Diode Forward Voltage

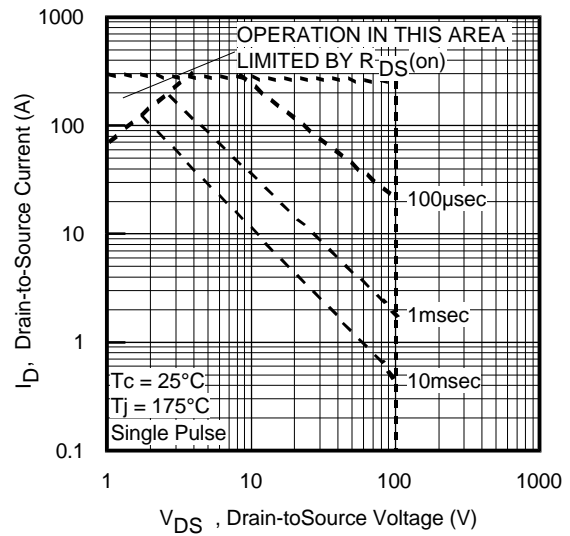


Fig 8. Maximum Safe Operating Area

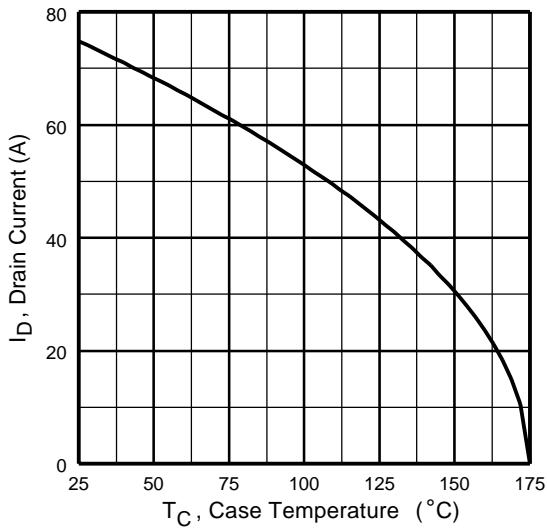


Fig 9. Maximum Drain Current Vs. Case Temperature

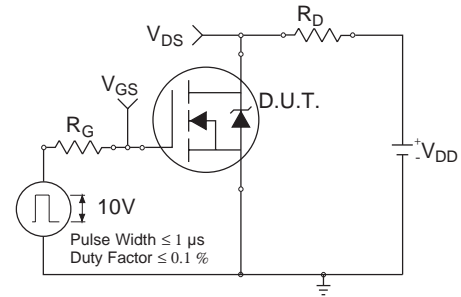


Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

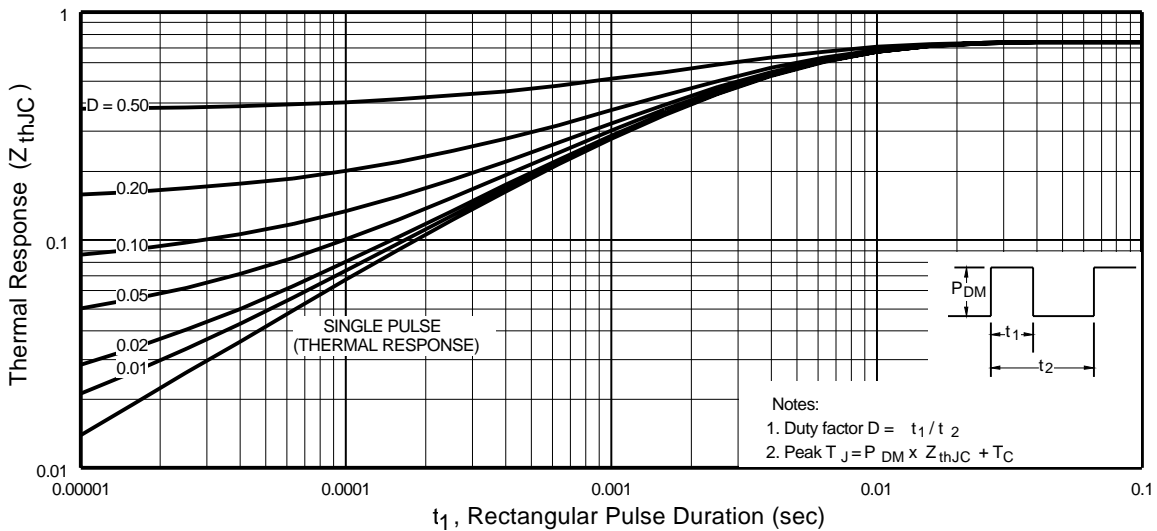


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

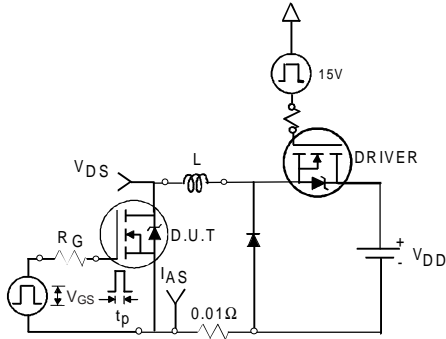


Fig 12a. Unclamped Inductive Test Circuit

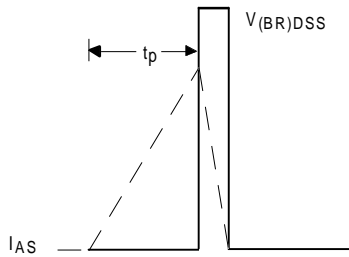


Fig 12b. Unclamped Inductive Waveforms

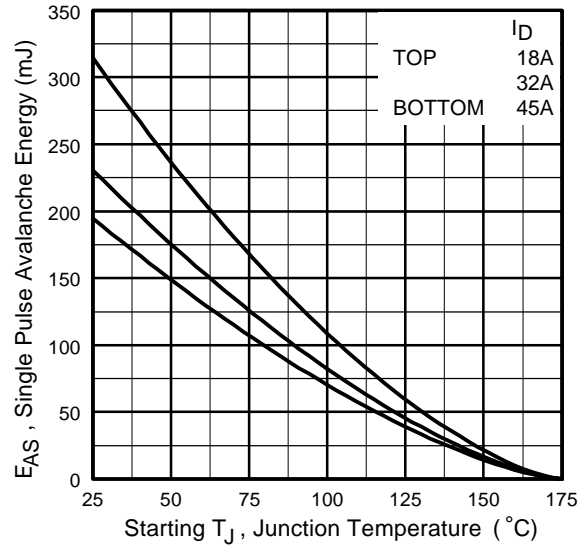


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

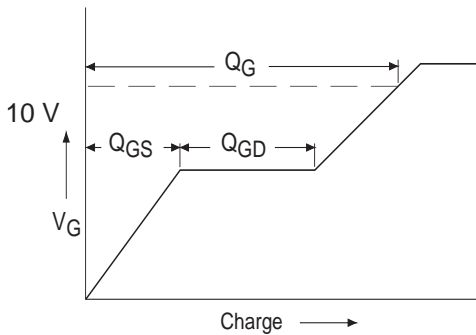


Fig 13a. Basic Gate Charge Waveform

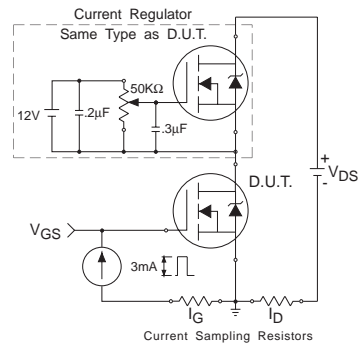


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

IRFB/IRFS/IRFL4710



TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

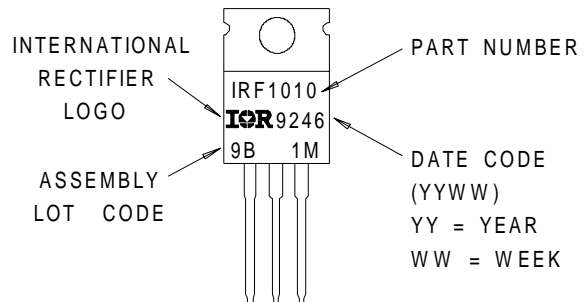


NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010 WITH ASSEMBLY LOT CODE 9B1M



D²Pak Package Outline



NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

D²Pak Part Marking Information



IRFB/IRFS/IRFL4710



TO-262 Package Outline



LEAD ASSIGNMENTS

- 1 = GATE 3 = SOURCE
- 2 = DRAIN 4 = DRAIN

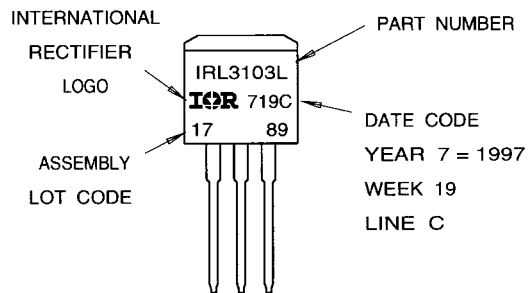


NOTES:

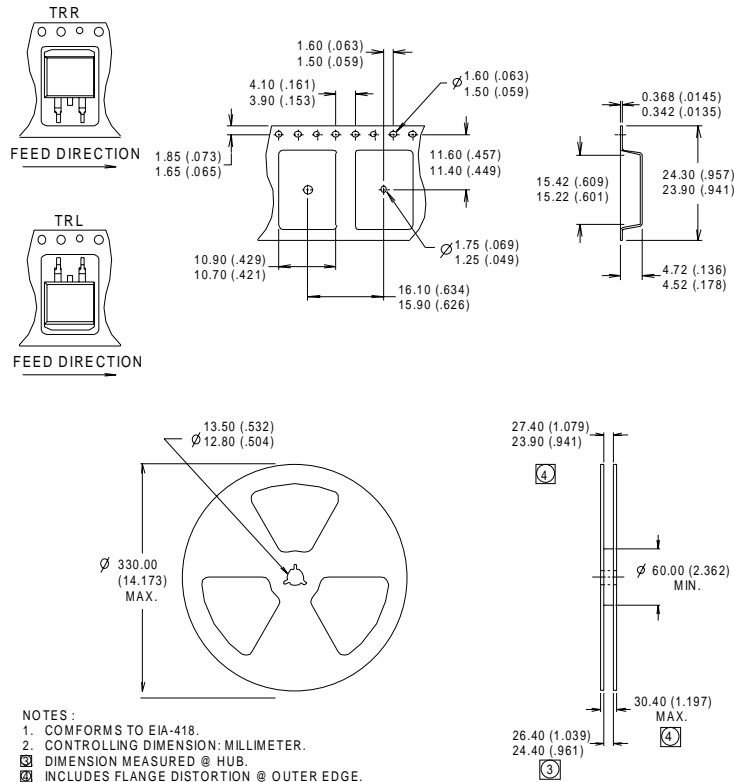
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 190\mu\text{H}$
 $R_G = 25\Omega$, $I_{AS} = 45\text{A}$, $V_{GS} = 10\text{V}$
- ③ $I_{SD} \leq 45\text{A}$, $di/dt \leq 420\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

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