

# DATA SHEET

## **74ALS573B/74ALS574A** Latch flip–flop

Product specification  
IC05 Data Handbook

1991 Feb 08

## Latch/flip-flop

## 74ALS573B/74ALS574A

**74ALS573B** Octal transparent latch (3-State)  
**74ALS574A** Octal D flip-flop (3-State)

### FEATURES

- 74ALS573B is broadside pinout version of 74ALS373
- 74ALS574A is broadside pinout version of 74ALS374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- 74ALS563A and 74ALS564A are inverting version of 74ALS573B and 74ALS574A respectively

### DESCRIPTION

The 74ALS573B is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ( $\overline{OE}$ ) control gates.

The 74ALS573B is functionally identical to the 74ALS373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 74ALS574A is functionally identical to the 74ALS374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ( $\overline{OE}$ ) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The active-Low output enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation. When  $\overline{OE}$  is Low, latched or transparent data appears at the output.

When  $\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

| TYPE      | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|-----------|---------------------------|--------------------------------|
| 74ALS573B | 5.0ns                     | 12mA                           |
| 74ALS574A | 6.0ns                     | 15mA                           |

### ORDERING INFORMATION

| DESCRIPTION                    | ORDER CODE                                                                                      | DRAWING NUMBER |
|--------------------------------|-------------------------------------------------------------------------------------------------|----------------|
|                                | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 10\%$ ,<br>$T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ |                |
| 20-pin plastic DIP             | 74ALS573BN, 74ALS574AN                                                                          | SOT146-1       |
| 20-pin plastic SOL             | 74ALS573BD, 74ALS574AD                                                                          | SOT163-1       |
| 20-pin plastic SSOP<br>Type II | 74ALS573BDB,<br>74ALS574ADB                                                                     | SOT339-1       |

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

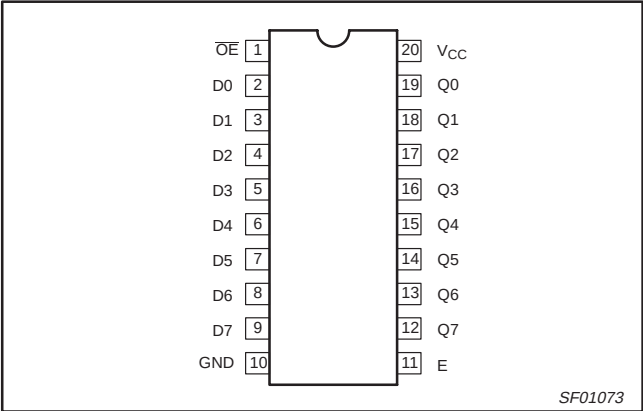
| PINS            | DESCRIPTION                            | 74ALS (U.L.)<br>HIGH/LOW | LOAD VALUE<br>HIGH/LOW |
|-----------------|----------------------------------------|--------------------------|------------------------|
| D0 – D7         | Data inputs                            | 1.0/1.0                  | 20 $\mu$ A/0.2mA       |
| E (74ALS573B)   | Latch enable input                     | 1.0/1.0                  | 20 $\mu$ A/0.1mA       |
| $\overline{OE}$ | Output Enable input (active-Low)       | 1.0/1.0                  | 20 $\mu$ A/0.1mA       |
| CP (74ALS574A)  | Clock pulse input (active rising edge) | 1.0/2.0                  | 20 $\mu$ A/0.2mA       |
| Q0 – Q7         | Data outputs                           | 130/240                  | 2.6mA/24mA             |

**NOTE:** One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

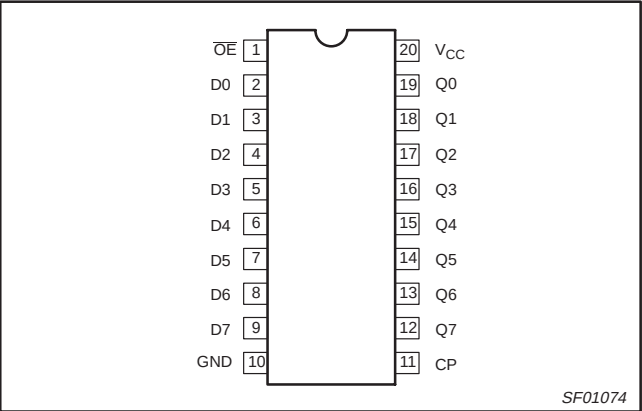
Latch/flip-flop

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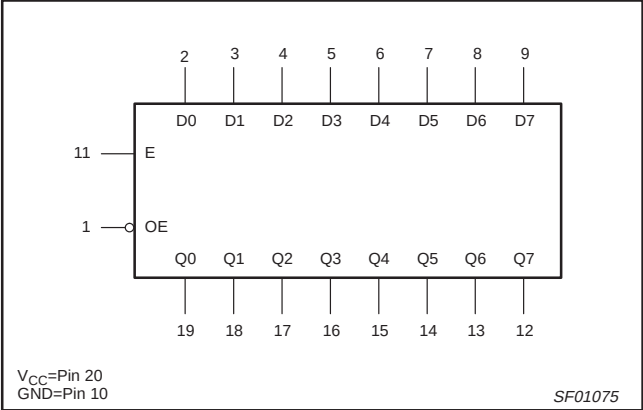
PIN CONFIGURATION – 74ALS573B



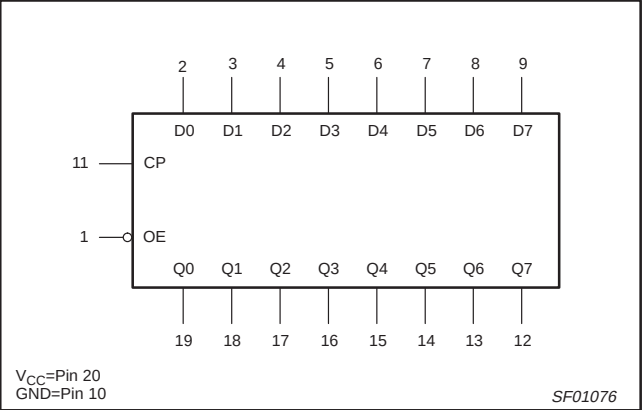
PIN CONFIGURATION – 74ALS574A



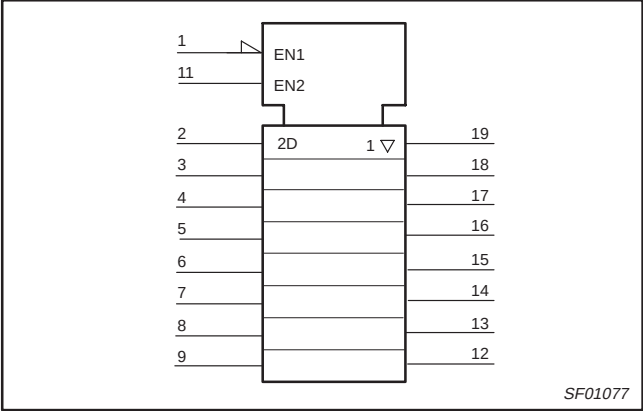
LOGIC SYMBOL – 74ALS573B



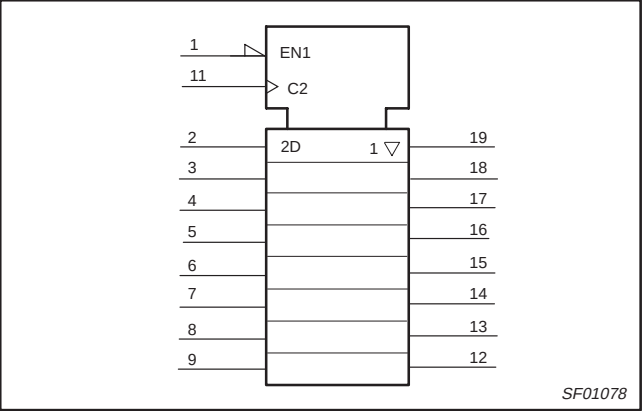
LOGIC SYMBOL – 74ALS574A



IEC/IEEE SYMBOL – 74ALS573B



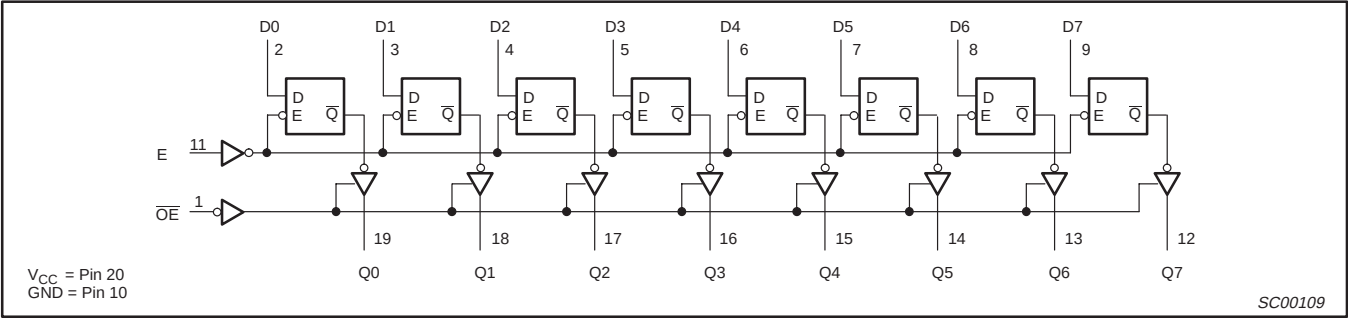
IEC/IEEE SYMBOL – 74ALS574A



Latch/flip-flop

74ALS573B/74ALS574A

LOGIC DIAGRAM – 74ALS573B

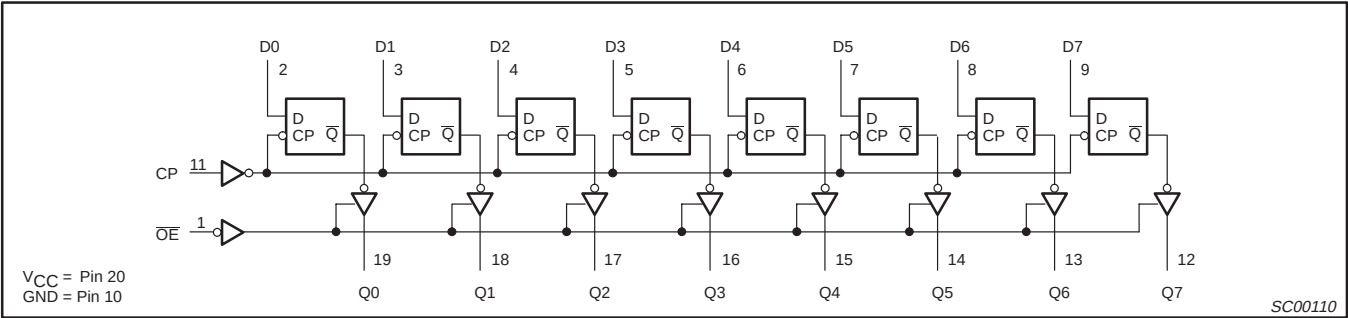


FUNCTION TABLE – 74ALS573B

| INPUTS          |   |    | OUTPUTS<br>REGISTER | INTERNAL | OPERATING MODE           |
|-----------------|---|----|---------------------|----------|--------------------------|
| $\overline{OE}$ | E | Dn |                     | Q0 – Q7  |                          |
| L               | H | L  | L                   | L        | Enable and read register |
| L               | H | H  | H                   | H        |                          |
| L               | ↓ | l  | L                   | L        | Latch and read register  |
| L               | ↓ | h  | H                   | H        |                          |
| L               | L | X  | NC                  | NC       | Hold                     |
| H               | L | X  | NC                  | Z        | Disable outputs          |
| H               | H | Dn | Dn                  | Z        |                          |

H = High-voltage level  
h = High state must be present one setup time before the High-to-Low enable transition  
L = Low-voltage level  
l = Low state must be present one setup time before the High-to-Low enable transition  
NC= No change  
X = Don't care  
Z = High impedance "off" state  
↓ = High-to-Low enable transition

LOGIC DIAGRAM – 74ALS574A



## Latch/flip-flop

## 74ALS573B/74ALS574A

FUNCTION TABLE – 74ALS574A

| INPUTS          |            |    | OUTPUTS<br>REGISTER | INTERNAL | OPERATING MODE          |
|-----------------|------------|----|---------------------|----------|-------------------------|
| $\overline{OE}$ | CP         | Dn |                     | Q0 – Q7  |                         |
| L               | $\uparrow$ | L  | L                   | L        | Latch and read register |
| L               | $\uparrow$ | h  | H                   | H        |                         |
| L               | $\uparrow$ | X  | NC                  | NC       | Hold                    |
| H               | $\uparrow$ | X  | NC                  | Z        | Disable outputs         |
| H               | $\uparrow$ | Dn | Dn                  | Z        |                         |

H = High-voltage level

h = High state must be present one setup time before the Low-to-High clock transition

L = Low-voltage level

L = Low state must be present one setup time before the Low-to-High clock transition

NC = No change

X = Don't care

Z = High impedance "off" state

 $\uparrow$  = Low-to-High clock transition $\uparrow$  = Not Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL    | PARAMETER                                      | RATING           | UNIT |
|-----------|------------------------------------------------|------------------|------|
| $V_{CC}$  | Supply voltage                                 | –0.5 to +7.0     | V    |
| $V_{IN}$  | Input voltage                                  | –0.5 to +7.0     | V    |
| $I_{IN}$  | Input current                                  | –30 to +5        | mA   |
| $V_{OUT}$ | Voltage applied to output in High output state | –0.5 to $V_{CC}$ | V    |
| $I_{OUT}$ | Current applied to output in Low output state  | 48               | mA   |
| $T_{amb}$ | Operating free-air temperature range           | 0 to +70         | °C   |
| $T_{stg}$ | Storage temperature range                      | –65 to +150      | °C   |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL    | PARAMETER                            | LIMITS |     |      | UNIT |
|-----------|--------------------------------------|--------|-----|------|------|
|           |                                      | MIN    | NOM | MAX  |      |
| $V_{CC}$  | Supply voltage                       | 4.5    | 5.0 | 5.5  | V    |
| $V_{IH}$  | High-level input voltage             | 2.0    |     |      | V    |
| $V_{IL}$  | Low-level input voltage              |        |     | 0.8  | V    |
| $I_{IK}$  | Input clamp current                  |        |     | –18  | mA   |
| $I_{OH}$  | High-level output current            |        |     | –2.6 | mA   |
| $I_{OL}$  | Low-level output current             |        |     | 24   | mA   |
| $T_{amb}$ | Operating free-air temperature range | 0      |     | +70  | °C   |

## Latch/flip-flop

## 74ALS573B/74ALS574A

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL    | PARAMETER                                               |           | TEST CONDITIONS <sup>1</sup>                                             | LIMITS                   |                  |      | UNIT          |
|-----------|---------------------------------------------------------|-----------|--------------------------------------------------------------------------|--------------------------|------------------|------|---------------|
|           |                                                         |           |                                                                          | MIN                      | TYP <sup>2</sup> | MAX  |               |
| $V_{OH}$  | High-level output voltage                               |           | $V_{CC} = \pm 10\%$ , $V_{IL} = \text{MAX}$ ,<br>$V_{IH} = \text{MIN}$   | $I_{OH} = -0.4\text{mA}$ | $V_{CC} - 2$     |      | V             |
|           |                                                         |           |                                                                          | $I_{OH} = \text{MAX}$    | 2.4              | 3.2  | V             |
| $V_{OL}$  | Low-level output voltage                                |           | $V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ ,<br>$V_{IH} = \text{MIN}$ | $I_{OL} = 12\text{mA}$   | 0.25             | 0.40 | V             |
|           |                                                         |           |                                                                          | $I_{OL} = 24\text{mA}$   | 0.35             | 0.50 | V             |
| $V_{IK}$  | Input clamp voltage                                     |           | $V_{CC} = \text{MIN}$ , $I_I = I_{IK}$                                   |                          | -0.73            | -1.2 | V             |
| $I_I$     | Input current at minimum input voltage                  |           | $V_{CC} = \text{MAX}$ , $V_I = 7.0\text{V}$                              |                          |                  | 0.1  | mA            |
| $I_{IH}$  | High-level input current                                |           | $V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$                              |                          |                  | 20   | $\mu\text{A}$ |
| $I_{IL}$  | Low-level input current                                 | 74ALS573B | $V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$                              |                          |                  | -0.1 | mA            |
|           |                                                         | 74ALS574A | $V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$                              |                          |                  | -0.2 | mA            |
| $I_{OZH}$ | Off-state output current,<br>High-level voltage applied |           | $V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$                              |                          |                  | 20   | $\mu\text{A}$ |
| $I_{OZL}$ | Off-state output current,<br>Low-level voltage applied  |           | $V_{CC} = \text{MAX}$ , $V_I = 0.4\text{V}$                              |                          |                  | -20  | $\mu\text{A}$ |
| $I_O$     | Output current <sup>3</sup>                             |           | $V_{CC} = \text{MAX}$ , $V_O = 2.25\text{V}$                             | -30                      |                  | -112 | mA            |
| $I_{CC}$  | Supply current (total)                                  | 74ALS573B | $V_{CC} = \text{MAX}$                                                    |                          | 7                | 12   | mA            |
|           |                                                         |           |                                                                          |                          | 13               | 21   | mA            |
|           |                                                         |           |                                                                          |                          | 15               | 24   | mA            |
|           |                                                         | 74ALS574A | $V_{CC} = \text{MAX}$                                                    |                          | 10               | 16   | mA            |
|           |                                                         |           |                                                                          |                          | 17               | 27   | mA            |
|           |                                                         |           |                                                                          |                          | 18               | 28   | mA            |

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## Latch/flip-flop

## 74ALS573B/74ALS574A

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL                 | PARAMETER                                     |           | TEST CONDITION           | LIMITS                                                                                                                            |              | UNIT |
|------------------------|-----------------------------------------------|-----------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------|--------------|------|
|                        |                                               |           |                          | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$<br>$V_{CC} = +5.0\text{V} \pm 10\%$<br>$C_L = 50\text{pF}, R_L = 500\Omega$ |              |      |
|                        |                                               |           |                          | MIN                                                                                                                               | MAX          |      |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>Dn to Qn                 | 74ALS573B | Waveform 3               | 2.0<br>2.0                                                                                                                        | 10.0<br>10.0 | ns   |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>E to Qn                  |           | Waveform 2               | 4.0<br>4.0                                                                                                                        | 12.0<br>12.0 | ns   |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>to High or Low level    |           | Waveform 6<br>Waveform 7 | 2.0<br>4.0                                                                                                                        | 9.0<br>11.0  | ns   |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>from High or Low level |           | Waveform 6<br>Waveform 7 | 1.0<br>2.0                                                                                                                        | 9.0<br>11.0  | ns   |
| $f_{MAX}$              | Maximum clock frequency                       | 74ALS574A | Waveform 1               | 45                                                                                                                                |              | MHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to Qn                 |           | Waveform 1               | 3.0<br>4.0                                                                                                                        | 12.0<br>12.0 | ns   |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>to High or Low level    |           | Waveform 6<br>Waveform 7 | 2.0<br>4.0                                                                                                                        | 9.0<br>11.0  | ns   |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>from High or Low level |           | Waveform 6<br>Waveform 7 | 1.0<br>2.0                                                                                                                        | 9.0<br>11.0  | ns   |

## AC SETUP CHARACTERISTICS

| SYMBOL                     | PARAMETER                           |           | TEST CONDITION | LIMITS                                                                                                                            |     | UNIT |
|----------------------------|-------------------------------------|-----------|----------------|-----------------------------------------------------------------------------------------------------------------------------------|-----|------|
|                            |                                     |           |                | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$<br>$V_{CC} = +5.0\text{V} \pm 10\%$<br>$C_L = 50\text{pF}, R_L = 500\Omega$ |     |      |
|                            |                                     |           |                | MIN                                                                                                                               | MAX |      |
| $t_{su(H)}$<br>$t_{su(L)}$ | Setup time, High or Low<br>Dn to E  | 74ALS573B | Waveform 4     | 6.0<br>6.0                                                                                                                        |     | ns   |
| $t_h(H)$<br>$t_h(L)$       | Hold time, High or Low<br>Dn to E   |           | Waveform 4     | 6.0<br>6.0                                                                                                                        |     | ns   |
| $t_w(H)$                   | E Pulse width, High                 |           | Waveform 1     | 10.0                                                                                                                              |     | ns   |
| $t_{su(H)}$<br>$t_{su(L)}$ | Setup time, High or Low<br>Dn to CP | 74ALS574A | Waveform 5     | 6.0<br>6.0                                                                                                                        |     | ns   |
| $t_h(H)$<br>$t_h(L)$       | Hold time, High or Low<br>Dn to CP  |           | Waveform 5     | 1.0<br>1.0                                                                                                                        |     | ns   |
| $t_w(H)$<br>$t_w(L)$       | CP Pulse width,<br>High or Low      |           | Waveform 5     | 8.0<br>12.0                                                                                                                       |     | ns   |

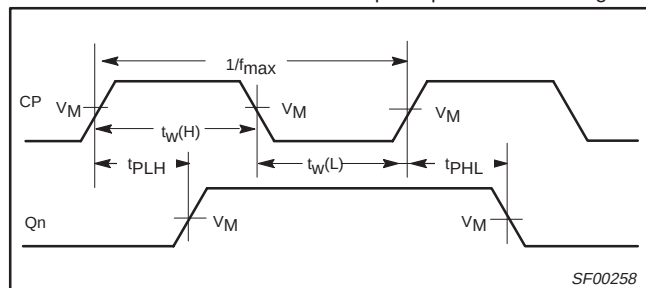
## Latch/flip-flop

## 74ALS573B/74ALS574A

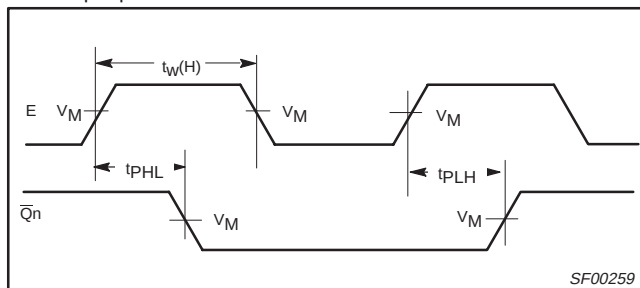
## AC WAVEFORMS

For all waveforms,  $V_M = 1.3V$ .

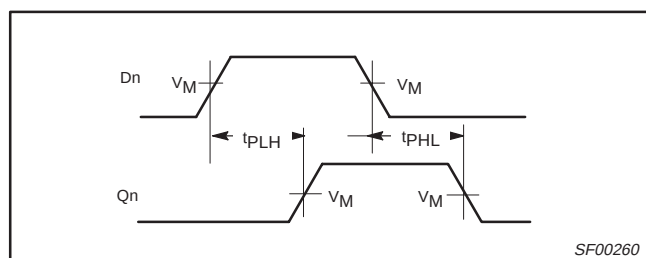
The shaded areas indicate when the input is permitted to change for predictable output performance.



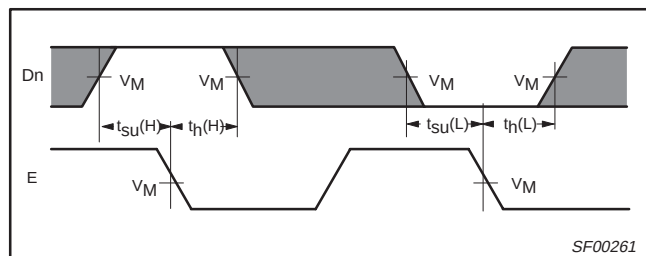
**Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Widths, and Maximum Clock Frequency**



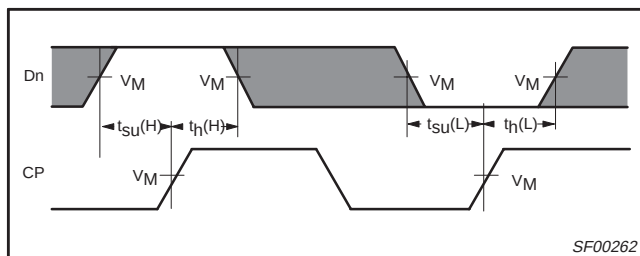
**Waveform 2. Propagation Delay for Enable to Output and Enable Pulse Width**



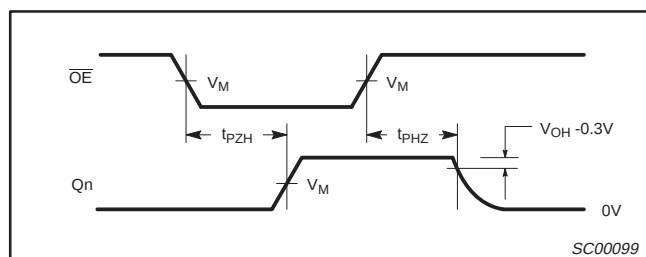
**Waveform 3. Propagation Delay for Data to Output**



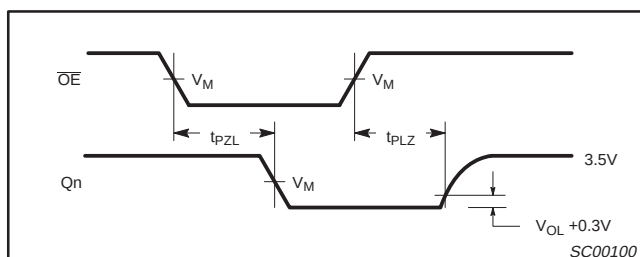
**Waveform 4. Data Setup Time and Hold Times**



**Waveform 5. Data Setup Time and Hold Times**



**Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



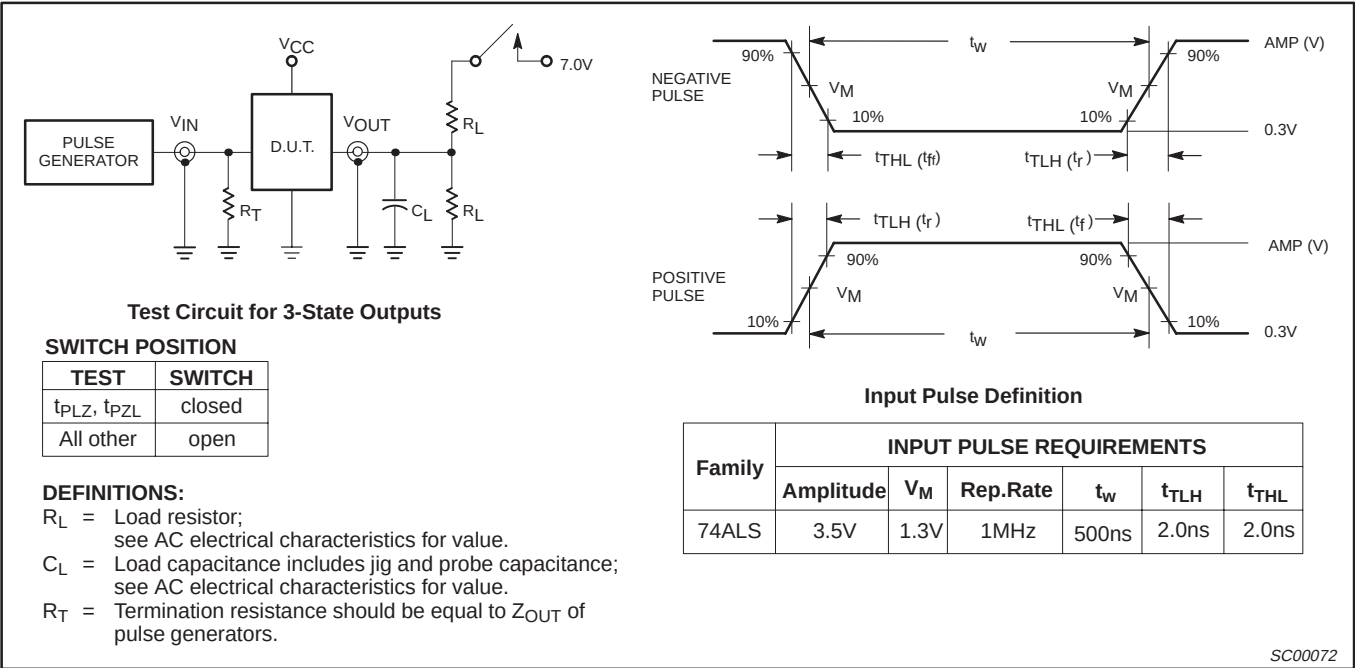
**Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**



Latch/flip-flop

74ALS573B/74ALS574A

TEST CIRCUIT AND WAVEFORMS

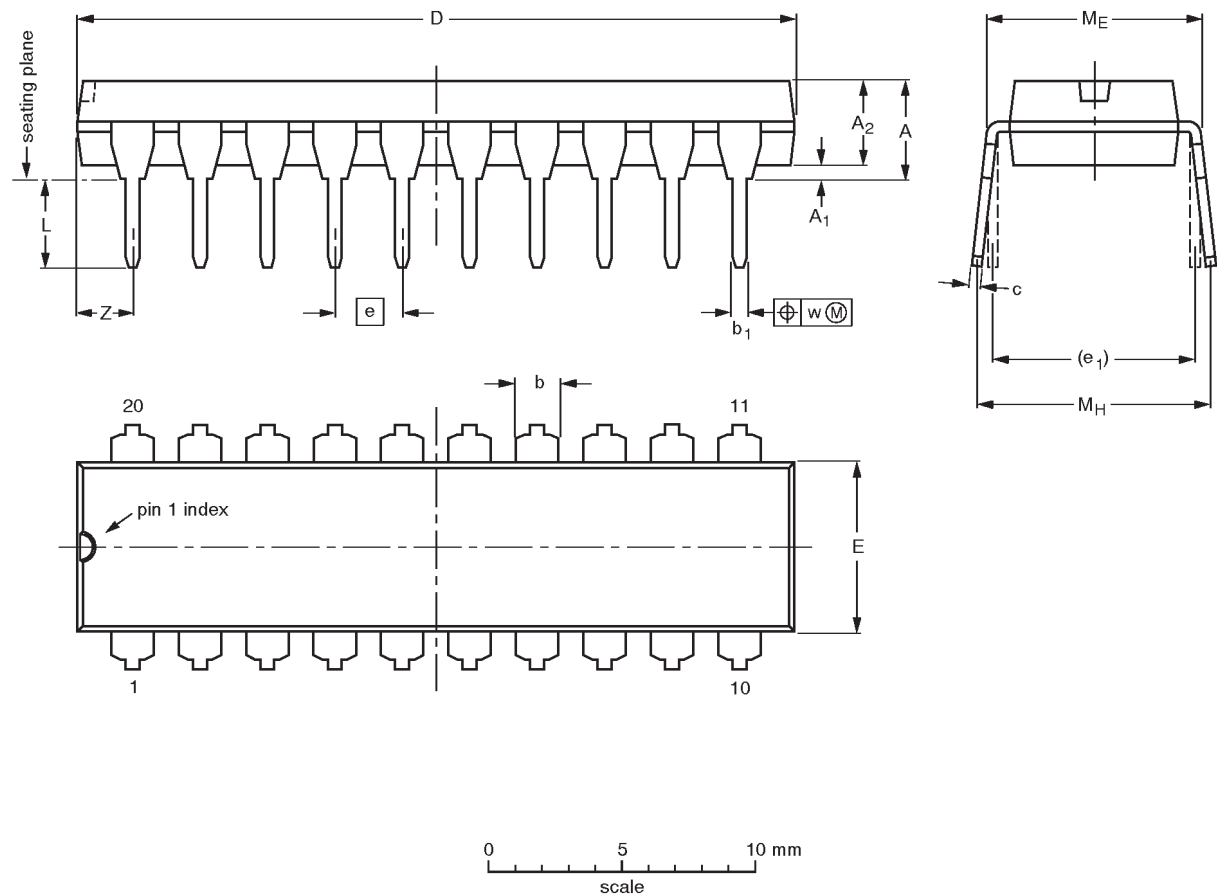


Latch/flip-flop

74ALS573B/74ALS574A

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.2    | 0.51                | 3.2                 | 1.73<br>1.30   | 0.53<br>0.38   | 0.36<br>0.23   | 26.92<br>26.54   | 6.40<br>6.22     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.0                   |
| inches | 0.17   | 0.020               | 0.13                | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045   | 0.25<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.078                 |

**Note**  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

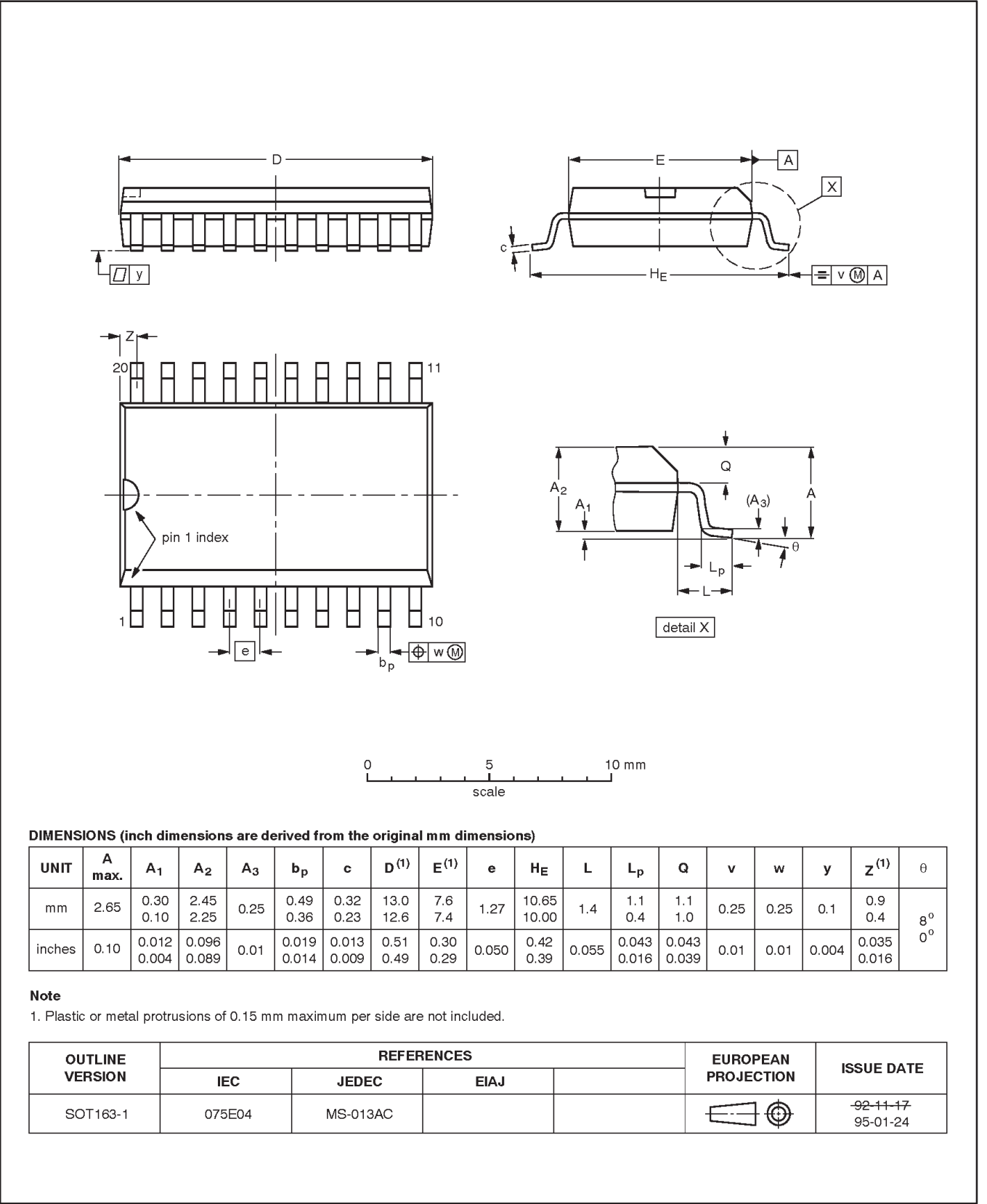
| OUTLINE<br>VERSION | REFERENCES |       |       |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|-------|-------|--|------------------------|----------------------|
|                    | IEC        | JEDEC | EIAJ  |  |                        |                      |
| SOT146-1           |            |       | SC603 |  |                        | 92-11-17<br>95-05-24 |

Latch/flip-flop

74ALS573B/74ALS574A

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

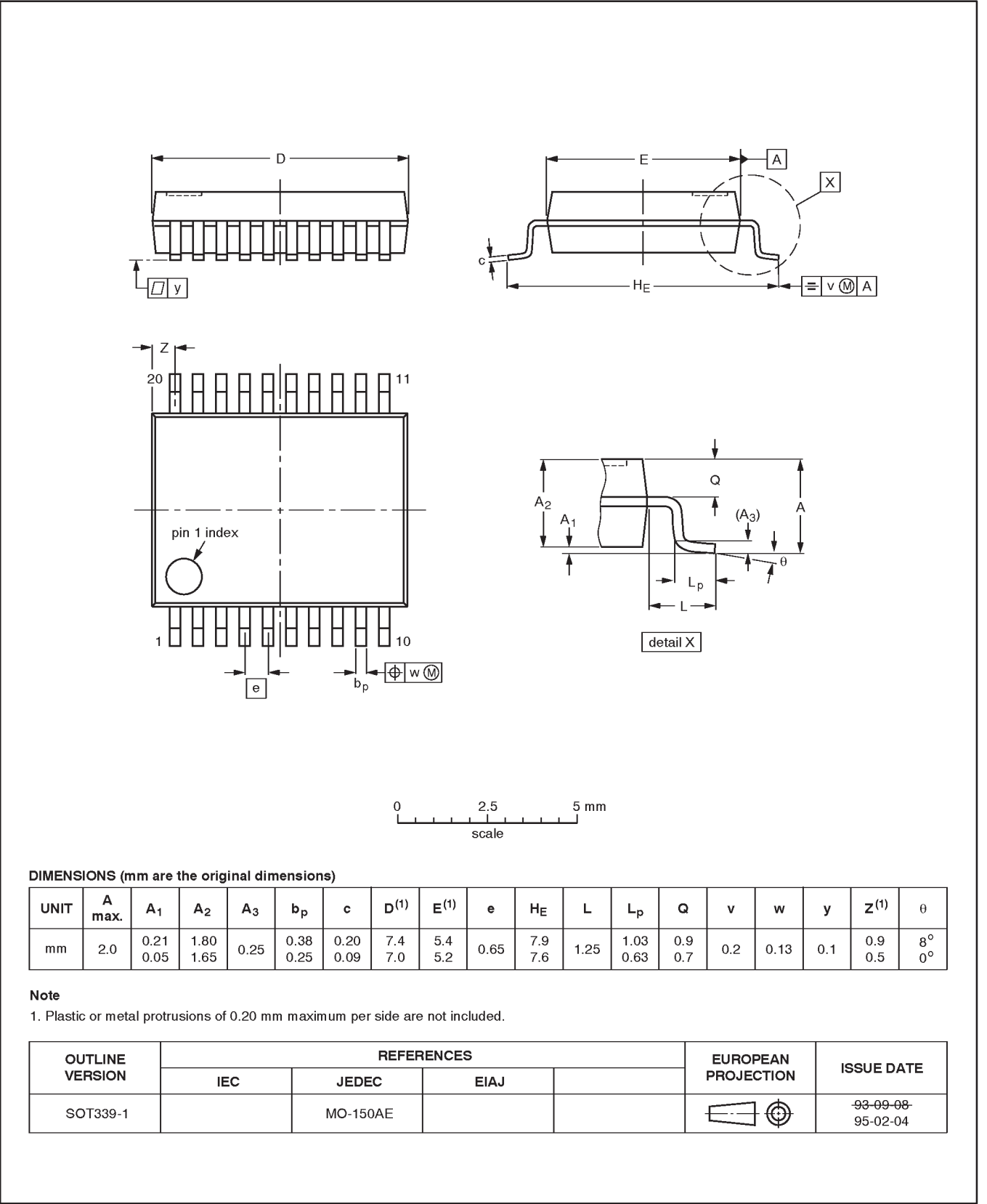


Latch/flip-flop

74ALS573B/74ALS574A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



Latch/flip–flop

74ALS573B/74ALS574A

| DEFINITIONS               |                        |                                                                                                                                                                                                                                                            |
|---------------------------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data Sheet Identification | Product Status         | Definition                                                                                                                                                                                                                                                 |
| Objective Specification   | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.                                                                                                         |
| Preliminary Specification | Preproduction Product  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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