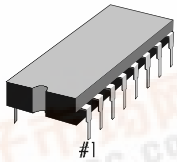
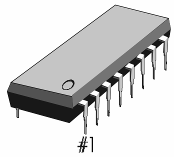
INTRODUCTION

The S5T8554B/7B are single-chip PCM encoders and decoders (PCM CODECs) and PCM line filters. These devices provide all the functions required to interface a full-duplex voice telephone circuit with a time-division-multiplex (TDM) system.
These devices are designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering functions in PCM system. They are intended to be used at the analog termination of a PCM line or trunk.
These devices provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signalling and supervision information.

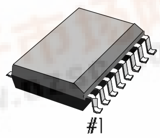
16-CERDIP



16-DIP-300A



8–DIP–300



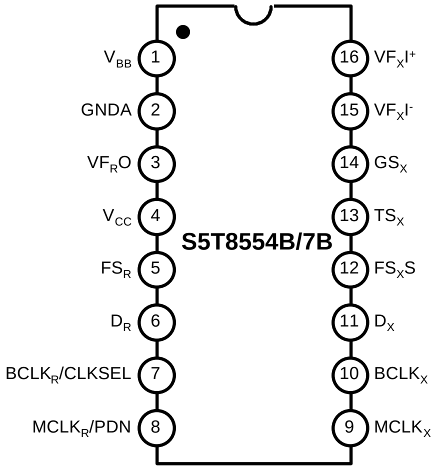
FEATURES

- Complete CODEC and filtering system
- Meets or exceeds AT&T D3/D4 and CCITT specifications
  µ-Law: S5T8554B, A-Law: S5T8557B
- On-chip auto zero, sample and hold, and precision voltage references
- Low power dissipation: 60mW (operating), 3mW (standby)
- ± 5V operation
- TTL or CMOS compatible
- Automatic power down

ORDERING INFORMATION

Device	Package	Operating Temperature
S5T8554B02-L0B0 S5T8557B02-L0B0	16-CERDIP	–25°C to 125°C
S5T8554B01-D0B0 S5T8557B01-D0B0	16-DIP-300A	–25°C to +70°C
S5T8554B01-S0B0 S5T8557B01-S0B0	16-SOP-BD300	–25°C to +70°C

PIN CONFIGURATION



PIN DISCRIPTION

Pin No	Symbol	Description
1	V_{BB}	V_{BB} = –5V ± 5%
2	GNDA	Analog ground.
3	VF_RO	Analog output of the receive power Amp.
4	V_{CC}	V_{CC} = +5 V ± 5%
5	FS_R	Receive frame sync pulse. 8kHz pulse train
6	D_R	PCM data input.
7	$BLCK_R$/ CLKSEL	Logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in normal operation and $BCLK_X$ is used for both TX and RX directions. Alternately direct clock input available, vary from 60kHz to 2.048MHz.
8	$MCLK_R$/ PDN	When $MCLK_R$ is connected continuously high, the device is powered down. Normally connected continuously low, $MCLK_X$ is selected for all DAC timing. Alternately direct 1.536MHz/1.544MHz or 2.048MHz clock input available.
9	$MCLK_X$	Must be 1.536MHz/1.544MHz or 2.048MHz.
10	$BLCK_X$	May be vary from 64kHz to 2.048MHz but $BCLK_X$ is externally tied with $MCLK_X$ in normal operation.
11	D_X	PCM data output.
12	FS_X	TX frame sync pulse. 8kHz pulse train.
13	TS_X	Changed from high to low during the encoder timeslot. Open drain output.
14	GS_X	Analog output of the TX input amplifier. Used to set gain through external resistor.
15	VF_XI^-	Inverting input stage of the TX analog signal.
16	VF_XI^+	Non-inverting input stage of the TX analog signal.

ABSOLUTE MAXIMUM RATING

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	7	V
Negative Supply Voltage	V_{BB}	–7	V
Voltage at Any Analog Input or Output	$V_{I\ (A)}$	V_{CC} + 0.3 ~ V_{BB} - 0.3	V
Voltage at Any Digital Input or Output	$V_{I\ (D)}$	V_{CC} + 0.3 ~ GND_A - 0.3	V
Operating Temperature Range	Ta	–25 ~ +125	°C
Storage Temperature Range	T_{STG}	–65 ~ +150	°C
Lead Temperature (Soldering, 10 secs)	T_{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 5.0V ± 5%, V_{BB} = –5.0V ± 5%, GND_A = 0V, Ta = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0V, V_{BB} = –5.0V, Ta=25°C; all signals referenced to GND_A)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER DISSIPATION						
Power-Down Current	$I_{CC\ (DOWN)}$	No Load	–	0.5	1.5	mA
Power-Down Current	$I_{BB\ (DOWN)}$	No Load	–	0.05	0.3	mA
Active Current	$I_{CC\ (A)}$	No Load	–	6.0	9.0	mA
Active Current	$I_{BB\ (A)}$	No Load	–	6.0	9.0	mA
DIGITAL INTERFACE						
Input Low Voltage	V_{IL}	–	–	–	0.6	V
Input High Voltage	V_{IH}	–	2.2	–	–	V
Input Low Current	I_{IL}	$GND_A \leq V_{IN} \leq V_{IL}$, all digital input	–10	–	10	µA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{CC}$	–10	–	10	µA
Output Low Voltage	V_{OL}	D_X, I_L = 3.2mA SIG_R, I_L = 1.0mA TS_X, I_L = 3.2mA, open drain	–	–	0.4 0.4 0.4	V V V
Output High Voltage	$I_{O\ (HZ)}$	D_X, I_H = –3.2mA SIG_R, I_H = –1.0mA	2.4 2.4	–	–	V V
Output Current in High Impedance State (Tri -state)	$I_{O\ (HZ)}$	D_X, $GND_A \leq V_O \leq V_{CC}$	–10	–	10	µA
ANALOG INTERFACE WITH RECEIVE FILTER						
Output Resistance	R_O	Pin VF_RO	–	1	3	Ω

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 5.0V ± 5%, V_{BB} = –5.0V ± 5%, GND_A = 0V, Ta = 0°C to 70°C;
typical characteristics specified at V_{CC} = 5.0V, V_{BB} = –5.0V, Ta=25°C; all signals referenced to GND_A)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Load Resistance	R_L	VF_RO = ± 2.5V	600	–	–	Ω
Load Capacitance	C_L	–	–	–	500	pF
Output DC Offset Voltage	$V_{OO\ (RX)}$	–	–200	–	200	mV
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
Input Leakage Current	I_{LKG}	-2.5V≤V≤+2.5V, VF_XI+ or VF_XI-	–200	–	200	nA
Input Resistance	R_I	-2.5V≤V≤+2.5V, VF_XI+ or VF_XI-	10	–	–	MΩ
Output Resistance	R_O	Closed loop, unity gain	–	1	3	Ω
Load Resistance	R_L	GS_X	10	–	–	kΩ
Load Capacitance	C_L	GS_X	–	–	50	pF
Output Dynamic Range	$V_{OD\ (TX)}$	GS_X, R_L≤10KW	± 2.8	–	–	V
Voltage Gain	G_V	VF_XI+ to GSX	5,000	–	–	V/N
Unity Gain Bandwidth	BW	–	1	2	–	MHz
Offset Voltage	$V_{IO\ (TX)}$	–	–20	–	20	mV
Common-Mode Voltage	$V_{CM\ (TX)}$	CMRRXA > 60dB	–2.5	–	2.5	V
Common-Mode Rejection Ratio	CMRR	DC Test	60	–	–	dB
Power Supply Rejection Ratio	PSRR	DC Test	60	–	–	dB

TIMING CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 5.0V ± 5%, V_{BB} = –5.0V ± 5%, GND_A = 0V, Ta = 0°C to 70°C;
typical characteristics specified at V_{CC} = 5.0V, V_{BB} = –5.0V, Ta=25°C; all signals referenced to GND_A)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Frequency of Master Clock	f_{MCK}	Depends on the device used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$	–	1.536 1.544 2.048	–	nS
Rise Time of Bit Clock	$t_{R\ (BCK)}$	t_{PB} = 488ns	–	–	50	nS
Fall Time of Bit Clock	$t_{F\ (BCK)}$	t_{PB} = 488ns	–	–	50	nS
Holding Time from Bit Clock Low to Frame Sync	$t_{H\ (LFS)}$	Long frame only	0	–	–	nS
Holding Time from Bit Clock High to Frame Sync	$t_{H\ (RFS)}$	Short frame only	0	–	–	nS
Set-Up Time from Frame Sync to Bit Clock Low	$t_{SU\ (FBCL)}$	Long frame only	80	–	–	nS
Delay Time from $BCLK_X$ High to Data Valid	$t_{D\ (HDV)}$	Load = 150pF plse 2 LSTTL loads	0	–	180	nS
Delay Time to TS_X Low	$t_{D\ (\overline{TSX}L)}$	Load = 150pF plse 2 LSTTL loads	–	–	140	nS
Delay Time from $BCLK_X$ Low to Data Output Disabled	$t_{D\ (LDD)}$	–	50	–	165	nS
Delay Time to Valid Data from FSX or $BCLK_X$, Whichever Comes Later	$t_{D\ (VD)}$	C_L = 0pF to 150pF	20	–	165	nS
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	$t_{SU\ (DRBL)}$	–	50	–	–	nS
Hold Time from $FS_{R/X}$ Low to D_R Invalid	$t_{H\ (BLDR)}$	–	50	–	–	nS
Set-Up Time from $FS_{R/X}$ to $BCLK_{R/X}$ Low	$t_{SU\ (FBLS)}$	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	50	–	–	nS
Width of Master Clock High	$t_{W\ (MCKH)}$	$MCLK_X$ and $MCLK_R$	160	–	–	nS
Width of Master Clock Low	$t_{W\ (MCKL)}$	$MCLK_X$ and $MCLK_R$	160	–	–	nS
Rise Time of Master Clock	$t_{R\ (MCK)}$	$MCLK_X$ and $MCLK_R$	–	–	50	nS
Fall Time of Master Clock	$t_{F\ (MCK)}$	$MCLK_X$ and $MCLK_R$	–	–	50	nS
Set-Up Time from $BCLK_X$ High (and FS_X In Long Frame Sync Mode) to $MCLK_X$ Falling Edge	$t_{SU\ (BHMF)}$	First bit clock after the leading edge FS_X	–	–	–	–

TIMING CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 5.0V ± 5%, V_{BB} = –5.0V ± 5%, GND_A = 0V, Ta = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0V, V_{BB} = –5.0V, Ta=25°C; all signals referenced to GND_A)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Period of Bit Clock	t_{CK}	–	485	488	15,725	nS
Width of Bit Clock High	$t_{W (BCKH)}$	V_{IH} = 2.2	160	–	–	nS
Width of Bit Clock Low	$t_{W (BCKL)}$	VIL = 0.6V	160	–	–	nS
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	$t_{H (BLFL)}$	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	–	–	–	nS
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	$t_{H (3rd)}$	Long frame sync pulse (From 3 to 8 bit clock periods long)	100	–	–	nS
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	–	–	–	nS

NOTE: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

TIMING DIAGRAM

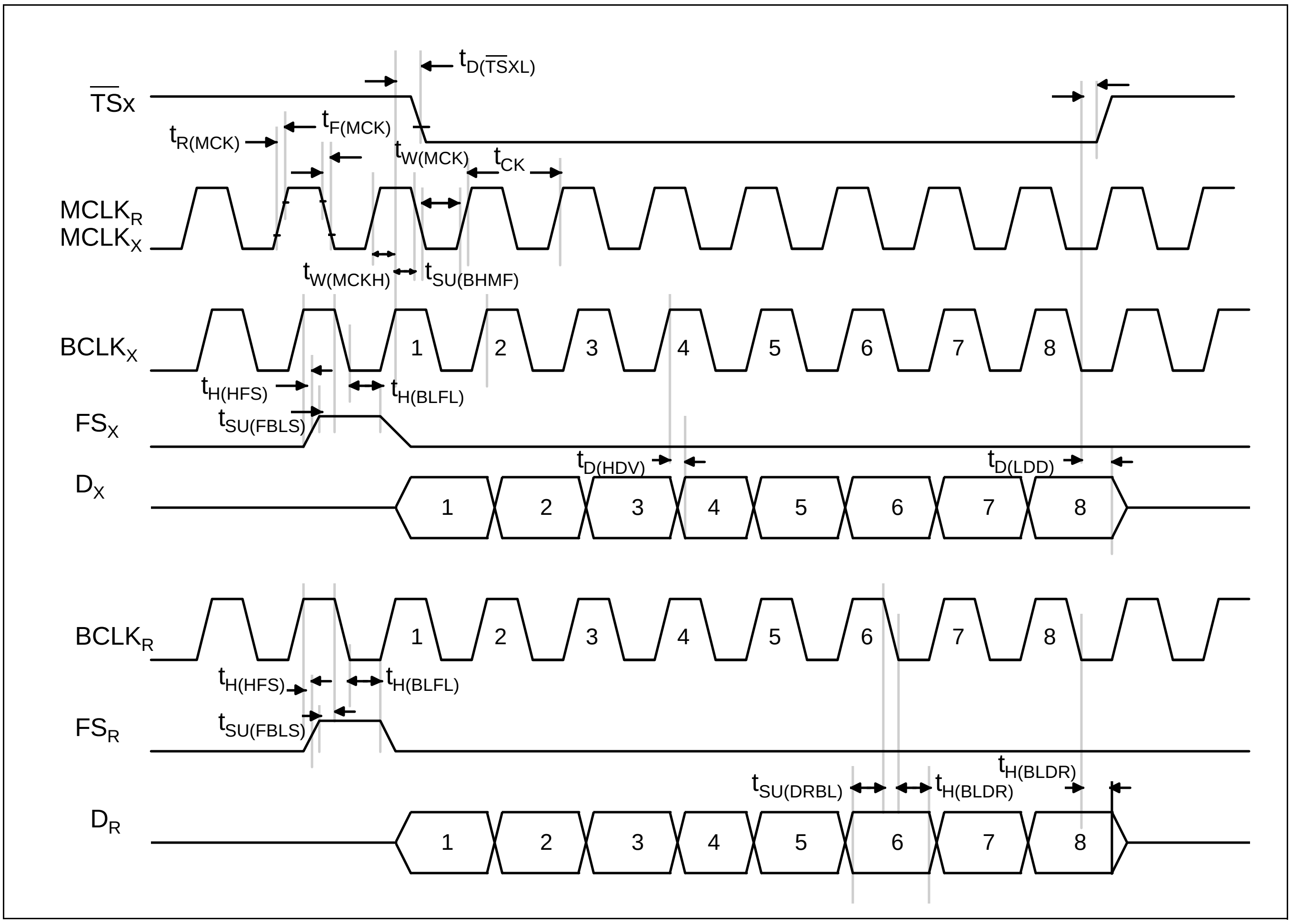


Figure 1. Short Frame Sync Timing

TIMING DIAGRAM (Continued)

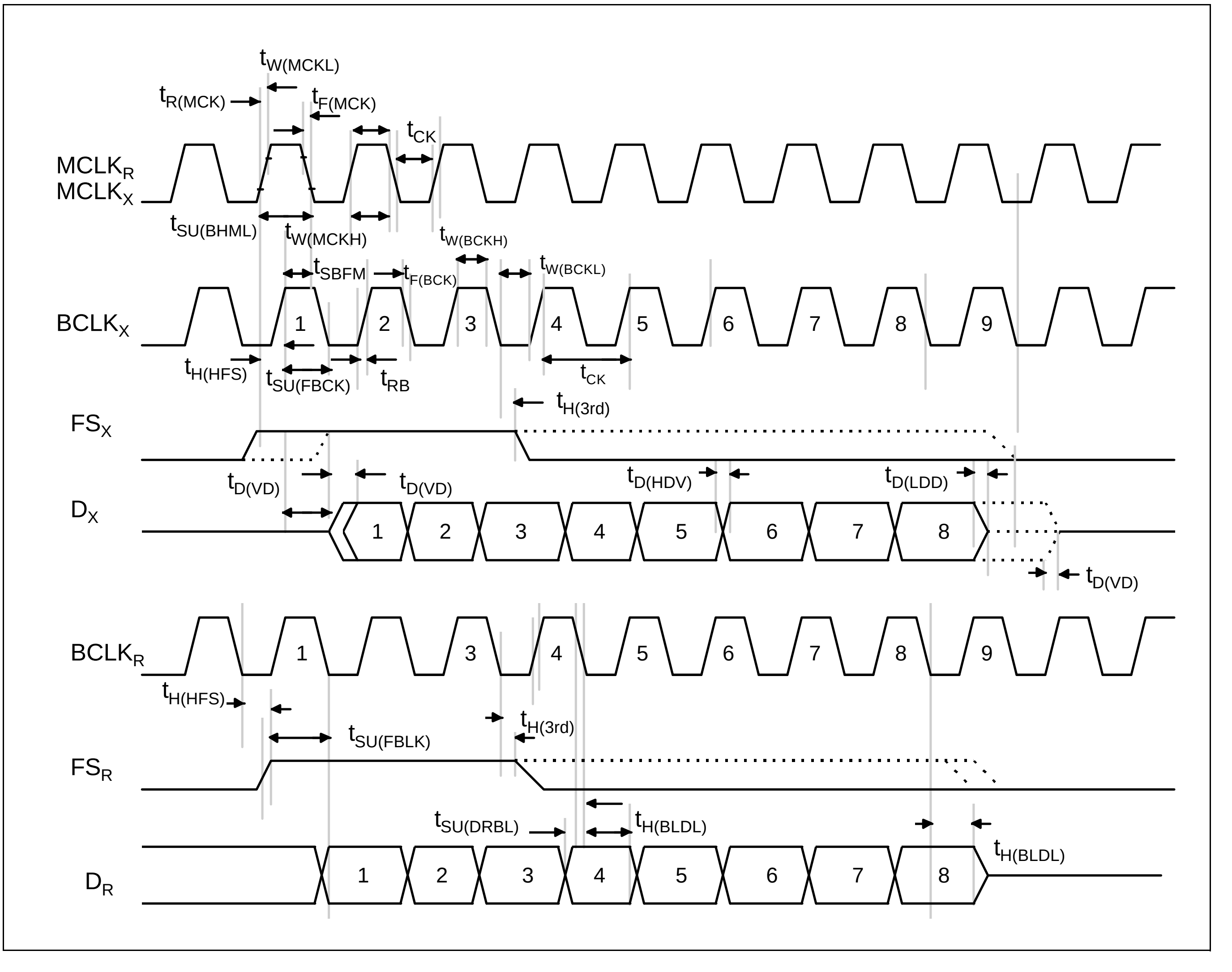


Figure 2. Long Frame Sync Timing

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, GND_A = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
AMPLITUDE RESPONSE						
Receive Gain, Absolute	$G_{V\ (ARX)}$	Ta=25°C, V_{CC}=5V, V_{BB}=–5V Input = Digital code sequence for 0dBm signal at 1020Hz	–0.15	–	0.15	dB
Receive Gain, Relative to $G_{V\ (ARX)}$	$G_{V\ (RRX)}$	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	–0.15 –0.35 –0.7	–	0.15 0.05 0 –14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	$\Delta G_{V\ (ARX)}$ /ΔT	Ta = 0°C to 70°C	–	–	±0.1	dB
Absolute Receive gain Variation with Supply Voltage	$\Delta G_{V\ (ARX)}$ /ΔV	V_{CC}=5V ± 5%, V_{BB}=–5V ± 5%	–	–	±0.05	dB
Receive Gain Variations with Level	$\Delta G_{V\ (RXL)}$	Sinusoidal test method, reference input PCM code corresponds to an ideally encoded –10dB0 signal PCM level = –40dBm0 to +3dBm0 PCM level = –50dBm0 to –10dBm0 PCM level = –55dBm0 to –50dBm0	–0.2 –0.4 –1.2	–	0.2 0.4 1.2	dB dB dB
Receive Output Drive Level	$V_{O\ (RX)}$	R_L = 600Ω	–2.5	–	2.5	V
Absolute Level	V_{AL}	Norminal 0dBm0 level is 4dBm (600Ω) 0dBm0	–	1.2276	–	Vrms
Max Overload Level	$V_{OL\ (AMX)}$	Max overload level (3.17dBm0): S5T8554B Max overload level (3.14dBm0): S5T8557B	–	2.501	–	V_{PK}
Transmit Gain, Absolute	$G_{V\ (ATX)}$	Ta = 25°C, V_{CC} = 5V, V_{BB} = –5V Input at GS_X = 0dBm0 at 1020Hz	–0.15	–	0.15	dB
Transmit Gain, Relative to $G_{V\ (ARX)}$	$G_{V\ (RTX)}$	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz - 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	 –1.8 –0.15 –0.35 –0.7	–	–40 –30 –26 –0.1 0.15 0.05 0 – –14 –32	dB dB dB dB dB dB dB dB dB dB

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, GND_A = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Absolute Transmit Gain Variation with Temperature	$\Delta G_{V(ATX)}$ /ΔT	Ta = 0°C to 70°C	–	–	±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	$\Delta G_{V(ATX)}$ /ΔV	V_{CC} = 5V ±5%, V_{BB} = –5V ±5%	–	–	±0.05	dB
Transmit Gain Variations with Level	–	Sinusoldal test method Reference level = – 10dBm0 VF_XI + = – 40dBm0 to +3dBm0 VF_X + = – 50dBm0 to – 40dBm0 VF_XI + = – 55dBm0 to – 50dBm0	 –0.2 –0.4 –1.2	–	 0.2 0.4 1.2	 dB dB dB
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
Receive Delay, Absolute	$t_{D\ (ARX)}$	f = 1600Hz	–	180	200	µs
Receive Delay, Relative to $t_{D\ (ARX)}$	$t_{D\ (RRX)}$	f = 500Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz	–40 –30	–25 –120 70 100 145	 90 125 175	µs µs µs µs µs
Transmit Delay, Absolute	$t_{D\ (ATX)}$	f = 1600Hz	–	290	315	µs
Transmit Delay, Relative to $t_{D\ (ATX)}$	$t_{D\ (RTX)}$	f = 500Hz - 600Hz f = 600Hz - 800Hz f = 800Hz - 1000Hz f = 1000Hz - 1600Hz f = 1600Hz - 2600Hz f = 2600Hz - 2800Hz f = 2800Hz - 3000Hz	–	195 120 50 20 55 80 130	220 145 75 40 75 105 155	µs µs µs µs µs µs µs
NOISE						
Receive Noise, CMessage Weighted	N_{RXC}	PCM code equals alternating positive and negative zero, S5T8554B	–	8	11	dBrnc0
Receive Noise, PMessage Weighted	N_{RXP}	PCM code equals, positive zero, S5T8557B	–	–82	–79	dBm0p
Transmit Noise, CMessage Weighted	N_{TXC}	S5T8554B	–	12	15	dBrnc0
Transmit Noise, PMessage Weighted	N_{TXP}	S5T8557B	–	74	–67	dBm0p
Noise, Single Frequency	N_{SF}	f = 0kHz to 100kHz, loop around measurement, VF_XI + = 0Vrms	–	–	–53	dBm0
Positive Power Supply Rejection, Transmit	PSRR (PTX)	VF_XI + = 0Vrms, V_{CC} = 5.0V_{DC} + 100mVrms f = 0kHz - 50kHz	40	–	–	dBC

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, GND_A = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Negative Power Supply Rejection, Transmit	PSRR (NTX)	VF_XI + = 0Vrms, V_{BB} = –5.0V_{DC} + 100mVrms f = 0kHz - 50kHz	40	–	–	dBC
Positive Power Supply Rejection, Receive	PSRR (PRX)	PCM code equals positive zero V_{CC} = 5.0V_{DC} + 100mVrms f = 0Hz - 4000Hz f = 4kHz - 25kHz f = 25kHz - 50kHz	 40 40 36	–	–	 dBC dB dB
Negative Power Supply Rejection, Receive	PSRR (NRX)	PCM code equals positive zero V_{BB} = 5.0V_{DC} + 100mVrms f = 0Hz - 4000Hz f = 4kHz - 25kHz f = 25kHz - 50kHz	 40 40 36	–	–	 dBC dB dB
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz - 3400Hz input PCM applied to D_R, Measure individual image signals at VF_RO 4600Hz - 760Hz 7600Hz - 8400Hz 8400Hz - 100,000Hz	–	–	 –32 –40 –32	 dB dB dB
DISTORTION						
Signal to Total Distortion Transmit or Receive Half-Channel	THD_{TX} THD_{RX}	Sinusoidal test method Level = 3.0dBm0 = 0dBm0 to 30dBm0 = –40dBm0 XMT RCV = –55dBm0 XMT RCV	 33 26 29 30 14 15	–	–	 dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	THD_{SF} (TDO)	–	–	–	–46	dB
Single Frequency Distortion, Receive	THD_{SF} (RX)	–	–	–	–46	dB
Intermodulation Distortion	THD_{IMD}	Loop around measurement, VF_XI + = –4dBm0 to –21dBm0, two frequencies in the range 300Hz - 3400Hz	–	–	–41	dB
CROSSTALK						
Transmit to Receive Crosstalk, 0dB0 Transmit Level	CT (TX-RX)	f = 300Hz - 3400Hz D_R = Steady PCM code	–	–90	–75	dB

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, GND_A = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

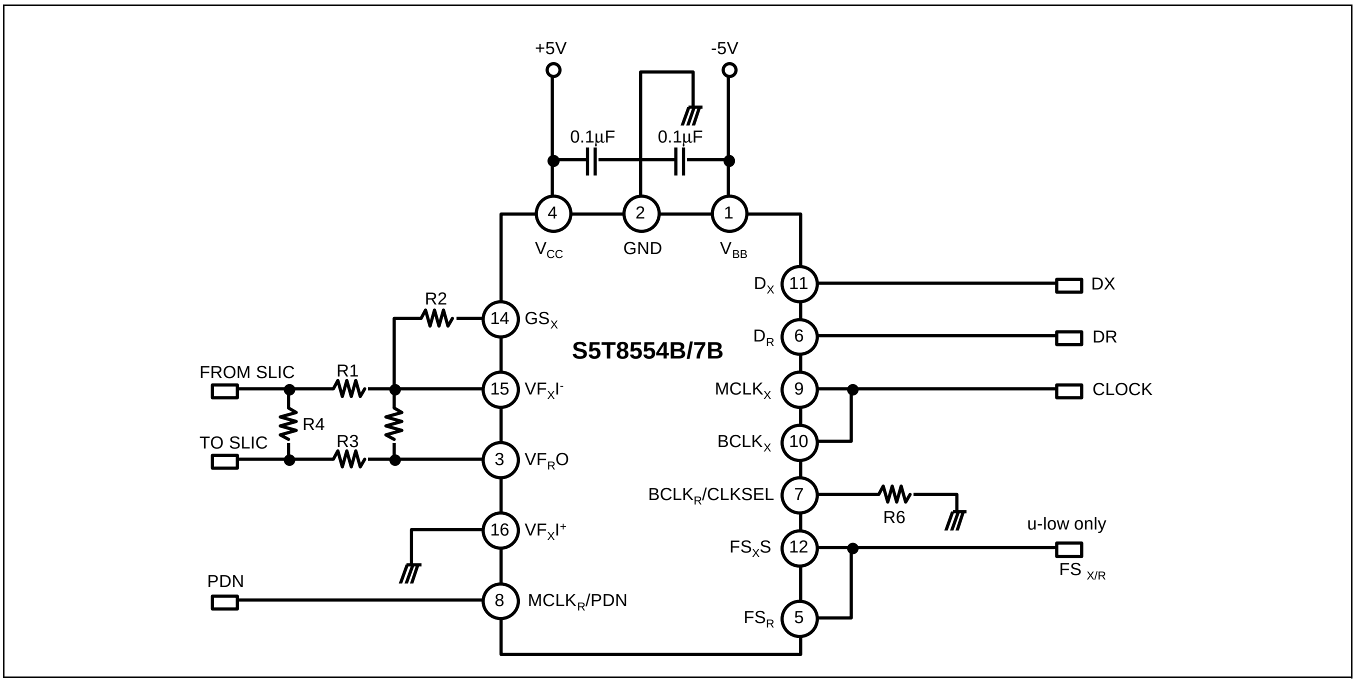
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Receive to Transmit Crosstalk, 0dBm0 Receive Level	$CT_{(RX-TX)}$	–	–	–90	–70 (Note1)	dB

NOTE: $CT_{(RX-TX)}$ is measured with a - 40dBm0 activating signal applied at VF_XI +

Encoding Format At D_X Output

	m-Law KT8554	A-Law KT8557
V_{IN} (at GS_X) = + Full Scale	10000000	10101010
V_{IN} (at GS_X) = 0V	11111111 01111111	11010101 01010101
V_{IN} (at GS_X) = -Full Scale	0000000	00101010

APPLICATION CIRCUIT



NOTES:

1. Supposing Desired Line Termination Impedance R_L = 600ohm
   It is 0dBm = 0.77459Vrms
2. T_X Gain 20 log (R2/R1), R1 + R2 < 100Kohm, or The Correspondence of 1-CHIP CODEC 0dBm 0 = 4dBm.

SELECTION OF MASTER CLOCK FREQUENCY

BCLKR/CLKSEL	S5T8554B	S5T8557B
Clocked	1.536 / 1.544MHz	2.048MHz
0	2.048MHz	1.536 / 1.544MHz
1 (or open)	1.536 / 1.544MHz	2.048MHz

NOTES