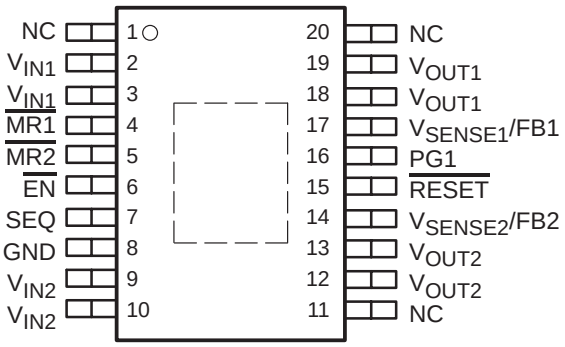
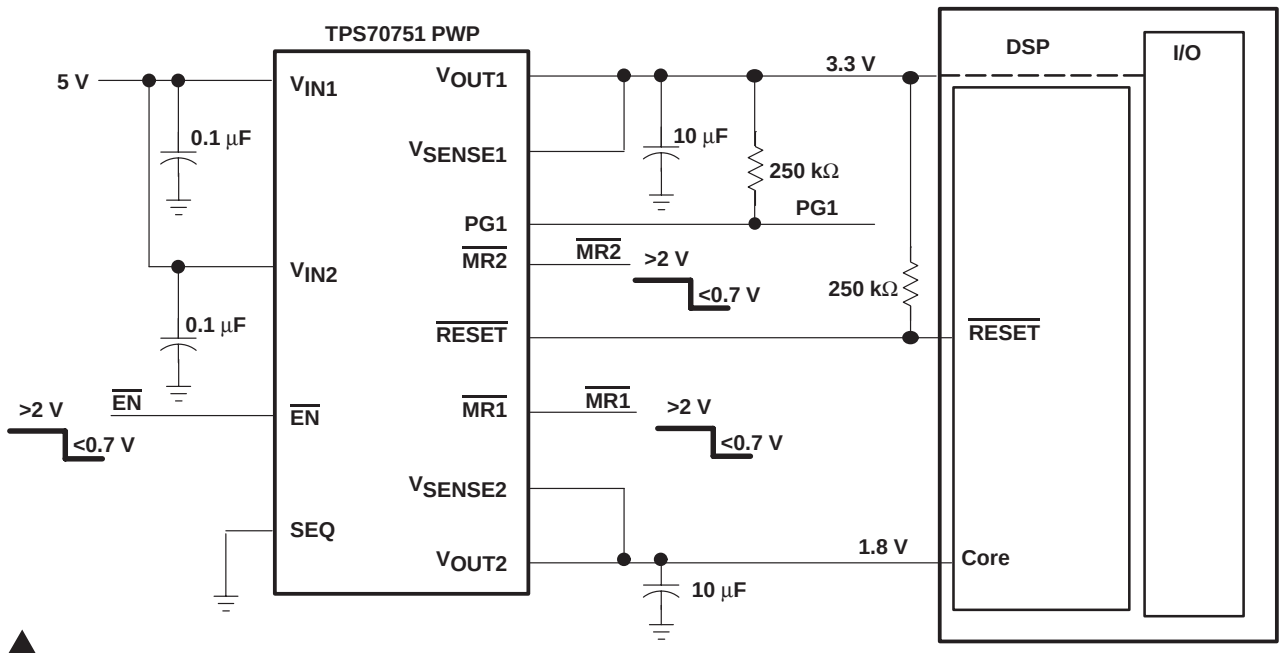
- Dual Output Voltages for Split-Supply Applications
- Selectable Power Up Sequencing for DSP Applications
- Output Current Range of 250 mA on Regulator 1 and 125 mA on Regulator 2
- Fast Transient Response
- Voltage Options are 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and Dual Adjustable Outputs
- Open Drain Power-On Reset With 120-ms Delay
- Open Drain Power Good for Regulator 1
- Ultra Low 190 μA (typ) Quiescent Current
- 1 μA Input Current During Standby
- Low Noise: 65 μV_{RMS} Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- Two Manual Reset Inputs
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 20-Pin PowerPAD™ TSSOP Package
- Thermal Shutdown Protection

description

TPS707xx family devices are designed to provide a complete power management solution for DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any DSP applications with power sequencing requirement. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset inputs, and enable function, provide a complete system solution.

PWP PACKAGE
(TOP VIEW)





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description (continued)

The TPS707xx family of voltage regulators offers very low dropout voltage and dual outputs with power up sequence control, which is designed primarily for DSP applications. These devices have extremely low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 10 uF low ESR capacitors.

These devices have fixed 3.3-V/2.5-V, 3.3-V/1.8-V, 3.3-V/1.5-V, 3.3-V/1.2-V, and adjustable/adjustable voltage options. Regulator 1 can support up to 250 mA and regulator 2 can support up to 125 mA. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 83 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 230 μA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to $\overline{EN}$ (enable) shuts down both regulators, reducing the input current to 1 μA at T_J = 25°C.

The device is enabled when the $\overline{EN}$ pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the V_{SENSE1} and V_{SENSE2} pins respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} will turn on first and V_{OUT1} will remain off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time V_{OUT1} will be turned on. If V_{OUT2} is pulled below 83% (i.e. over load condition) V_{OUT1} will be turned off. Pulling the SEQ terminal low, reverses the power-up order and V_{OUT1} will be turned on first. The SEQ pin is connected to an internal pullup current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off(disabled).

The PG1 pin reports the voltage conditions at VOUT1. Power good can be used to implement a SVS for the circuitry supplied by regulator 1.

The TPS707xx features a $\overline{RESET}$ (SVS, POR, or Power On Reset). $\overline{RESET}$ output initiates a reset in DSP systems and related digital applications in the event of an undervoltage condition. $\overline{RESET}$ indicates the status of V_{OUT2} and both manual reset pins ($\overline{MR1}$ and $\overline{MR2}$). When V_{OUT2} reaches 95% of its regulated voltage and $\overline{MR1}$ and $\overline{MR2}$ are in the logic high state, $\overline{RESET}$ will go to a high impedance state after 120 ms delay. $\overline{RESET}$ will go to logic low state when V_{OUT2} regulated output voltage is pulled below 95% (i.e. over load condition) of its regulated voltage. To monitor V_{OUT1} , the PG1 output pin can be connected to $\overline{MR1}$ or $\overline{MR2}$.

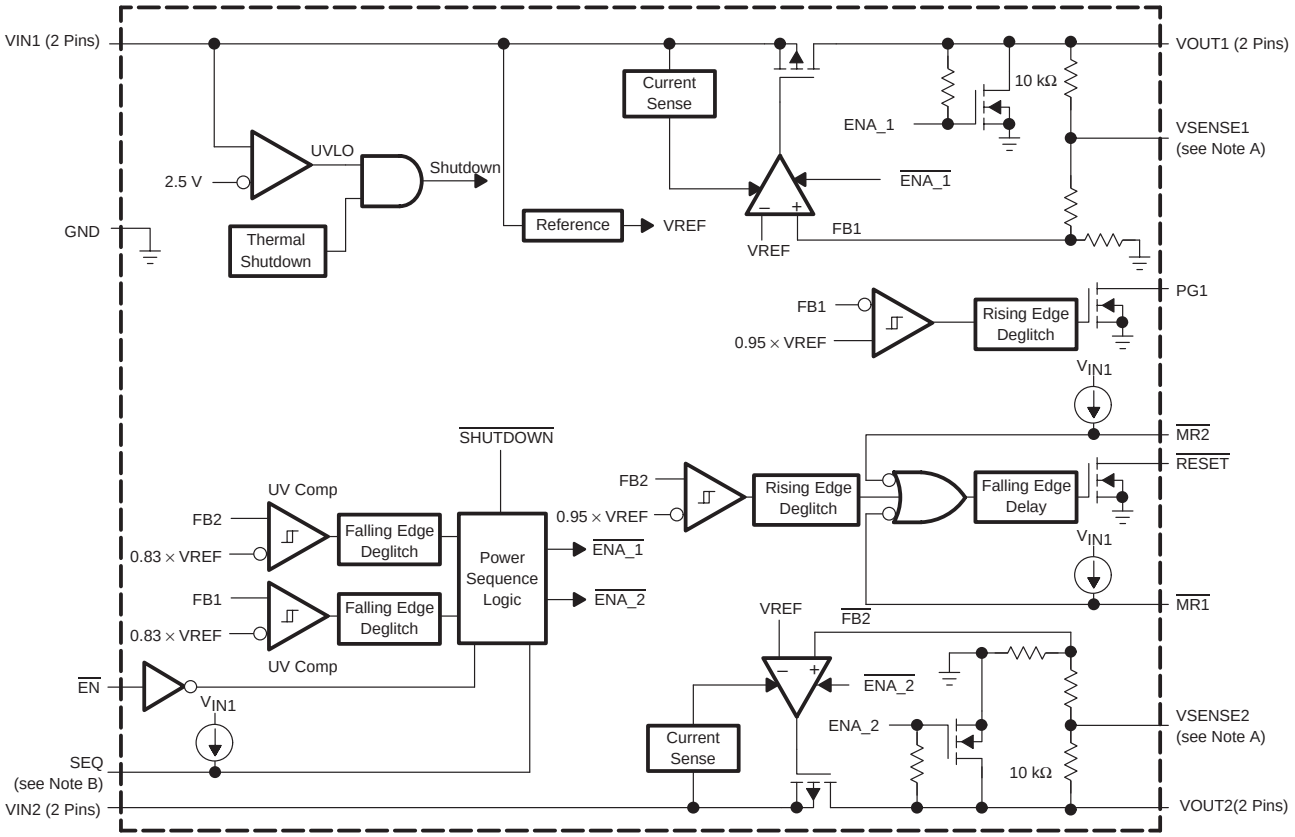
The device has an undervoltage lockout UVLO circuit which prevents the internal regulators from turning on until VIN1 reaches 2.5V.

AVAILABLE OPTIONS

T_J	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
–40°C to 125°C	3.3 V	1.2 V	TPS70745PWP
	3.3 V	1.5 V	TPS70748PWP
	3.3 V	1.8 V	TPS70751PWP
	3.3 V	2.5 V	TPS70758PWP
	Adjustable (1.22 V to 5.5 V)	Adjustable (1.22 V to 5.5 V)	TPS70702PWP

NOTE: The TPS70702 is programmable using external resistor dividers (see application information) The PWP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS70702PWPR).

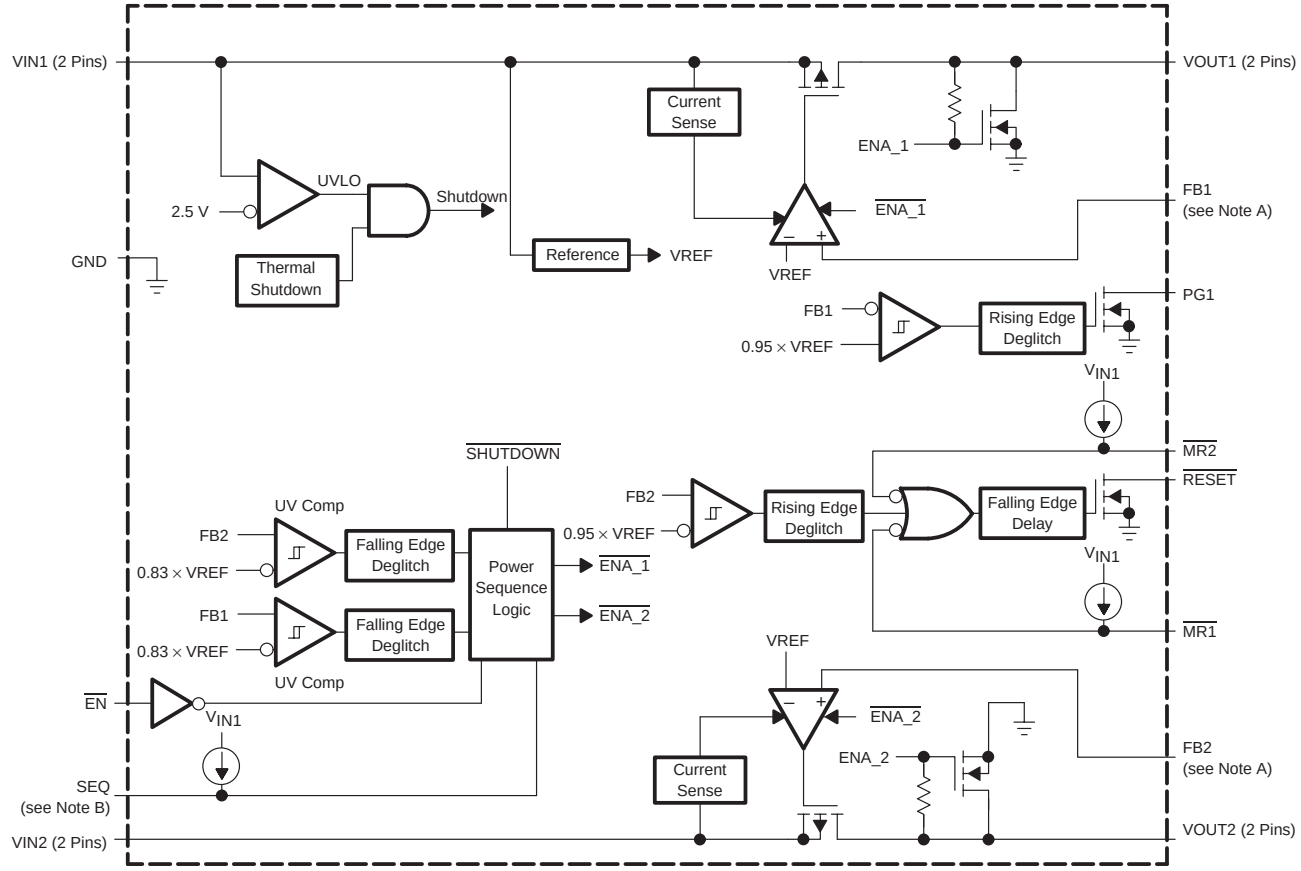
detailed block diagram – fixed voltage version



NOTES: A. For most applications, V_{SENSE1} and V_{SENSE2} should be externally connected to V_{OUT} as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the application information section.

B. If the SEQ terminal is floating at the input, V_{OUT2} will power up first.

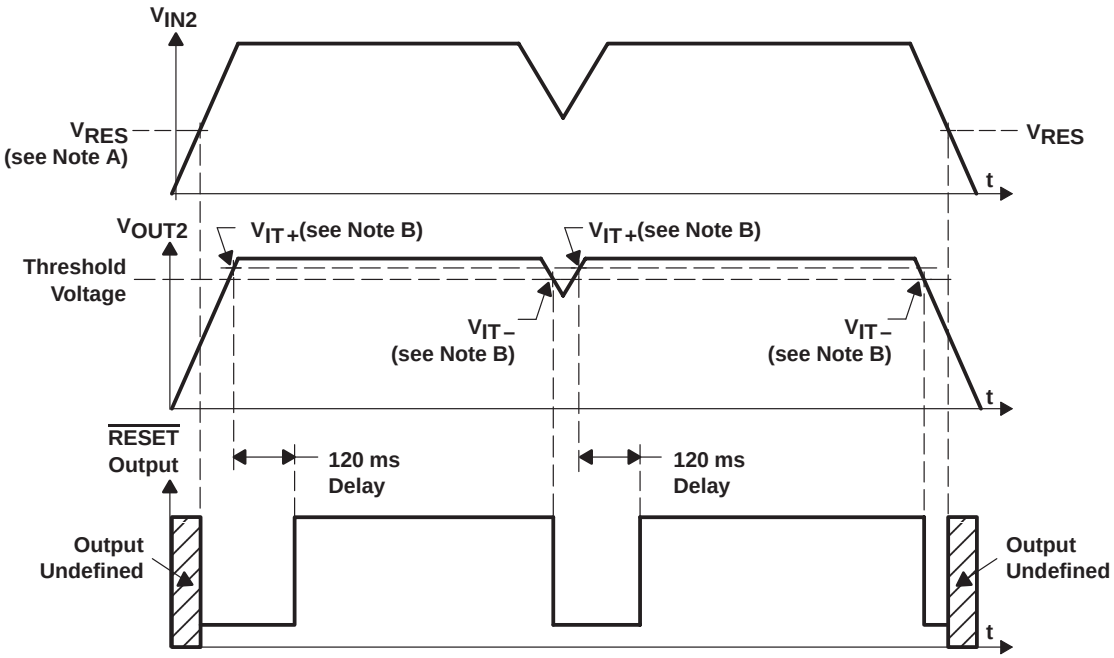
detailed block diagram – adjustable voltage version



NOTES: A. For most applications, FB1 and FB2 should be externally connected to resistor dividers as close as possible to the device. For other implementations, refer to FB terminals connection discussion in the application information section.

B. If the SEQ terminal is floating at the input, V_{OUT2} will power up first.

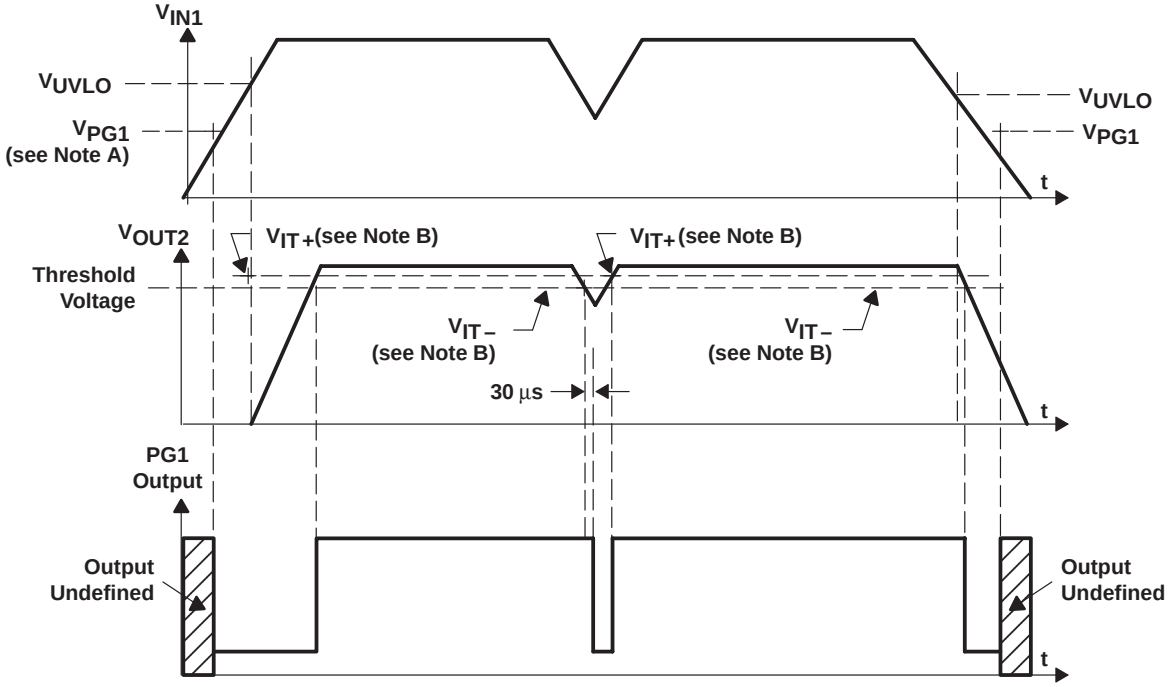
$\overline{\text{RESET}}$ timing diagram (with V_{IN1} powered up and $\overline{\text{MR1}}$ AND $\overline{\text{MR2}}$ at logic high)



NOTES: A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. VIT –Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

PG1 timing diagram



NOTES: A. V_{PG1} is the minimum input voltage for a valid PG1. The symbol V_{PG1} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. VIT –Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	6	I	Active low enable
GND	8		Ground
$\overline{MR1}$	4	I	Manual reset input 1, active low, pulled up internally
$\overline{MR2}$	5	I	Manual reset input 2, active low, pulled up internally
NC	1, 11, 20		No connection
PG1	16	O	Open drain output, low when V_{OUT1} voltage is less than 95% of the nominal regulated voltage
$\overline{RESET}$	15	O	Open drain output, SVS (power on reset) signal, active low
SEQ	7	I	Power up sequence control: SEQ=High, V_{OUT2} powers up first; SEQ=Low, V_{OUT1} powers up first, SEQ terminal pulled up internally.
V_{IN1}	2, 3	I	Input voltage of regulator 1
V_{IN2}	9, 10	I	Input voltage of regulator 2
V_{OUT1}	18, 19	O	Output voltage of regulator 1
V_{OUT2}	12, 13	O	Output voltage of regulator 2
V_{SENSE2}/FB2	14	I	Regulator 2 output voltage sense/ regulator 2 feedback for adjustable
V_{SENSE1}/FB1	17	I	Regulator 1 output voltage sense/ regulator 1 feedback for adjustable

absolute maximum ratings over operating junction temperature (unless otherwise noted)†

Input voltage range‡: V_{IN1} . . . . . –0.3 V to 7 V
V_{IN2} . . . . . –0.3 V to 7 V
Voltage range at $\overline{EN}$ . . . . . –0.3 V to 7 V
Output voltage range (V_{OUT1}, V_{SENSE1}) . . . . . 5.5 V
Output voltage range (V_{OUT2}, V_{SENSE2}) . . . . . 5.5 V
Maximum $\overline{RESET}$, PG1 voltage . . . . . 7 V
Maximum $\overline{MR1}$, $\overline{MR2}$, and SEQ voltage . . . . . V_{IN1}
Peak output current . . . . . Internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Tables
Operating virtual junction temperature range, T_J . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
ESD rating, HBM . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are tied to network ground.

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP§	0	3.067 W	30.67 mW/°C	1.687 W	1.227 W
	250	4.115 W	41.15 mW/°C	2.265 W	1.646 W

§ This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1 oz. copper on 4-in × 4-in ground layer. For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I †	2.7	6	V
Output current, I_O (regulator 1)	0	250	mA
Output current, I_O (regulator 2)	0	125	mA
Output voltage range (for adjustable option)	1.22	5.5	V
Operating virtual junction temperature, T_J	–40	125	°C

† To calculate the minimum input voltage for maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

electrical characteristics over recommended operating junction temperature (T_J = –40°C to 125°C) V_{IN1} or $V_{IN2} = V_{O(nom)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0, C_O = 33 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_O	Output voltage (see Notes 1 and 3)	Reference voltage	2.7 V < V_I < 6 V,	FB connected to V_O	T_J = 25°C		1.22		V
			2.7 V < V_I < 6 V,	FB connected to V_O		1.196		1.244	
		1.2 V Output	2.7 V < V_I < 6 V,		T_J = 25°C		1.2		
			2.7 V < V_I < 6 V			1.176		1.224	
		1.5 V Output	2.7 V < V_I < 6 V,		T_J = 25°C		1.5		
			2.7 V < V_I < 6 V			1.47		1.53	
		1.8 V Output	2.8 V < V_I < 6 V,		T_J = 25°C		1.8		
			2.8 V < V_I < 6 V			1.764		1.836	
		2.5 V Output	3.5 V < V_I < 6 V,		T_J = 25°C		2.5		
			3.5 V < V_I < 6 V			2.45		2.55	
		3.3 V Output	4.3 V < V_I < 6 V,		T_J = 25°C		3.3		V
			4.3 V < V_I < 6 V			3.234		3.366	
Quiescent current (GND current) for regulator 1 and regulator 2, $\overline{EN}$ = 0 V, (see Note 1)			See Note 3,		T_J = 25°C		190		µA
			See Note 3					230	
Output voltage line regulation ($\Delta V_O/V_O$) for regulator 1 and regulator 2 (see Note 2)			V_O + 1 V < V_I ≤ 6 V,		T_J = 25°C, See Note 1		0.01%		V
			V_O + 1 V < V_I ≤ 6 V,		See Note 1			0.1%	
Load regulation for V_{OUT1} and V_{OUT2}			T_J = 25°C,		See Note 3		1		mV
V_n	Output noise voltage	Regulator 1	BW = 300 Hz to 50 kHz,	C_O = 33 µF,	T_J = 25°C		65		µVrms
		Regulator 2					65		
Output current limit		Regulator 1	V_O = 0 V				1.6	1.9	A
		Regulator 2					0.750	1	
Thermal shutdown junction temperature							150		°C
$I_{I(standby)}$	Standby current	Regulator 1 and Regulator 2	$\overline{EN}$ = V_I,		T_J = 25°C			2	µA
			$\overline{EN}$ = V_I					6	
PSRR	Power supply ripple rejection		f = 1 kHz, C_O = 33 µF,		T_J = 25°C, See Note 1		60		dB

NOTES: 1. Minimum input operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum input voltage = 6 V, minimum output current 1 mA.

2. If V_O < 1.8 V then V_{Imax} = 6 V, V_{Imin} = 2.7 V:

$$\text{Line Regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - 2.7\ V\right)}{100} \times 1000$$

If V_O > 2.5 V then V_{Imax} = 6 V, V_{Imin} = Vo + 1 V:

$$\text{Line Regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - \left(V_O + 1\right)\right)}{100} \times 1000$$

3. I_O = 1 mA to 250 mA for Regulator 1 and 1 mA to 125 mA for Regulator 2.

electrical characteristics over recommended operating junction temperature (T_J = –40°C to 125°C) V_{IN1} or V_{IN2} = $V_{O(nom)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0, C_O = 33 µF(unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET	Minimum input voltage for valid $\overline{RESET}$	$I_{(RESET)}$ = 300 µA, $V_{(RESET)} \le$ 0.8 V		1.0	1.3	V
	Trip threshold voltage	V_O decreasing	92%	95%	98%	V_O
	Hysteresis voltage	Measured at V_O		0.5%		V_O
	$t_{(RESET)}$	$\overline{RESET}$ pulse duration	80	120	160	ms
	$t_{r(RESET)}$	Rising edge deglitch		30		µs
	Output low voltage	V_I = 3.5 V, $I_{(RESET)}$ = 1 mA		0.15	0.4	V
	Leakage current	$V_{(RESET)}$ = 6 V			1	µA
PG1	Minimum input voltage for valid PG1	$I_{O(PG1)}$ = 300 µA, $V_{(PG1)} \le$ 0.8 V		1.0	1.3	V
	Trip threshold voltage	V_O decreasing	92%	95%	98%	V_O
	Hysteresis voltage	Measured at V_O		0.5%		V_O
	$t_{f(PG1)}$	Falling edge deglitch		30		µs
	Output low voltage	V_I = 2.7 V, $I_{(PG1)}$ = 1 mA		0.15	0.4	V
	Leakage current	$V_{(PG1)}$ = 6 V			1	µA
EN	High level $\overline{EN}$ input voltage		2			V
	Low level $\overline{EN}$ input voltage				0.7	V
	Input current ($\overline{EN}$)		–1		1	µA
SEQ	High level SEQ input voltage		2			V
	Low level SEQ input voltage				0.7	V
	SEQ pull up current source			6		µA
MR1 / MR2	High level input voltage		2			V
	Low level input voltage				0.7	V
	Pull up current source			6		µA
V_{OUT2}	V_{OUT2} UV comparator – positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
	V_{OUT2} UV comparator – hysteresis			0.5% V_O		mV
	V_{OUT2} UV comparator – falling edge deglitch	V_{SENSE_2} decreasing below threshold		140		µs
	Peak output current	2 ms pulse width		375		mA
	Discharge transistor current	V_{OUT2} = 1.5 V		7.5		mA
V_{OUT1}	V_{OUT1} UV comparator – positive-going input threshold voltage of V_{OUT1} UV comparator		80% V_O	83% V_O	86% V_O	V
	V_{OUT1} UV comparator – hysteresis			0.5% V_O		mV
	V_{OUT1} UV comparator – falling edge deglitch	V_{SENSE_1} decreasing below threshold		140		µs
	Dropout voltage (see Note 4)	I_O = 250 mA, V_{IN1} = 3.2 V, T_J = 25°C		83		mV
		I_O = 250 mA, V_{IN1} = 3.2 V			140	
	Peak output current	2 ms pulse width		750		mA
	Discharge transistor current	V_{OUT1} = 1.5 V		7.5		mA
VOUT1 UVLO	UVLO threshold		2.4		2.65	V
FB	Input current – TPS70702	FB = 1.8 V		1		µA

NOTE 4: Input voltage(V_{IN1} or V_{IN2}) = V_O(Typ) – 100 mV. For the 1.5 V, 1.8 V and 2.5 V regulators, the dropout voltage is limited by input voltage range. The 3.3 V regulator input voltage is to 3.2 V to perform this test.

Table of Graphs

TYPICAL CHARACTERISTICS

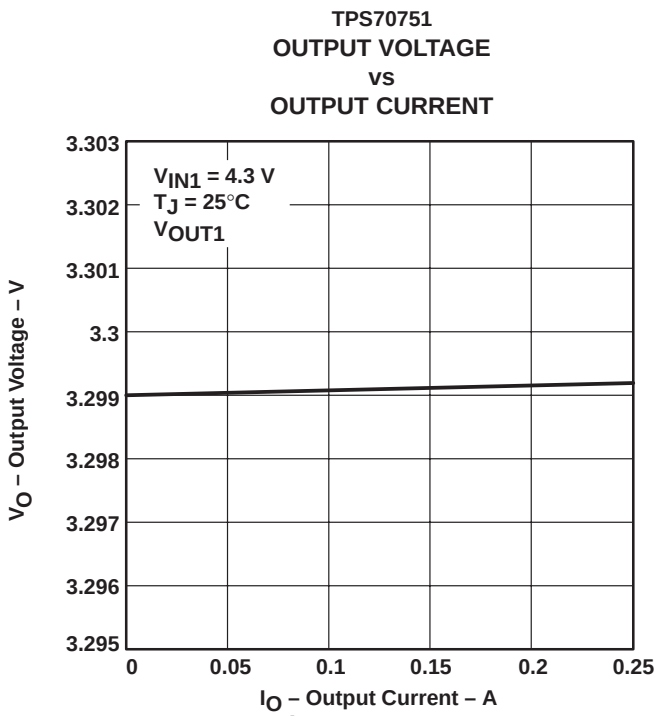


Figure 1

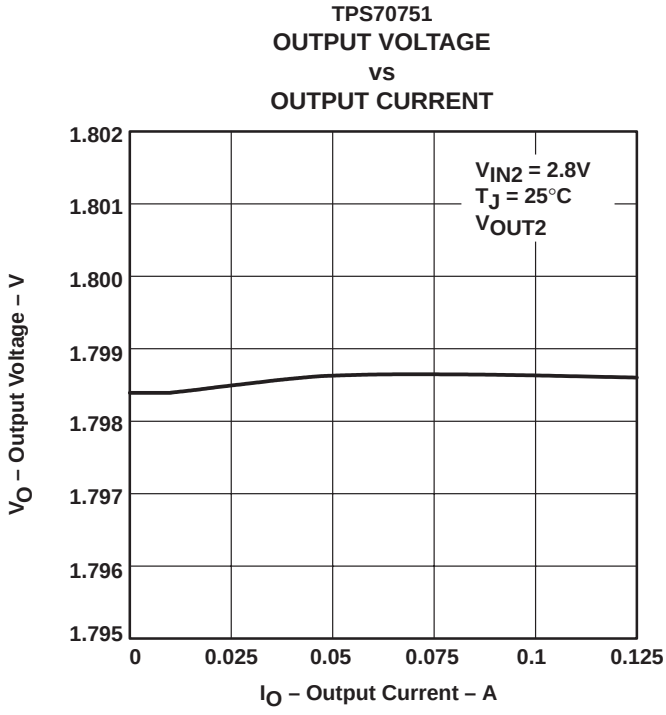


Figure 2

TYPICAL CHARACTERISTICS

TPS70745
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

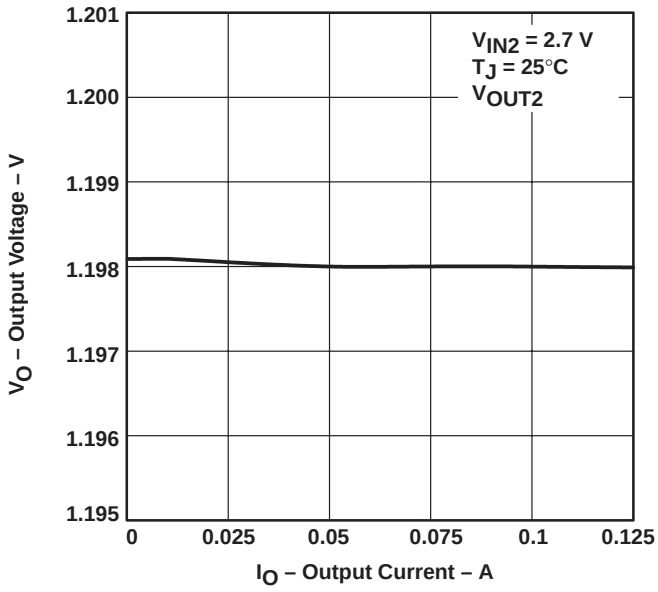


Figure 3

TPS70751
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

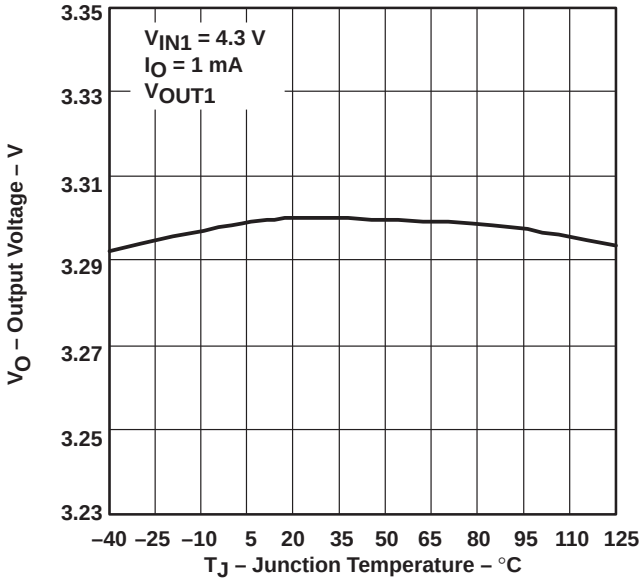


Figure 4

TPS70751
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

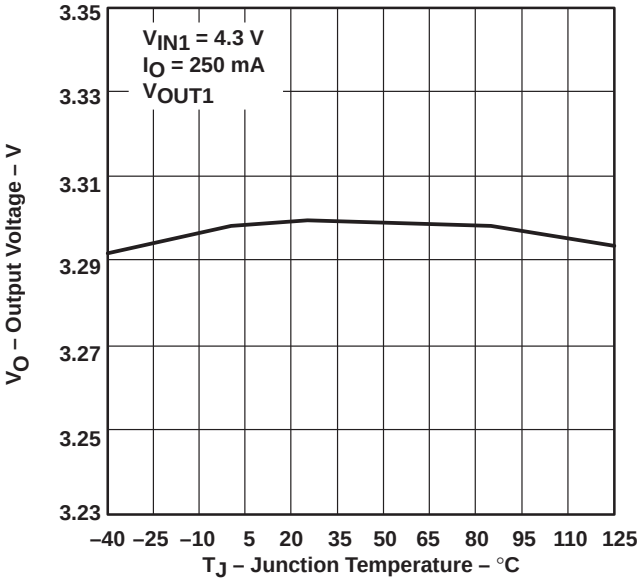


Figure 5

TYPICAL CHARACTERISTICS

TPS70751
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

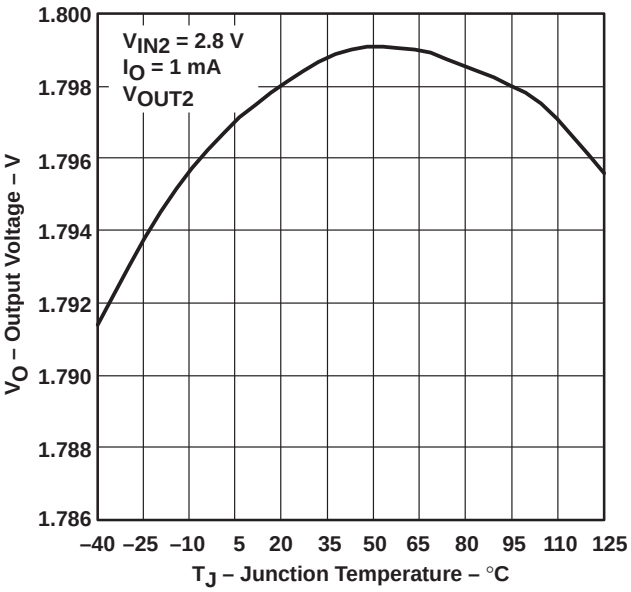


Figure 6

TPS70751
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

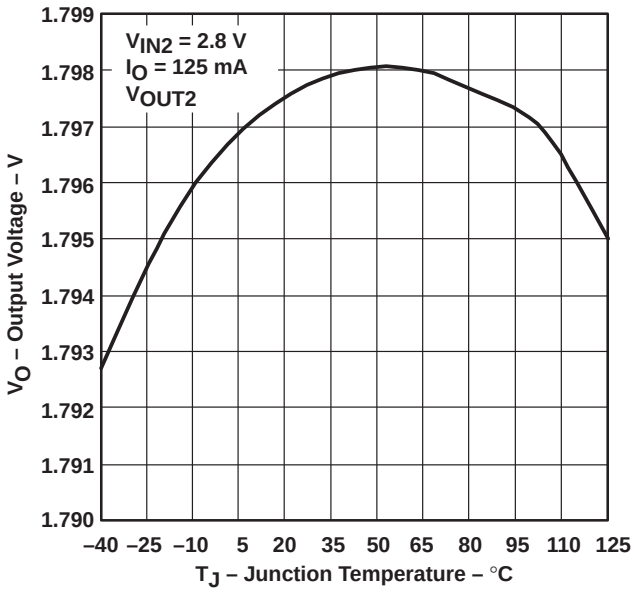


Figure 7

GROUND CURRENT
vs
JUNCTION TEMPERATURE

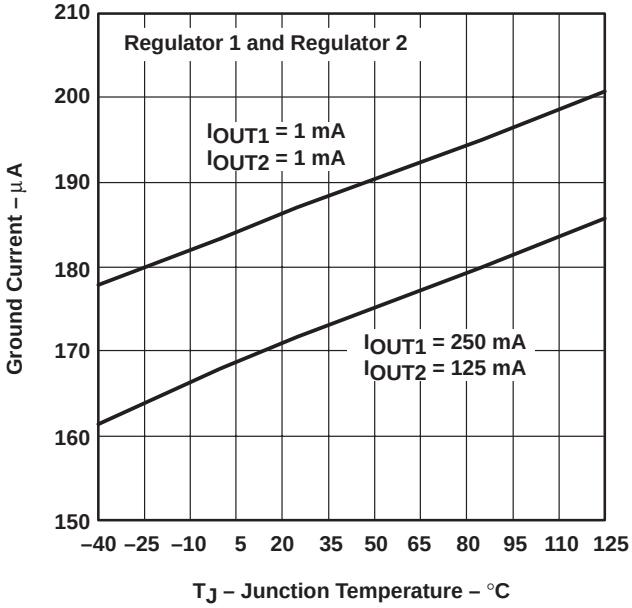


Figure 8

TYPICAL CHARACTERISTICS

TPS70751
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

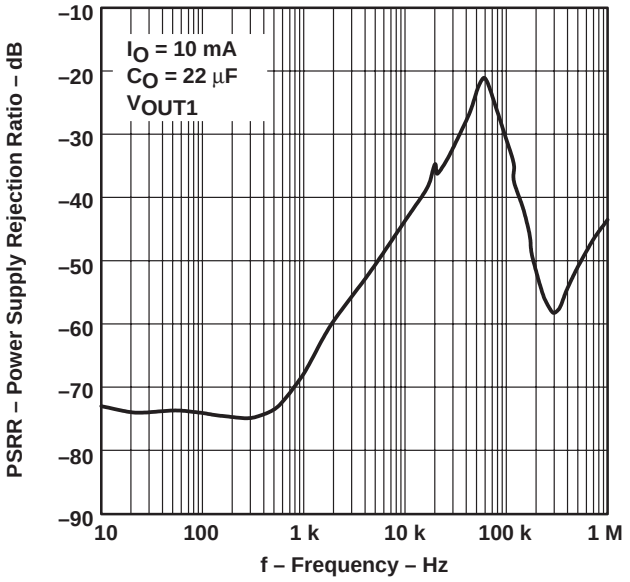


Figure 9

TPS70751
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

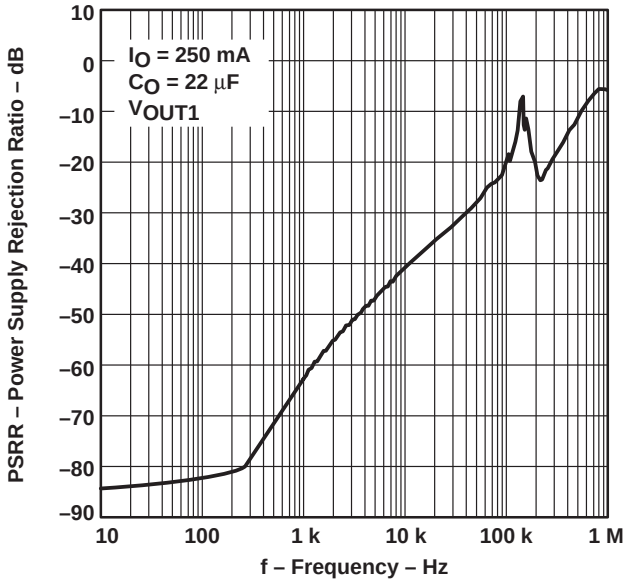


Figure 10

TPS70751
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

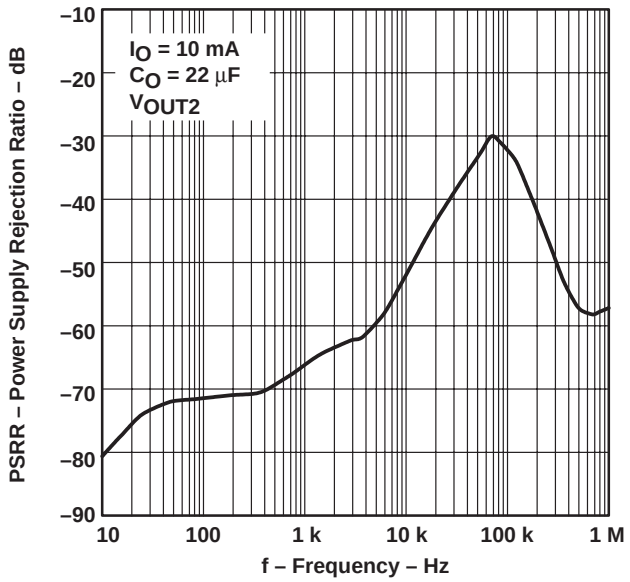


Figure 11

TPS70751
POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

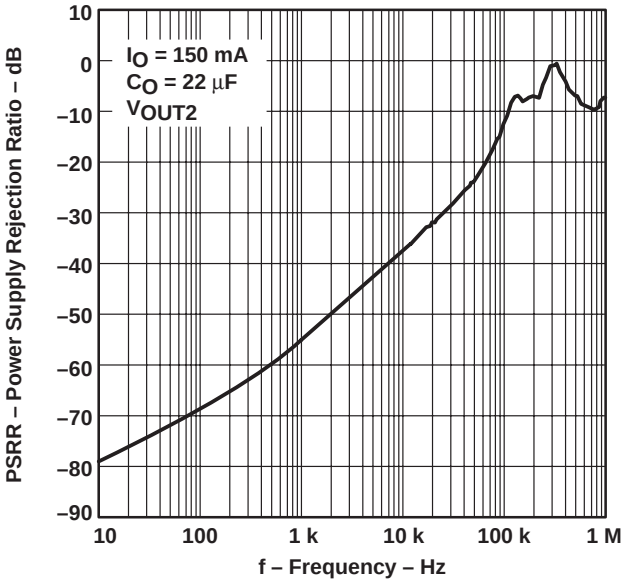


Figure 12

TYPICAL CHARACTERISTICS

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

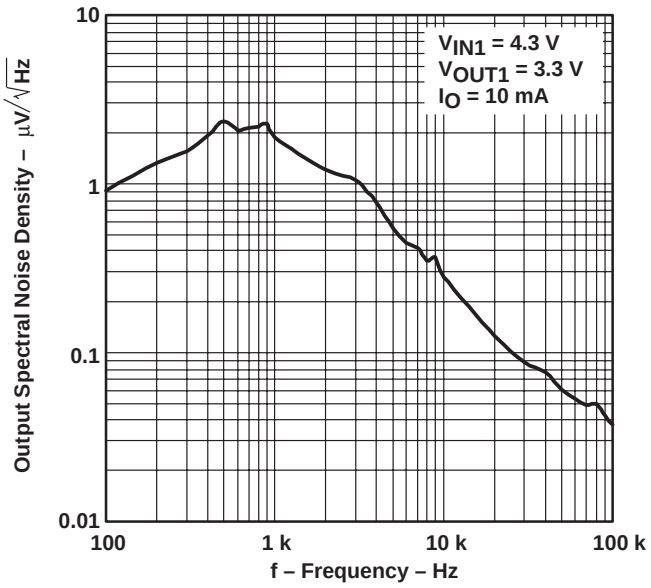


Figure 13

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

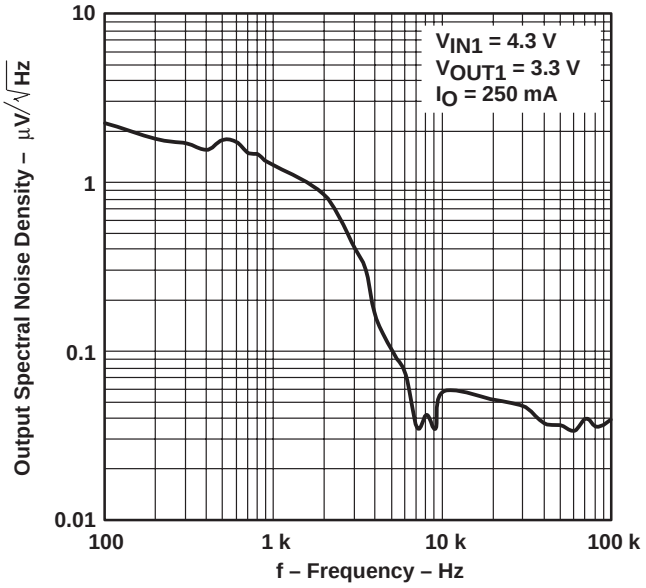


Figure 14

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

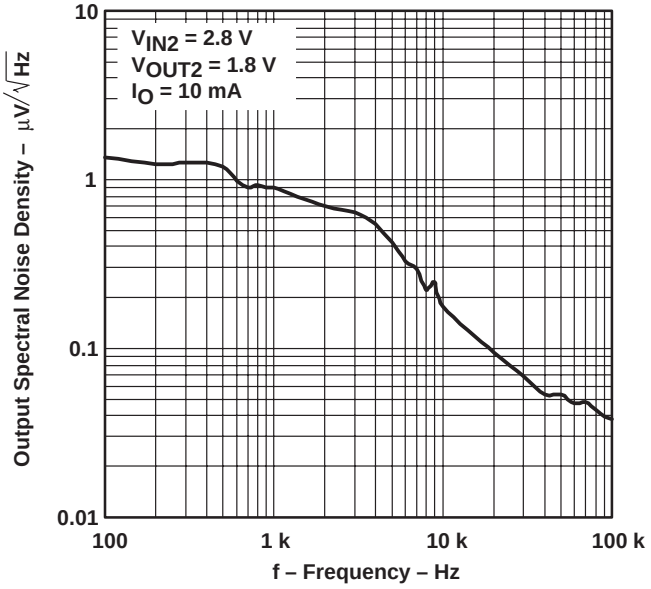


Figure 15

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

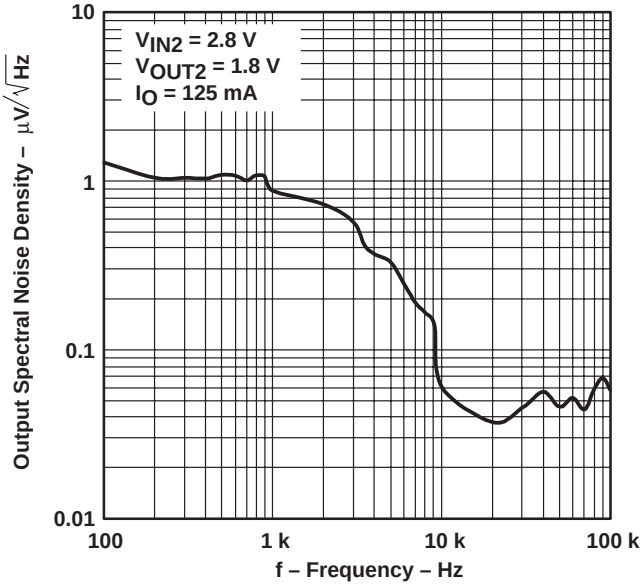


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

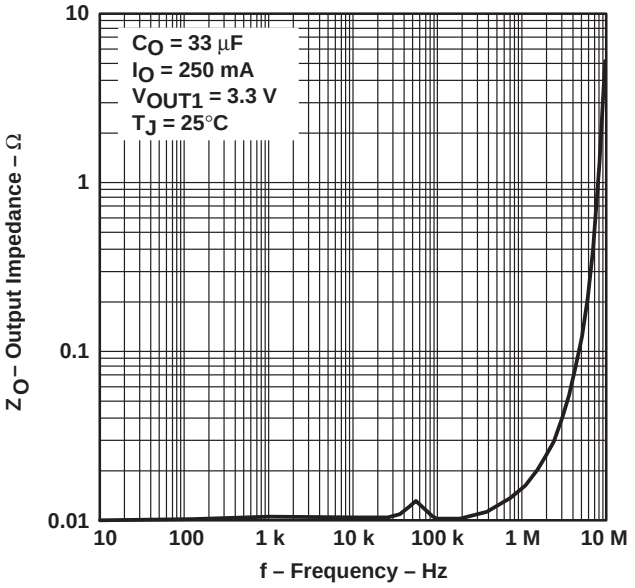


Figure 17

OUTPUT IMPEDANCE
vs
FREQUENCY

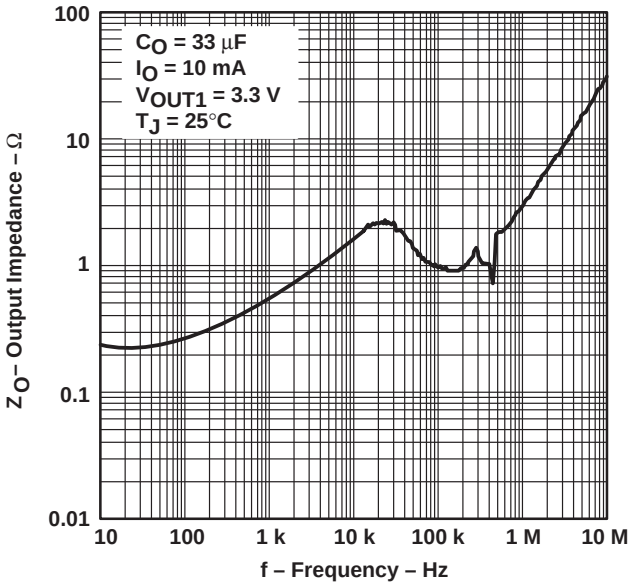


Figure 18

OUTPUT IMPEDANCE
vs
FREQUENCY

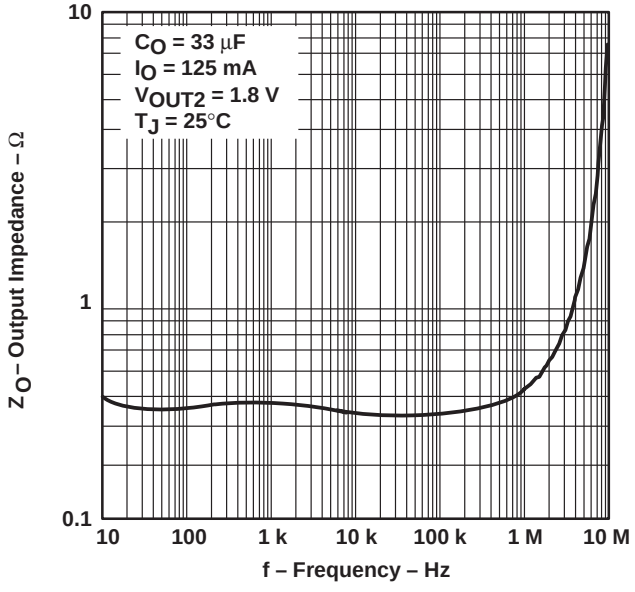


Figure 19

OUTPUT IMPEDANCE
vs
FREQUENCY

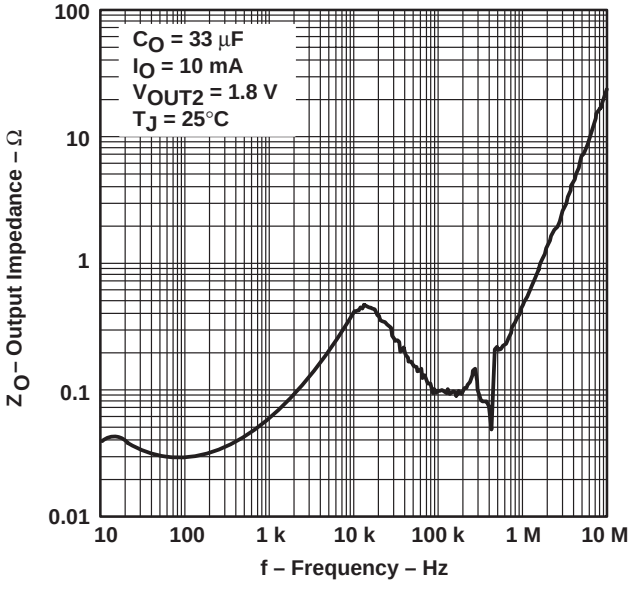


Figure 20

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

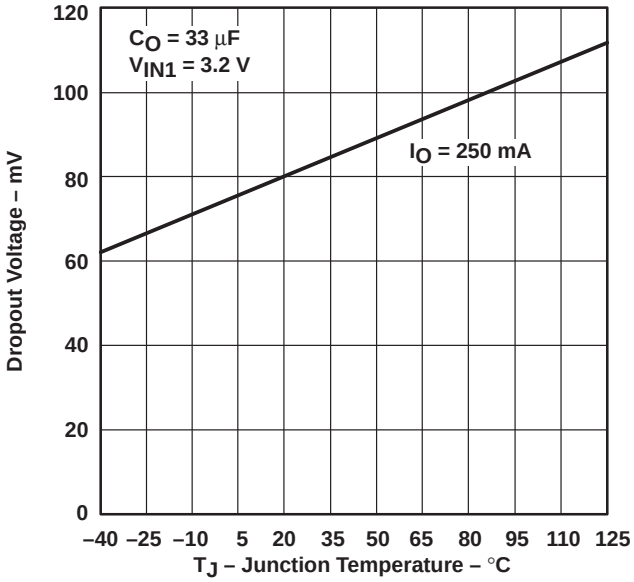


Figure 21

DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

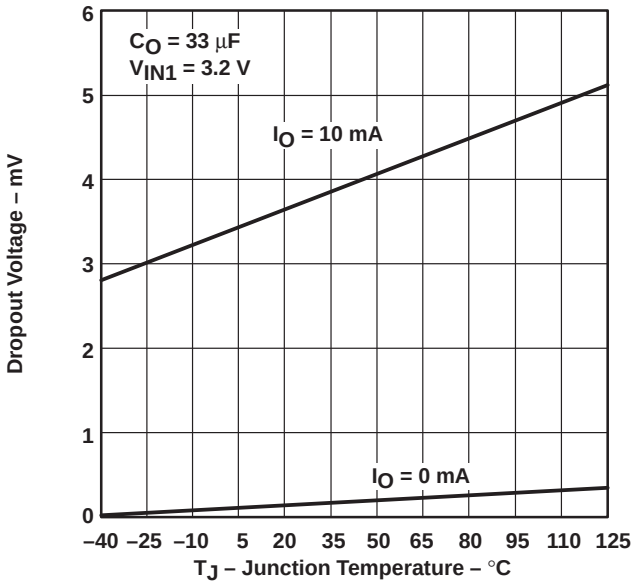


Figure 22

TPS70702 DROPOUT VOLTAGE vs INPUT VOLTAGE

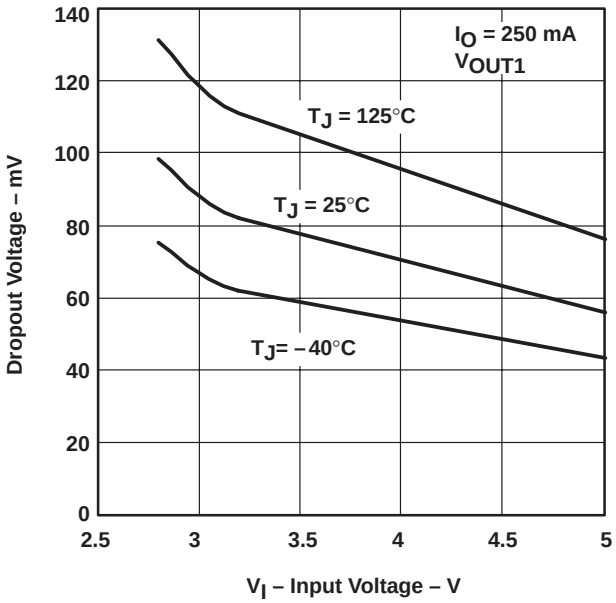


Figure 23

TPS70702 DROPOUT VOLTAGE vs INPUT VOLTAGE

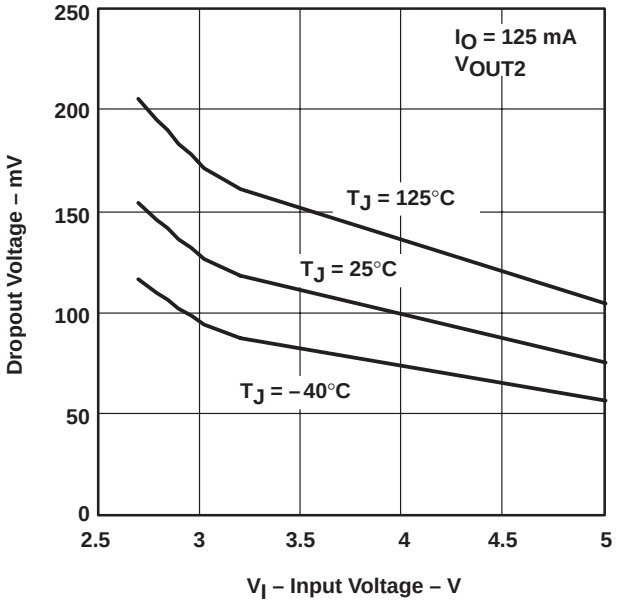


Figure 24

TYPICAL CHARACTERISTICS

LOAD TRANSIENT RESPONSE

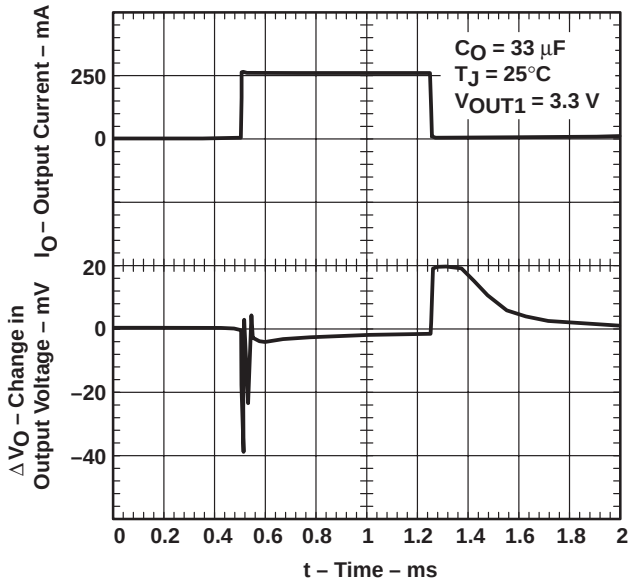


Figure 25

LOAD TRANSIENT RESPONSE

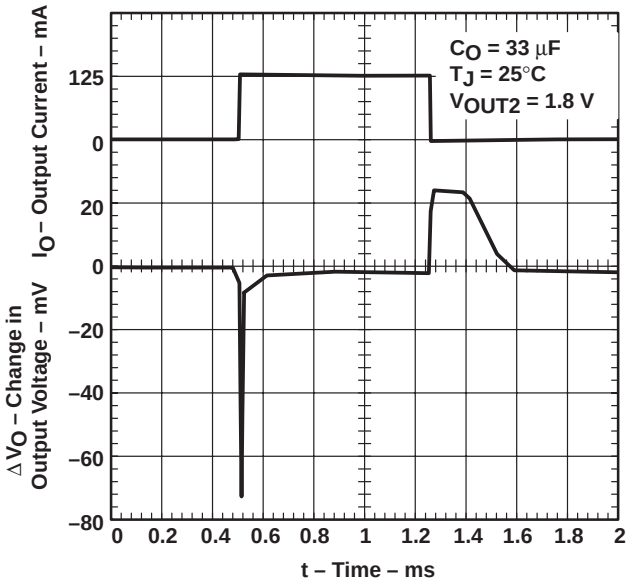


Figure 26

LINE TRANSIENT RESPONSE

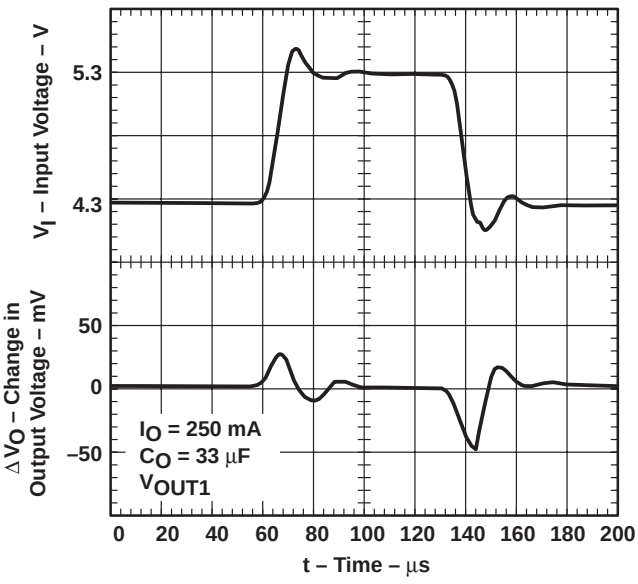


Figure 27

LINE TRANSIENT RESPONSE

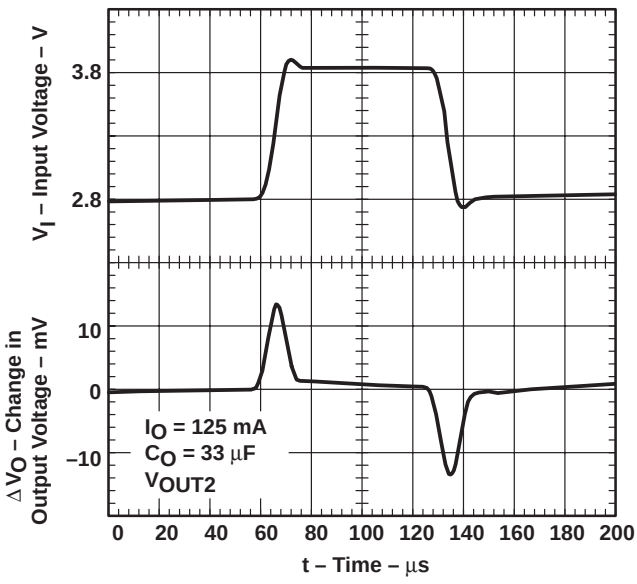


Figure 28

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs TIME (START-UP)

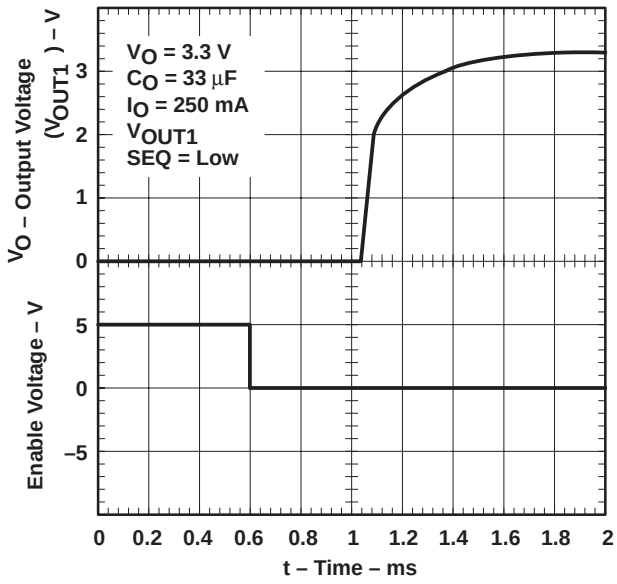


Figure 29

OUTPUT VOLTAGE vs TIME (START-UP)

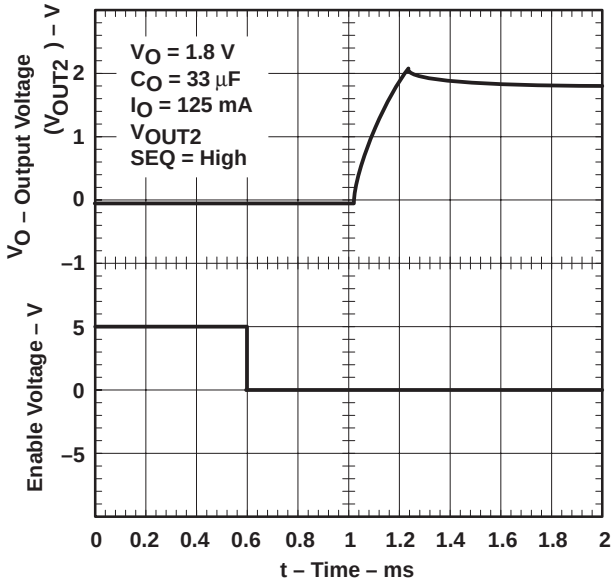


Figure 30

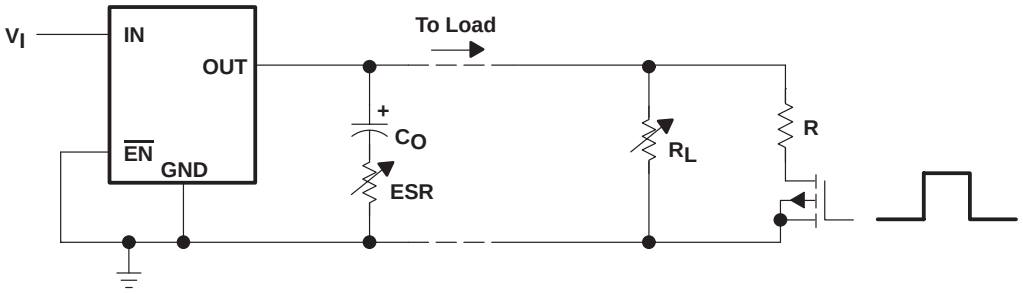


Figure 31. Test Circuit for Typical Regions of Stability

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

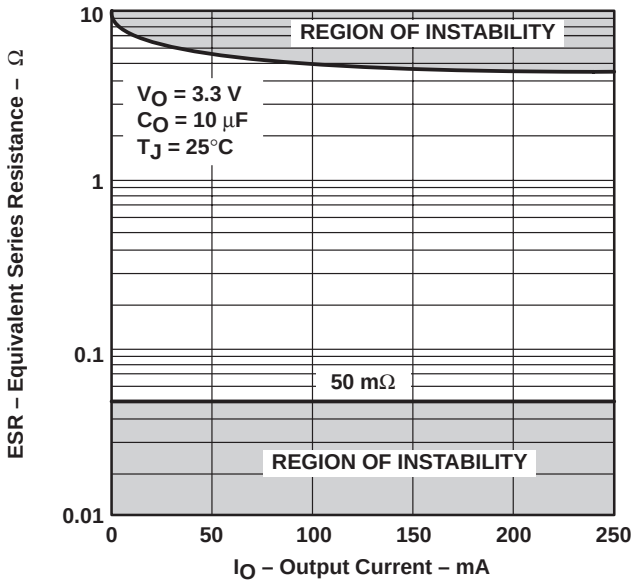


Figure 32

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

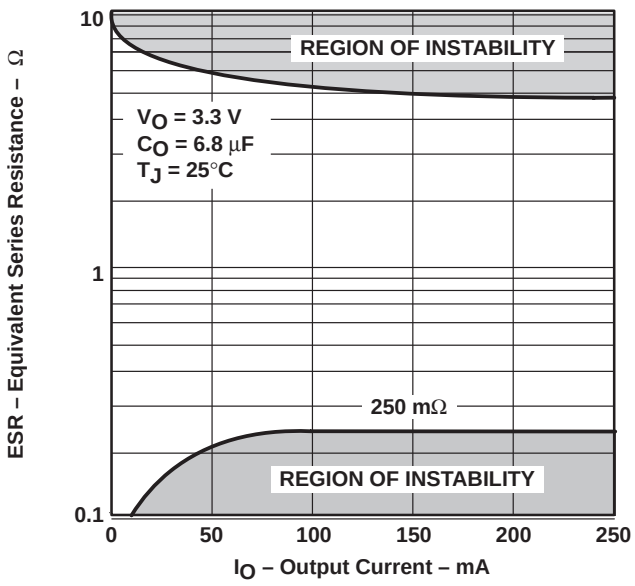


Figure 33

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

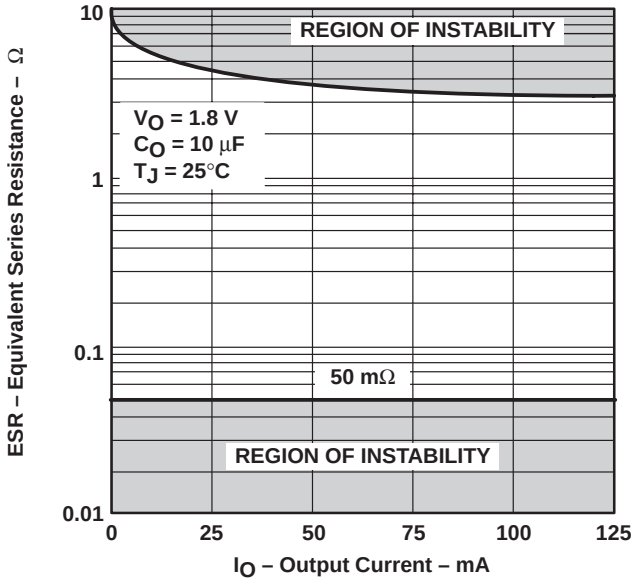


Figure 34

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

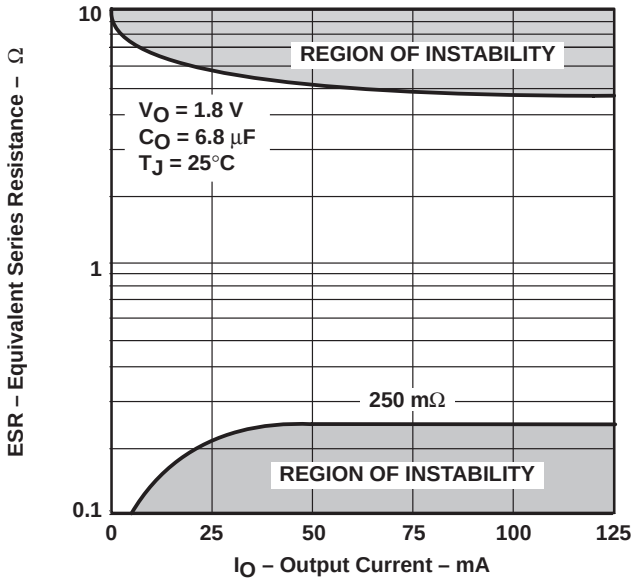


Figure 35

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

detailed description

The TPS707xx low dropout regulator family provides dual regulated output voltages for DSP applications that require a high-performance power management solution. These devices provide fast transient response and high accuracy with small output capacitors, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This reduces the component cost and board space while increasing total system reliability. TPS707xx family has an enable feature which puts the device in sleep mode reducing the input currents to less than 3 μA. Other features are integrated SVS (power on reset, $\overline{\text{RESET}}$) and power good (PG1) that monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

The TPS707xx, unlike many other LDOs, feature very low quiescent current which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS707xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and stable over the full load range.

pin functions

enable

The $\overline{\text{EN}}$ terminal is an input which enables or shuts down the device. If $\overline{\text{EN}}$ is at a voltage high signal the device will be in shutdown mode. When the $\overline{\text{EN}}$ goes to voltage low, then the device will be enabled.

sequence

The SEQ terminal is an input that programs which output voltage (V_{OUT1} or V_{OUT2}) will be turned on first. When the device is enabled and the SEQ terminal is pulled high or left open, V_{OUT2} will turn on first and V_{OUT1} will remain off until V_{OUT2} reaches approximately 83% of its regulated output voltage. At that time the V_{OUT1} will be turned on. If V_{OUT2} is pulled below 83% (i.e., over load condition) V_{OUT1} will be turned off. This terminal has a 6-μA pullup current to V_{IN1}.

Pulling the SEQ terminal low reverses the power-up order and V_{OUT1} will be turned on first. For detail timing diagrams refer to Figures 36 and 42.

power–good

The PG1 terminal is an open drain, active high output terminal which indicates the status of the V_{OUT1} regulator. When the V_{OUT1} reaches 95% of its regulated voltage, PG1 goes into a high impedance state. PG1 goes into a low impedance state when V_{OUT1} is pulled below 95% (i.e. over-load condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pullup resistor.

manual reset pins ($\overline{\text{MR1}}$ and $\overline{\text{MR2}}$)

$\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ are active low input terminals used to trigger a reset condition. When either $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$ is pulled to logic low, a POR ($\overline{\text{RESET}}$) will occur. These terminals have a 6-μA pullup current to V_{IN1}.

sense (V_{SENSE1}, V_{SENSE2})

The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, sense connects to high-impedance wide-bandwidth amplifiers through a resistor-divider network and noise pickup feeds through to the regulator output. It is essential to route the sense connection in such a way to minimize/avoid noise pickup. Adding RC networks between the V_{SENSE} terminals and V_{OUT} terminals to filter noise is not recommended because it can cause the regulators to oscillate.

FB1 and FB2

FB1 and FB2 are input terminals used for adjustable-output devices and must be connected to the external feedback resistor divider. FB1 and FB2 connections should be as short as possible. It is essential to route them in such a way as to minimize/avoid noise pickup. Adding RC networks between the FB terminals and V_{OUT} terminals to filter noise is not recommended because it can cause the regulators to oscillate.

detailed description (continued)

$\overline{\text{RESET}}$ indicator

The TPS707xx features a $\overline{\text{RESET}}$ (SVS, POR, or power on reset). $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or a low-battery indicator. $\overline{\text{RESET}}$ is an active low, open drain output which indicates the status of the V_{OUT2} regulator and both manual reset pins ($\overline{\text{MR1}}$ and $\overline{\text{MR2}}$). When V_{OUT2} exceeds 95% of its regulated voltage, and $\overline{\text{MR1}}$ and $\overline{\text{MR2}}$ are in the high impedance state, $\overline{\text{RESET}}$ will go to a high-impedance state after 120-ms delay. $\overline{\text{RESET}}$ will go to a low impedance state when V_{OUT2} is pulled below 95% (i.e. over load condition) of its regulated voltage. To monitor V_{OUT1} , PG1 output pin can be connected to $\overline{\text{MR1}}$ or $\overline{\text{MR2}}$. The open drain output of the $\overline{\text{RESET}}$ terminal requires a pullup resistor. If $\overline{\text{RESET}}$ is not used, it can be left floating.

V_{IN1} and V_{IN2}

V_{IN1} and V_{IN2} are input to the regulators. Internal bias voltages are powered by V_{IN1}.

V_{OUT1} and V_{OUT2}

V_{OUT1} and V_{OUT2} are output terminals.

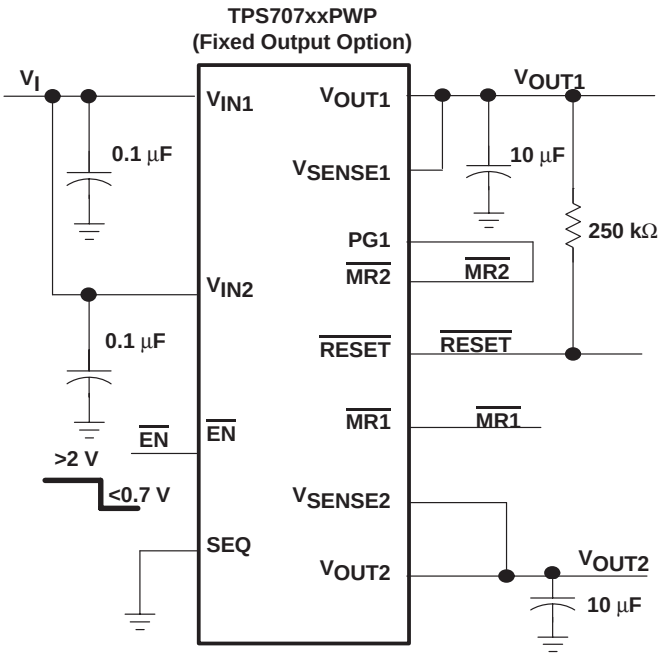
APPLICATION INFORMATION

sequencing timing diagrams

The following figures provide a timing diagram of how this device functions in different configurations.

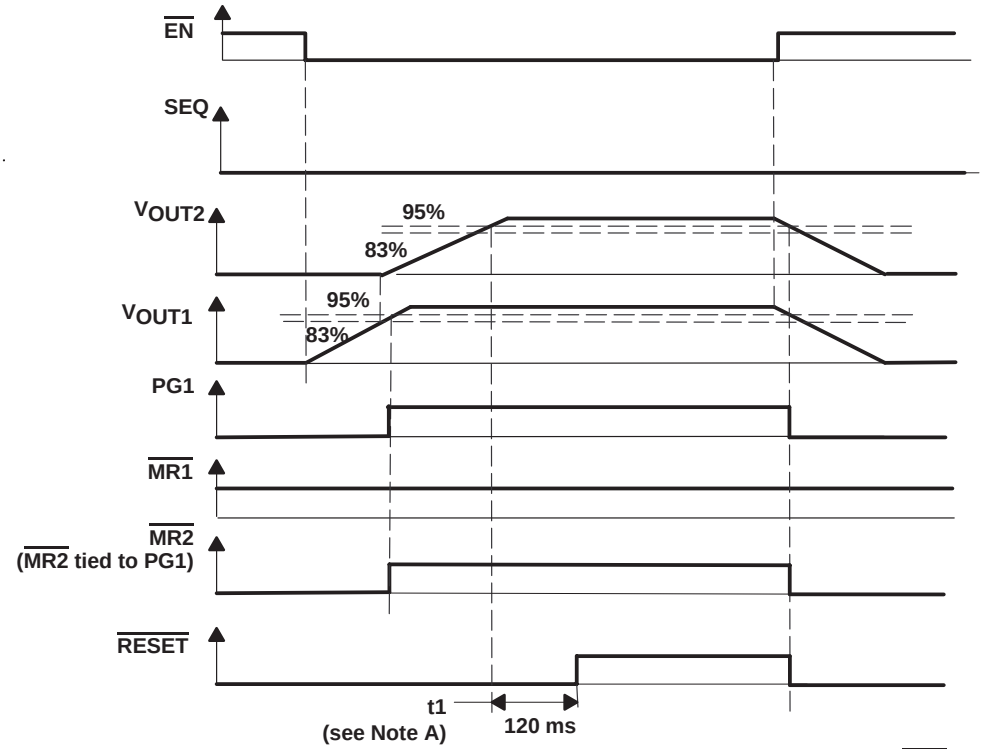
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic low; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is left unconnected and is therefore at logic high.



explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic low, when $\overline{EN}$ is taken to logic low, V_{OUT1} turns on. V_{OUT2} turns on after V_{OUT1} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{EN}$ is returned to logic high, both devices power down and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.



NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 36. Timing When SEQ = Low

APPLICATION INFORMATION

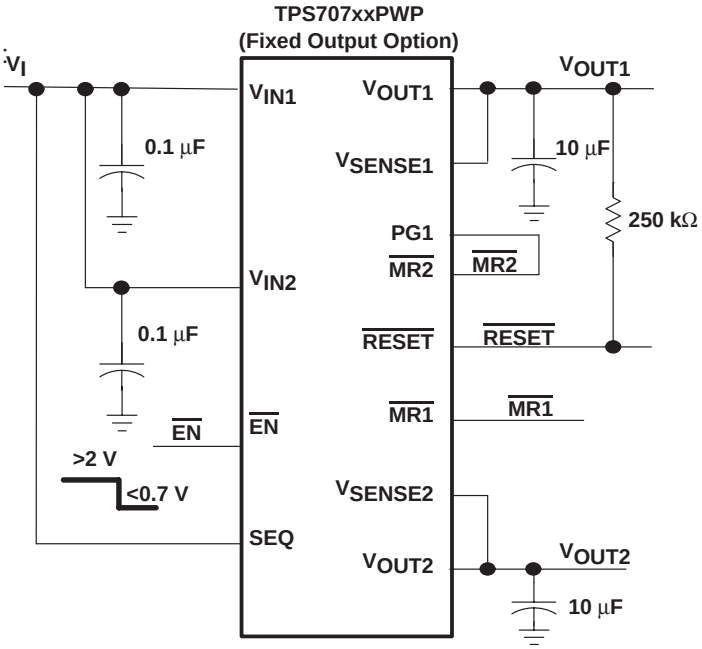
sequencing timing diagrams (continued)

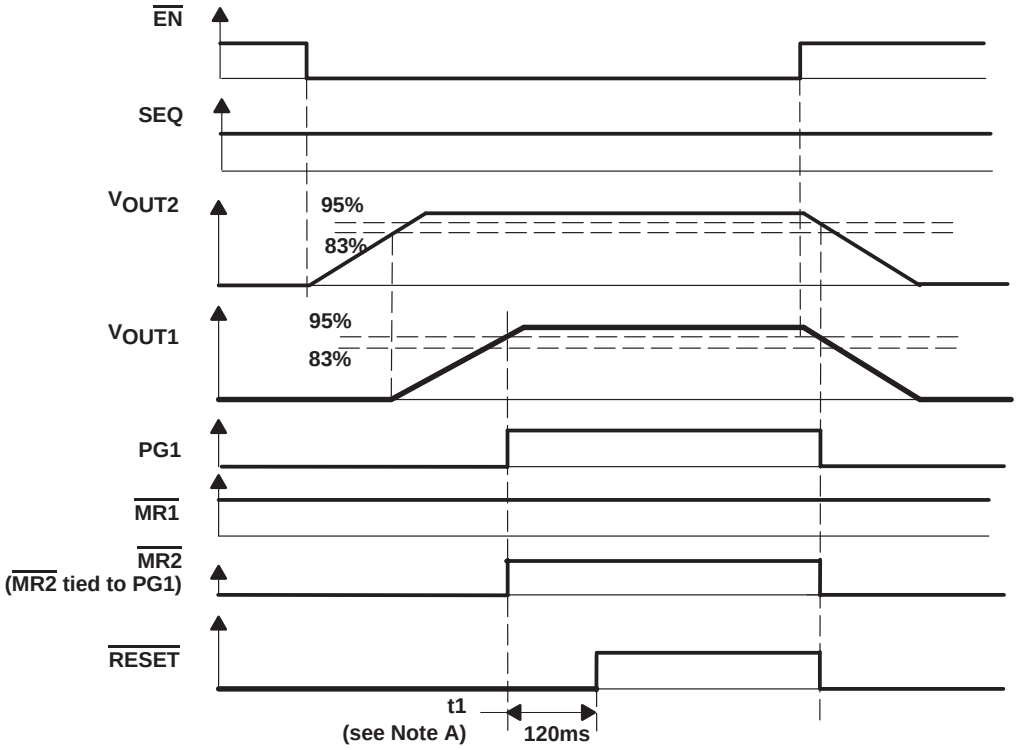
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is left unconnected and is therefore at logic high.

explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken to logic low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{EN}$ is returned to logic high, both devices turn off and both PG1 (tied to $\overline{MR2}$) and $\overline{RESET}$ return to logic low.





NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

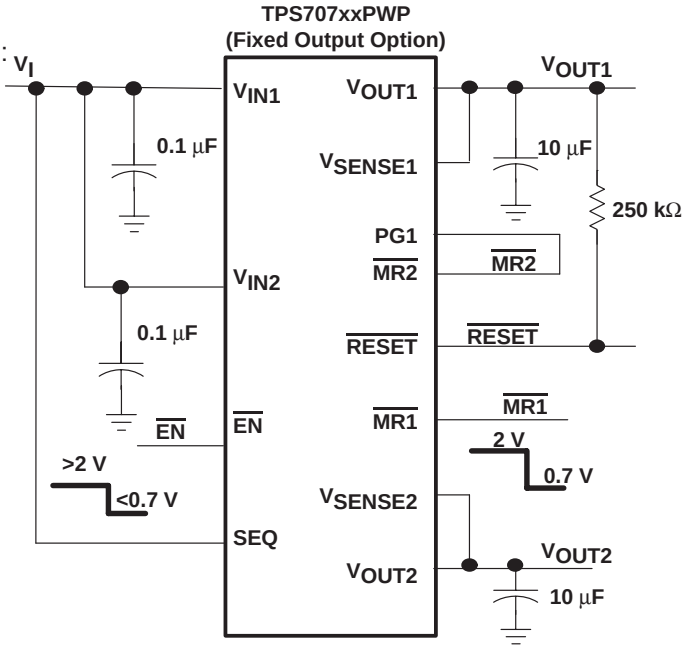
Figure 37. Timing When SEQ = High

APPLICATION INFORMATION

sequencing timing diagrams (continued)

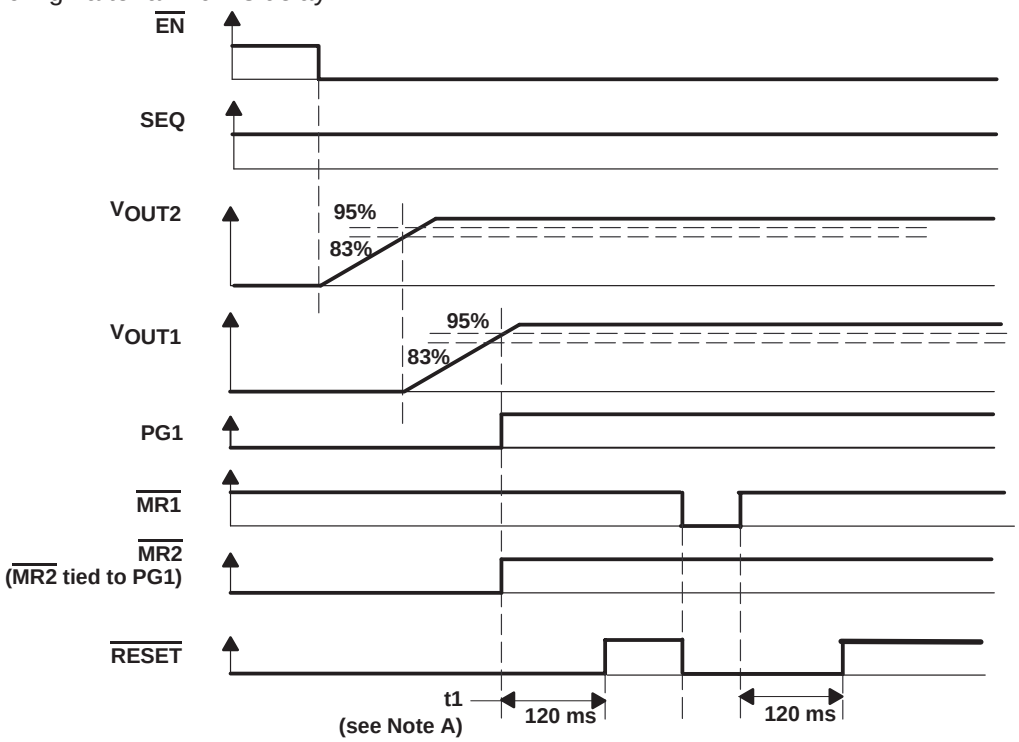
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is initially at logic high but is eventually toggled.



explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When $\overline{MR1}$ is taken low, $\overline{RESET}$ returns to logic low but the outputs remain in regulation. When $\overline{MR1}$ is returned to logic high, since both V_{OUT1} and V_{OUT2} remain above 95% of their respective regulated output voltages and $\overline{MR2}$ (tied to PG1) remains at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay.



NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 38. Timing When $\overline{MR1}$ is Toggled

APPLICATION INFORMATION

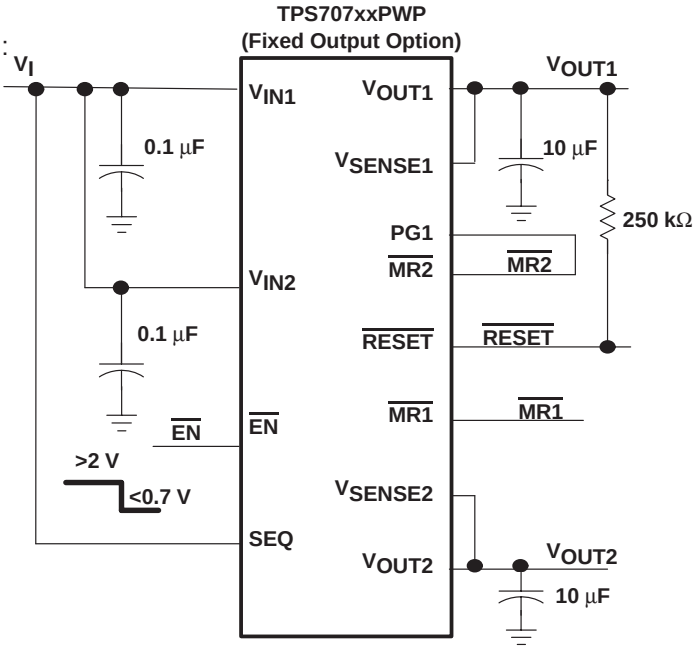
sequencing timing diagrams (continued)

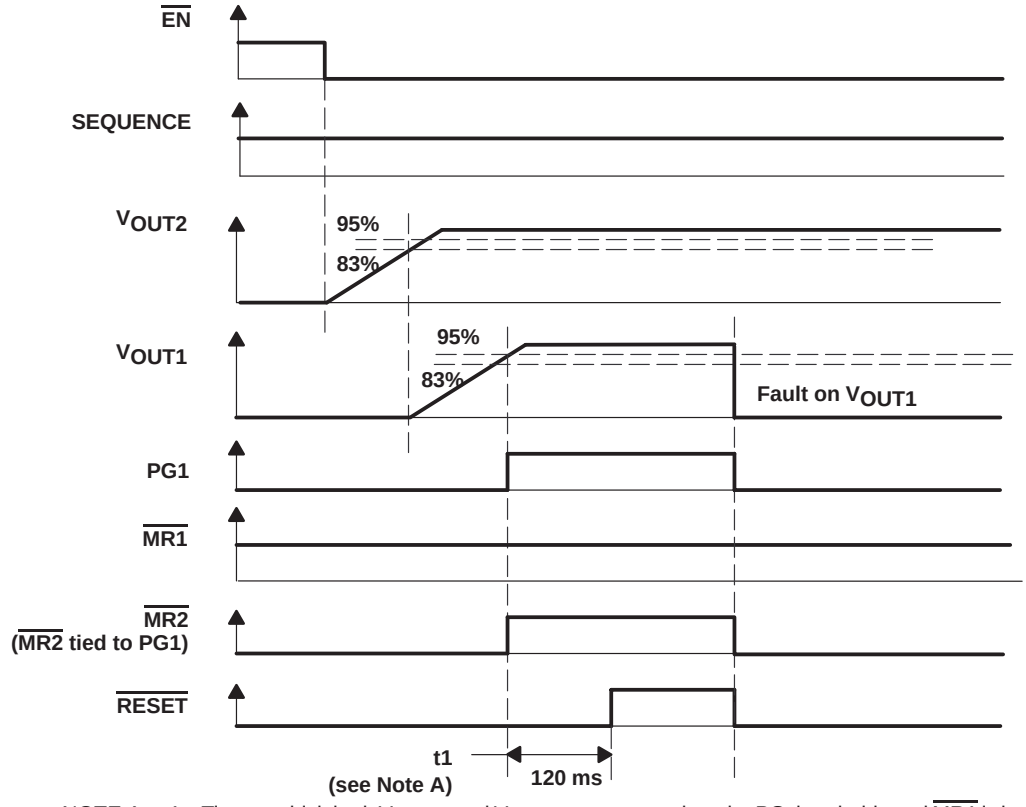
application conditions not shown in block diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is left unconnected and is therefore at logic high.

explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When a fault on V_{OUT1} causes it to fall below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic low, causing $\overline{RESET}$ to return to logic low. V_{OUT2} remains on because SEQ is high.





NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

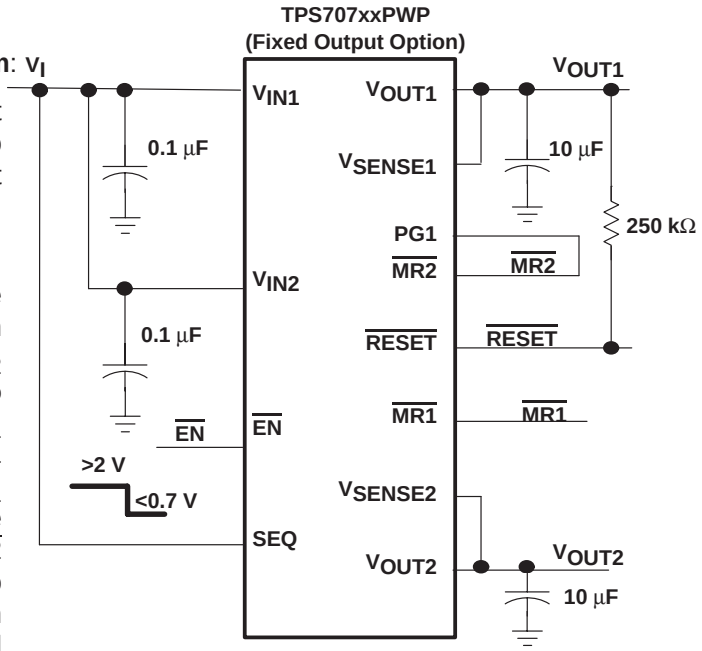
Figure 39. Timing When V_{OUT1} Faults Out

APPLICATION INFORMATION

sequencing timing diagrams (continued)

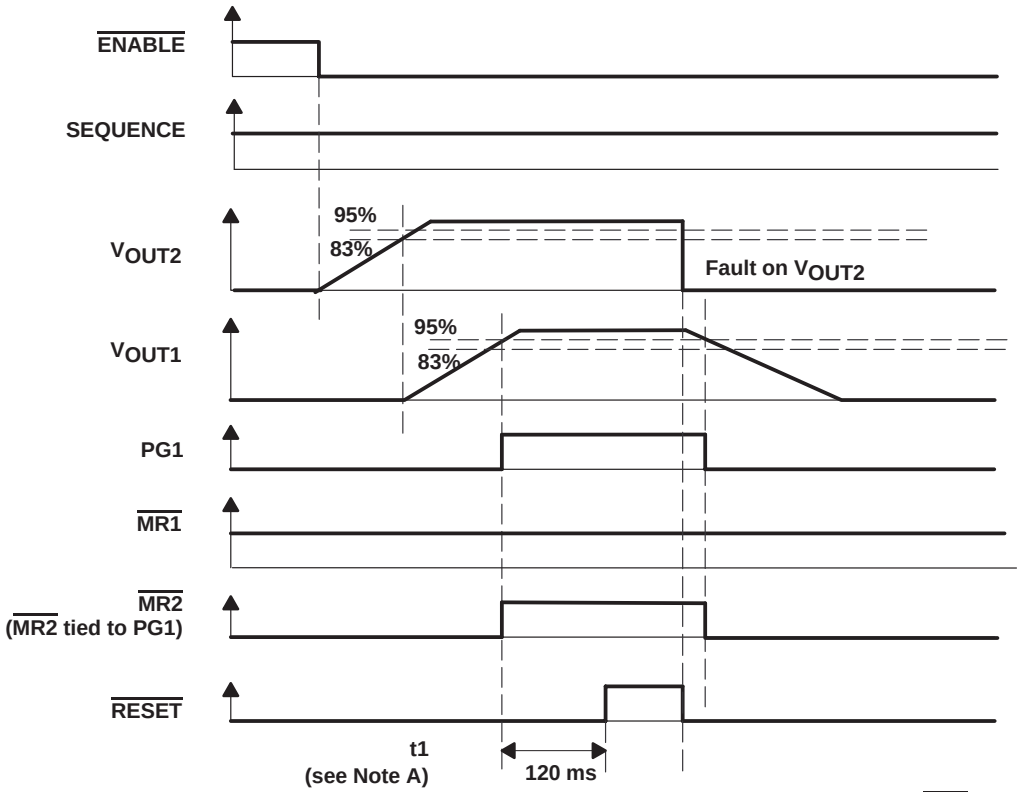
application conditions not shown in block diagram: V_I

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to $\overline{MR2}$; $\overline{MR1}$ is left unconnected and is therefore at logic high.



explanation of timing diagrams:

$\overline{EN}$ is initially high; therefore, both regulators are off and PG1 and $\overline{RESET}$ are at logic low. With SEQ at logic high, when $\overline{EN}$ is taken low, V_{OUT2} turns on. V_{OUT1} turns on after V_{OUT2} reaches 83% of its regulated output voltage. When V_{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) goes to logic high. When both V_{OUT1} and V_{OUT2} reach 95% of their respective regulated output voltages and both $\overline{MR1}$ and $\overline{MR2}$ (tied to PG1) are at logic high, $\overline{RESET}$ is pulled to logic high after a 120 ms delay. When a fault on V_{OUT2} causes it to fall below 95% of its regulated output voltage, $\overline{RESET}$ returns to logic low and V_{OUT1} begins to power down because SEQ is high. When V_{OUT1} falls below 95% of its regulated output voltage, PG1 (tied to $\overline{MR2}$) returns to logic low.



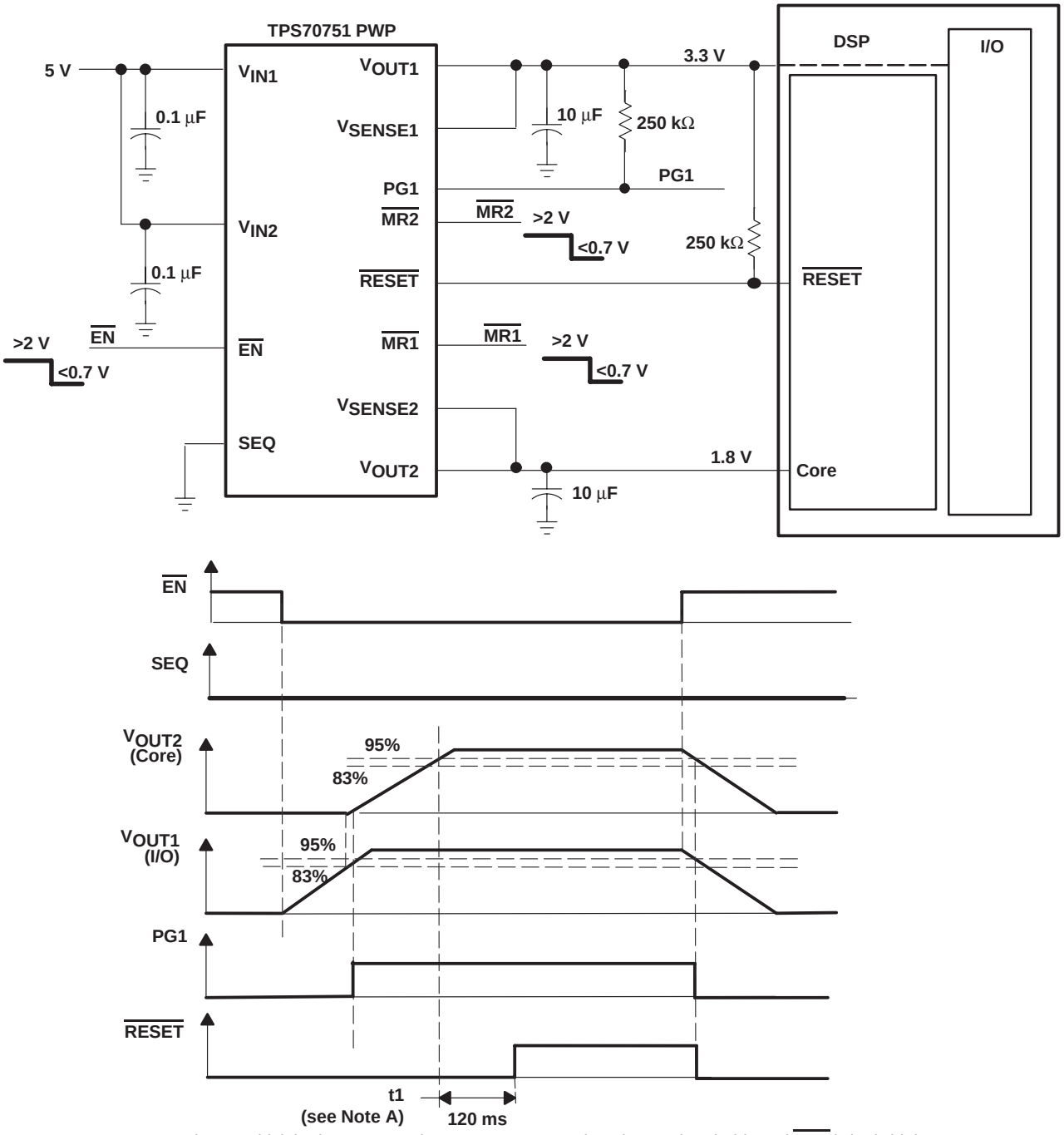
NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 40. Timing When V_{OUT2} Faults Out

APPLICATION INFORMATION

split voltage DSP application

Figure 41 shows a typical application where the TPS70751 is powering up a DSP. In this application by grounding the SEQ pin, V_{OUT1}(I/O) will be powered up first, and then V_{OUT2}(core).



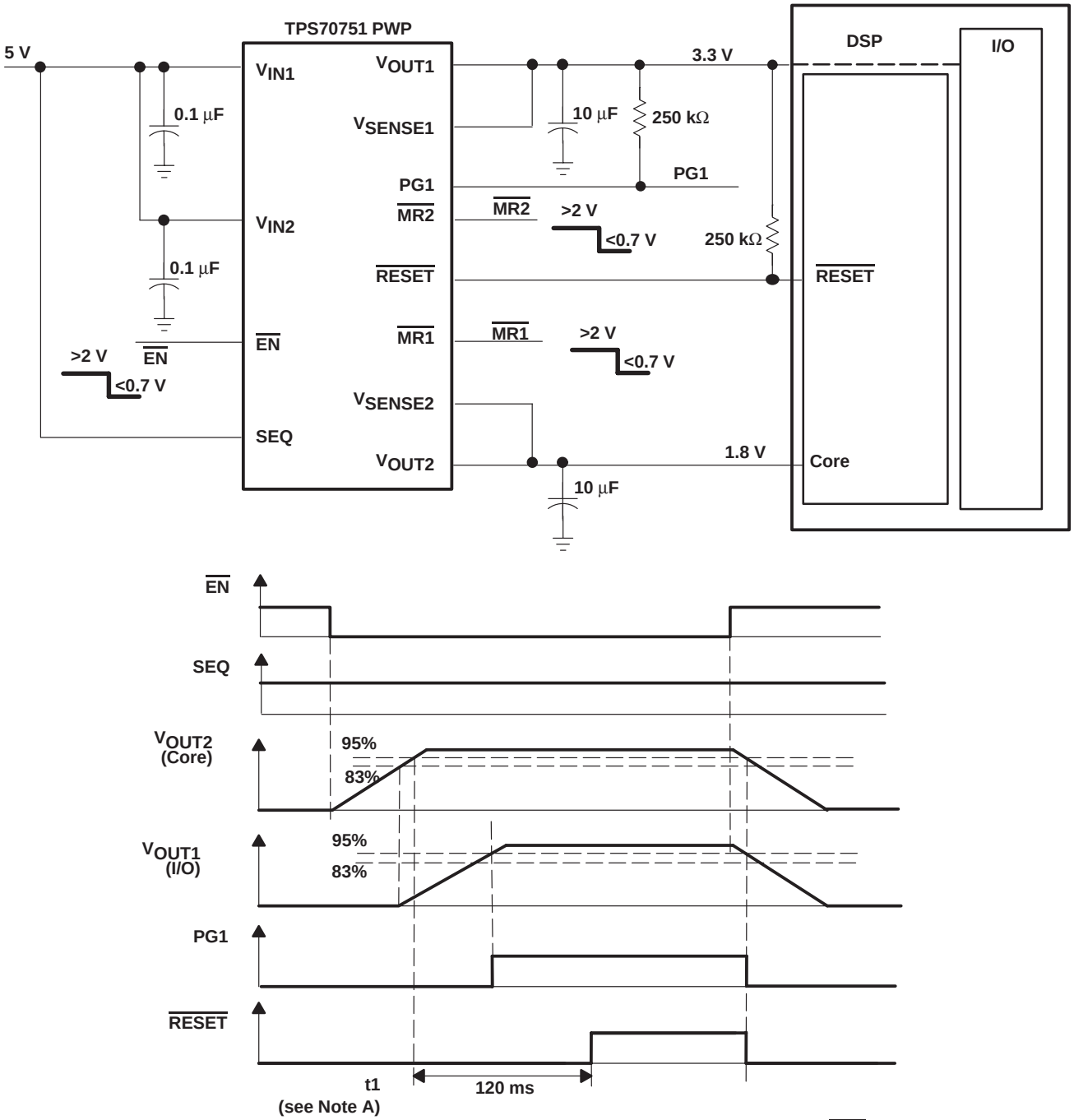
NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 41. Application Timing Diagram (SEQ = Low)

APPLICATION INFORMATION

split voltage DSP application (continued)

Figure 42 shows a typical application where the TPS70751 is powering up a DSP. In this application by pulling up the SEQ pin, V_{OUT2}(Core) will be powered up first, and then V_{OUT1}(I/O).



NOTE A: t1 – Time at which both V_{OUT1} and V_{OUT2} are greater than the PG thresholds and $\overline{MR1}$ is logic high.

Figure 42. Application Timing Diagram (SEQ = High)

APPLICATION INFORMATION

input capacitor

For a typical application, an input bypass capacitor (0.1 μF – 1 μF) is recommended. This capacitor will filter any high frequency noise generated in the line. For fast transient condition where droop at the input of the LDO may occur due to high inrush current, it is recommended to place a larger capacitor at the input as well. The size of this capacitor is dependant on the output current and response time of the main power supply, as well as the distance to the V_I pins of the LDO.

output capacitor

As with most LDO regulators, the TPS707xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance values are 10 μF ceramic capacitors with an ESR (equivalent series resistance) between 50 mΩ and 2.5 Ω or 6.8 μF tantalum capacitors with ESR between 250 mΩ and 4 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors with capacitance values greater than 10 μF are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Below is a partial listing of surface-mount capacitors usable with the TPS707xx. for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

VALUE	MFR.	MAX ESR†	PART NO.
22 μF	Kemet	345 mΩ	7495C226K0010AS
33 μF	Sanyo	100 mΩ	10TPA33M
47 μF	Sanyo	100 mΩ	6TPA47M
68 μF	Sanyo	45 mΩ	10TPC68M

ESR and transient response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

Besides its capacitance, every capacitor also contains parasitic impedances. These parasitic impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 43.

Figure 43. – ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

APPLICATION INFORMATION

Figure 44 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

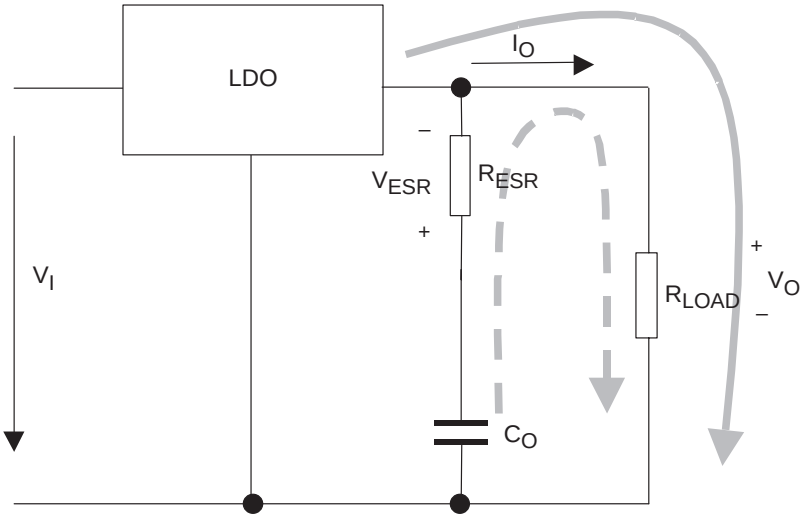


Figure 44. LDO Output Stage With Parasitic Resistances ESR

In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_O) = V_O$). This means no current is flowing into the C_O branch. If I_O suddenly increases (transient condition), the following occurs:

The LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 45). Therefore, capacitor C_O provides the current for the new load condition (dashed arrow). C_O now acts like a battery with an internal resistance, ESR. Depending on the current demand at the output, a voltage drop will occur at R_{ESR}. This voltage is shown as V_{ESR} in Figure 44.

When C_O is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) – V_{ESR}$. Due to the discharge of C_O, the output voltage V_O will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 45.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

APPLICATION INFORMATION

conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement.

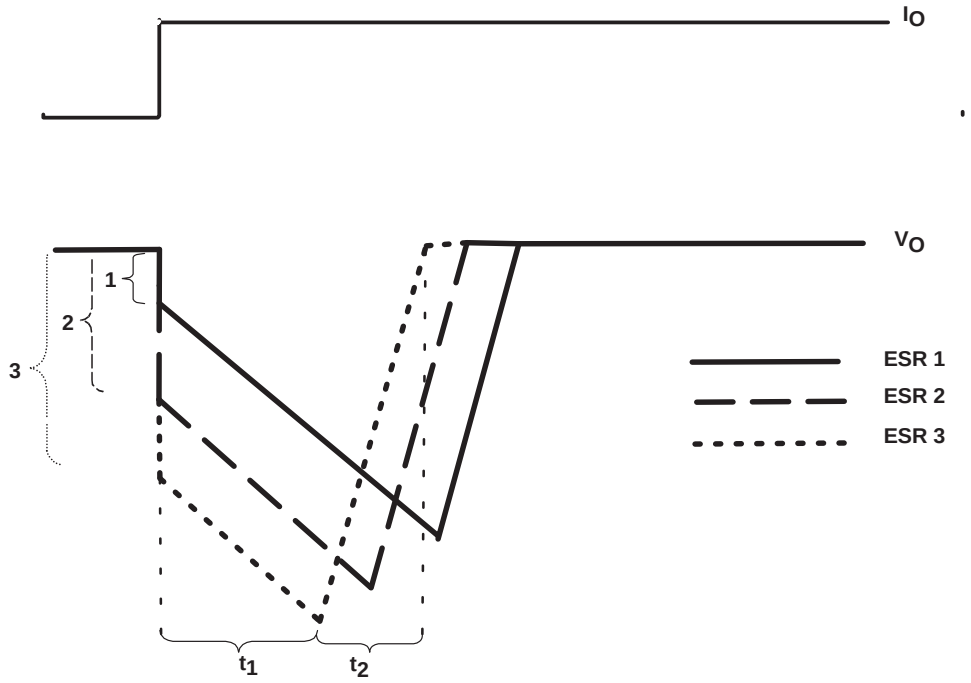


Figure 45. – Correlation of Different ESRs and Their Influence to the Regulation of V_O at a Load Step From Low-to-High Output Current

APPLICATION INFORMATION

programming the TPS70702 adjustable LDO regulator

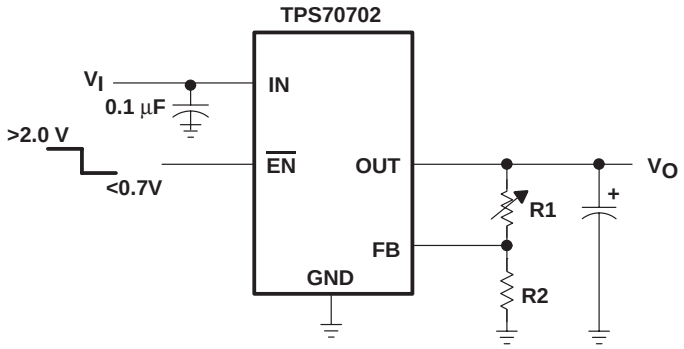
The output voltage of the TPS70702 adjustable regulators is programmed using external resistor dividers as shown in Figure 46.

Resistors R1 and R2 should be chosen for approximately 7 μA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at the sense terminal increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at approximately 7 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$

Where:

V_{ref} = 1.224 V typ (the internal reference voltage)



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	174	169	kΩ
3.3 V	287	169	kΩ
3.6 V	324	169	kΩ

Figure 46. TPS70702 Adjustable LDO Regulator Programming

regulator protection

Both TPS707xx PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS707xx also features internal current limiting and thermal protection. During normal operation, the TPS707xx regulator 1 limits output current to approximately 1.6 A (typ) and regulator 2 limits output current to approximately 750 mA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

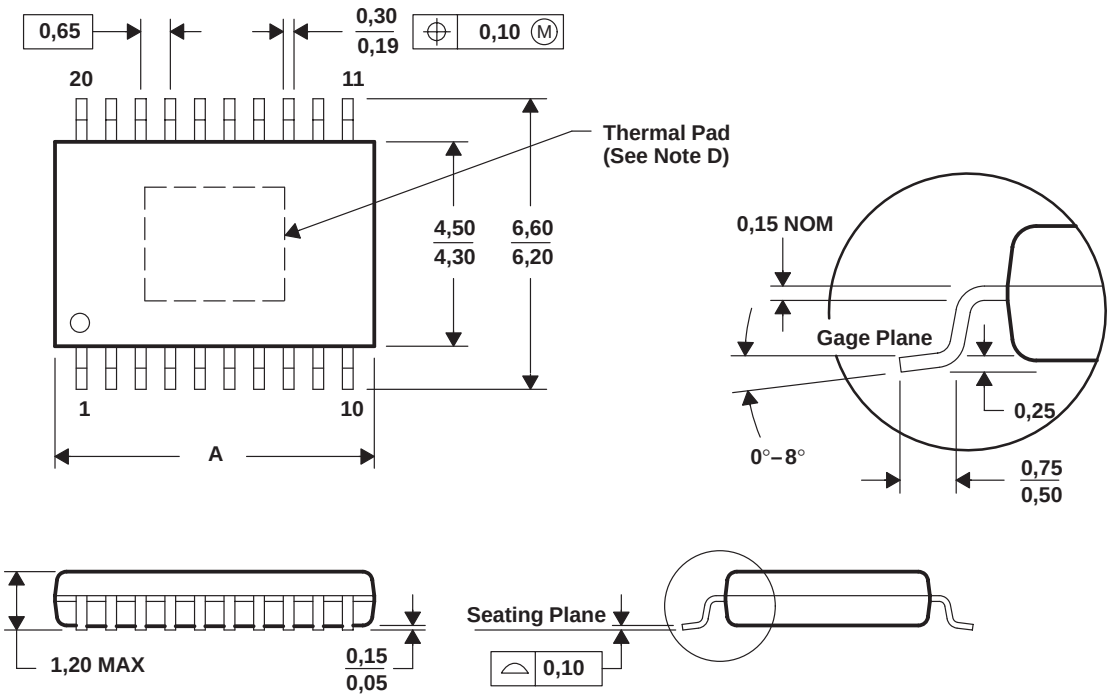
$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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