查询S75PL127JBDBFWU2供应商 捷多邦，专业PCB打样工厂，24小时加急出货

S75PLI27J MCPs

Stacked Multi-Chip Product (MCP)
CODE Flash, pSRAM and DATA Flash I28M (8M x I6-Bit CMOS 3.0 Volt-Only, Simultaneous Operation, Page Mode CODE Flash Memory, with 64M/32M (4M/2M x I6-Bit) pSRAM and 5I2M/256/I28M (32M/I6M/8M x I6-Bit) Data Flash Memory

Data Sheet

SPANSION™

ADVANCE INFORMATION

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High Performance**
  - 65ns for PL-J, 70ns for pSRAM, and 110ns for GL-N
  - Page access - 25ns
- **Package**
  - 9 x 12 mm 84 ball FBGA
- **Operating Temperature**
  - –25°C to +85°C (Wireless)
- **Other temperature grade options**
  - Please contact the factory through the local sales support team

General Description

The 75PL Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One S29PL127J based CODE Flash device(s)
- pSRAM
- One or more S29GLxxxN based DATA Flash device(s)

32M pSRAM		Data Flash		
Code Flash	Density	128M	256M	512M
	128M	S75PL127JBD	S75PL127JBE	S75PL127JBF

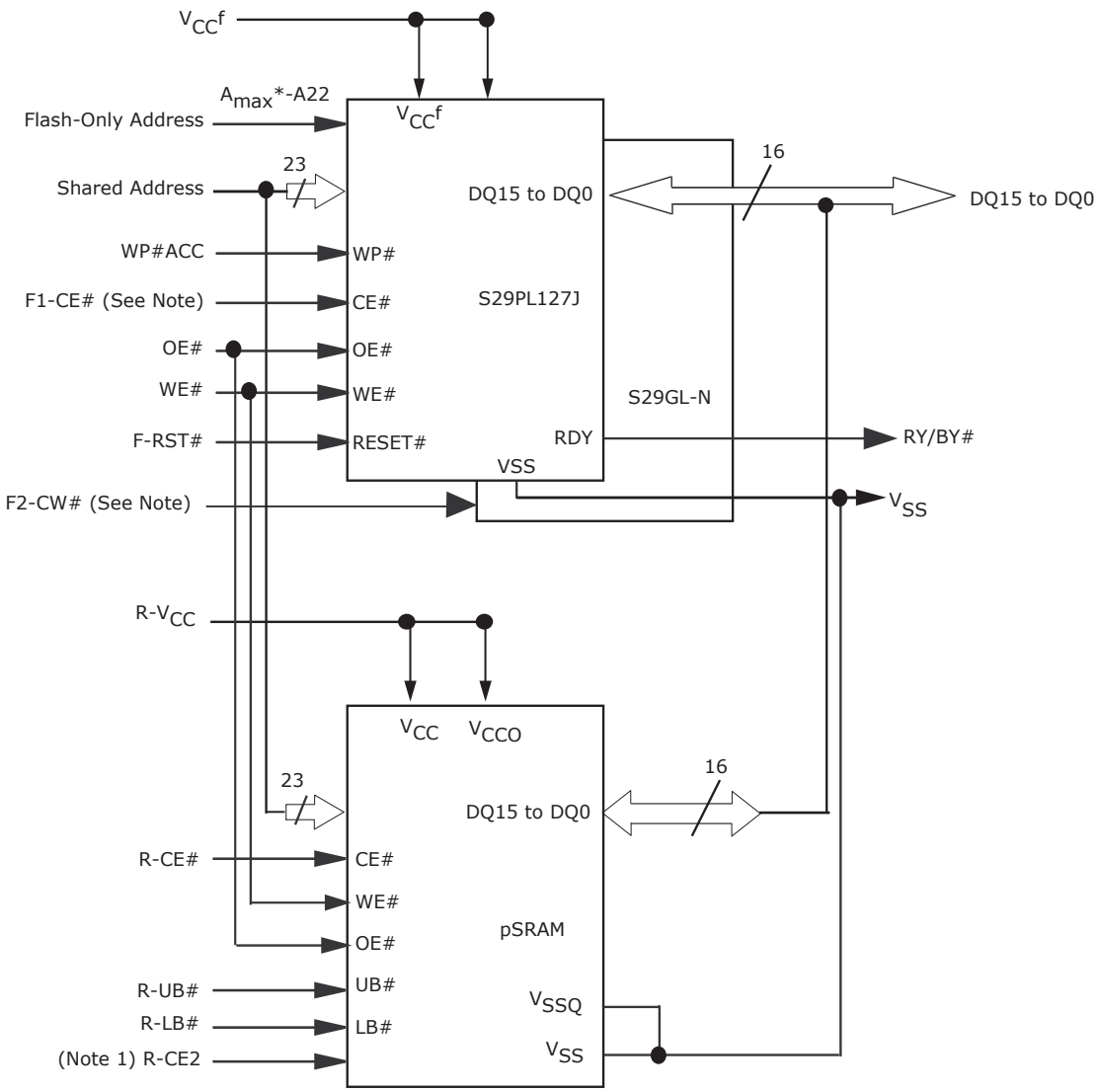
64M pSRAM		Data Flash		
Code Flash	Density	128M	256M	512M
	128M	S75PL127JCD	S75PL127JCE	S75PL127JCF

找PDF 维库一下 pdf.dzsc.com

Product Selector Guide

Device-Model#	PL127J Access Times (ns)	pSRAM density	pSRAM Access Time (ns)	Supplier	Data Storage Density	Package
S75PL127JBD-KU	65	32 Mb	70	Type 6	128 Mb (110ns)	9x12 mm 84-ball FBGA
S75PL127JBD-KB				Type 2		
S75PL127JCD-KU		64 Mb		Type 6		
S75PL127JCD-KB				Type 2		
S75PL127JBE-KU	65	32 Mb	70	Type 6	256 Mb (110ns)	9x12 mm 84-ball FBGA
S75PL127JBE-KB				Type 2		
S75PL127JCE-KU		64 Mb		Type 6		
S75PL127JCE-KB				Type 2		
S75PL127JBF-KU	65	32 Mb	70	Type 6	512 Mb (110ns)	9x12 mm 84-ball FBGA
S75PL127JBF-KB				Type 2		
S75PL127JCF-KU		64 Mb		Type 6		
S75PL127JCF-KB				Type 2		

MCP Block Diagram

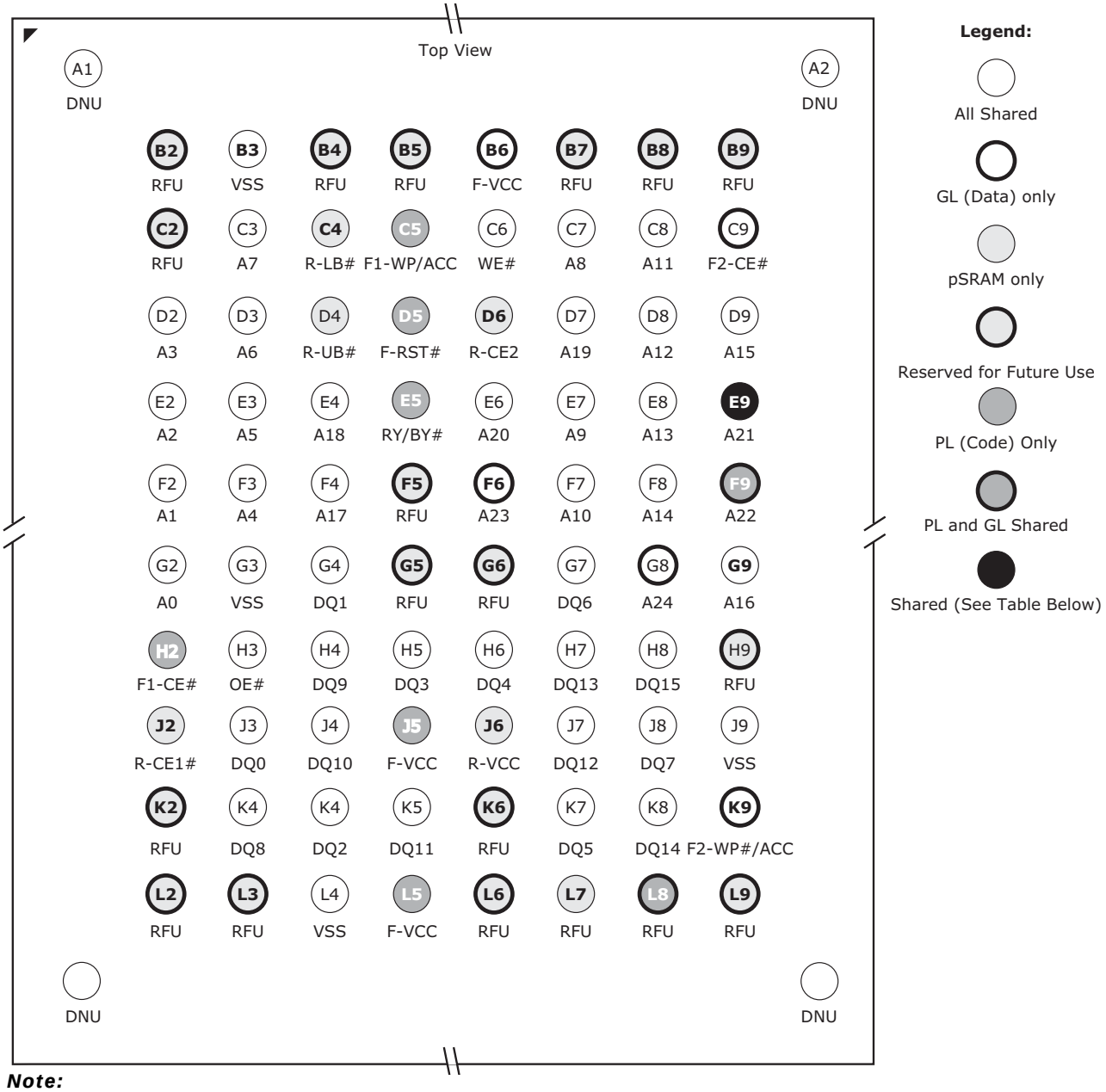


Note:

F1-CE# and F2-CE# are the chip-enable pins for the PL and GL Flash devices, respectively.

Amax -A24 for GL512, A23 for GL256N, A22 for GL128 and PL127J. Flash-only addressess may be shared between PL and GL, but is not shared with pSRAM. For more details, refer to the table following the connection diagram.

Connection Diagram



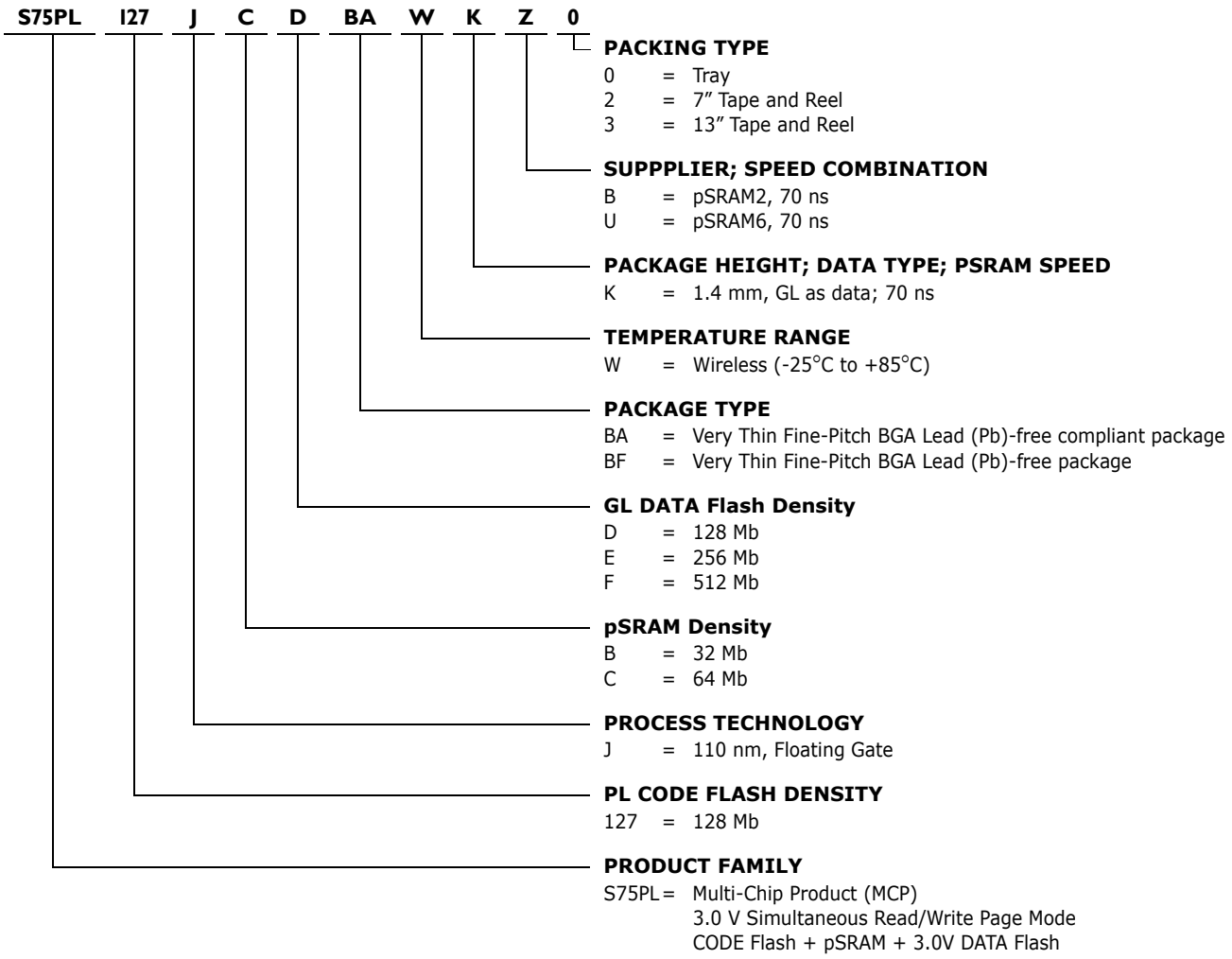
Note:
Connect 2-WP#/ ACC (K9) to Flash Vcc.

MCP	GL-Only Addresses	PL-GL Shared Addresses	PL, GL, and pSRAM Shared Addresses
S75PL127JBD	-	A22–A21	A20–A0
S75PL127JCD	-	A22	A21–A0
S75PL127JBE	A23	A22–A21	A20–A0
S75PL127JCE	A23	A22	A21–A0
S75PL127JBF	A24-A23	A22–A21	A20–A0
S75PL127JCF	A24-A23	A22	A21–A0

Pin Description

Amax–A0	=	Address Inputs
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
F1-CE#	=	Chip Enable for PL
F2-CE	=	Chip Enable for GL
	=	
R-CE#1	=	Chip Enable 1 (pSRAM)
R-CE#2	=	Chip Enable 2 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash)
R-UB#	=	Upper Byte Control (pSRAM)
R-LB#	=	Lower Byte Control (pSRAM)
F-RST#	=	Hardware Reset Pin (Flash)
F1-WP#/ACC	=	Hardware Write Protect /Acceleration Pin (PL) Hardware Write Protect/Acceleration Pin (GL) Should be tied to Vcc
F-VCC	=	Flash 3.0 volt-only single power supply
R-VCCs	=	pSRAM Power Supply
VSS	=	Device Ground (Common)
DNU	=	Do Not Use

Ordering Information



Valid Combinations

Data: S29GLI28N

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	PL127J Speed Options (ns)	pSRAM Supplier/ Access Time (ns)	Package Marking
S75PL127JBD	BAW	KU	0, 2, 3, (Note 1)	65	Type 6 / 70	(Note 2)
S75PL127JBD		KB			Type 2 / 70	
S75PL127JCD		KU			Type 6/ 70	
S75PL127JCD		KB			Type 2 / 70	
S75PL127JBD	BFW	KU			Type 6 / 70	
S75PL127JBD		KB			Type 2 / 70	
S75PL127JCD		KU			Type 6 / 70	
S75PL127JCD		KB			Type 2 / 70	

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading **S** and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Data: S29GL256N

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	PL127J Speed Options (ns)	pSRAM Supplier/ Access Time (ns)	Package Marking
S75PL127JBE	BAW	KU	0, 2, 3, (Note 1)	65	Type 6 / 70	(Note 2)
S75PL127JBE		KB			Type 2 / 70	
S75PL127JCE		KU			Type 6 / 70	
S75PL127JCE		KB			Type 2 / 70	
S75PL127JBE	BFW	KU			Type 6 / 70	
S75PL127JBE		KB			Type 2 / 70	
S75PL127JCE		KU			Type 6 / 70	
S75PL127JCE		KB			Type 2 / 70	

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading **S** and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Data: S29GL5I2N

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	PL127J Speed Options (ns)	pSRAM Supplier/ Access Time (ns)	Package Marking
S75PL127JBF	BAW	KU	0, 2, 3, (Note 1)	65	Type 6 / 70	(Note 2)
S75PL127JBF		KB			Type 2 / 70	
S75PL127JCF		KU			Type 6 / 70	
S75PL127JCF		KB			Type 2 / 70	
S75PL127JBF	BFW	KU			Type 6 / 70	
S75PL127JBF		KB			Type 2 / 70	
S75PL127JCF		KU			Type 6 / 70	
S75PL127JCF		KB			Type 2 / 70	

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading **S** and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29PL127J/S29PL064J/S29PL032J for MCP
128/64/32 Megabit (8/4/2 M x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Read/Write Flash Memory with Enhanced VersatileIO™ Control

SPANSION™

PRELIMINARY

Distinctive Characteristics

ARCHITECTURAL ADVANTAGES

- **128/64/32 Mbit Page Mode devices**
  - Page size of 8 words: Fast page read access from random locations within the page
- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.1 volt read, erase, and program operations for battery-powered applications
- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- **FlexBank Architecture (PL127J/PL064J/PL032J)**
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A:
    PL127J -16 Mbit (4 Kw x 8 and 32 Kw x 31)
    PL064J - 8 Mbit (4 Kw x 8 and 32 Kw x 15)
    PL032J - 4 Mbit (4 Kw x 8 and 32 Kw x 7)
  - Bank B:
    PL127J - 48 Mbit (32 Kw x 96)
    PL064J - 24 Mbit (32 Kw x 48)
    PL032J - 12 Mbit (32 Kw x 24)
  - Bank C:
    PL127J - 48 Mbit (32 Kw x 96)
    PL064J - 24 Mbit (32 Kw x 48)
    PL032J - 12 Mbit (32 Kw x 24)
  - Bank D:
    PL127J -16 Mbit (4 Kw x 8 and 32 Kw x 31)
    PL064J - 8 Mbit (4 Kw x 8 and 32 Kw x 15)
    PL032J - 4 Mbit (4 Kw x 8 and 32 Kw x 7)
- **Enhanced VersatileI/O™ (V_{IO}) Control**
  - Output voltage generated and input voltages tolerated on all control inputs and I/Os is determined by the voltage on the V_{IO} pin
  - V_{IO} options at 1.8 V and 3 V I/O for PL127J devices
  - 3V V_{IO} for PL064J and PL032J devices
- **SecSi™ (Secured Silicon) Sector region**
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words
- **Both top and bottom boot blocks in one device**
- **Manufactured on 110 nm process technology**
- **Data Retention: 20 years typical**
- **Cycling Endurance: 1 million cycles per sector typical**

PERFORMANCE CHARACTERISTICS

- **High Performance**
  - Page access times as fast as 20 ns
  - Random access times as fast as 55 ns
- **Power consumption (typical values at 10 MHz)**
  - 45 mA active read current
  - 17 mA program/erase current
  - 0.2 µA typical standby mode current

SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F, Am29LV, Am29DL, and AM29PDL families and MBM29QM/RM, MBM29LV, MBM29DL, MBM29PDL families
- **CFI (Common Flash Interface) compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP#/ ACC (Write Protect/Acceleration) input**
  - At V_{IL}, hardware level protection for the first and last two 4K word sectors.
  - At V_{IH}, allows removal of sector protection
  - At V_{HH}, provides accelerated programming in a factory setting
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **Package options**
  - Standard discrete pinouts
    11 x 8 mm, 80-ball Fine-pitch BGA (PL127J) (VBG080)
    8 x 6 mm, 48-ball Fine pitch BGA (PL064J/PL032J) (VBK048)
  - MCP-compatible pinout
    8 x 11.6 mm, 64-ball Fine-pitch BGA (PL127J) 7 x 9 mm, 56-ball Fine-pitch BGA (PL064J and PL032J) Compatible with MCP pinout, allowing easy integration of RAM into existing designs

General Description

The PL127J/PL064J/PL032J is a 128/128/64/32 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8/8/4/2 Mwords. The devices are offered in the following packages:

- 11mm x 8mm, 64-ball Fine-pitch BGA standalone (all)
- 9mm x 8mm, 80-ball Fine-pitch BGA standalone (PL127J)
- 8mm x 11.6mm, 64-ball Fine pitch BGA multi-chip compatible (PL127J)

The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

The device offers fast page access times of 20 to 30 ns, with corresponding random access times of 55 to 70 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Bank	PLI27J Sectors
A	16 Mbit (4 Kw x 8 and 32 Kw x 31)
B	48 Mbit (32 Kw x 96)
C	48 Mbit (32 Kw x 96)
D	16 Mbit (4 Kw x 8 and 32 Kw x 31)

Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry.

Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Pin Description

Amax–A0	=	Address bus
DQ15–DQ0	=	16-bit data inputs/outputs/float
CE#	=	Chip Enable Inputs
OE#	=	Output Enable Input
WE#	=	Write Enable
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally
RY/BY#	=	Ready/Busy output and open drain. When RY/BY#= V_{IH}, the device is ready to accept read operations and commands. When RY/BY#= V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
WP#/ACC	=	Write Protect/Acceleration Input. When WP#/ACC= V_{IL}, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP#/ACC= V_{IH}, these sector are unprotected unless the DYB or PPB is programmed. When WP#/ACC= 12V, program and erase operations are accelerated.
V_{IO}	=	Input/Output Buffer Power Supply (1.65 V to 1.95 V (for PL127J) or 2.7 V to 3.6 V (for all PLxxxJ devices)
V_{CC}	=	Chip Power Supply (2.7 V to 3.6 V or 2.7 to 3.3 V)
RESET#	=	Hardware Reset Pin
CE#1	=	Chip Enable Inputs

Notes:

1. Amax = A22 (PL127J), A21 (PL064J), A20 (PL032J)

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. PLI27J Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Amax–A0)	DQI5–DQ0
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write	L	H	L	H	X (Note 2)	A_{IN}	D_{IN}
Standby	V_{IO}± 0.3 V	X	X	V_{IO} ± 0.3 V	X (Note 2)	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5-12.5 V, V_{HH} = 8.5-9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the High Voltage Sector Protection section.*
2. *WP#/ACC must be high when writing to upper two and lower two sectors.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to Table 19 for timing specifications and to Figure 11 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A3 select an 8 word page, and address bits A2–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. Fast page mode accesses are obtained by keeping Amax–A3 constant and changing A2–A0 to select the specific word within that page.

Table 2. Page Select

Word	A2	AI	A0
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

Simultaneous Read/Write Operation

In addition to the conventional features (read, program, erase-suspend read, and erase-suspend program), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (PL127J: A22–A20, L064J: A21–A19, PL032J: A20–A18) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 3. Bank Select

Bank	PLI27J: A22–A20 PL064J: A2I–AI9 PL032J: A20–AI8
Bank A	000
Bank B	001, 010, 011
Bank C	100, 101, 110
Bank D	111

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The "Word Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the set of address space that each sector occupies. A "bank address" is the set of address bits required to uniquely select a bank. Similarly, a "sector address" refers to the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. See the timing specification tables and timing diagrams in the Reset for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to V_{CC} when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the SecSiTM Sector Addresses and Autoselect Command Sequence for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{IO} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{IO} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device

requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in "DC Characteristics" represents the CMOS standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. I_{CC5} in "DC Characteristics" represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristic tables for RESET# parameters and to 13 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

Table 4. PLI27J Sector Architecture

Bank	Sector	Sector Address (A22-AI2)	Sector Size (Kwords)	Address Range (xI6)
Bank A	SA0	00000000000	4	000000h–000FFFh
	SA1	00000000001	4	001000h–001FFFh
	SA2	00000000010	4	002000h–002FFFh
	SA3	00000000011	4	003000h–003FFFh
	SA4	00000000100	4	004000h–004FFFh
	SA5	00000000101	4	005000h–005FFFh
	SA6	00000000110	4	006000h–006FFFh
	SA7	00000000111	4	007000h–007FFFh
	SA8	00000001XXX	32	008000h–00FFFFh
	SA9	00000010XXX	32	010000h–017FFFh
	SA10	00000011XXX	32	018000h–01FFFFh
	SA11	00000100XXX	32	020000h–027FFFh
	SA12	00000101XXX	32	028000h–02FFFFh
	SA13	00000110XXX	32	030000h–037FFFh
	SA14	00000111XXX	32	038000h–03FFFFh
	SA15	00001000XXX	32	040000h–047FFFh
	SA16	00001001XXX	32	048000h–04FFFFh
	SA17	00001010XXX	32	050000h–057FFFh
	SA18	00001011XXX	32	058000h–05FFFFh
	SA19	00001100XXX	32	060000h–067FFFh
	SA20	00001101XXX	32	068000h–06FFFFh
	SA21	00001110XXX	32	070000h–077FFFh
	SA22	00001111XXX	32	078000h–07FFFFh
	SA23	00010000XXX	32	080000h–087FFFh
	SA24	00010001XXX	32	088000h–08FFFFh
	SA25	00010010XXX	32	090000h–097FFFh
	SA26	00010011XXX	32	098000h–09FFFFh
	SA27	00010100XXX	32	0A0000h–0A7FFFh
	SA28	00010101XXX	32	0A8000h–0AFFFFh
	SA29	00010110XXX	32	0B0000h–0B7FFFh
	SA30	00010111XXX	32	0B8000h–0BFFFFh
	SA31	00011000XXX	32	0C0000h–0C7FFFh
	SA32	00011001XXX	32	0C8000h–0CFFFFh
	SA33	00011010XXX	32	0D0000h–0D7FFFh
	SA34	00011011XXX	32	0D8000h–0DFFFFh
	SA35	00011100XXX	32	0E0000h–0E7FFFh
	SA36	00011101XXX	32	0E8000h–0EFFFFh
	SA37	00011110XXX	32	0F0000h–0F7FFFh
	SA38	00011111XXX	32	0F8000h–0FFFFFh

Table 4. PLl27J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-Al2)	Sector Size (Kwords)	Address Range (xl6)
Bank B	SA39	00100000XXX	32	100000h–107FFFh
	SA40	00100001XXX	32	108000h–10FFFFh
	SA41	00100010XXX	32	110000h–117FFFh
	SA42	00100011XXX	32	118000h–11FFFFh
	SA43	00100100XXX	32	120000h–127FFFh
	SA44	00100101XXX	32	128000h–12FFFFh
	SA45	00100110XXX	32	130000h–137FFFh
	SA46	00100111XXX	32	138000h–13FFFFh
	SA47	00101000XXX	32	140000h–147FFFh
	SA48	00101001XXX	32	148000h–14FFFFh
	SA49	00101010XXX	32	150000h–157FFFh
	SA50	00101011XXX	32	158000h–15FFFFh
	SA51	00101100XXX	32	160000h–167FFFh
	SA52	00101101XXX	32	168000h–16FFFFh
	SA53	00101110XXX	32	170000h–177FFFh
	SA54	00101111XXX	32	178000h–17FFFFh
	SA55	00110000XXX	32	180000h–187FFFh
	SA56	00110001XXX	32	188000h–18FFFFh
	SA57	00110010XXX	32	190000h–197FFFh
	SA58	00110011XXX	32	198000h–19FFFFh
	SA59	00110100XXX	32	1A0000h–1A7FFFh
	SA60	00110101XXX	32	1A8000h–1AFFFFh
	SA61	00110110XXX	32	1B0000h–1B7FFFh
	SA62	00110111XXX	32	1B8000h–1BFFFFh
	SA63	00111000XXX	32	1C0000h–1C7FFFh
	SA64	00111001XXX	32	1C8000h–1CFFFFh
	SA65	00111010XXX	32	1D0000h–1D7FFFh
	SA66	00111011XXX	32	1D8000h–1DFFFFh
	SA67	00111100XXX	32	1E0000h–1E7FFFh
	SA68	00111101XXX	32	1E8000h–1EFFFFh
	SA69	00111110XXX	32	1F0000h–1F7FFFh
	SA70	00111111XXX	32	1F8000h–1FFFFFh
	SA71	01000000XXX	32	200000h–207FFFh
	SA72	01000001XXX	32	208000h–20FFFFh
	SA73	01000010XXX	32	210000h–217FFFh
	SA74	01000011XXX	32	218000h–21FFFFh
	SA75	01000100XXX	32	220000h–227FFFh
	SA76	01000101XXX	32	228000h–22FFFFh
	SA77	01000110XXX	32	230000h–237FFFh
	SA78	01000111XXX	32	238000h–23FFFFh

Table 4. PLl27J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-Al2)	Sector Size (Kwords)	Address Range (xl6)
Bank B	SA79	01001000XXX	32	240000h–247FFFh
	SA80	01001001XXX	32	248000h–24FFFFh
	SA81	01001010XXX	32	250000h–257FFFh
	SA82	01001011XXX	32	258000h–25FFFFh
	SA83	01001100XXX	32	260000h–267FFFh
	SA84	01001101XXX	32	268000h–26FFFFh
	SA85	01001110XXX	32	270000h–277FFFh
	SA86	01001111XXX	32	278000h–27FFFFh
	SA87	01010000XXX	32	280000h–287FFFh
	SA88	01010001XXX	32	288000h–28FFFFh
	SA89	01010010XXX	32	290000h–297FFFh
	SA90	01010011XXX	32	298000h–29FFFFh
	SA91	01010100XXX	32	2A0000h–2A7FFFh
	SA92	01010101XXX	32	2A8000h–2AFFFFh
	SA93	01010110XXX	32	2B0000h–2B7FFFh
	SA94	01010111XXX	32	2B8000h–2BFFFFh
	SA95	01011000XXX	32	2C0000h–2C7FFFh
	SA96	01011001XXX	32	2C8000h–2CFFFFh
	SA97	01011010XXX	32	2D0000h–2D7FFFh
	SA98	01011011XXX	32	2D8000h–2DFFFFh
	SA99	01011100XXX	32	2E0000h–2E7FFFh
	SA100	01011101XXX	32	2E8000h–2EFFFFh
	SA101	01011110XXX	32	2F0000h–2F7FFFh
	SA102	01011111XXX	32	2F8000h–2FFFFFh
	SA103	01100000XXX	32	300000h–307FFFh
	SA104	01100001XXX	32	308000h–30FFFFh
	SA105	01100010XXX	32	310000h–317FFFh
	SA106	01100011XXX	32	318000h–31FFFFh
	SA107	01100100XXX	32	320000h–327FFFh
	SA108	01100101XXX	32	328000h–32FFFFh
	SA109	01100110XXX	32	330000h–337FFFh
	SA110	01100111XXX	32	338000h–33FFFFh
	SA111	01101000XXX	32	340000h–347FFFh
	SA112	01101001XXX	32	348000h–34FFFFh
	SA113	01101010XXX	32	350000h–357FFFh
	SA114	01101011XXX	32	358000h–35FFFFh
	SA115	01101100XXX	32	360000h–367FFFh
	SA116	01101101XXX	32	368000h–36FFFFh
	SA117	01101110XXX	32	370000h–377FFFh
	SA118	01101111XXX	32	378000h–37FFFFh

Table 4. PLl27J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-Al2)	Sector Size (Kwords)	Address Range (xl6)
Bank B	SA119	01110000XXX	32	380000h–387FFFh
	SA120	01110001XXX	32	388000h–38FFFFh
	SA121	01110010XXX	32	390000h–397FFFh
	SA122	01110011XXX	32	398000h–39FFFFh
	SA123	01110100XXX	32	3A0000h–3A7FFFh
	SA124	01110101XXX	32	3A8000h–3AFFFFh
	SA125	01110110XXX	32	3B0000h–3B7FFFh
	SA126	01110111XXX	32	3B8000h–3BFFFFh
	SA127	01111000XXX	32	3C0000h–3C7FFFh
	SA128	01111001XXX	32	3C8000h–3CFFFFh
	SA129	01111010XXX	32	3D0000h–3D7FFFh
	SA130	01111011XXX	32	3D8000h–3DFFFFh
	SA131	01111100XXX	32	3E0000h–3E7FFFh
	SA132	01111101XXX	32	3E8000h–3EFFFFh
	SA133	01111110XXX	32	3F0000h–3F7FFFh
	SA134	01111111XXX	32	3F8000h–3FFFFFh
Bank C	SA135	10000000XXX	32	400000h–407FFFh
	SA136	10000001XXX	32	408000h–40FFFFh
	SA137	10000010XXX	32	410000h–417FFFh
	SA138	10000011XXX	32	418000h–41FFFFh
	SA139	10000100XXX	32	420000h–427FFFh
	SA140	10000101XXX	32	428000h–42FFFFh
	SA141	10000110XXX	32	430000h–437FFFh
	SA142	10000111XXX	32	438000h–43FFFFh
	SA143	10001000XXX	32	440000h–447FFFh
	SA144	10001001XXX	32	448000h–44FFFFh
	SA145	10001010XXX	32	450000h–457FFFh
	SA146	10001011XXX	32	458000h–45FFFFh
	SA147	10001100XXX	32	460000h–467FFFh
	SA148	10001101XXX	32	468000h–46FFFFh
	SA149	10001110XXX	32	470000h–477FFFh
	SA150	10001111XXX	32	478000h–47FFFFh
	SA151	10010000XXX	32	480000h–487FFFh
	SA152	10010001XXX	32	488000h–48FFFFh
	SA153	10010010XXX	32	490000h–497FFFh
	SA154	10010011XXX	32	498000h–49FFFFh
	SA155	10010100XXX	32	4A0000h–4A7FFFh
	SA156	10010101XXX	32	4A8000h–4AFFFFh
	SA157	10010110XXX	32	4B0000h–4B7FFFh
	SA158	10010111XXX	32	4B8000h–4BFFFFh

Table 4. PLI27J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank C	SA159	10011000XXX	32	4C0000h–4C7FFFh
	SA160	10011001XXX	32	4C8000h–4CFFFFh
	SA161	10011010XXX	32	4D0000h–4D7FFFh
	SA162	10011011XXX	32	4D8000h–4DFFFFh
	SA163	10011100XXX	32	4E0000h–4E7FFFh
	SA164	10011101XXX	32	4E8000h–4EFFFFh
	SA165	10011110XXX	32	4F0000h–4F7FFFh
	SA166	10011111XXX	32	4F8000h–4FFFFFh
	SA167	10100000XXX	32	500000h–507FFFh
	SA168	10100001XXX	32	508000h–50FFFFh
	SA169	10100010XXX	32	510000h–517FFFh
	SA170	10100011XXX	32	518000h–51FFFFh
	SA171	10100100XXX	32	520000h–527FFFh
	SA172	10100101XXX	32	528000h–52FFFFh
	SA173	10100110XXX	32	530000h–537FFFh
	SA174	10100111XXX	32	538000h–53FFFFh
	SA175	10101000XXX	32	540000h–547FFFh
	SA176	10101001XXX	32	548000h–54FFFFh
	SA177	10101010XXX	32	550000h–557FFFh
	SA178	10101011XXX	32	558000h–15FFFFh
	SA179	10101100XXX	32	560000h–567FFFh
	SA180	10101101XXX	32	568000h–56FFFFh
	SA181	10101110XXX	32	570000h–577FFFh
	SA182	10101111XXX	32	578000h–57FFFFh
	SA183	10110000XXX	32	580000h–587FFFh
	SA184	10110001XXX	32	588000h–58FFFFh
	SA185	10110010XXX	32	590000h–597FFFh
	SA186	10110011XXX	32	598000h–59FFFFh
	SA187	10110100XXX	32	5A0000h–5A7FFFh
	SA188	10110101XXX	32	5A8000h–5AFFFFh
	SA189	10110110XXX	32	5B0000h–5B7FFFh
	SA190	10110111XXX	32	5B8000h–5BFFFFh
	SA191	10111000XXX	32	5C0000h–5C7FFFh
	SA192	10111001XXX	32	5C8000h–5CFFFFh
	SA193	10111010XXX	32	5D0000h–5D7FFFh
	SA194	10111011XXX	32	5D8000h–5DFFFFh
	SA195	10111100XXX	32	5E0000h–5E7FFFh
	SA196	10111101XXX	32	5E8000h–5EFFFFh
	SA197	10111110XXX	32	5F0000h–5F7FFFh
	SA198	10111111XXX	32	5F8000h–5FFFFFh

Table 4. PLl27J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-Al2)	Sector Size (Kwords)	Address Range (xl6)
Bank C	SA199	11000000XXX	32	600000h–607FFFh
	SA200	11000001XXX	32	608000h–60FFFFh
	SA201	11000010XXX	32	610000h–617FFFh
	SA202	11000011XXX	32	618000h–61FFFFh
	SA203	11000100XXX	32	620000h–627FFFh
	SA204	11000101XXX	32	628000h–62FFFFh
	SA205	11000110XXX	32	630000h–637FFFh
	SA206	11000111XXX	32	638000h–63FFFFh
	SA207	11001000XXX	32	640000h–647FFFh
	SA208	11001001XXX	32	648000h–64FFFFh
	SA209	11001010XXX	32	650000h–657FFFh
	SA210	11001011XXX	32	658000h–65FFFFh
	SA211	11001100XXX	32	660000h–667FFFh
	SA212	11001101XXX	32	668000h–66FFFFh
	SA213	11001110XXX	32	670000h–677FFFh
	SA214	11001111XXX	32	678000h–67FFFFh
	SA215	11010000XXX	32	680000h–687FFFh
	SA216	11010001XXX	32	688000h–68FFFFh
	SA217	11010010XXX	32	690000h–697FFFh
	SA218	11010011XXX	32	698000h–69FFFFh
	SA219	11010100XXX	32	6A0000h–6A7FFFh
	SA220	11010101XXX	32	6A8000h–6AFFFFh
	SA221	11010110XXX	32	6B0000h–6B7FFFh
	SA222	11010111XXX	32	6B8000h–6BFFFFh
	SA223	11011000XXX	32	6C0000h–6C7FFFh
	SA224	11011001XXX	32	6C8000h–6CFFFFh
	SA225	11011010XXX	32	6D0000h–6D7FFFh
	SA226	11011011XXX	32	6D8000h–6DFFFFh
	SA227	11011100XXX	32	6E0000h–6E7FFFh
	SA228	11011101XXX	32	6E8000h–6EFFFFh
	SA229	11011110XXX	32	6F0000h–6F7FFFh
	SA230	11011111XXX	32	6F8000h–6FFFFFh

Table 5. SecSiTM Sector Addresses

	Sector Size	Address Range
Factory-Locked Area	64 words	000000h-00003Fh
Customer-Lockable Area	64 words	000040h-00007Fh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device

to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be set as shown in Table 6. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 3). Table 6 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 13. *Note that if a Bank Address (BA) (on address bits PL127J: A22–A20, PL064J: A21–A19, PL032J: A20–*A18*) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 13. This method does not require V_{ID}. Refer to the Autoselect Command Sequence for more information.

Table 6. Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	Amax to A12	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: Spansion products		L	L	H	BA	X	V_{ID}	X	L	L	X	L	L	L	L	0001h
Device ID	Read Cycle 1	L	L	H	BA	X	V_{ID}	X	L	L	L	L	L	L	H	227Eh
	Read Cycle 2	L										H	H	H	L	2220h (PL127J) 2202h (PL064J) 220Ah (PL032J)
	Read Cycle 3	L										H	H	H	H	2200h (PL127J) 2201h (PL064J) 2201h (PL032J)
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0001h (protected), 0000h (unprotected)
SecSi Indicator Bit (DQ7, DQ6)		L	L	H	BA	X	V_{ID}	X	X	L	X	L	L	H	H	00C4h (factory and customer locked), 0084h (factory locked), 0004h (not locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care.*

Note: *The autoselect codes may also be accessed in-system via command sequences*

Table 7. PL127J Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A22-A12	Sector/ Sector Block Size
SA0	00000000000	4 Kwords
SA1	00000000001	4 Kwords
SA2	00000000010	4 Kwords
SA3	00000000011	4 Kwords
SA4	00000000100	4 Kwords
SA5	00000000101	4 Kwords
SA6	00000000110	4 Kwords
SA7	00000000111	4 Kwords
SA8	00000001XXX	32 Kwords
SA9	00000010XXX	32 Kwords
SA10	00000011XXX	32 Kwords
SA11-SA14	000001XXXXX	128 (4x32) Kwords
SA15-SA18	000010XXXXX	128 (4x32) Kwords
SA19-SA22	000011XXXXX	128 (4x32) Kwords
SA23-SA26	000100XXXXX	128 (4x32) Kwords
SA27-SA30	000101XXXXX	128 (4x32) Kwords
SA31-SA34	000110XXXXX	128 (4x32) Kwords
SA35-SA38	000111XXXXX	128 (4x32) Kwords
SA39-SA42	001000XXXXX	128 (4x32) Kwords
SA43-SA46	001001XXXXX	128 (4x32) Kwords
SA47-SA50	001010XXXXX	128 (4x32) Kwords
SA51-SA54	001011XXXXX	128 (4x32) Kwords
SA55-SA58	001100XXXXX	128 (4x32) Kwords
SA59-SA62	001101XXXXX	128 (4x32) Kwords
SA63-SA66	001110XXXXX	128 (4x32) Kwords
SA67-SA70	001111XXXXX	128 (4x32) Kwords
SA71-SA74	010000XXXXX	128 (4x32) Kwords
SA75-SA78	010001XXXXX	128 (4x32) Kwords
SA79-SA82	010010XXXXX	128 (4x32) Kwords
SA83-SA86	010011XXXXX	128 (4x32) Kwords
SA87-SA90	010100XXXXX	128 (4x32) Kwords
SA91-SA94	010101XXXXX	128 (4x32) Kwords
SA95-SA98	010110XXXXX	128 (4x32) Kwords
SA99-SA102	010111XXXXX	128 (4x32) Kwords
SA103-SA106	011000XXXXX	128 (4x32) Kwords
SA107-SA110	011001XXXXX	128 (4x32) Kwords
SA111-SA114	011010XXXXX	128 (4x32) Kwords
SA115-SA118	011011XXXXX	128 (4x32) Kwords
SA119-SA122	011100XXXXX	128 (4x32) Kwords
SA123-SA126	011101XXXXX	128 (4x32) Kwords
SA127-SA130	011110XXXXX	128 (4x32) Kwords
SA131-SA134	011111XXXXX	128 (4x32) Kwords
SA135-SA138	100000XXXXX	128 (4x32) Kwords
SA139-SA142	100001XXXXX	128 (4x32) Kwords
SA143-SA146	100010XXXXX	128 (4x32) Kwords
SA147-SA150	100011XXXXX	128 (4x32) Kwords
SA151-SA154	100100XXXXX	128 (4x32) Kwords
SA155-SA158	100101XXXXX	128 (4x32) Kwords
SA159-SA162	100110XXXXX	128 (4x32) Kwords
SA163-SA166	100111XXXXX	128 (4x32) Kwords
SA167-SA170	101000XXXXX	128 (4x32) Kwords
SA171-SA174	101001XXXXX	128 (4x32) Kwords
SA175-SA178	101010XXXXX	128 (4x32) Kwords
SA179-SA182	101011XXXXX	128 (4x32) Kwords
SA183-SA186	101100XXXXX	128 (4x32) Kwords
SA187-SA190	101101XXXXX	128 (4x32) Kwords
SA191-SA194	101110XXXXX	128 (4x32) Kwords
SA195-SA198	101111XXXXX	128 (4x32) Kwords
SA199-SA202	110000XXXXX	128 (4x32) Kwords
SA203-SA206	110001XXXXX	128 (4x32) Kwords
SA207-SA210	110010XXXXX	128 (4x32) Kwords
SA211-SA214	110011XXXXX	128 (4x32) Kwords
SA215-SA218	110100XXXXX	128 (4x32) Kwords
SA219-SA222	110101XXXXX	128 (4x32) Kwords
SA223-SA226	110110XXXXX	128 (4x32) Kwords
SA227-SA230	110111XXXXX	128 (4x32) Kwords
SA231-SA234	111000XXXXX	128 (4x32) Kwords
SA235-SA238	111001XXXXX	128 (4x32) Kwords
SA239-SA242	111010XXXXX	128 (4x32) Kwords
SA243-SA246	111011XXXXX	128 (4x32) Kwords
SA247-SA250	111100XXXXX	128 (4x32) Kwords
SA251-SA254	111101XXXXX	128 (4x32) Kwords
SA255-SA258	111110XXXXX	128 (4x32) Kwords
SA259	11111100XXX	32 Kwords
SA260	11111101XXX	32 Kwords
SA261	11111110XXX	32 Kwords
SA262	11111111000	4 Kwords
SA263	11111111001	4 Kwords
SA264	11111111010	4 Kwords
SA265	11111111011	4 Kwords

Selecting a Sector Protection Mode

The device is shipped with all sectors unprotected. Optional Spansion programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See the SecSiTM Sector Addresses for details.

Table 8. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	1	Unprotected—PPB not changeable, DYB is changeable
0	1	0	Protected—PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected—PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

Sector Protection

The PL127J, PL064J, and PL032J features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups.

Sector Protection Schemes

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors SA1-133, SA1-134, SA2-0 and SA2-1.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the Persistent Sector Protection method is desired, programming the Persistent Sector Protection Mode Locking Bit permanently sets the device to the Persistent Sector Protection mode. If the Password Sector Protection method is desired, programming the Password Mode Locking Bit permanently sets the device to the Password Sector Protection mode. It is not possible to switch between the two protection modes once a locking bit has been set. One of the two modes must be selected when the device is first programmed. This prevents a program or virus from later setting the Password

Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. Optional Spansion programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

Persistent Sector Protection

The Persistent Sector Protection method replaces the 12 V controlled protection method in previous flash devices. This new method provides three different sector protection states:

- Persistently Locked—The sector is protected and cannot be changed.
- Dynamically Locked—The sector is protected and can be changed by a simple command.
- Unlocked—The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of "bits" are used:

- Persistent Protection Bit
- Persistent Protection Bit Lock
- Persistent Sector Protection Mode Locking Bit

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing sector PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected.

By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors SA1-133, SA1-134, SA2-0 and SA2-1. When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

For customers who are concerned about malicious viruses there is another level of security - the persistently locked state. To persistently protect a given sector or sector group, the PPBs associated with that sector need to be set to "1". Once all PPBs are programmed to the desired settings, the PPB Lock should be set to "1". Setting the PPB Lock automatically disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock "freezes" the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = VIL.

Table 8 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock.

If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device. There is an alternative means of reading the protection status. Take RESET# to VIL and hold WE# at VIH.(The high voltage A9 Autoselect Mode also works for reading the status of the PPBs). Scanning the addresses (A18–A11) while (A6, A1, A0) = (0, 1, 0) will produce a logical '1" code at device output DQ0 for a protected sector or a "0" for an unprotected sector. In this mode, the other addresses are don't cares. Address location with A1 = VIL are reserved for autoselect manufacturer and device codes.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the locked state, rather than cleared to the unlocked state.

The only means to clear the PPB Lock bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.

Disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Verify Command"). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the upper two and lower two sectors without using V_{ID}. This function is provided by the WP# pin and overrides the previously discussed High Voltage Sector Protection method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts the upper two and lower two sectors to whether they were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in the High Voltage Sector Protection.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1" when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (V_{ID}) to be placed on the RESET# pin. Refer to Figure 1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

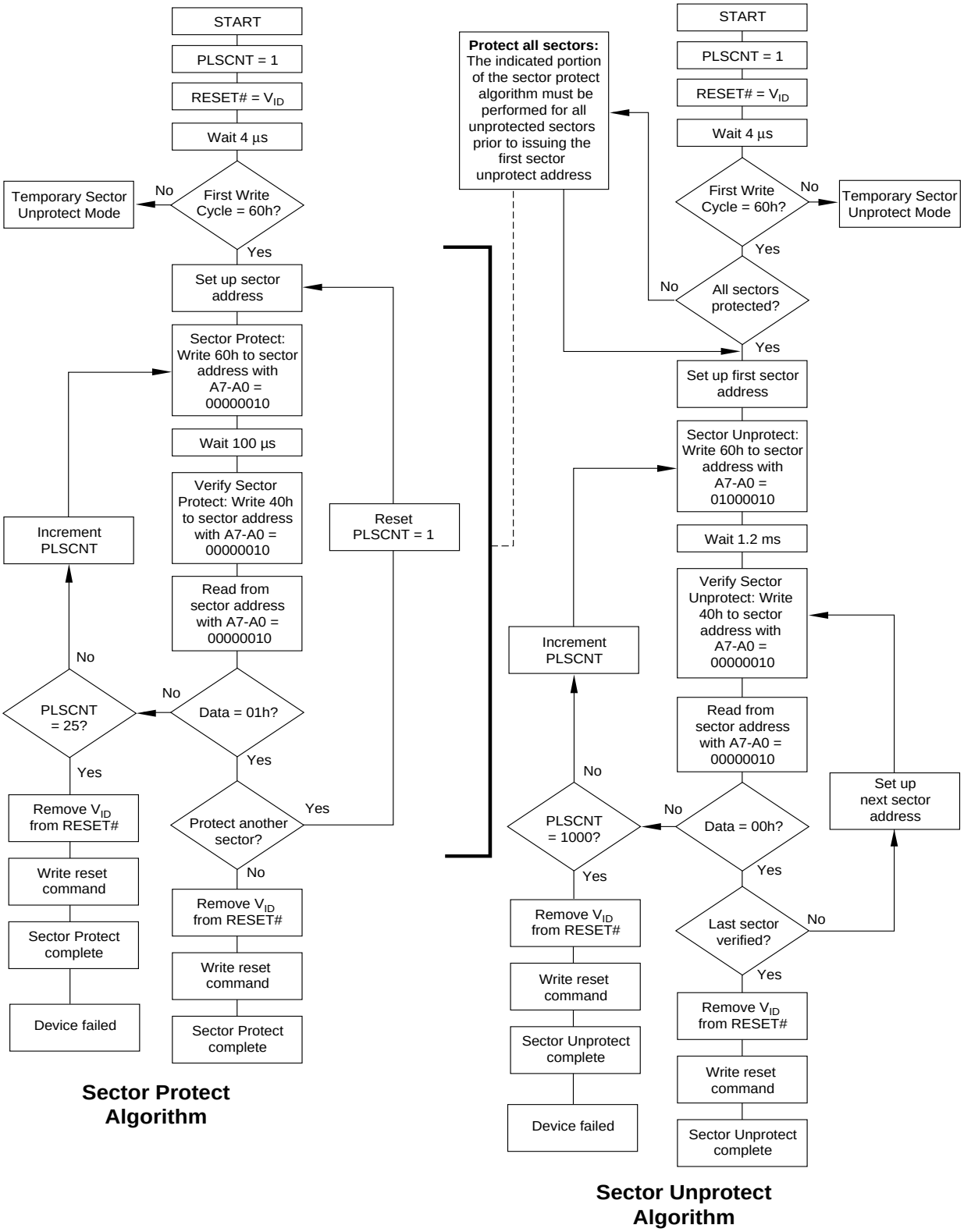
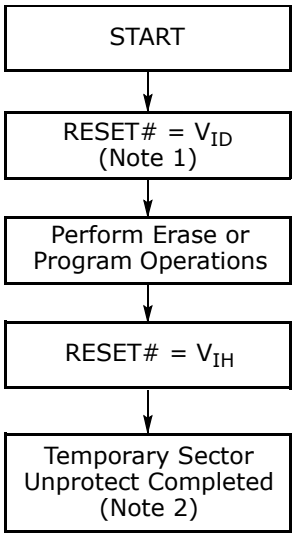


Figure I. In-System Sector Protection/Sector Unprotection Algorithms

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. 2 shows the algorithm, and 21 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.



Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, upper two and lower two sectors will remain protected).*
2. *All previously protected sectors are protected once again*

Figure 2. Temporary Sector Unprotect Operation

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN) The 128-word SecSi sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The SecSi sector is located at addresses 000000h-00007Fh in both Persistent Protection mode and Password Protection mode. It uses indicator bits (DQ6, DQ7) to indicate the factory-locked and customer-locked status of the part.

The system accesses the SecSi Sector through a command sequence (see the Enter SecSi™ Sector/Exit SecSi Sector Command Sequence). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Factory-Locked Area (64 words)

The factory-locked area of the SecSi Sector (000000h-00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The

SecSi Sector Factory-locked Indicator Bit (DQ7) is permanently set to a "1". Optional Spansion programming services can program the factory-locked area with a random ESN, a customer-defined code, or any combination of the two. Because only Spansion can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact your local sales office for details on using Spansion's programming services. Note that the ACC function and unlock bypass modes are not available when the SecSi sector is enabled.

Customer-Lockable Area (64 words)

The customer-lockable area of the SecSi Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The SecSi Sector Customer-locked Indicator Bit (DQ6) is shipped as "0" and can be permanently locked to "1" by issuing the SecSi Protection Bit Program Command. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The Customer-lockable SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 1, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

SecSi Sector Protection Bits

The SecSi Sector Protection Bits prevent programming of the SecSi Sector memory area. Once set, the SecSi Sector memory area contents are non-modifiable.

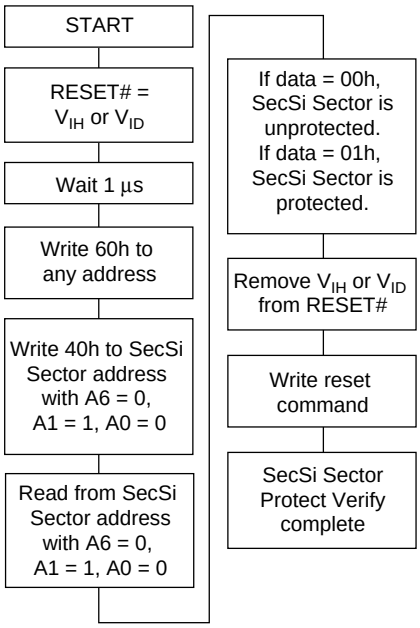


Figure 3. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 3 ns (typical) on OE#, CE#, or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 9–12. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 9–12. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact your local sales office for copies of these documents.

Table 9. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses	Data	Description
27h	0018h (PL127J) 0017h (PL064J) 0016h (PL032J)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h	00FDh (PL127J) 007Dh (PL064J) 003Dh (PL032J)	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
32h 33h 34h	0000h 0000h 0001h	
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 12. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	TBD	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h (PLxxxJ)	Sector Protect/Unprotect scheme 07 = Advanced Sector Protection
4Ah	00E7h (PL127J) 0077h (PL064J) 003Fh (PL032J)	Simultaneous Operation 00 = Not Supported, X = Number of Sectors excluding Bank 1
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0002h (PLxxxJ)	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 01h = Both top and bottom boot with write protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0027h (PL127J) 0017h (PL064J) 000Fh (PL032J)	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0060h (PL127J) 0030h (PL064J) 0018h (PL032J)	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0060h (PL127J) 0030h (PL064J) 0018h (PL032J)	Bank 3 Region Information X = Number of Sectors in Bank 3

Table 12. Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
5Bh	0027h (PL127J) 0017h (PL064J) 000Fh (PL032J)	Bank 4 Region Information X = Number of Sectors in Bank 4

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 13 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristic section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The AC Characteristic table provides the read parameters, and Figure 12 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 13 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 3 shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 13 shows the address and data requirements for both command sequences. See also "SecSi™ (Secured Silicon) Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 13 shows the address and data requirements for the program command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program

operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. Note that the SecSi Sector, autoselect and CFI functions are unavailable when the SecSi Sector is enabled.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

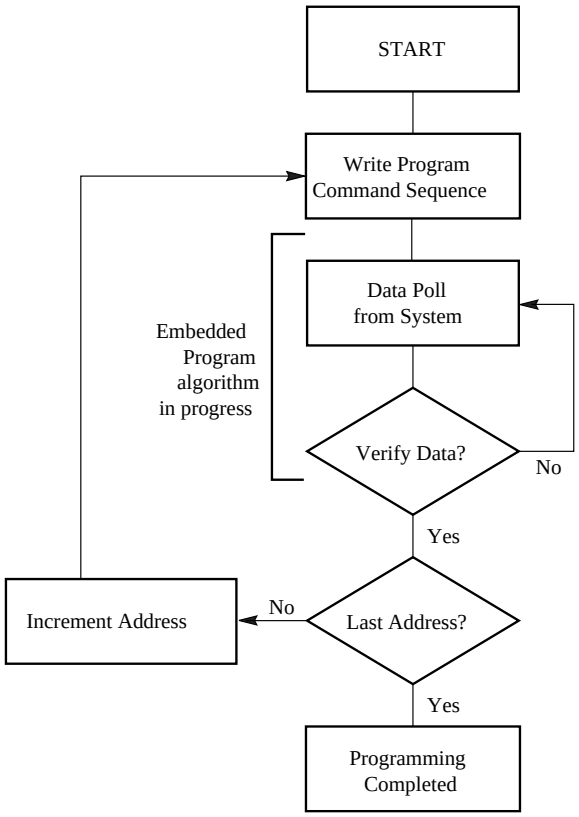
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 13 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 14)

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

4 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 14 for timing diagrams.



Note: *See Table 13 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 13 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.* However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

5 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 13 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

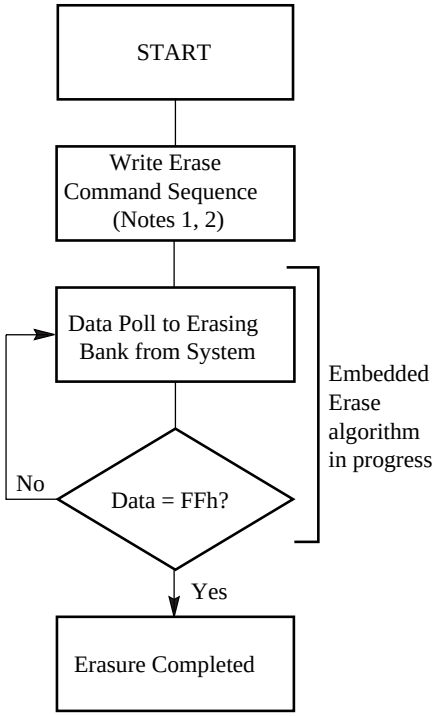
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands. *Note that SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

5 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.



Notes:
1. *See Table 13 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 5. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program

operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to the SecSiTM Sector Addresses and the Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don't care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin. μμ*After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.*

After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin. The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

Command Definitions Tables

Table 13. Memory Array Command Definitions

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	01				
	Device ID (Note 10)	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	227E	(BA) X0E	(Note 10)	(BA) X0F	(Note 10)
	SecSi Sector Factory Protect (Note 8)	4	555	AA	2AA	55	(BA) 555	90	X03	(Note 8)				
	Sector Group Protect Verify (Note 9)	4	555	AAA	2AA	55	(BA) 555	90	(SA) X02	XX00/ XX01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 11)		1	BA	B0										
Program/Erase Resume (Note 12)		1	BA	30										

Table 13. Memory Array Command Definitions

Command (Notes)	Cycles	Bus Cycles (Notes 1–4)											
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
CFI Query (Note 13)	1	55	98										
Accelerated Program (Note 15)	2	XX	A0	PA	PD								
Unlock Bypass Entry (Note 15)	3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 15)	2	XX	A0	PA	PD								
Unlock Bypass Erase (Note 15)	2	XX	80	XX	10								
Unlock Bypass CFI (Notes 13, 15)	1	XX	98										
Unlock Bypass Reset (Note 15)	2	XXX	90	XXX	00								

Legend:

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by PL127J: Amax:A20, PL064J: Amax:A19, PL032J: Amax:A18.

PA = Program Address (Amax:A0). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (Amax:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (Amax:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).*
7. *Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence section for more information.*
8. *The data is C4h for factory and customer locked, 84h for factory locked and 04h for not locked.*
9. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
10. *Device ID must be read across cycles 4, 5, and 6. PL127J (X0Eh = 2220h, X0Fh = 2200h),PL064J (X0Eh = 2202h, X0Fh = 2201h), PL032J (X0Eh = 220Ah, X0Fh = 2201h).*
11. *System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.*
12. *Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.*
13. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
14. *WP#/ACC must be at V_{ID} during the entire operation of command.*
15. *Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.*

Table 14. Sector Protection Command Definitions

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)													
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0												
SecSi Sector Entry	3	555	AA	2AA	55	555	88								
SecSi Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
SecSi Protection Bit Program (Notes 5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD(0)		
SecSi Protection Bit Status	5	555	AA	2AA	55	555	60	OW	48	OW	RD(0)				
Password Program (Notes 5, 7, 8)	4	555	AA	2AA	55	555	38	XX[0-3]	PD[0-3]						
Password Verify (Notes 6, 8, 9)	4	555	AA	2AA	55	555	C8	PWA[0-3]	PWD[0-3]						
Password Unlock (Notes 7, 10, 11)	7	555	AA	2AA	55	555	28	PWA[0]	PWD[0]	PWA[1]	PWD[1]	PWA[2]	PWD[2]	PWA[3]	PWD[3]
PPB Program (Notes 5, 6, 12)	6	555	AA	2AA	55	555	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)		

Table 14. Sector Protection Command Definitions

PPB Status	4	555	AA	2AA	55	555	90	(SA)WP	RD(0)						
All PPB Erase (Notes 5, 6, 13, 14)	6	555	AA	2AA	55	555	60	WP	60	(SA)	40	(SA)WP	RD(0)		
PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
PPB Lock Bit Status (Note 15)	4	555	AA	2AA	55	555	58	SA	RD(1)						
DYB Write (Note 7)	4	555	AA	2AA	55	555	48	SA	X1						
DYB Erase (Note 7)	4	555	AA	2AA	55	555	48	SA	X0						
DYB Status (Note 6)	4	555	AA	2AA	55	555	58	SA	RD(0)						
PPMLB Program (Notes 5, 6, 12)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD(0)		
PPMLB Status (Note 5)	5	555	AA	2AA	55	555	60	PL	48	PL	RD(0)				
SPMLB Program (Notes 5, 6, 12)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD(0)		
SPMLB Status (Note 5)	5	555	AA	2AA	55	555	60	SL	48	SL	RD(0)				

Legend:

DYB = Dynamic Protection Bit
OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
PWA = Password Address. A1:A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A7:A0) is (00001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
SA = Sector Address where security command applies. Address bits Amax:A12 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns device to reading array.*
6. *Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *Entire command sequence must be entered for each portion of password.*
9. *Command sequence returns FFh if PPMLB is set.*
10. *The password is written over four consecutive cycles, at addresses 0-3.*
11. *A 2 µs timeout is required between any two portions of password.*
12. *A 100 µs timeout is required between cycles 4 and 5.*
13. *A 1.2 ms timeout is required between cycles 4 and 5.*
14. *Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.*
15. *DQ1 = 1 if PPB locked, 0 if unlocked.*

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 15 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

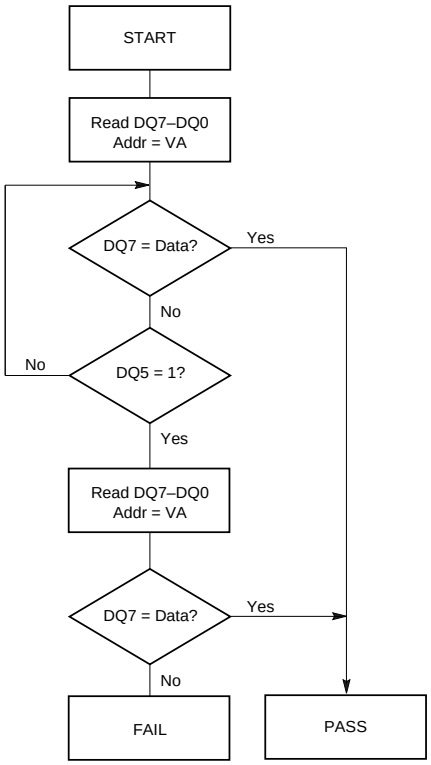
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 400 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles.

Table 15 shows the outputs for Data# Polling on DQ7. 6 shows the Data# Polling algorithm. 18 in the AC Characteristic section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 6. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 15 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

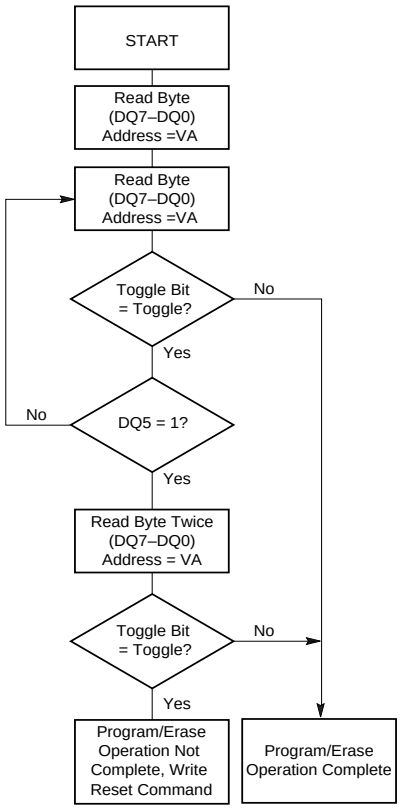
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 15 shows the outputs for Toggle Bit I on DQ6. Figure 7 shows the toggle bit algorithm. Figure 19 in "Read Operation Timings" shows the toggle bit timing diagrams. Figure 20 shows the differences between DQ2 and DQ6 in graphical form. See also the DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the DQ6: Toggle Bit I and DQ2: Toggle Bit II for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 15 to compare outputs for DQ2 and DQ6.

Figure 7 shows the toggle bit algorithm in flowchart form, and the DQ2: Toggle Bit II explains the algorithm. See also the DQ6: Toggle Bit I. Figure 19 shows the toggle bit timing diagram. Figure 20 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and

store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 7).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." See also the Sector Erase Command Sequence.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 15 shows the status of DQ3 relative to the other status bits.

Table 15. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

Absolute Maximum Ratings

Storage Temperature Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1). . . . . –0.5 V to +4.0 V

RESET# (Note 2) . . . . . –0.5 V to +13.0 V

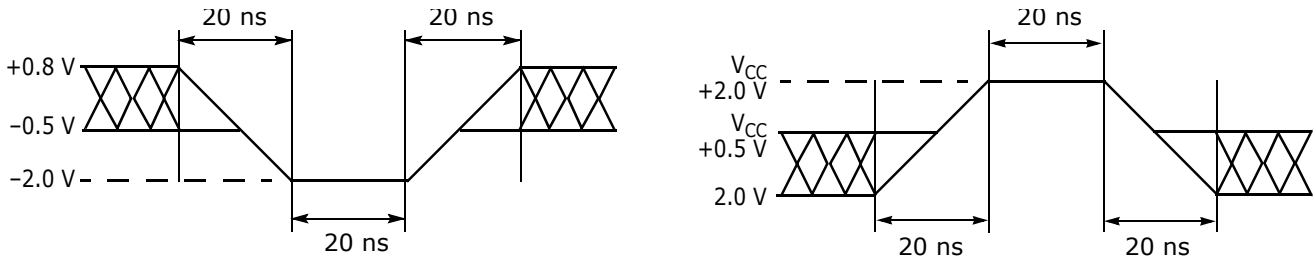
WP#/ACC (Note 2) . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC input voltage on pin A9, OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*



Maximum Negative Overshoot Waveform

Maximum Positive Overshoot Waveform

Figure 8. Maximum Overshoot Waveforms

Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Wireless Devices

Ambient Temperature (T_A) . . . . . –25°C to +85°C

Supply Voltages

V_{CC} . . . . . .2.7–3.1 V

V_{IO} (see Note) . .1.65–1.95 V (for PL127J) or 2.7–3.1 V (for all PLxxxJ devices)

Notes:

For all AC and DC specifications, V_{IO} = V_{CC}; contact your local sales office for other V_{IO} options.

DC Characteristics

Table 16. CMOS Compatible

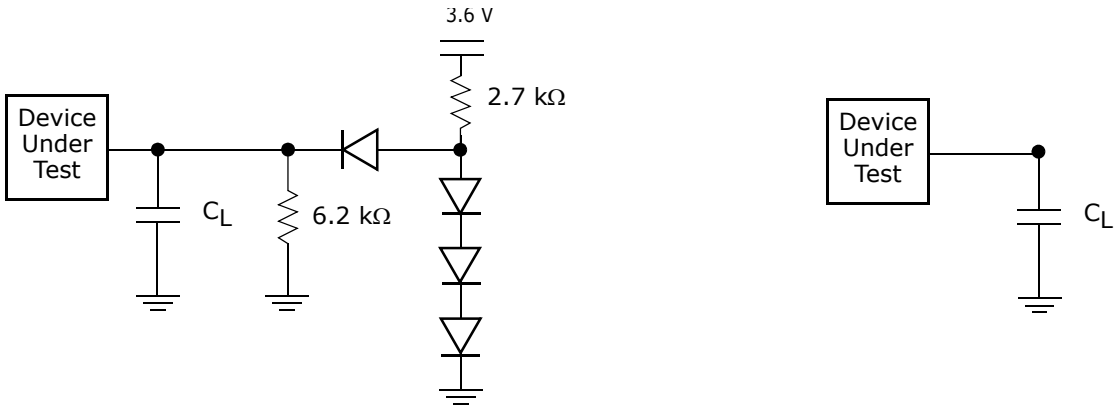
Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, OE#, RESET# Input Load Current	V_{CC} = $V_{CC\ max}$; V_{ID}= 12.5 V				35	µA
I_{LR}	Reset Leakage Current	V_{CC} = $V_{CC\ max}$; V_{ID}= 12.5 V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, OE# = V_{IH} V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	OE# = V_{IH}, V_{CC} = $V_{CC\ max}$ (Note 1)	5 MHz		15	25	mA
			10 MHz		45	55	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3)	OE# = V_{IH}, WE# = V_{IL}			15	25	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET#, WP#/ACC = V_{IO} ± 0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	V_{IH} = V_{IO} ± 0.3 V; V_{IL} = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC6}	V_{CC} Active Read-While-Program Current (Notes 1, 2)	OE# = V_{IH},	5 MHz		21	45	mA
			10 MHz		46	70	
I_{CC7}	V_{CC} Active Read-While-Erase Current (Notes 1, 2)	OE# = V_{IH},	5 MHz		21	45	mA
			10 MHz		46	70	
I_{CC8}	V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	OE# = V_{IH}			17	25	mA
I_{CC9}	V_{CC} Active Page Read Current (Note 2)	OE# = V_{IH}, 8 word Page Read			10	15	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.65–1.95 V (PL127J)		–0.4		0.4	V
		V_{IO} = 2.7–3.6 V		–0.5		0.8	V
V_{IH}	Input High Voltage	V_{IO} = 1.65–1.95 V (PL127J)		V_{IO}–0.4		V_{IO}+0.4	V
		V_{IO} = 2.7–3.6 V		2.0		V_{CC}+0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CC} = $V_{CC\ min}$, V_{IO} = 1.65–1.95 V (PL127J)				0.1	V
		I_{OL} = 2.0 mA, V_{CC} = $V_{CC\ min}$, V_{IO} = 2.7–3.6 V				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = $V_{CC\ min}$, V_{IO} = 1.65–1.95 V (PL127J)		V_{IO}–0.1			V
		I_{OH} = –2.0 mA, V_{CC} = $V_{CC\ min}$, V_{IO} = 2.7–3.6 V		2.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 5 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CCmax}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 1 mA.*
5. *Not 100% tested.*
6. *Valid CE1#/CE2# conditions: (CE1# = V_{IL}, CE2# = V_{IH},) or (CE1# = V_{IH}, CE2# = V_{IL}) or (CE1# = V_{IH}, CE2# = V_{IH})*

AC Characteristic

Test Conditions



V_{IO} = 3.0 V **V_{IO} = 1.8 V (PL127J)**

Note: *Diodes are IN3064 or equivalent*

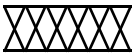
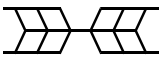
Figure 9. Test Setups

Table 17. Test Specifications

Test Condition		All Speeds	Unit
Output Load		1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)		30	pF
Input Rise and Fall Times	V_{IO} = 1.8 V (PL127J)	5	ns
	V_{IO} = 3.0 V		
Input Pulse Levels	V_{IO} = 1.8 V (PL127J)	0.0 - 1.8	V
	V_{IO} = 3.0 V	0.0–3.0	
Input timing measurement reference levels		$V_{IO}/2$	V
Output timing measurement reference levels		$V_{IO}/2$	V

SWITCHING WAVEFORMS

Table 18. KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

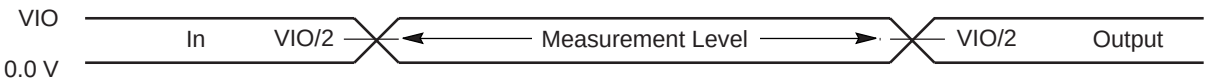


Figure 10. Input Waveforms and Measurement Levels

VCC RampRate

All DC characteristics are specified for a V_{CC} ramp rate > 1V/100 µs and V_{CC} >=V_{CCQ} - 100 mV. If the V_{CC} ramp rate is < 1V/100 µs, a hardware reset required.+

Read Operations

Table 19. Read-Only Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					55	60	65	70	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	55	60	65	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	55	60	65	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	55	60	65	70	ns
	t_{PACC}	Page Access Time			Max	20	25	30		ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	20	25	30		ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 3)			Max	16				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	16				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 3)			Min	5				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns

Notes:

1. *Not 100% tested.*
2. *See Figure 9 and Table 17 for test specifications*
3. *Measurements performed by placing a 50 ohm termination on the data pin with a bias of V_{CC} /2. The time from OE# high to the data bus driven to V_{CC} /2 is taken as t_{DF}.*
4. *For 70pF Output Load Capacitance, 2 ns will be added to the above t_{ACC},t_{CE},t_{PACC},t_{OE} values for all speed grades*

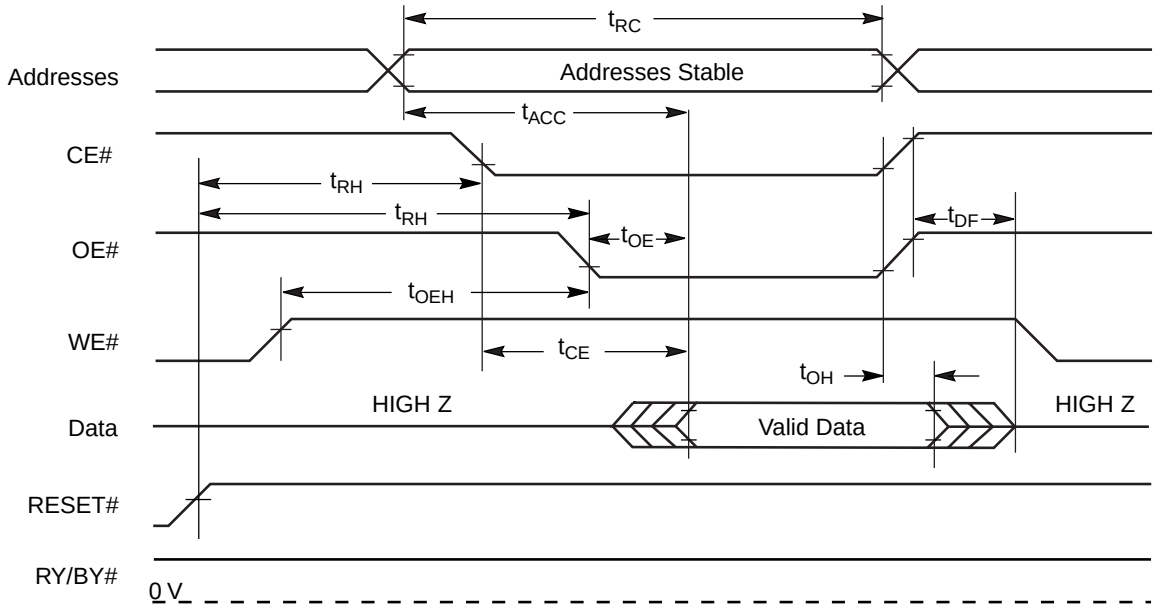


Figure 11. Read Operation Timings

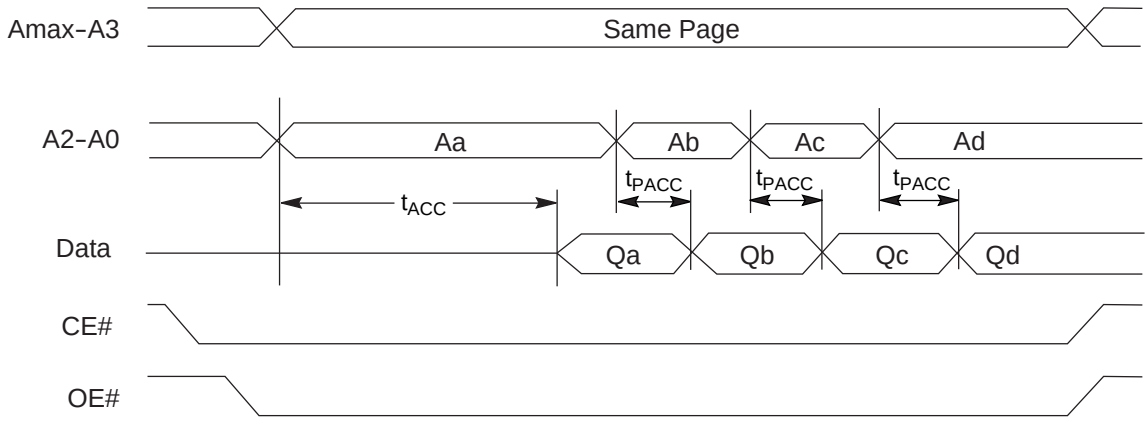


Figure 12. Page Read Operation Timings

Reset

Table 20. Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

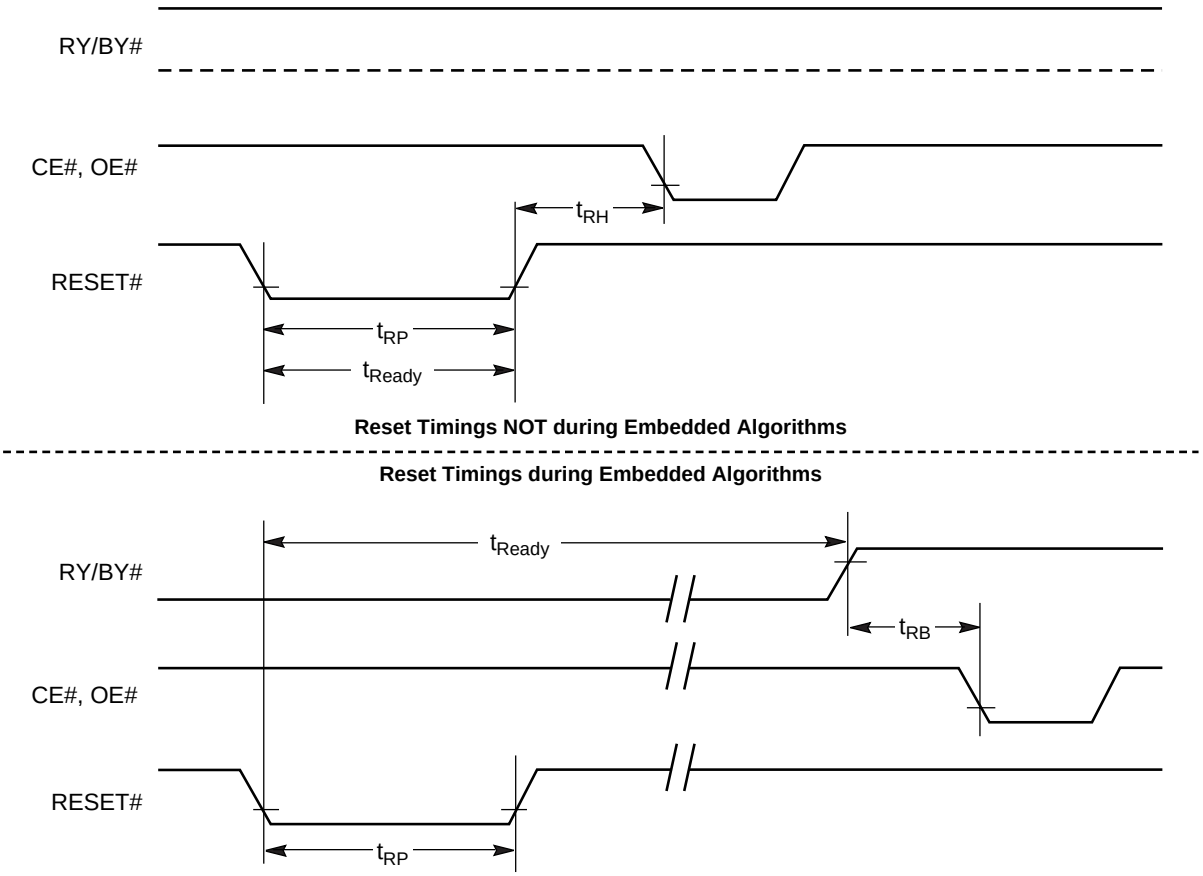


Figure 13. Reset Timings

Erase/Program Operations

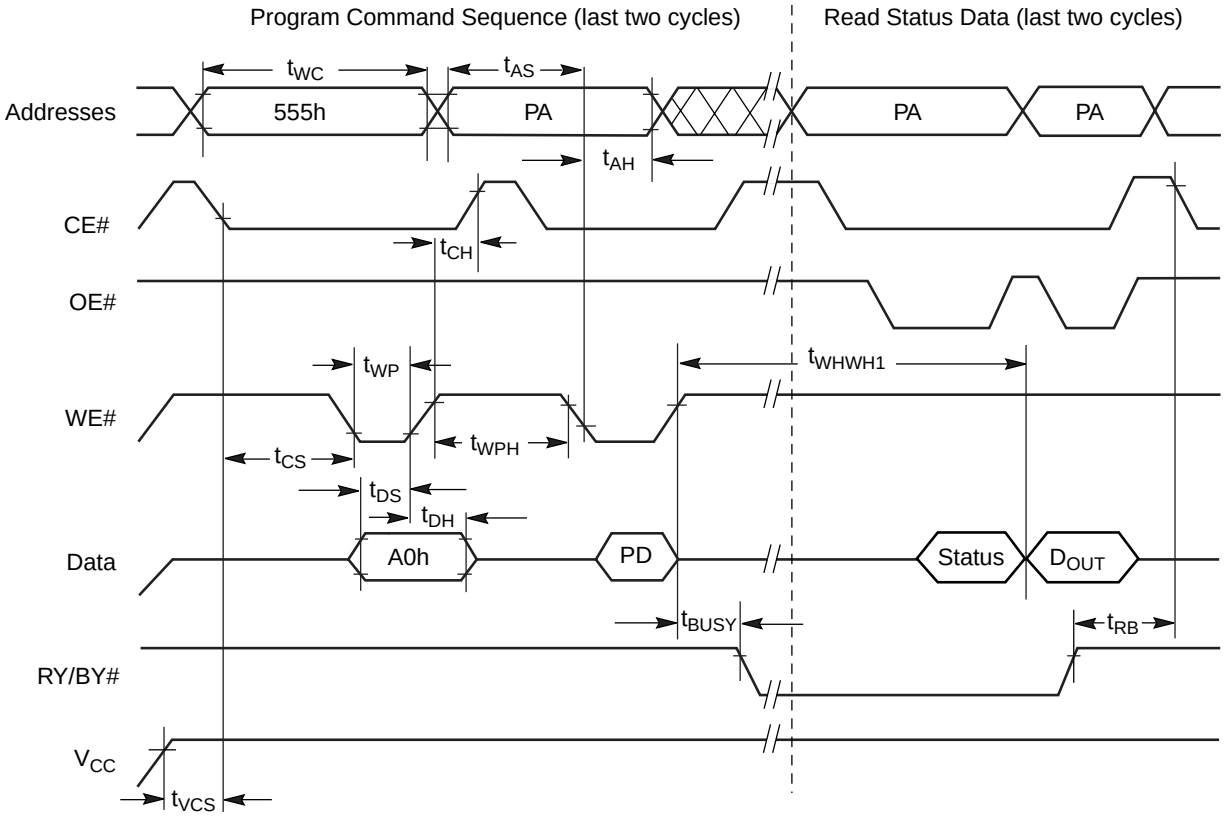
Table 21. Erase and Program Operations

Parameter				Speed Options				
JEDEC	Std	Description		55	60	65	70	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	60	65	70	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	30	35			ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	25	30			ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	10				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	40			ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	20	25			ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6				µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50				µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Max	90				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

Timing Diagrams



Notes:

1. PA = program address, PD = program data, D_{OUT} is the true data at the program address

Figure 14. Program Operation Timings

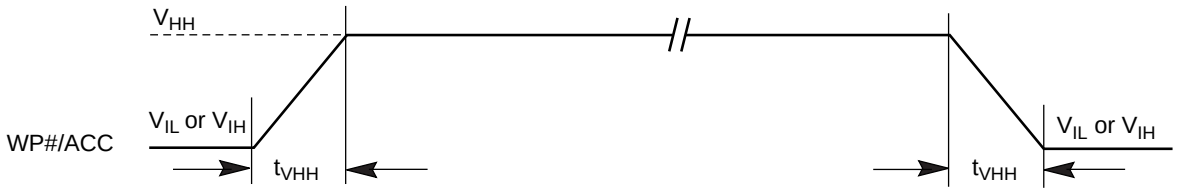
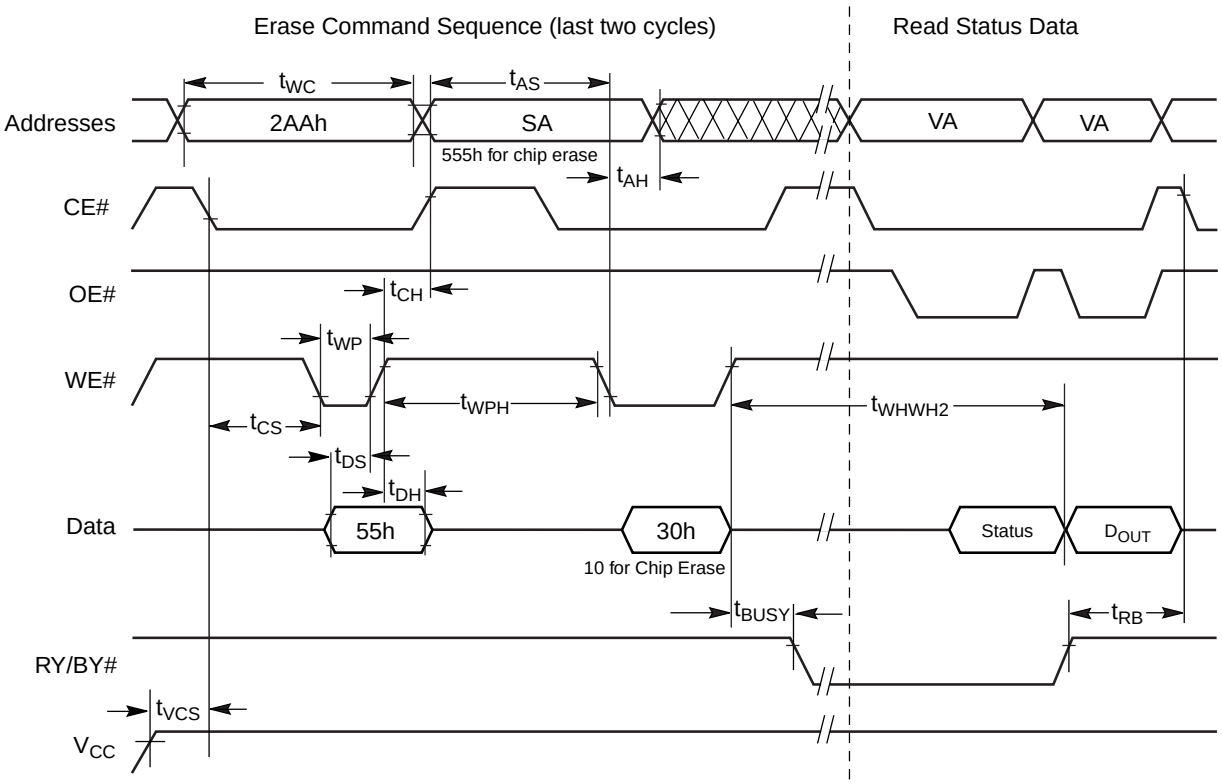


Figure 15. Accelerated Program Timing Diagram



Notes:

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status"

Figure 16. Chip/Sector Erase Operation Timings

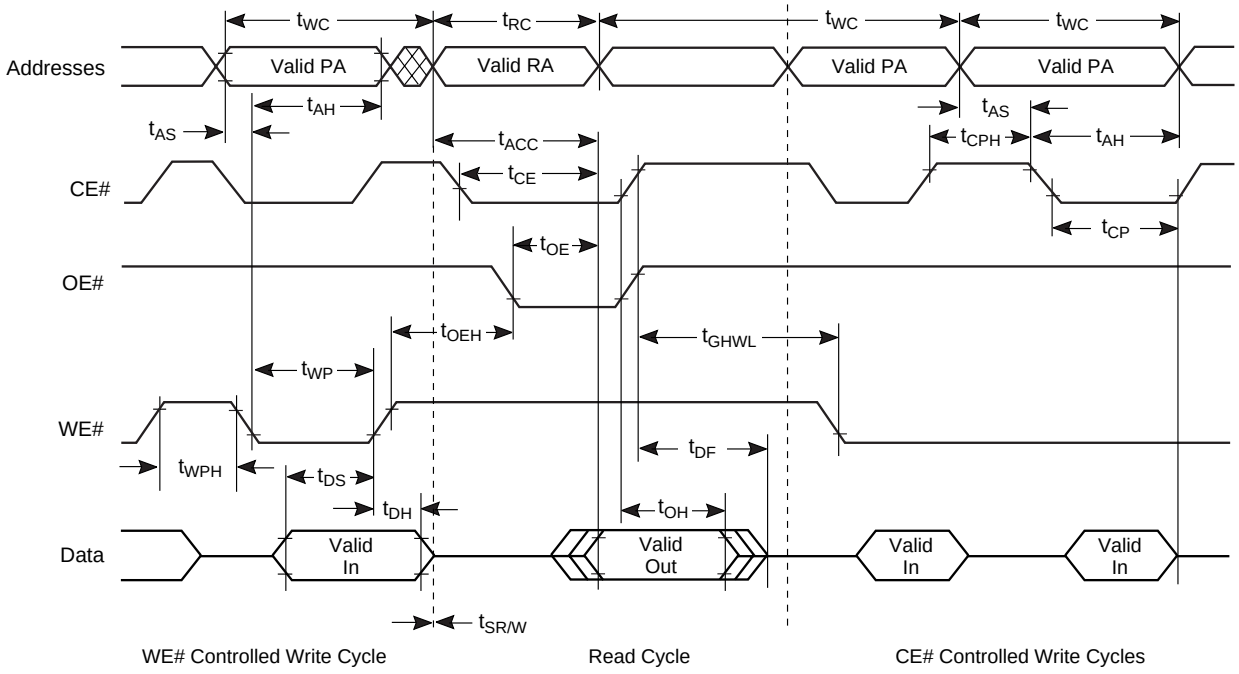
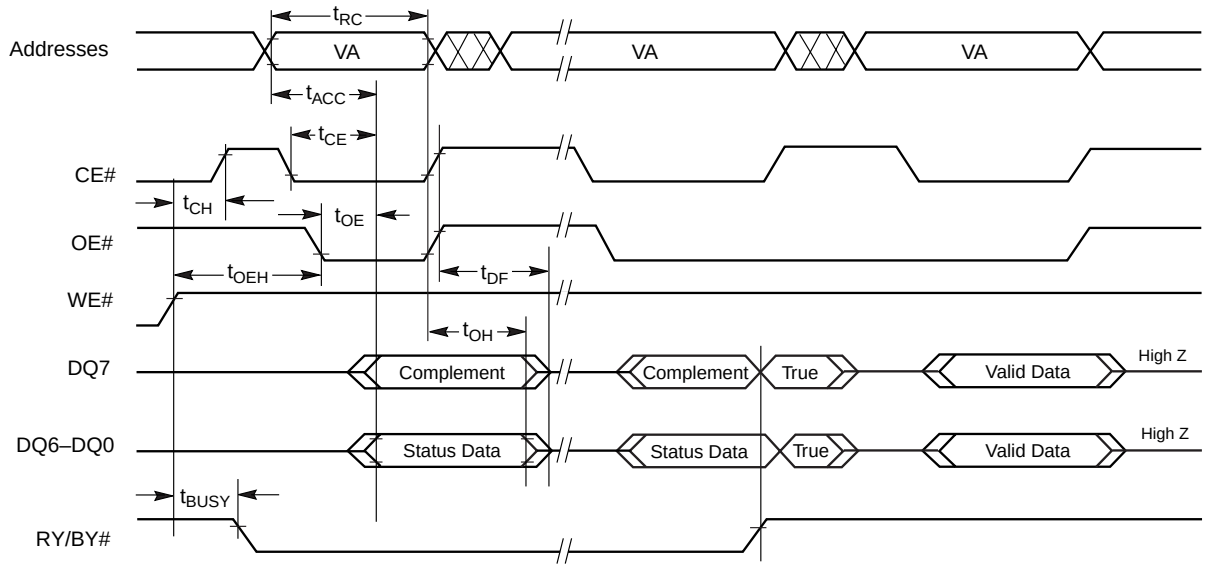
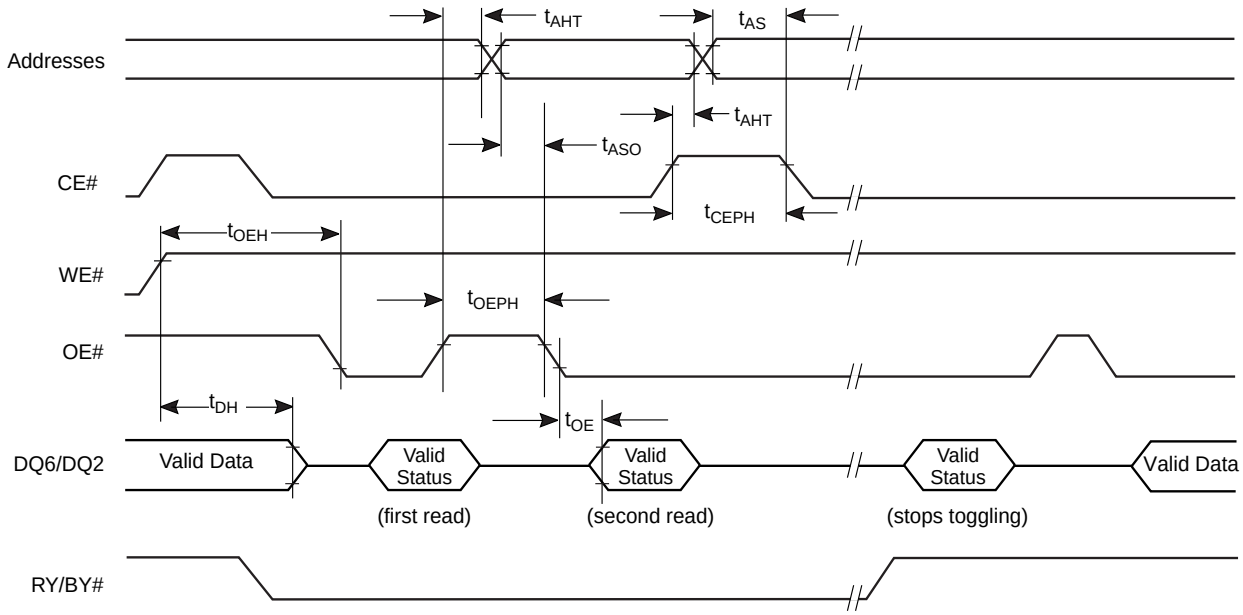


Figure 17. Back-to-back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle*

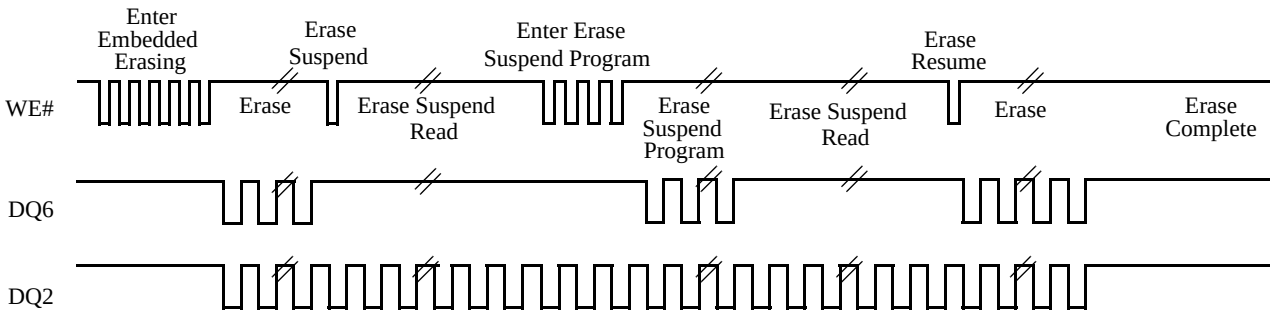
Figure 18. Data# Polling Timings (During Embedded Algorithms)



Notes:

1. *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 19. Toggle Bit Timings (During Embedded Algorithms)



Note: *Note: DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 20. DQ2 vs. DQ6

Protect/Unprotect

Table 22. Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

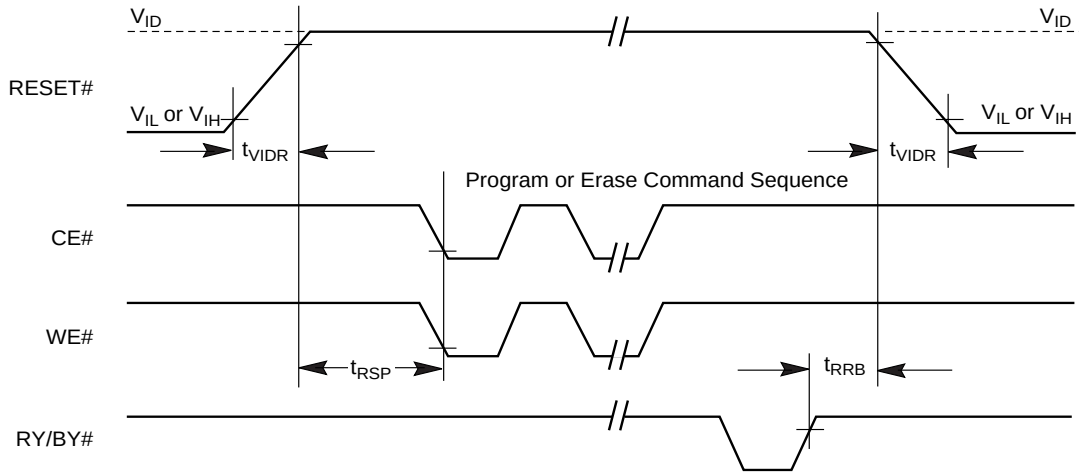
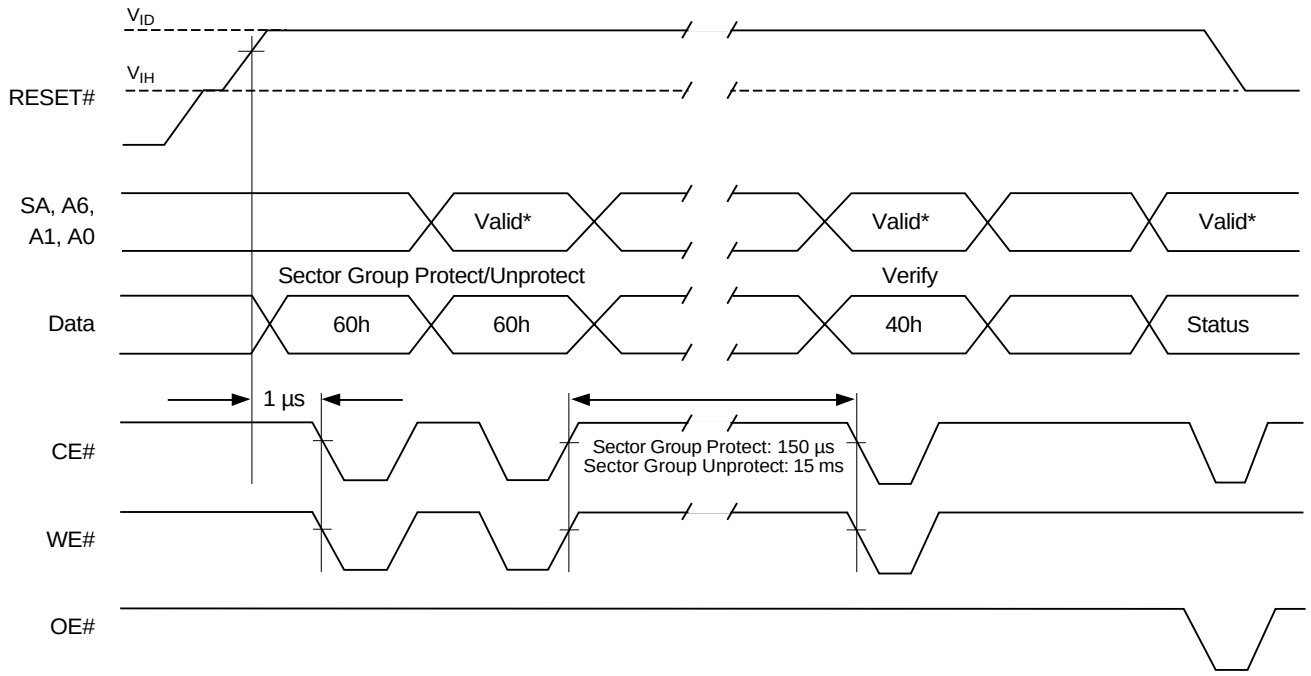


Figure 21. Temporary Sector Unprotect Timing Diagram



Notes:

1. For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

Figure 22. Sector/Sector Block Protect and Unprotect Timing Diagram

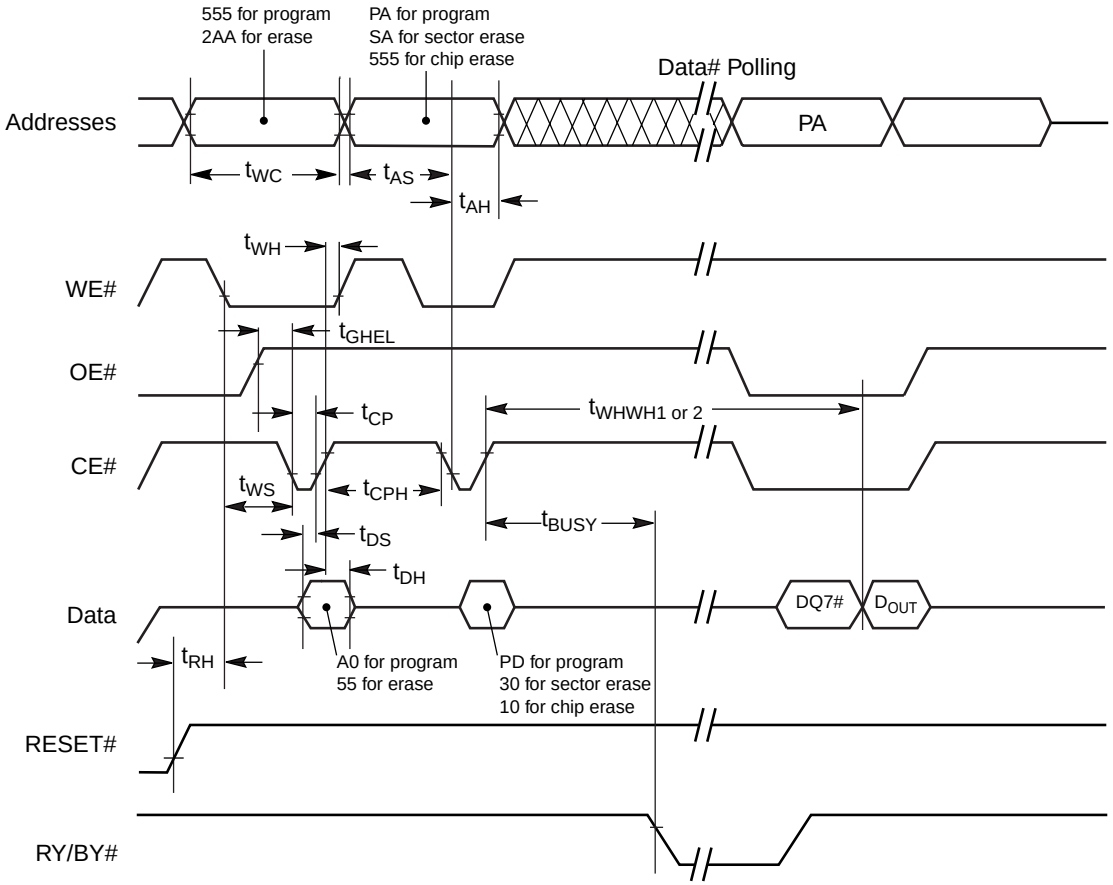
Controlled Erase Operations

Table 23. Alternate CE# Controlled Erase and Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			55	60	65	70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	60	65	70	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	30	35			ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	25	30			ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	40			ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	20	25			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	6				µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 2)	Typ	4				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device*

Table 24. Alternate CE# Controlled Write (Erase/Program) Operation Timings

Table 25. Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	2	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	PL127J	135	216	sec	
	PL064J	71	113.6	sec	
	PL032J	39	62.4	sec	
Word Program Time		6	100	µs	Excludes system level overhead (Note 5)
Accelerated Word Program Time		4	60	µs	
Chip Program Time (Note 3)	PL127J	50.4	200	sec	
	PL064J	25.2	50.4	sec	
	PL032J	12.6	25.2	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25×C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern. All values are subject to change.*
2. *Under worst case conditions of 90×C, V_{CC} = 2.7 V, 100,000 cycles. All values are subject to change.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 13 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

BGA Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6.3	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	7.0	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	5.5	8	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	11	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

S29GLxxxN MirrorBit™ Flash Family

S29GL512N, S29GL256N, S29GL128N
512 Megabit, 256 Megabit, and 128 Megabit, 3.0 Volt-only Page Mode Flash Memory featuring 110 nm MirrorBit process technology

Data Sheet

ADVANCE INFORMATION

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **Enhanced VersatileI/O™ control**
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- **Manufactured on 110 nm MirrorBit process technology**
- **Secured Silicon Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - S29GL512N: Five hundred twelve 64 Kword (128 Kbyte) sectors
  - S29GL256N: Two hundred fifty-six 64 Kword (128 Kbyte) sectors
  - S29GL128N: One hundred twenty-eight 64 Kword (128 Kbyte) sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **100,000 erase cycles per sector typical**
- **20-year data retention typical**

Performance Characteristics

- **High performance**
  - 90 ns access time (S29GL128N, S29GL256N, S29GL512N)
  - 8-word/16-byte page read buffer
  - 25 ns page read times
  - 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 25 mA typical active read current;
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current

Software & Hardware Features

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Advanced Sector Protection
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

Publication Number S29GLxxxN_MCP **Revision** A **Amendment** 1 **Issue Date** December 15, 2004

This document contains information on a product under development at Spansion LLC. The information is intended to help you evaluate this product. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice.

General Description

The S29GL512/256/128N family of devices are 3.0V single power flash memory manufactured using 110 nm MirrorBit technology. The S29GL512N is a 512 Mbit, organized as 33,554,432 words or 67,108,864 bytes. The S29GL256N is a 256 Mbit, organized as 16,777,216 words or 33,554,432 bytes. The S29GL128N is a 128 Mbit, organized as 8,388,608 words or 16,777,216 bytes. The device can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 90 ns (S29GL128N, S29GL256N, S29GL512N) are available. Note that each access time has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in the "Product Selector Guide" section. The devices are offered in a 56-pin TSOP or 64-ball Fortified BGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (**WP#/**ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The devices are entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

The **Enhanced VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on all input levels (address, chip control, and DQ input levels) to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in a 1.8 V or 3 V system environment as required.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. **Persistent Sector Protection** provides in-system, command-enabled protection of any combination of sectors using a single power supply at V_{CC}. **Password Sector Protection** prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be

tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

The **Write Protect (WP#/ACC)** feature protects the first or last sector by asserting a logic low on the WP# pin.

MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

Product Selector Guide

S29GL5I2N

Part Number			S29GL512N			
Speed Option	V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V		**10**	**11**	
		V_{IO} = 1.65–1.95 V				**11**
	V_{CC} = 3.0-3.6V	V_{IO} = 3.0-3.6V	**90**			
Max. Access Time (ns)			90	100	110	110
Max. CE# Access Time (ns)			90	100	110	110
Max. Page access time (ns)			25	25	25	30
Max. OE# Access Time (ns)			25	25	25	30

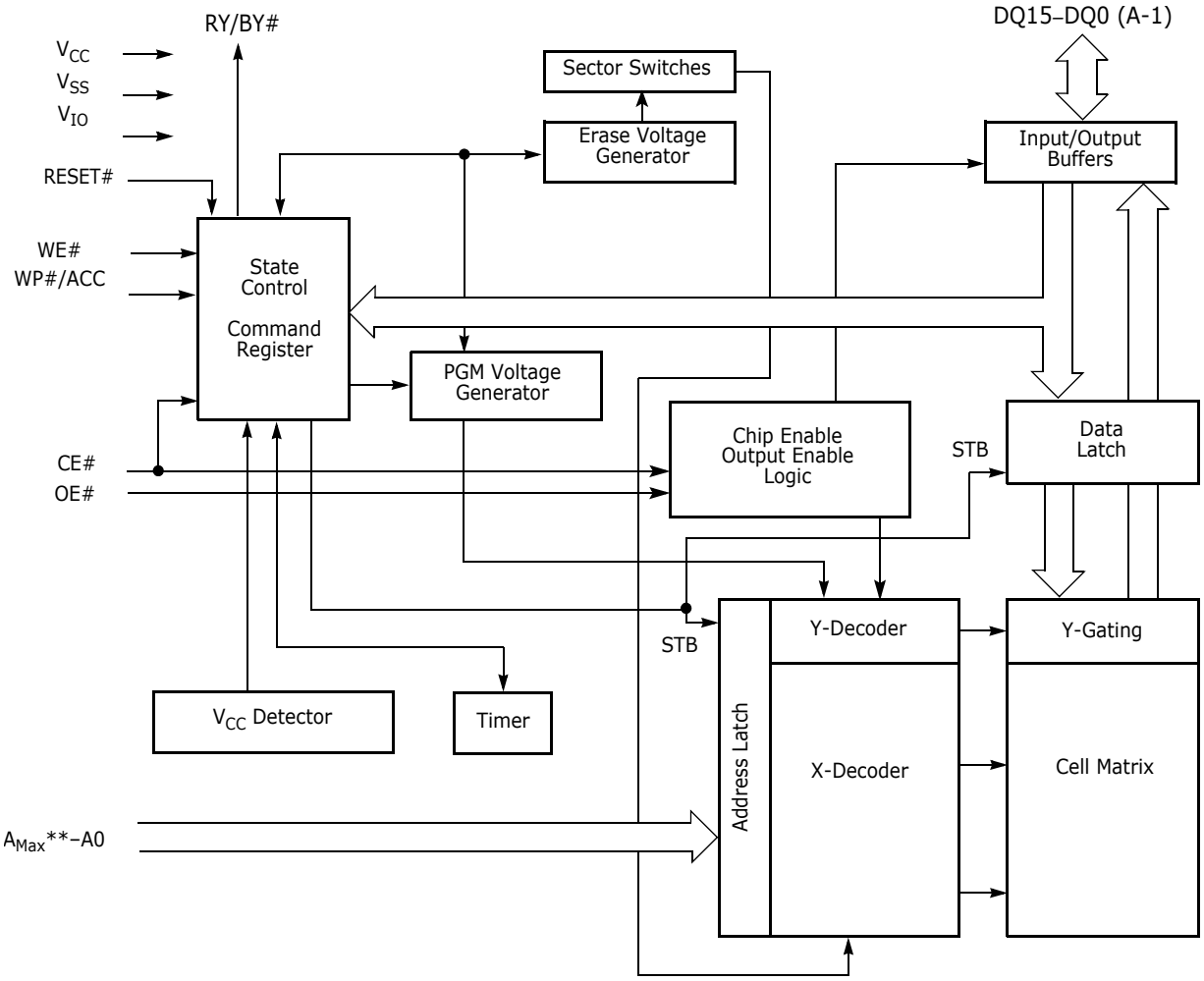
S29GL256N

Part Number		S29GL256N				
Speed Option	V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V		**10**	**11**	
		V_{IO} = 1.65–1.95 V				**11**
	V_{CC} = Regulated (3.0-3.6V)	V_{IO} = Regulated (3.0-3.6V)	**90**			
Max. Access Time (ns)			90	100	110	110
Max. CE# Access Time (ns)			90	100	110	110
Max. Page access time (ns)			25	25	25	30
Max. OE# Access Time (ns)			25	25	25	30

S29GLI28N

Part Number		S29GL128N				
Speed Option	V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V		**10**	**11**	
		V_{IO} = 1.65–1.95 V				**11**
	V_{CC} = Regulated (3.0-3.6V)	V_{IO} = Regulated (3.0-3.6V)	**90**			
Max. Access Time (ns)			90	100	110	110
Max. CE# Access Time (ns)			90	100	110	110
Max. Page access time (ns)			25	25	25	30
Max. OE# Access Time (ns)			25	25	25	30

Block Diagram



Notes:

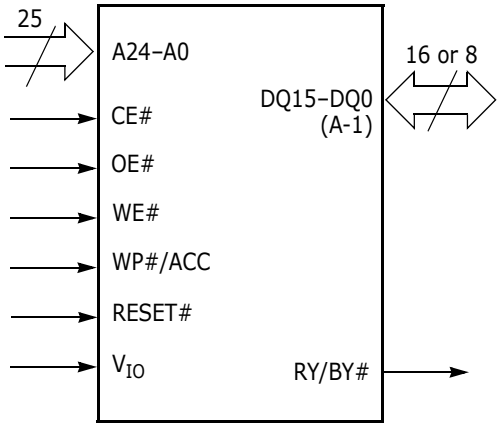
1. A_{Max} GL512N = A24, A_{Max} GL256N = A23, A_{Max} GL128N = A22

Pin Description

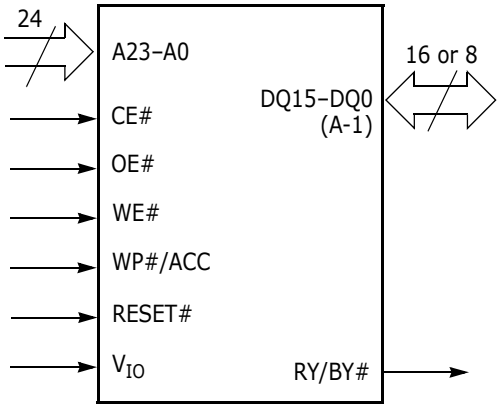
A24–A0	=	25 Address inputs (512 Mb)
A23–A0	=	24 Address inputs (256 Mb)
A22–A0	=	23 Address inputs (128 Mb)
DQ14–DQ0	=	15 Data inputs/outputs
DQ15/A-1	=	DQ15 (Data input/output, word mode), A-1 (LSB Address input
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
WP#/ACC	=	Hardware Write Protect input; Acceleration input
RESET#	=	Hardware Reset Pin input
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	=	Output Buffer power
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

Logic Symbol

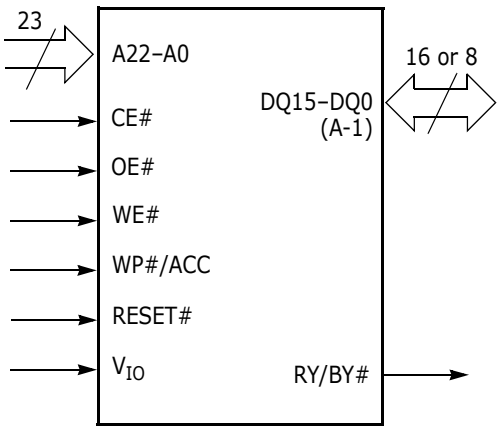
S29GL512N



S29GL256N



S29GL128N



Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ ACC	Addresses (Note 1)	DQ0–DQ15
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write (Program/Erase)	L	H	L	H	Note 2	A_{IN}	(Note 3)
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	H	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are AMax:A0 in word mode. Sector addresses are A_{Max}:A16 in both modes.*
2. *If WP# = V_{IL}, the first or last sector group remains protected. If WP# = V_{IH}, the first or last sector will be protected or unprotected as determined by the method described in "Write Protect (WP#)". All sectors are unprotected when shipped from the factory (The Secured Silicon Sector may be factory protected depending on version ordered.)*
3. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2, Figure 4, and Figure 5).*

VersatileIO™ (V_{IO}) Control

The **VersatileIO**™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on CE# and DQ I/Os to the same voltage level that is asserted on V_{IO}. See Ordering Information for V_{IO} options on this device.

For example, a $V_{I/O}$ of 1.65 V to 3.6 V allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8-V or 3-V devices on the same data bus.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory

content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" on page 127 for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 11 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A(max)–A3. Address bits A2–A0 determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is de-asserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2, Table 4, and Table 5 indicate the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See "Write Buffer" for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sector groups, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" section on page 113 and "Autoselect Command Sequence" section on page 127 sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{IO} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{IO} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the "DC Characteristics" section on page 151 for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the "DC Characteristics" section on page 151 for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC5}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 13 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table–S29GL5I2N

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	0	0	128/64	0000000–000FFFF
SA1	0	0	0	0	0	0	0	0	1	128/64	0010000–001FFFF
SA2	0	0	0	0	0	0	0	1	0	128/64	0020000–002FFFF
SA3	0	0	0	0	0	0	0	1	1	128/64	0030000–003FFFF
SA4	0	0	0	0	0	0	1	0	0	128/64	0040000–004FFFF
SA5	0	0	0	0	0	0	1	0	1	128/64	0050000–005FFFF
SA6	0	0	0	0	0	0	1	1	0	128/64	0060000–006FFFF
SA7	0	0	0	0	0	0	1	1	1	128/64	0070000–007FFFF
SA8	0	0	0	0	0	1	0	0	0	128/64	0080000–008FFFF
SA9	0	0	0	0	0	1	0	0	1	128/64	0090000–009FFFF
SA10	0	0	0	0	0	1	0	1	0	128/64	00A0000–00AFFFF
SA11	0	0	0	0	0	1	0	1	1	128/64	00B0000–00BFFFF
SA12	0	0	0	0	0	1	1	0	0	128/64	00C0000–00CFFFF
SA13	0	0	0	0	0	1	1	0	1	128/64	00D0000–00DFFFF
SA14	0	0	0	0	0	1	1	1	0	128/64	00E0000–00EFFFF
SA15	0	0	0	0	0	1	1	1	1	128/64	00F0000–00FFFFF
SA16	0	0	0	0	1	0	0	0	0	128/64	0100000–010FFFF
SA17	0	0	0	0	1	0	0	0	1	128/64	0110000–011FFFF
SA18	0	0	0	0	1	0	0	1	0	128/64	0120000–012FFFF
SA19	0	0	0	0	1	0	0	1	1	128/64	0130000–013FFFF
SA20	0	0	0	0	1	0	1	0	0	128/64	0140000–014FFFF
SA21	0	0	0	0	1	0	1	0	1	128/64	0150000–015FFFF
SA22	0	0	0	0	1	0	1	1	0	128/64	0160000–016FFFF
SA23	0	0	0	0	1	0	1	1	1	128/64	0170000–017FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA24	0	0	0	0	1	1	0	0	0	128/64	0180000–018FFFF
SA25	0	0	0	0	1	1	0	0	1	128/64	0190000–019FFFF
SA26	0	0	0	0	1	1	0	1	0	128/64	01A0000–01AFFFF
SA27	0	0	0	0	1	1	0	1	1	128/64	01B0000–01BFFFF
SA28	0	0	0	0	1	1	1	0	0	128/64	01C0000–01CFFFF
SA29	0	0	0	0	1	1	1	0	1	128/64	01D0000–01DFFFF
SA30	0	0	0	0	1	1	1	1	0	128/64	01E0000–01EFFFF
SA31	0	0	0	0	1	1	1	1	1	128/64	01F0000–01FFFFF
SA32	0	0	0	1	0	0	0	0	0	128/64	0200000–020FFFF
SA33	0	0	0	1	0	0	0	0	1	128/64	0210000–021FFFF
SA34	0	0	0	1	0	0	0	1	0	128/64	0220000–022FFFF
SA35	0	0	0	1	0	0	0	1	1	128/64	0230000–023FFFF
SA36	0	0	0	1	0	0	1	0	0	128/64	0240000–024FFFF
SA37	0	0	0	1	0	0	1	0	1	128/64	0250000–025FFFF
SA38	0	0	0	1	0	0	1	1	0	128/64	0260000–026FFFF
SA39	0	0	0	1	0	0	1	1	1	128/64	0270000–027FFFF
SA40	0	0	0	1	0	1	0	0	0	128/64	0280000–028FFFF
SA41	0	0	0	1	0	1	0	0	1	128/64	0290000–029FFFF
SA42	0	0	0	1	0	1	0	1	0	128/64	02A0000–02AFFFF
SA43	0	0	0	1	0	1	0	1	1	128/64	02B0000–02BFFFF
SA44	0	0	0	1	0	1	1	0	0	128/64	02C0000–02CFFFF
SA45	0	0	0	1	0	1	1	0	1	128/64	02D0000–02DFFFF
SA46	0	0	0	1	0	1	1	1	0	128/64	02E0000–02EFFFF
SA47	0	0	0	1	0	1	1	1	1	128/64	02F0000–02FFFFF
SA48	0	0	0	1	1	0	0	0	0	128/64	0300000–030FFFF
SA49	0	0	0	1	1	0	0	0	1	128/64	0310000–031FFFF
SA50	0	0	0	1	1	0	0	1	0	128/64	0320000–032FFFF
SA51	0	0	0	1	1	0	0	1	1	128/64	0330000–033FFFF
SA52	0	0	0	1	1	0	1	0	0	128/64	0340000–034FFFF
SA53	0	0	0	1	1	0	1	0	1	128/64	0350000–035FFFF
SA54	0	0	0	1	1	0	1	1	0	128/64	0360000–036FFFF
SA55	0	0	0	1	1	0	1	1	1	128/64	0370000–037FFFF
SA56	0	0	0	1	1	1	0	0	0	128/64	0380000–038FFFF
SA57	0	0	0	1	1	1	0	0	1	128/64	0390000–039FFFF
SA58	0	0	0	1	1	1	0	1	0	128/64	03A0000–03AFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA59	0	0	0	1	1	1	0	1	1	128/64	03B0000–03BFFFF
SA60	0	0	0	1	1	1	1	0	0	128/64	03C0000–03CFFFF
SA61	0	0	0	1	1	1	1	0	1	128/64	03D0000–03DFFFF
SA62	0	0	0	1	1	1	1	1	0	128/64	03E0000–03EFFFF
SA63	0	0	0	1	1	1	1	1	1	128/64	03F0000–03FFFFF
SA64	0	0	1	0	0	0	0	0	0	128/64	0400000–040FFFF
SA65	0	0	1	0	0	0	0	0	1	128/64	0410000–041FFFF
SA66	0	0	1	0	0	0	0	1	0	128/64	0420000–042FFFF
SA67	0	0	1	0	0	0	0	1	1	128/64	0430000–043FFFF
SA68	0	0	1	0	0	0	1	0	0	128/64	0440000–044FFFF
SA69	0	0	1	0	0	0	1	0	1	128/64	0450000–045FFFF
SA70	0	0	1	0	0	0	1	1	0	128/64	0460000–046FFFF
SA71	0	0	1	0	0	0	1	1	1	128/64	0470000–047FFFF
SA72	0	0	1	0	0	1	0	0	0	128/64	0480000–048FFFF
SA73	0	0	1	0	0	1	0	0	1	128/64	0490000–049FFFF
SA74	0	0	1	0	0	1	0	1	0	128/64	04A0000–04AFFFF
SA75	0	0	1	0	0	1	0	1	1	128/64	04B0000–04BFFFF
SA76	0	0	1	0	0	1	1	0	0	128/64	04C0000–04CFFFF
SA77	0	0	1	0	0	1	1	0	1	128/64	04D0000–04DFFFF
SA78	0	0	1	0	0	1	1	1	0	128/64	04E0000–04EFFFF
SA79	0	0	1	0	0	1	1	1	1	128/64	04F0000–04FFFFF
SA80	0	0	1	0	1	0	0	0	0	128/64	0500000–050FFFF
SA81	0	0	1	0	1	0	0	0	1	128/64	0510000–051FFFF
SA82	0	0	1	0	1	0	0	1	0	128/64	0520000–052FFFF
SA83	0	0	1	0	1	0	0	1	1	128/64	0530000–053FFFF
SA84	0	0	1	0	1	0	1	0	0	128/64	0540000–054FFFF
SA85	0	0	1	0	1	0	1	0	1	128/64	0550000–055FFFF
SA86	0	0	1	0	1	0	1	1	0	128/64	0560000–056FFFF
SA87	0	0	1	0	1	0	1	1	1	128/64	0570000–057FFFF
SA88	0	0	1	0	1	1	0	0	0	128/64	0580000–058FFFF
SA89	0	0	1	0	1	1	0	0	1	128/64	0590000–059FFFF
SA90	0	0	1	0	1	1	0	1	0	128/64	05A0000–05AFFFF
SA91	0	0	1	0	1	1	0	1	1	128/64	05B0000–05BFFFF
SA92	0	0	1	0	1	1	1	0	0	128/64	05C0000–05CFFFF
SA93	0	0	1	0	1	1	1	0	1	128/64	05D0000–05DFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA94	0	0	1	0	1	1	1	1	0	128/64	05E0000–05EFFFF
SA95	0	0	1	0	1	1	1	1	1	128/64	05F0000–05FFFFF
SA96	0	0	1	1	0	0	0	0	0	128/64	0600000–060FFFF
SA97	0	0	1	1	0	0	0	0	1	128/64	0610000–061FFFF
SA98	0	0	1	1	0	0	0	1	0	128/64	0620000–062FFFF
SA99	0	0	1	1	0	0	0	1	1	128/64	0630000–063FFFF
SA100	0	0	1	1	0	0	1	0	0	128/64	0640000–064FFFF
SA101	0	0	1	1	0	0	1	0	1	128/64	0650000–065FFFF
SA102	0	0	1	1	0	0	1	1	0	128/64	0660000–066FFFF
SA103	0	0	1	1	0	0	1	1	1	128/64	0670000–067FFFF
SA104	0	0	1	1	0	1	0	0	0	128/64	0680000–068FFFF
SA105	0	0	1	1	0	1	0	0	1	128/64	0690000–069FFFF
SA106	0	0	1	1	0	1	0	1	0	128/64	06A0000–06AFFFF
SA107	0	0	1	1	0	1	0	1	1	128/64	06B0000–06BFFFF
SA108	0	0	1	1	0	1	1	0	0	128/64	06C0000–06CFFFF
SA109	0	0	1	1	0	1	1	0	1	128/64	06D0000–06DFFFF
SA110	0	0	1	1	0	1	1	1	0	128/64	06E0000–06EFFFF
SA111	0	0	1	1	0	1	1	1	1	128/64	06F0000–06FFFFF
SA112	0	0	1	1	1	0	0	0	0	128/64	0700000–070FFFF
SA113	0	0	1	1	1	0	0	0	1	128/64	0710000–071FFFF
SA114	0	0	1	1	1	0	0	1	0	128/64	0720000–072FFFF
SA115	0	0	1	1	1	0	0	1	1	128/64	0730000–073FFFF
SA116	0	0	1	1	1	0	1	0	0	128/64	0740000–074FFFF
SA117	0	0	1	1	1	0	1	0	1	128/64	0750000–075FFFF
SA118	0	0	1	1	1	0	1	1	0	128/64	0760000–076FFFF
SA119	0	0	1	1	1	0	1	1	1	128/64	0770000–077FFFF
SA120	0	0	1	1	1	1	0	0	0	128/64	0780000–078FFFF
SA121	0	0	1	1	1	1	0	0	1	128/64	0790000–079FFFF
SA122	0	0	1	1	1	1	0	1	0	128/64	07A0000–07AFFFF
SA123	0	0	1	1	1	1	0	1	1	128/64	07B0000–07BFFFF
SA124	0	0	1	1	1	1	1	0	0	128/64	07C0000–07CFFFF
SA125	0	0	1	1	1	1	1	0	1	128/64	07D0000–07DFFFF
SA126	0	0	1	1	1	1	1	1	0	128/64	07E0000–07EFFFF
SA127	0	0	1	1	1	1	1	1	1	128/64	07F0000–07FFFFF
SA128	0	1	0	0	0	0	0	0	0	128/64	0800000–080FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA129	0	1	0	0	0	0	0	0	1	128/64	0810000–081FFFF
SA130	0	1	0	0	0	0	0	1	0	128/64	0820000–082FFFF
SA131	0	1	0	0	0	0	0	1	1	128/64	0830000–083FFFF
SA132	0	1	0	0	0	0	1	0	0	128/64	0840000–084FFFF
SA133	0	1	0	0	0	0	1	0	1	128/64	0850000–085FFFF
SA134	0	1	0	0	0	0	1	1	0	128/64	0860000–086FFFF
SA135	0	1	0	0	0	0	1	1	1	128/64	0870000–087FFFF
SA136	0	1	0	0	0	1	0	0	0	128/64	0880000–088FFFF
SA137	0	1	0	0	0	1	0	0	1	128/64	0890000–089FFFF
SA138	0	1	0	0	0	1	0	1	0	128/64	08A0000–08AFFFF
SA139	0	1	0	0	0	1	0	1	1	128/64	08B0000–08BFFFF
SA140	0	1	0	0	0	1	1	0	0	128/64	08C0000–08CFFFF
SA141	0	1	0	0	0	1	1	0	1	128/64	08D0000–08DFFFF
SA142	0	1	0	0	0	1	1	1	0	128/64	08E0000–08EFFFF
SA143	0	1	0	0	0	1	1	1	1	128/64	08F0000–08FFFFF
SA144	0	1	0	0	1	0	0	0	0	128/64	0900000–090FFFF
SA145	0	1	0	0	1	0	0	0	1	128/64	0910000–091FFFF
SA146	0	1	0	0	1	0	0	1	0	128/64	0920000–092FFFF
SA147	0	1	0	0	1	0	0	1	1	128/64	0930000–093FFFF
SA148	0	1	0	0	1	0	1	0	0	128/64	0940000–094FFFF
SA149	0	1	0	0	1	0	1	0	1	128/64	0950000–095FFFF
SA150	0	1	0	0	1	0	1	1	0	128/64	0960000–096FFFF
SA151	0	1	0	0	1	0	1	1	1	128/64	0970000–097FFFF
SA152	0	1	0	0	1	1	0	0	0	128/64	0980000–098FFFF
SA153	0	1	0	0	1	1	0	0	1	128/64	0990000–099FFFF
SA154	0	1	0	0	1	1	0	1	0	128/64	09A0000–09AFFFF
SA155	0	1	0	0	1	1	0	1	1	128/64	09B0000–09BFFFF
SA156	0	1	0	0	1	1	1	0	0	128/64	09C0000–09CFFFF
SA157	0	1	0	0	1	1	1	0	1	128/64	09D0000–09DFFFF
SA158	0	1	0	0	1	1	1	1	0	128/64	09E0000–09EFFFF
SA159	0	1	0	0	1	1	1	1	1	128/64	09F0000–09FFFFF
SA160	0	1	0	1	0	0	0	0	0	128/64	0A00000–0A0FFFF
SA161	0	1	0	1	0	0	0	0	1	128/64	0A10000–0A1FFFF
SA162	0	1	0	1	0	0	0	1	0	128/64	0A20000–0A2FFFF
SA163	0	1	0	1	0	0	0	1	1	128/64	0A30000–0A3FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA164	0	1	0	1	0	0	1	0	0	128/64	0A40000–0A4FFFF
SA165	0	1	0	1	0	0	1	0	1	128/64	0A50000–0A5FFFF
SA166	0	1	0	1	0	0	1	1	0	128/64	0A60000–0A6FFFF
SA167	0	1	0	1	0	0	1	1	1	128/64	0A70000–0A7FFFF
SA168	0	1	0	1	0	1	0	0	0	128/64	0A80000–0A8FFFF
SA169	0	1	0	1	0	1	0	0	1	128/64	0A90000–0A9FFFF
SA170	0	1	0	1	0	1	0	1	0	128/64	0AA0000–0AAFFFF
SA171	0	1	0	1	0	1	0	1	1	128/64	0AB0000–0ABFFFF
SA172	0	1	0	1	0	1	1	0	0	128/64	0AC0000–0ACFFFF
SA173	0	1	0	1	0	1	1	0	1	128/64	0AD0000–0ADFFFF
SA174	0	1	0	1	0	1	1	1	0	128/64	0AE0000–0AEFFFF
SA175	0	1	0	1	0	1	1	1	1	128/64	0AF0000–0AFFFFF
SA176	0	1	0	1	1	0	0	0	0	128/64	0B00000–0B0FFFF
SA177	0	1	0	1	1	0	0	0	1	128/64	0B10000–0B1FFFF
SA178	0	1	0	1	1	0	0	1	0	128/64	0B20000–0B2FFFF
SA179	0	1	0	1	1	0	0	1	1	128/64	0B30000–0B3FFFF
SA180	0	1	0	1	1	0	1	0	0	128/64	0B40000–0B4FFFF
SA181	0	1	0	1	1	0	1	0	1	128/64	0B50000–0B5FFFF
SA182	0	1	0	1	1	0	1	1	0	128/64	0B60000–0B6FFFF
SA183	0	1	0	1	1	0	1	1	1	128/64	0B70000–0B7FFFF
SA184	0	1	0	1	1	1	0	0	0	128/64	0B80000–0B8FFFF
SA185	0	1	0	1	1	1	0	0	1	128/64	0B90000–0B9FFFF
SA186	0	1	0	1	1	1	0	1	0	128/64	0BA0000–0BAFFFF
SA187	0	1	0	1	1	1	0	1	1	128/64	0BB0000–0BBFFFF
SA188	0	1	0	1	1	1	1	0	0	128/64	0BC0000–0BCFFFF
SA189	0	1	0	1	1	1	1	0	1	128/64	0BD0000–0BDFFFF
SA190	0	1	0	1	1	1	1	1	0	128/64	0BE0000–0BEFFFF
SA191	0	1	0	1	1	1	1	1	1	128/64	0BF0000–0BFFFFF
SA192	0	1	1	0	0	0	0	0	0	128/64	0C00000–0C0FFFF
SA193	0	1	1	0	0	0	0	0	1	128/64	0C10000–0C1FFFF
SA194	0	1	1	0	0	0	0	1	0	128/64	0C20000–0C2FFFF
SA195	0	1	1	0	0	0	0	1	1	128/64	0C30000–0C3FFFF
SA196	0	1	1	0	0	0	1	0	0	128/64	0C40000–0C4FFFF
SA197	0	1	1	0	0	0	1	0	1	128/64	0C50000–0C5FFFF
SA198	0	1	1	0	0	0	1	1	0	128/64	0C60000–0C6FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA199	0	1	1	0	0	0	1	1	1	128/64	0C70000–0C7FFFF
SA200	0	1	1	0	0	1	0	0	0	128/64	0C80000–0C8FFFF
SA201	0	1	1	0	0	1	0	0	1	128/64	0C90000–0C9FFFF
SA202	0	1	1	0	0	1	0	1	0	128/64	0CA0000–0CAFFFF
SA203	0	1	1	0	0	1	0	1	1	128/64	0CB0000–0CBFFFF
SA204	0	1	1	0	0	1	1	0	0	128/64	0CC0000–0CCFFFF
SA205	0	1	1	0	0	1	1	0	1	128/64	0CD0000–0CDFFFF
SA206	0	1	1	0	0	1	1	1	0	128/64	0CE0000–0CEFFFF
SA207	0	1	1	0	0	1	1	1	1	128/64	0CF0000–0CFFFFF
SA208	0	1	1	0	1	0	0	0	0	128/64	0D00000–0D0FFFF
SA209	0	1	1	0	1	0	0	0	1	128/64	0D10000–0D1FFFF
SA210	0	1	1	0	1	0	0	1	0	128/64	0D20000–0D2FFFF
SA211	0	1	1	0	1	0	0	1	1	128/64	0D30000–0D3FFFF
SA212	0	1	1	0	1	0	1	0	0	128/64	0D40000–0D4FFFF
SA213	0	1	1	0	1	0	1	0	1	128/64	0D50000–0D5FFFF
SA214	0	1	1	0	1	0	1	1	0	128/64	0D60000–0D6FFFF
SA215	0	1	1	0	1	0	1	1	1	128/64	0D70000–0D7FFFF
SA216	0	1	1	0	1	1	0	0	0	128/64	0D80000–0D8FFFF
SA217	0	1	1	0	1	1	0	0	1	128/64	0D90000–0D9FFFF
SA218	0	1	1	0	1	1	0	1	0	128/64	0DA0000–0DAFFFF
SA219	0	1	1	0	1	1	0	1	1	128/64	0DB0000–0DBFFFF
SA220	0	1	1	0	1	1	1	0	0	128/64	0DC0000–0DCFFFF
SA221	0	1	1	0	1	1	1	0	1	128/64	0DD0000–0DDFFFF
SA222	0	1	1	0	1	1	1	1	0	128/64	0DE0000–0DEFFFF
SA223	0	1	1	0	1	1	1	1	1	128/64	0DF0000–0DFFFFF
SA224	0	1	1	1	0	0	0	0	0	128/64	0E00000–0E0FFFF
SA225	0	1	1	1	0	0	0	0	1	128/64	0E10000–0E1FFFF
SA226	0	1	1	1	0	0	0	1	0	128/64	0E20000–0E2FFFF
SA227	0	1	1	1	0	0	0	1	1	128/64	0E30000–0E3FFFF
SA228	0	1	1	1	0	0	1	0	0	128/64	0E40000–0E4FFFF
SA229	0	1	1	1	0	0	1	0	1	128/64	0E50000–0E5FFFF
SA230	0	1	1	1	0	0	1	1	0	128/64	0E60000–0E6FFFF
SA231	0	1	1	1	0	0	1	1	1	128/64	0E70000–0E7FFFF
SA232	0	1	1	1	0	1	0	0	0	128/64	0E80000–0E8FFFF
SA233	0	1	1	1	0	1	0	0	1	128/64	0E90000–0E9FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA234	0	1	1	1	0	1	0	1	0	128/64	0EA0000–0EAFFFF
SA235	0	1	1	1	0	1	0	1	1	128/64	0EB0000–0EBFFFF
SA236	0	1	1	1	0	1	1	0	0	128/64	0EC0000–0ECFFFF
SA237	0	1	1	1	0	1	1	0	1	128/64	0ED0000–0EDFFFF
SA238	0	1	1	1	0	1	1	1	0	128/64	0EE0000–0EEFFFF
SA239	0	1	1	1	0	1	1	1	1	128/64	0EF0000–0EFFFFF
SA240	0	1	1	1	1	0	0	0	0	128/64	0F00000–0F0FFFF
SA241	0	1	1	1	1	0	0	0	1	128/64	0F10000–0F1FFFF
SA242	0	1	1	1	1	0	0	1	0	128/64	0F20000–0F2FFFF
SA243	0	1	1	1	1	0	0	1	1	128/64	0F30000–0F3FFFF
SA244	0	1	1	1	1	0	1	0	0	128/64	0F40000–0F4FFFF
SA245	0	1	1	1	1	0	1	0	1	128/64	0F50000–0F5FFFF
SA246	0	1	1	1	1	0	1	1	0	128/64	0F60000–0F6FFFF
SA247	0	1	1	1	1	0	1	1	1	128/64	0F70000–0F7FFFF
SA248	0	1	1	1	1	1	0	0	0	128/64	0F80000–0F8FFFF
SA249	0	1	1	1	1	1	0	0	1	128/64	0F90000–0F9FFFF
SA250	0	1	1	1	1	1	0	1	0	128/64	0FA0000–0FAFFFF
SA251	0	1	1	1	1	1	0	1	1	128/64	0FB0000–0FBFFFF
SA252	0	1	1	1	1	1	1	0	0	128/64	0FC0000–0FCFFFF
SA253	0	1	1	1	1	1	1	0	1	128/64	0FD0000–0FDFFFF
SA254	0	1	1	1	1	1	1	1	0	128/64	0FE0000–0FEFFFF
SA255	0	1	1	1	1	1	1	1	1	128/64	0FF0000–0FFFFFF
SA256	1	0	0	0	0	0	0	0	0	128/64	1000000–100FFFF
SA257	1	0	0	0	0	0	0	0	1	128/64	1010000–101FFFF
SA258	1	0	0	0	0	0	0	1	0	128/64	1020000–102FFFF
SA259	1	0	0	0	0	0	0	1	1	128/64	1030000–103FFFF
SA260	1	0	0	0	0	0	1	0	0	128/64	1040000–104FFFF
SA261	1	0	0	0	0	0	1	0	1	128/64	1050000–105FFFF
SA262	1	0	0	0	0	0	1	1	0	128/64	1060000–106FFFF
SA263	1	0	0	0	0	0	1	1	1	128/64	1070000–107FFFF
SA264	1	0	0	0	0	1	0	0	0	128/64	1080000–108FFFF
SA265	1	0	0	0	0	1	0	0	1	128/64	1090000–109FFFF
SA266	1	0	0	0	0	1	0	1	0	128/64	10A0000–10AFFFF
SA267	1	0	0	0	0	1	0	1	1	128/64	10B0000–10BFFFF
SA268	1	0	0	0	0	1	1	0	0	128/64	10C0000–10CFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA269	1	0	0	0	0	1	1	0	1	128/64	10D0000–10DFFFF
SA270	1	0	0	0	0	1	1	1	0	128/64	10E0000–10EFFFF
SA271	1	0	0	0	0	1	1	1	1	128/64	10F0000–10FFFFF
SA272	1	0	0	0	1	0	0	0	0	128/64	1100000–110FFFF
SA273	1	0	0	0	1	0	0	0	1	128/64	1110000–111FFFF
SA274	1	0	0	0	1	0	0	1	0	128/64	1120000–112FFFF
SA275	1	0	0	0	1	0	0	1	1	128/64	1130000–113FFFF
SA276	1	0	0	0	1	0	1	0	0	128/64	1140000–114FFFF
SA277	1	0	0	0	1	0	1	0	1	128/64	1150000–115FFFF
SA278	1	0	0	0	1	0	1	1	0	128/64	1160000–116FFFF
SA279	1	0	0	0	1	0	1	1	1	128/64	1170000–117FFFF
SA280	1	0	0	0	1	1	0	0	0	128/64	1180000–118FFFF
SA281	1	0	0	0	1	1	0	0	1	128/64	1190000–119FFFF
SA282	1	0	0	0	1	1	0	1	0	128/64	11A0000–11AFFFF
SA283	1	0	0	0	1	1	0	1	1	128/64	11B0000–11BFFFF
SA284	1	0	0	0	1	1	1	0	0	128/64	11C0000–11CFFFF
SA285	1	0	0	0	1	1	1	0	1	128/64	11D0000–11DFFFF
SA286	1	0	0	0	1	1	1	1	0	128/64	11E0000–11EFFFF
SA287	1	0	0	0	1	1	1	1	1	128/64	11F0000–11FFFFF
SA288	1	0	0	1	0	0	0	0	0	128/64	1200000–120FFFF
SA289	1	0	0	1	0	0	0	0	1	128/64	1210000–121FFFF
SA290	1	0	0	1	0	0	0	1	0	128/64	1220000–122FFFF
SA291	1	0	0	1	0	0	0	1	1	128/64	1230000–123FFFF
SA292	1	0	0	1	0	0	1	0	0	128/64	1240000–124FFFF
SA293	1	0	0	1	0	0	1	0	1	128/64	1250000–125FFFF
SA294	1	0	0	1	0	0	1	1	0	128/64	1260000–126FFFF
SA295	1	0	0	1	0	0	1	1	1	128/64	1270000–127FFFF
SA296	1	0	0	1	0	1	0	0	0	128/64	1280000–128FFFF
SA297	1	0	0	1	0	1	0	0	1	128/64	1290000–129FFFF
SA298	1	0	0	1	0	1	0	1	0	128/64	12A0000–12AFFFF
SA299	1	0	0	1	0	1	0	1	1	128/64	12B0000–12BFFFF
SA300	1	0	0	1	0	1	1	0	0	128/64	12C0000–12CFFFF
SA301	1	0	0	1	0	1	1	0	1	128/64	12D0000–12DFFFF
SA302	1	0	0	1	0	1	1	1	0	128/64	12E0000–12EFFFF
SA303	1	0	0	1	0	1	1	1	1	128/64	12F0000–12FFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA304	1	0	0	1	1	0	0	0	0	128/64	1300000–130FFFF
SA305	1	0	0	1	1	0	0	0	1	128/64	1310000–131FFFF
SA306	1	0	0	1	1	0	0	1	0	128/64	1320000–132FFFF
SA307	1	0	0	1	1	0	0	1	1	128/64	1330000–133FFFF
SA308	1	0	0	1	1	0	1	0	0	128/64	1340000–134FFFF
SA309	1	0	0	1	1	0	1	0	1	128/64	1350000–135FFFF
SA310	1	0	0	1	1	0	1	1	0	128/64	1360000–136FFFF
SA311	1	0	0	1	1	0	1	1	1	128/64	1370000–137FFFF
SA312	1	0	0	1	1	1	0	0	0	128/64	1380000–138FFFF
SA313	1	0	0	1	1	1	0	0	1	128/64	1390000–139FFFF
SA314	1	0	0	1	1	1	0	1	0	128/64	13A0000–13AFFFF
SA315	1	0	0	1	1	1	0	1	1	128/64	13B0000–13BFFFF
SA316	1	0	0	1	1	1	1	0	0	128/64	13C0000–13CFFFF
SA317	1	0	0	1	1	1	1	0	1	128/64	13D0000–13DFFFF
SA318	1	0	0	1	1	1	1	1	0	128/64	13E0000–13EFFFF
SA319	1	0	0	1	1	1	1	1	1	128/64	13F0000–13FFFFF
SA320	1	0	1	0	0	0	0	0	0	128/64	1400000–140FFFF
SA321	1	0	1	0	0	0	0	0	1	128/64	1410000–141FFFF
SA322	1	0	1	0	0	0	0	1	0	128/64	1420000–142FFFF
SA323	1	0	1	0	0	0	0	1	1	128/64	1430000–143FFFF
SA324	1	0	1	0	0	0	1	0	0	128/64	1440000–144FFFF
SA325	1	0	1	0	0	0	1	0	1	128/64	1450000–145FFFF
SA326	1	0	1	0	0	0	1	1	0	128/64	1460000–146FFFF
SA327	1	0	1	0	0	0	1	1	1	128/64	1470000–147FFFF
SA328	1	0	1	0	0	1	0	0	0	128/64	1480000–148FFFF
SA329	1	0	1	0	0	1	0	0	1	128/64	1490000–149FFFF
SA330	1	0	1	0	0	1	0	1	0	128/64	14A0000–14AFFFF
SA331	1	0	1	0	0	1	0	1	1	128/64	14B0000–14BFFFF
SA332	1	0	1	0	0	1	1	0	0	128/64	14C0000–14CFFFF
SA333	1	0	1	0	0	1	1	0	1	128/64	14D0000–14DFFFF
SA334	1	0	1	0	0	1	1	1	0	128/64	14E0000–14EFFFF
SA335	1	0	1	0	0	1	1	1	1	128/64	14F0000–14FFFFF
SA336	1	0	1	0	1	0	0	0	0	128/64	1500000–150FFFF
SA337	1	0	1	0	1	0	0	0	1	128/64	1510000–151FFFF
SA338	1	0	1	0	1	0	0	1	0	128/64	1520000–152FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA339	1	0	1	0	1	0	0	1	1	128/64	1530000–153FFFF
SA340	1	0	1	0	1	0	1	0	0	128/64	1540000–154FFFF
SA341	1	0	1	0	1	0	1	0	1	128/64	1550000–155FFFF
SA342	1	0	1	0	1	0	1	1	0	128/64	1560000–156FFFF
SA343	1	0	1	0	1	0	1	1	1	128/64	1570000–157FFFF
SA344	1	0	1	0	1	1	0	0	0	128/64	1580000–158FFFF
SA345	1	0	1	0	1	1	0	0	1	128/64	1590000–159FFFF
SA346	1	0	1	0	1	1	0	1	0	128/64	15A0000–15AFFFF
SA347	1	0	1	0	1	1	0	1	1	128/64	15B0000–15BFFFF
SA348	1	0	1	0	1	1	1	0	0	128/64	15C0000–15CFFFF
SA349	1	0	1	0	1	1	1	0	1	128/64	15D0000–15DFFFF
SA350	1	0	1	0	1	1	1	1	0	128/64	15E0000–15EFFFF
SA351	1	0	1	0	1	1	1	1	1	128/64	15F0000–15FFFFF
SA352	1	0	1	1	0	0	0	0	0	128/64	1600000–160FFFF
SA353	1	0	1	1	0	0	0	0	1	128/64	1610000–161FFFF
SA354	1	0	1	1	0	0	0	1	0	128/64	1620000–162FFFF
SA355	1	0	1	1	0	0	0	1	1	128/64	1630000–163FFFF
SA356	1	0	1	1	0	0	1	0	0	128/64	1640000–164FFFF
SA357	1	0	1	1	0	0	1	0	1	128/64	1650000–165FFFF
SA358	1	0	1	1	0	0	1	1	0	128/64	1660000–166FFFF
SA359	1	0	1	1	0	0	1	1	1	128/64	1670000–167FFFF
SA360	1	0	1	1	0	1	0	0	0	128/64	1680000–168FFFF
SA361	1	0	1	1	0	1	0	0	1	128/64	1690000–169FFFF
SA362	1	0	1	1	0	1	0	1	0	128/64	16A0000–16AFFFF
SA363	1	0	1	1	0	1	0	1	1	128/64	16B0000–16BFFFF
SA364	1	0	1	1	0	1	1	0	0	128/64	16C0000–16CFFFF
SA365	1	0	1	1	0	1	1	0	1	128/64	16D0000–16DFFFF
SA366	1	0	1	1	0	1	1	1	0	128/64	16E0000–16EFFFF
SA367	1	0	1	1	0	1	1	1	1	128/64	16F0000–16FFFFF
SA368	1	0	1	1	1	0	0	0	0	128/64	1700000–170FFFF
SA369	1	0	1	1	1	0	0	0	1	128/64	1710000–171FFFF
SA370	1	0	1	1	1	0	0	1	0	128/64	1720000–172FFFF
SA371	1	0	1	1	1	0	0	1	1	128/64	1730000–173FFFF
SA372	1	0	1	1	1	0	1	0	0	128/64	1740000–174FFFF
SA373	1	0	1	1	1	0	1	0	1	128/64	1750000–175FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA374	1	0	1	1	1	0	1	1	0	128/64	1760000–176FFFF
SA375	1	0	1	1	1	0	1	1	1	128/64	1770000–177FFFF
SA376	1	0	1	1	1	1	0	0	0	128/64	1780000–178FFFF
SA377	1	0	1	1	1	1	0	0	1	128/64	1790000–179FFFF
SA378	1	0	1	1	1	1	0	1	0	128/64	17A0000–17AFFFF
SA379	1	0	1	1	1	1	0	1	1	128/64	17B0000–17BFFFF
SA380	1	0	1	1	1	1	1	0	0	128/64	17C0000–17CFFFF
SA381	1	0	1	1	1	1	1	0	1	128/64	17D0000–17DFFFF
SA382	1	0	1	1	1	1	1	1	0	128/64	17E0000–17EFFFF
SA383	1	0	1	1	1	1	1	1	1	128/64	17F0000–17FFFFF
SA384	1	1	0	0	0	0	0	0	0	128/64	1800000–180FFFF
SA385	1	1	0	0	0	0	0	0	1	128/64	1810000–181FFFF
SA386	1	1	0	0	0	0	0	1	0	128/64	1820000–182FFFF
SA387	1	1	0	0	0	0	0	1	1	128/64	1830000–183FFFF
SA388	1	1	0	0	0	0	1	0	0	128/64	1840000–184FFFF
SA389	1	1	0	0	0	0	1	0	1	128/64	1850000–185FFFF
SA390	1	1	0	0	0	0	1	1	0	128/64	1860000–186FFFF
SA391	1	1	0	0	0	0	1	1	1	128/64	1870000–187FFFF
SA392	1	1	0	0	0	1	0	0	0	128/64	1880000–188FFFF
SA393	1	1	0	0	0	1	0	0	1	128/64	1890000–189FFFF
SA394	1	1	0	0	0	1	0	1	0	128/64	18A0000–18AFFFF
SA395	1	1	0	0	0	1	0	1	1	128/64	18B0000–18BFFFF
SA396	1	1	0	0	0	1	1	0	0	128/64	18C0000–18CFFFF
SA397	1	1	0	0	0	1	1	0	1	128/64	18D0000–18DFFFF
SA398	1	1	0	0	0	1	1	1	0	128/64	18E0000–18EFFFF
SA399	1	1	0	0	0	1	1	1	1	128/64	18F0000–18FFFFF
SA400	1	1	0	0	1	0	0	0	0	128/64	1900000–190FFFF
SA401	1	1	0	0	1	0	0	0	1	128/64	1910000–191FFFF
SA402	1	1	0	0	1	0	0	1	0	128/64	1920000–192FFFF
SA403	1	1	0	0	1	0	0	1	1	128/64	1930000–193FFFF
SA404	1	1	0	0	1	0	1	0	0	128/64	1940000–194FFFF
SA405	1	1	0	0	1	0	1	0	1	128/64	1950000–195FFFF
SA406	1	1	0	0	1	0	1	1	0	128/64	1960000–196FFFF
SA407	1	1	0	0	1	0	1	1	1	128/64	1970000–197FFFF
SA408	1	1	0	0	1	1	0	0	0	128/64	1980000–198FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA409	1	1	0	0	1	1	0	0	1	128/64	1990000–199FFFF
SA410	1	1	0	0	1	1	0	1	0	128/64	19A0000–19AFFFF
SA411	1	1	0	0	1	1	0	1	1	128/64	19B0000–19BFFFF
SA412	1	1	0	0	1	1	1	0	0	128/64	19C0000–19CFFFF
SA413	1	1	0	0	1	1	1	0	1	128/64	19D0000–19DFFFF
SA414	1	1	0	0	1	1	1	1	0	128/64	19E0000–19EFFFF
SA415	1	1	0	0	1	1	1	1	1	128/64	19F0000–19FFFFF
SA416	1	1	0	1	0	0	0	0	0	128/64	1A00000–1A0FFFF
SA417	1	1	0	1	0	0	0	0	1	128/64	1A10000–1A1FFFF
SA418	1	1	0	1	0	0	0	1	0	128/64	1A20000–1A2FFFF
SA419	1	1	0	1	0	0	0	1	1	128/64	1A30000–1A3FFFF
SA420	1	1	0	1	0	0	1	0	0	128/64	1A40000–1A4FFFF
SA421	1	1	0	1	0	0	1	0	1	128/64	1A50000–1A5FFFF
SA422	1	1	0	1	0	0	1	1	0	128/64	1A60000–1A6FFFF
SA423	1	1	0	1	0	0	1	1	1	128/64	1A70000–1A7FFFF
SA424	1	1	0	1	0	1	0	0	0	128/64	1A80000–1A8FFFF
SA425	1	1	0	1	0	1	0	0	1	128/64	1A90000–1A9FFFF
SA426	1	1	0	1	0	1	0	1	0	128/64	1AA0000–1AAFFFF
SA427	1	1	0	1	0	1	0	1	1	128/64	1AB0000–1ABFFFF
SA428	1	1	0	1	0	1	1	0	0	128/64	1AC0000–1ACFFFF
SA429	1	1	0	1	0	1	1	0	1	128/64	1AD0000–1ADFFFF
SA430	1	1	0	1	0	1	1	1	0	128/64	1AE0000–1AEFFFF
SA431	1	1	0	1	0	1	1	1	1	128/64	1AF0000–1AFFFFF
SA432	1	1	0	1	1	0	0	0	0	128/64	1B00000–1B0FFFF
SA433	1	1	0	1	1	0	0	0	1	128/64	1B10000–1B1FFFF
SA434	1	1	0	1	1	0	0	1	0	128/64	1B20000–1B2FFFF
SA435	1	1	0	1	1	0	0	1	1	128/64	1B30000–1B3FFFF
SA436	1	1	0	1	1	0	1	0	0	128/64	1B40000–1B4FFFF
SA437	1	1	0	1	1	0	1	0	1	128/64	1B50000–1B5FFFF
SA438	1	1	0	1	1	0	1	1	0	128/64	1B60000–1B6FFFF
SA439	1	1	0	1	1	0	1	1	1	128/64	1B70000–1B7FFFF
SA440	1	1	0	1	1	1	0	0	0	128/64	1B80000–1B8FFFF
SA441	1	1	0	1	1	1	0	0	1	128/64	1B90000–1B9FFFF
SA442	1	1	0	1	1	1	0	1	0	128/64	1BA0000–1BAFFFF
SA443	1	1	0	1	1	1	0	1	1	128/64	1BB0000–1BBFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA444	1	1	0	1	1	1	1	0	0	128/64	1BC0000–1BCFFFF
SA445	1	1	0	1	1	1	1	0	1	128/64	1BD0000–1BDFFFF
SA446	1	1	0	1	1	1	1	1	0	128/64	1BE0000–1BEFFFF
SA447	1	1	0	1	1	1	1	1	1	128/64	1BF0000–1BFFFFF
SA448	1	1	1	0	0	0	0	0	0	128/64	1C00000–1C0FFFF
SA449	1	1	1	0	0	0	0	0	1	128/64	1C10000–1C1FFFF
SA450	1	1	1	0	0	0	0	1	0	128/64	1C20000–1C2FFFF
SA451	1	1	1	0	0	0	0	1	1	128/64	1C30000–1C3FFFF
SA452	1	1	1	0	0	0	1	0	0	128/64	1C40000–1C4FFFF
SA453	1	1	1	0	0	0	1	0	1	128/64	1C50000–1C5FFFF
SA454	1	1	1	0	0	0	1	1	0	128/64	1C60000–1C6FFFF
SA455	1	1	1	0	0	0	1	1	1	128/64	1C70000–1C7FFFF
SA456	1	1	1	0	0	1	0	0	0	128/64	1C80000–1C8FFFF
SA457	1	1	1	0	0	1	0	0	1	128/64	1C90000–1C9FFFF
SA458	1	1	1	0	0	1	0	1	0	128/64	1CA0000–1CAFFFF
SA459	1	1	1	0	0	1	0	1	1	128/64	1CB0000–1CBFFFF
SA460	1	1	1	0	0	1	1	0	0	128/64	1CC0000–1CCFFFF
SA461	1	1	1	0	0	1	1	0	1	128/64	1CD0000–1CDFFFF
SA462	1	1	1	0	0	1	1	1	0	128/64	1CE0000–1CEFFFF
SA463	1	1	1	0	0	1	1	1	1	128/64	1CF0000–1CFFFFF
SA464	1	1	1	0	1	0	0	0	0	128/64	1D00000–1D0FFFF
SA465	1	1	1	0	1	0	0	0	1	128/64	1D10000–1D1FFFF
SA466	1	1	1	0	1	0	0	1	0	128/64	1D20000–1D2FFFF
SA467	1	1	1	0	1	0	0	1	1	128/64	1D30000–1D3FFFF
SA468	1	1	1	0	1	0	1	0	0	128/64	1D40000–1D4FFFF
SA469	1	1	1	0	1	0	1	0	1	128/64	1D50000–1D5FFFF
SA470	1	1	1	0	1	0	1	1	0	128/64	1D60000–1D6FFFF
SA471	1	1	1	0	1	0	1	1	1	128/64	1D70000–1D7FFFF
SA472	1	1	1	0	1	1	0	0	0	128/64	1D80000–1D8FFFF
SA473	1	1	1	0	1	1	0	0	1	128/64	1D90000–1D9FFFF
SA474	1	1	1	0	1	1	0	1	0	128/64	1DA0000–1DAFFFF
SA475	1	1	1	0	1	1	0	1	1	128/64	1DB0000–1DBFFFF
SA476	1	1	1	0	1	1	1	0	0	128/64	1DC0000–1DCFFFF
SA477	1	1	1	0	1	1	1	0	1	128/64	1DD0000–1DDFFFF
SA478	1	1	1	0	1	1	1	1	0	128/64	1DE0000–1DEFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA479	1	1	1	0	1	1	1	1	1	128/64	1DF0000–1DFFFFF
SA480	1	1	1	1	0	0	0	0	0	128/64	1E00000–1E0FFFF
SA481	1	1	1	1	0	0	0	0	1	128/64	1E10000–1E1FFFF
SA482	1	1	1	1	0	0	0	1	0	128/64	1E20000–1E2FFFF
SA483	1	1	1	1	0	0	0	1	1	128/64	1E30000–1E3FFFF
SA484	1	1	1	1	0	0	1	0	0	128/64	1E40000–1E4FFFF
SA485	1	1	1	1	0	0	1	0	1	128/64	1E50000–1E5FFFF
SA486	1	1	1	1	0	0	1	1	0	128/64	1E60000–1E6FFFF
SA487	1	1	1	1	0	0	1	1	1	128/64	1E70000–1E7FFFF
SA488	1	1	1	1	0	1	0	0	0	128/64	1E80000–1E8FFFF
SA489	1	1	1	1	0	1	0	0	1	128/64	1E90000–1E9FFFF
SA490	1	1	1	1	0	1	0	1	0	128/64	1EA0000–1EAFFFF
SA491	1	1	1	1	0	1	0	1	1	128/64	1EB0000–1EBFFFF
SA492	1	1	1	1	0	1	1	0	0	128/64	1EC0000–1ECFFFF
SA493	1	1	1	1	0	1	1	0	1	128/64	1ED0000–1EDFFFF
SA494	1	1	1	1	0	1	1	1	0	128/64	1EE0000–1EEFFFF
SA495	1	1	1	1	0	1	1	1	1	128/64	1EF0000–1EFFFFF
SA496	1	1	1	1	1	0	0	0	0	128/64	1F00000–1F0FFFF
SA497	1	1	1	1	1	0	0	0	1	128/64	1F10000–1F1FFFF
SA498	1	1	1	1	1	0	0	1	0	128/64	1F20000–1F2FFFF
SA499	1	1	1	1	1	0	0	1	1	128/64	1F30000–1F3FFFF
SA500	1	1	1	1	1	0	1	0	0	128/64	1F40000–1F4FFFF
SA501	1	1	1	1	1	0	1	0	1	128/64	1F50000–1F5FFFF
SA502	1	1	1	1	1	0	1	1	0	128/64	1F60000–1F6FFFF
SA503	1	1	1	1	1	0	1	1	1	128/64	1F70000–1F7FFFF
SA504	1	1	1	1	1	1	0	0	0	128/64	1F80000–1F8FFFF
SA505	1	1	1	1	1	1	0	0	1	128/64	1F90000–1F9FFFF
SA506	1	1	1	1	1	1	0	1	0	128/64	1FA0000–1FAFFFF
SA507	1	1	1	1	1	1	0	1	1	128/64	1FB0000–1FBFFFF
SA508	1	1	1	1	1	1	1	0	0	128/64	1FC0000–1FCFFFF
SA509	1	1	1	1	1	1	1	0	1	128/64	1FD0000–1FDFFFF
SA510	1	1	1	1	1	1	1	1	0	128/64	1FE0000–1FEFFFF
SA511	1	1	1	1	1	1	1	1	1	128/64	1FF0000–1FFFFFF

Table 3. Sector Address Table–S29GL256N

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	0	128/64	0000000–000FFFF
SA1	0	0	0	0	0	0	0	1	128/64	0010000–001FFFF
SA2	0	0	0	0	0	0	1	0	128/64	0020000–002FFFF
SA3	0	0	0	0	0	0	1	1	128/64	0030000–003FFFF
SA4	0	0	0	0	0	1	0	0	128/64	0040000–004FFFF
SA5	0	0	0	0	0	1	0	1	128/64	0050000–005FFFF
SA6	0	0	0	0	0	1	1	0	128/64	0060000–006FFFF
SA7	0	0	0	0	0	1	1	1	128/64	0070000–007FFFF
SA8	0	0	0	0	1	0	0	0	128/64	0080000–008FFFF
SA9	0	0	0	0	1	0	0	1	128/64	0090000–009FFFF
SA10	0	0	0	0	1	0	1	0	128/64	00A0000–00AFFFF
SA11	0	0	0	0	1	0	1	1	128/64	00B0000–00BFFFF
SA12	0	0	0	0	1	1	0	0	128/64	00C0000–00CFFFF
SA13	0	0	0	0	1	1	0	1	128/64	00D0000–00DFFFF
SA14	0	0	0	0	1	1	1	0	128/64	00E0000–00EFFFF
SA15	0	0	0	0	1	1	1	1	128/64	00F0000–00FFFFF
SA16	0	0	0	1	0	0	0	0	128/64	0100000–010FFFF
SA17	0	0	0	1	0	0	0	1	128/64	0110000–011FFFF
SA18	0	0	0	1	0	0	1	0	128/64	0120000–012FFFF
SA19	0	0	0	1	0	0	1	1	128/64	0130000–013FFFF
SA20	0	0	0	1	0	1	0	0	128/64	0140000–014FFFF
SA21	0	0	0	1	0	1	0	1	128/64	0150000–015FFFF
SA22	0	0	0	1	0	1	1	0	128/64	0160000–016FFFF
SA23	0	0	0	1	0	1	1	1	128/64	0170000–017FFFF
SA24	0	0	0	1	1	0	0	0	128/64	0180000–018FFFF
SA25	0	0	0	1	1	0	0	1	128/64	0190000–019FFFF
SA26	0	0	0	1	1	0	1	0	128/64	01A0000–01AFFFF
SA27	0	0	0	1	1	0	1	1	128/64	01B0000–01BFFFF
SA28	0	0	0	1	1	1	0	0	128/64	01C0000–01CFFFF
SA29	0	0	0	1	1	1	0	1	128/64	01D0000–01DFFFF
SA30	0	0	0	1	1	1	1	0	128/64	01E0000–01EFFFF
SA31	0	0	0	1	1	1	1	1	128/64	01F0000–01FFFFF
SA32	0	0	1	0	0	0	0	0	128/64	0200000–020FFFF
SA33	0	0	1	0	0	0	0	1	128/64	0210000–021FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA34	0	0	1	0	0	0	1	0	128/64	0220000–022FFFF
SA35	0	0	1	0	0	0	1	1	128/64	0230000–023FFFF
SA36	0	0	1	0	0	1	0	0	128/64	0240000–024FFFF
SA37	0	0	1	0	0	1	0	1	128/64	0250000–025FFFF
SA38	0	0	1	0	0	1	1	0	128/64	0260000–026FFFF
SA39	0	0	1	0	0	1	1	1	128/64	0270000–027FFFF
SA40	0	0	1	0	1	0	0	0	128/64	0280000–028FFFF
SA41	0	0	1	0	1	0	0	1	128/64	0290000–029FFFF
SA42	0	0	1	0	1	0	1	0	128/64	02A0000–02AFFFF
SA43	0	0	1	0	1	0	1	1	128/64	02B0000–02BFFFF
SA44	0	0	1	0	1	1	0	0	128/64	02C0000–02CFFFF
SA45	0	0	1	0	1	1	0	1	128/64	02D0000–02DFFFF
SA46	0	0	1	0	1	1	1	0	128/64	02E0000–02EFFFF
SA47	0	0	1	0	1	1	1	1	128/64	02F0000–02FFFFF
SA48	0	0	1	1	0	0	0	0	128/64	0300000–030FFFF
SA49	0	0	1	1	0	0	0	1	128/64	0310000–031FFFF
SA50	0	0	1	1	0	0	1	0	128/64	0320000–032FFFF
SA51	0	0	1	1	0	0	1	1	128/64	0330000–033FFFF
SA52	0	0	1	1	0	1	0	0	128/64	0340000–034FFFF
SA53	0	0	1	1	0	1	0	1	128/64	0350000–035FFFF
SA54	0	0	1	1	0	1	1	0	128/64	0360000–036FFFF
SA55	0	0	1	1	0	1	1	1	128/64	0370000–037FFFF
SA56	0	0	1	1	1	0	0	0	128/64	0380000–038FFFF
SA57	0	0	1	1	1	0	0	1	128/64	0390000–039FFFF
SA58	0	0	1	1	1	0	1	0	128/64	03A0000–03AFFFF
SA59	0	0	1	1	1	0	1	1	128/64	03B0000–03BFFFF
SA60	0	0	1	1	1	1	0	0	128/64	03C0000–03CFFFF
SA61	0	0	1	1	1	1	0	1	128/64	03D0000–03DFFFF
SA62	0	0	1	1	1	1	1	0	128/64	03E0000–03EFFFF
SA63	0	0	1	1	1	1	1	1	128/64	03F0000–03FFFFF
SA64	0	1	0	0	0	0	0	0	128/64	0400000–040FFFF
SA65	0	1	0	0	0	0	0	1	128/64	0410000–041FFFF
SA66	0	1	0	0	0	0	1	0	128/64	0420000–042FFFF
SA67	0	1	0	0	0	0	1	1	128/64	0430000–043FFFF
SA68	0	1	0	0	0	1	0	0	128/64	0440000–044FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA69	0	1	0	0	0	1	0	1	128/64	0450000–045FFFF
SA70	0	1	0	0	0	1	1	0	128/64	0460000–046FFFF
SA71	0	1	0	0	0	1	1	1	128/64	0470000–047FFFF
SA72	0	1	0	0	1	0	0	0	128/64	0480000–048FFFF
SA73	0	1	0	0	1	0	0	1	128/64	0490000–049FFFF
SA74	0	1	0	0	1	0	1	0	128/64	04A0000–04AFFFF
SA75	0	1	0	0	1	0	1	1	128/64	04B0000–04BFFFF
SA76	0	1	0	0	1	1	0	0	128/64	04C0000–04CFFFF
SA77	0	1	0	0	1	1	0	1	128/64	04D0000–04DFFFF
SA78	0	1	0	0	1	1	1	0	128/64	04E0000–04EFFFF
SA79	0	1	0	0	1	1	1	1	128/64	04F0000–04FFFFF
SA80	0	1	0	1	0	0	0	0	128/64	0500000–050FFFF
SA81	0	1	0	1	0	0	0	1	128/64	0510000–051FFFF
SA82	0	1	0	1	0	0	1	0	128/64	0520000–052FFFF
SA83	0	1	0	1	0	0	1	1	128/64	0530000–053FFFF
SA84	0	1	0	1	0	1	0	0	128/64	0540000–054FFFF
SA85	0	1	0	1	0	1	0	1	128/64	0550000–055FFFF
SA86	0	1	0	1	0	1	1	0	128/64	0560000–056FFFF
SA87	0	1	0	1	0	1	1	1	128/64	0570000–057FFFF
SA88	0	1	0	1	1	0	0	0	128/64	0580000–058FFFF
SA89	0	1	0	1	1	0	0	1	128/64	0590000–059FFFF
SA90	0	1	0	1	1	0	1	0	128/64	05A0000–05AFFFF
SA91	0	1	0	1	1	0	1	1	128/64	05B0000–05BFFFF
SA92	0	1	0	1	1	1	0	0	128/64	05C0000–05CFFFF
SA93	0	1	0	1	1	1	0	1	128/64	05D0000–05DFFFF
SA94	0	1	0	1	1	1	1	0	128/64	05E0000–05EFFFF
SA95	0	1	0	1	1	1	1	1	128/64	05F0000–05FFFFF
SA96	0	1	1	0	0	0	0	0	128/64	0600000–060FFFF
SA97	0	1	1	0	0	0	0	1	128/64	0610000–061FFFF
SA98	0	1	1	0	0	0	1	0	128/64	0620000–062FFFF
SA99	0	1	1	0	0	0	1	1	128/64	0630000–063FFFF
SA100	0	1	1	0	0	1	0	0	128/64	0640000–064FFFF
SA101	0	1	1	0	0	1	0	1	128/64	0650000–065FFFF
SA102	0	1	1	0	0	1	1	0	128/64	0660000–066FFFF
SA103	0	1	1	0	0	1	1	1	128/64	0670000–067FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA104	0	1	1	0	1	0	0	0	128/64	0680000–068FFFF
SA105	0	1	1	0	1	0	0	1	128/64	0690000–069FFFF
SA106	0	1	1	0	1	0	1	0	128/64	06A0000–06AFFFF
SA107	0	1	1	0	1	0	1	1	128/64	06B0000–06BFFFF
SA108	0	1	1	0	1	1	0	0	128/64	06C0000–06CFFFF
SA109	0	1	1	0	1	1	0	1	128/64	06D0000–06DFFFF
SA110	0	1	1	0	1	1	1	0	128/64	06E0000–06EFFFF
SA111	0	1	1	0	1	1	1	1	128/64	06F0000–06FFFFF
SA112	0	1	1	1	0	0	0	0	128/64	0700000–070FFFF
SA113	0	1	1	1	0	0	0	1	128/64	0710000–071FFFF
SA114	0	1	1	1	0	0	1	0	128/64	0720000–072FFFF
SA115	0	1	1	1	0	0	1	1	128/64	0730000–073FFFF
SA116	0	1	1	1	0	1	0	0	128/64	0740000–074FFFF
SA117	0	1	1	1	0	1	0	1	128/64	0750000–075FFFF
SA118	0	1	1	1	0	1	1	0	128/64	0760000–076FFFF
SA119	0	1	1	1	0	1	1	1	128/64	0770000–077FFFF
SA120	0	1	1	1	1	0	0	0	128/64	0780000–078FFFF
SA121	0	1	1	1	1	0	0	1	128/64	0790000–079FFFF
SA122	0	1	1	1	1	0	1	0	128/64	07A0000–07AFFFF
SA123	0	1	1	1	1	0	1	1	128/64	07B0000–07BFFFF
SA124	0	1	1	1	1	1	0	0	128/64	07C0000–07CFFFF
SA125	0	1	1	1	1	1	0	1	128/64	07D0000–07DFFFF
SA126	0	1	1	1	1	1	1	0	128/64	07E0000–07EFFFF
SA127	0	1	1	1	1	1	1	1	128/64	07F0000–07FFFFF
SA128	1	0	0	0	0	0	0	0	128/64	0800000–080FFFF
SA129	1	0	0	0	0	0	0	1	128/64	0810000–081FFFF
SA130	1	0	0	0	0	0	1	0	128/64	0820000–082FFFF
SA131	1	0	0	0	0	0	1	1	128/64	0830000–083FFFF
SA132	1	0	0	0	0	1	0	0	128/64	0840000–084FFFF
SA133	1	0	0	0	0	1	0	1	128/64	0850000–085FFFF
SA134	1	0	0	0	0	1	1	0	128/64	0860000–086FFFF
SA135	1	0	0	0	0	1	1	1	128/64	0870000–087FFFF
SA136	1	0	0	0	1	0	0	0	128/64	0880000–088FFFF
SA137	1	0	0	0	1	0	0	1	128/64	0890000–089FFFF
SA138	1	0	0	0	1	0	1	0	128/64	08A0000–08AFFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA139	1	0	0	0	1	0	1	1	128/64	08B0000–08BFFFF
SA140	1	0	0	0	1	1	0	0	128/64	08C0000–08CFFFF
SA141	1	0	0	0	1	1	0	1	128/64	08D0000–08DFFFF
SA142	1	0	0	0	1	1	1	0	128/64	08E0000–08EFFFF
SA143	1	0	0	0	1	1	1	1	128/64	08F0000–08FFFFF
SA144	1	0	0	1	0	0	0	0	128/64	0900000–090FFFF
SA145	1	0	0	1	0	0	0	1	128/64	0910000–091FFFF
SA146	1	0	0	1	0	0	1	0	128/64	0920000–092FFFF
SA147	1	0	0	1	0	0	1	1	128/64	0930000–093FFFF
SA148	1	0	0	1	0	1	0	0	128/64	0940000–094FFFF
SA149	1	0	0	1	0	1	0	1	128/64	0950000–095FFFF
SA150	1	0	0	1	0	1	1	0	128/64	0960000–096FFFF
SA151	1	0	0	1	0	1	1	1	128/64	0970000–097FFFF
SA152	1	0	0	1	1	0	0	0	128/64	0980000–098FFFF
SA153	1	0	0	1	1	0	0	1	128/64	0990000–099FFFF
SA154	1	0	0	1	1	0	1	0	128/64	09A0000–09AFFFF
SA155	1	0	0	1	1	0	1	1	128/64	09B0000–09BFFFF
SA156	1	0	0	1	1	1	0	0	128/64	09C0000–09CFFFF
SA157	1	0	0	1	1	1	0	1	128/64	09D0000–09DFFFF
SA158	1	0	0	1	1	1	1	0	128/64	09E0000–09EFFFF
SA159	1	0	0	1	1	1	1	1	128/64	09F0000–09FFFFF
SA160	1	0	1	0	0	0	0	0	128/64	0A00000–0A0FFFF
SA161	1	0	1	0	0	0	0	1	128/64	0A10000–0A1FFFF
SA162	1	0	1	0	0	0	1	0	128/64	0A20000–0A2FFFF
SA163	1	0	1	0	0	0	1	1	128/64	0A30000–0A3FFFF
SA164	1	0	1	0	0	1	0	0	128/64	0A40000–0A4FFFF
SA165	1	0	1	0	0	1	0	1	128/64	0A50000–0A5FFFF
SA166	1	0	1	0	0	1	1	0	128/64	0A60000–0A6FFFF
SA167	1	0	1	0	0	1	1	1	128/64	0A70000–0A7FFFF
SA168	1	0	1	0	1	0	0	0	128/64	0A80000–0A8FFFF
SA169	1	0	1	0	1	0	0	1	128/64	0A90000–0A9FFFF
SA170	1	0	1	0	1	0	1	0	128/64	0AA0000–0AAFFFF
SA171	1	0	1	0	1	0	1	1	128/64	0AB0000–0ABFFFF
SA172	1	0	1	0	1	1	0	0	128/64	0AC0000–0ACFFFF
SA173	1	0	1	0	1	1	0	1	128/64	0AD0000–0ADFFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA174	1	0	1	0	1	1	1	0	128/64	0AE0000–0AEFFFF
SA175	1	0	1	0	1	1	1	1	128/64	0AF0000–0AFFFFF
SA176	1	0	1	1	0	0	0	0	128/64	0B00000–0B0FFFF
SA177	1	0	1	1	0	0	0	1	128/64	0B10000–0B1FFFF
SA178	1	0	1	1	0	0	1	0	128/64	0B20000–0B2FFFF
SA179	1	0	1	1	0	0	1	1	128/64	0B30000–0B3FFFF
SA180	1	0	1	1	0	1	0	0	128/64	0B40000–0B4FFFF
SA181	1	0	1	1	0	1	0	1	128/64	0B50000–0B5FFFF
SA182	1	0	1	1	0	1	1	0	128/64	0B60000–0B6FFFF
SA183	1	0	1	1	0	1	1	1	128/64	0B70000–0B7FFFF
SA184	1	0	1	1	1	0	0	0	128/64	0B80000–0B8FFFF
SA185	1	0	1	1	1	0	0	1	128/64	0B90000–0B9FFFF
SA186	1	0	1	1	1	0	1	0	128/64	0BA0000–0BAFFFF
SA187	1	0	1	1	1	0	1	1	128/64	0BB0000–0BBFFFF
SA188	1	0	1	1	1	1	0	0	128/64	0BC0000–0BCFFFF
SA189	1	0	1	1	1	1	0	1	128/64	0BD0000–0BDFFFF
SA190	1	0	1	1	1	1	1	0	128/64	0BE0000–0BEFFFF
SA191	1	0	1	1	1	1	1	1	128/64	0BF0000–0BFFFFF
SA192	1	1	0	0	0	0	0	0	128/64	0C00000–0C0FFFF
SA193	1	1	0	0	0	0	0	1	128/64	0C10000–0C1FFFF
SA194	1	1	0	0	0	0	1	0	128/64	0C20000–0C2FFFF
SA195	1	1	0	0	0	0	1	1	128/64	0C30000–0C3FFFF
SA196	1	1	0	0	0	1	0	0	128/64	0C40000–0C4FFFF
SA197	1	1	0	0	0	1	0	1	128/64	0C50000–0C5FFFF
SA198	1	1	0	0	0	1	1	0	128/64	0C60000–0C6FFFF
SA199	1	1	0	0	0	1	1	1	128/64	0C70000–0C7FFFF
SA200	1	1	0	0	1	0	0	0	128/64	0C80000–0C8FFFF
SA201	1	1	0	0	1	0	0	1	128/64	0C90000–0C9FFFF
SA202	1	1	0	0	1	0	1	0	128/64	0CA0000–0CAFFFF
SA203	1	1	0	0	1	0	1	1	128/64	0CB0000–0CBFFFF
SA204	1	1	0	0	1	1	0	0	128/64	0CC0000–0CCFFFF
SA205	1	1	0	0	1	1	0	1	128/64	0CD0000–0CDFFFF
SA206	1	1	0	0	1	1	1	0	128/64	0CE0000–0CEFFFF
SA207	1	1	0	0	1	1	1	1	128/64	0CF0000–0CFFFFF
SA208	1	1	0	1	0	0	0	0	128/64	0D00000–0D0FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA209	1	1	0	1	0	0	0	1	128/64	0D10000–0D1FFFF
SA210	1	1	0	1	0	0	1	0	128/64	0D20000–0D2FFFF
SA211	1	1	0	1	0	0	1	1	128/64	0D30000–0D3FFFF
SA212	1	1	0	1	0	1	0	0	128/64	0D40000–0D4FFFF
SA213	1	1	0	1	0	1	0	1	128/64	0D50000–0D5FFFF
SA214	1	1	0	1	0	1	1	0	128/64	0D60000–0D6FFFF
SA215	1	1	0	1	0	1	1	1	128/64	0D70000–0D7FFFF
SA216	1	1	0	1	1	0	0	0	128/64	0D80000–0D8FFFF
SA217	1	1	0	1	1	0	0	1	128/64	0D90000–0D9FFFF
SA218	1	1	0	1	1	0	1	0	128/64	0DA0000–0DAFFFF
SA219	1	1	0	1	1	0	1	1	128/64	0DB0000–0DBFFFF
SA220	1	1	0	1	1	1	0	0	128/64	0DC0000–0DCFFFF
SA221	1	1	0	1	1	1	0	1	128/64	0DD0000–0DDFFFF
SA222	1	1	0	1	1	1	1	0	128/64	0DE0000–0DEFFFF
SA223	1	1	0	1	1	1	1	1	128/64	0DF0000–0DFFFFF
SA224	1	1	1	0	0	0	0	0	128/64	0E00000–0E0FFFF
SA225	1	1	1	0	0	0	0	1	128/64	0E10000–0E1FFFF
SA226	1	1	1	0	0	0	1	0	128/64	0E20000–0E2FFFF
SA227	1	1	1	0	0	0	1	1	128/64	0E30000–0E3FFFF
SA228	1	1	1	0	0	1	0	0	128/64	0E40000–0E4FFFF
SA229	1	1	1	0	0	1	0	1	128/64	0E50000–0E5FFFF
SA230	1	1	1	0	0	1	1	0	128/64	0E60000–0E6FFFF
SA231	1	1	1	0	0	1	1	1	128/64	0E70000–0E7FFFF
SA232	1	1	1	0	1	0	0	0	128/64	0E80000–0E8FFFF
SA233	1	1	1	0	1	0	0	1	128/64	0E90000–0E9FFFF
SA234	1	1	1	0	1	0	1	0	128/64	0EA0000–0EAFFFF
SA235	1	1	1	0	1	0	1	1	128/64	0EB0000–0EBFFFF
SA236	1	1	1	0	1	1	0	0	128/64	0EC0000–0ECFFFF
SA237	1	1	1	0	1	1	0	1	128/64	0ED0000–0EDFFFF
SA238	1	1	1	0	1	1	1	0	128/64	0EE0000–0EEFFFF
SA239	1	1	1	0	1	1	1	1	128/64	0EF0000–0EFFFFF
SA240	1	1	1	1	0	0	0	0	128/64	0F00000–0F0FFFF
SA241	1	1	1	1	0	0	0	1	128/64	0F10000–0F1FFFF
SA242	1	1	1	1	0	0	1	0	128/64	0F20000–0F2FFFF
SA243	1	1	1	1	0	0	1	1	128/64	0F30000–0F3FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA244	1	1	1	1	0	1	0	0	128/64	0F40000–0F4FFFF
SA245	1	1	1	1	0	1	0	1	128/64	0F50000–0F5FFFF
SA246	1	1	1	1	0	1	1	0	128/64	0F60000–0F6FFFF
SA247	1	1	1	1	0	1	1	1	128/64	0F70000–0F7FFFF
SA248	1	1	1	1	1	0	0	0	128/64	0F80000–0F8FFFF
SA249	1	1	1	1	1	0	0	1	128/64	0F90000–0F9FFFF
SA250	1	1	1	1	1	0	1	0	128/64	0FA0000–0FAFFFF
SA251	1	1	1	1	1	0	1	1	128/64	0FB0000–0FBFFFF
SA252	1	1	1	1	1	1	0	0	128/64	0FC0000–0FCFFFF
SA253	1	1	1	1	1	1	0	1	128/64	0FD0000–0FDFFFF
SA254	1	1	1	1	1	1	1	0	128/64	0FE0000–0FEFFFF
SA255	1	1	1	1	1	1	1	1	128/64	0FF0000–0FFFFFF

Table 4. Sector Address Table–S29GLI28N

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	128/64	0000000–000FFFF
SA1	0	0	0	0	0	1	128/64	0010000–001FFFF
SA2	0	0	0	0	1	0	128/64	0020000–002FFFF
SA3	0	0	0	0	1	1	128/64	0030000–003FFFF
SA4	0	0	0	1	0	0	128/64	0040000–004FFFF
SA5	0	0	0	1	0	1	128/64	0050000–005FFFF
SA6	0	0	0	1	1	0	128/64	0060000–006FFFF
SA7	0	0	0	1	1	1	128/64	0070000–007FFFF
SA8	0	0	1	0	0	0	128/64	0080000–008FFFF
SA9	0	0	1	0	0	1	128/64	0090000–009FFFF
SA10	0	0	1	0	1	0	128/64	00A0000–00AFFFF
SA11	0	0	1	0	1	1	128/64	00B0000–00BFFFF
SA12	0	0	1	1	0	0	128/64	00C0000–00CFFFF
SA13	0	0	1	1	0	1	128/64	00D0000–00DFFFF
SA14	0	0	1	1	1	0	128/64	00E0000–00EFFFF
SA15	0	0	1	1	1	1	128/64	00F0000–00FFFFF
SA16	0	1	0	0	0	0	128/64	0100000–010FFFF
SA17	0	1	0	0	0	1	128/64	0110000–011FFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA18	0	1	0	0	1	0	128/64	0120000–012FFFF
SA19	0	1	0	0	1	1	128/64	0130000–013FFFF
SA20	0	1	0	1	0	0	128/64	0140000–014FFFF
SA21	0	1	0	1	0	1	128/64	0150000–015FFFF
SA22	0	1	0	1	1	0	128/64	0160000–016FFFF
SA23	0	1	0	1	1	1	128/64	0170000–017FFFF
SA24	0	1	1	0	0	0	128/64	0180000–018FFFF
SA25	0	1	1	0	0	1	128/64	0190000–019FFFF
SA26	0	1	1	0	1	0	128/64	01A0000–01AFFFF
SA27	0	1	1	0	1	1	128/64	01B0000–01BFFFF
SA28	0	1	1	1	0	0	128/64	01C0000–01CFFFF
SA29	0	1	1	1	0	1	128/64	01D0000–01DFFFF
SA30	0	1	1	1	1	0	128/64	01E0000–01EFFFF
SA31	0	1	1	1	1	1	128/64	01F0000–01FFFFF
SA32	1	0	0	0	0	0	128/64	0200000–020FFFF
SA33	1	0	0	0	0	1	128/64	0210000–021FFFF
SA34	1	0	0	0	1	0	128/64	0220000–022FFFF
SA35	1	0	0	0	1	1	128/64	0230000–023FFFF
SA36	1	0	0	1	0	0	128/64	0240000–024FFFF
SA37	1	0	0	1	0	1	128/64	0250000–025FFFF
SA38	1	0	0	1	1	0	128/64	0260000–026FFFF
SA39	1	0	0	1	1	1	128/64	0270000–027FFFF
SA40	1	0	1	0	0	0	128/64	0280000–028FFFF
SA41	1	0	1	0	0	1	128/64	0290000–029FFFF
SA42	1	0	1	0	1	0	128/64	02A0000–02AFFFF
SA43	1	0	1	0	1	1	128/64	02B0000–02BFFFF
SA44	1	0	1	1	0	0	128/64	02C0000–02CFFFF
SA45	1	0	1	1	0	1	128/64	02D0000–02DFFFF
SA46	1	0	1	1	1	0	128/64	02E0000–02EFFFF
SA47	1	0	1	1	1	1	128/64	02F0000–02FFFFF
SA48	1	1	0	0	0	0	128/64	0300000–030FFFF
SA49	1	1	0	0	0	1	128/64	0310000–031FFFF
SA50	1	1	0	0	1	0	128/64	0320000–032FFFF
SA51	1	1	0	0	1	1	128/64	0330000–033FFFF
SA52	1	1	0	1	0	0	128/64	0340000–034FFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA53	1	1	0	1	0	1	128/64	0350000–035FFFF
SA54	1	1	0	1	1	0	128/64	0360000–036FFFF
SA55	1	1	0	1	1	1	128/64	0370000–037FFFF
SA56	1	1	1	0	0	0	128/64	0380000–038FFFF
SA57	1	1	1	0	0	1	128/64	0390000–039FFFF
SA58	1	1	1	0	1	0	128/64	03A0000–03AFFFF
SA59	1	1	1	0	1	1	128/64	03B0000–03BFFFF
SA60	1	1	1	1	0	0	128/64	03C0000–03CFFFF
SA61	1	1	1	1	0	1	128/64	03D0000–03DFFFF
SA62	1	1	1	1	1	0	128/64	03E0000–03EFFFF
SA63	1	1	1	1	1	1	128/64	03F0000–03FFFFF
SA64	0	0	0	0	0	0	128/64	0400000–040FFFF
SA65	0	0	0	0	0	1	128/64	0410000–041FFFF
SA66	0	0	0	0	1	0	128/64	0420000–042FFFF
SA67	0	0	0	0	1	1	128/64	0430000–043FFFF
SA68	0	0	0	1	0	0	128/64	0440000–044FFFF
SA69	0	0	0	1	0	1	128/64	0450000–045FFFF
SA70	0	0	0	1	1	0	128/64	0460000–046FFFF
SA71	0	0	0	1	1	1	128/64	0470000–047FFFF
SA72	0	0	1	0	0	0	128/64	0480000–048FFFF
SA73	0	0	1	0	0	1	128/64	0490000–049FFFF
SA74	0	0	1	0	1	0	128/64	04A0000–04AFFFF
SA75	0	0	1	0	1	1	128/64	04B0000–04BFFFF
SA76	0	0	1	1	0	0	128/64	04C0000–04CFFFF
SA77	0	0	1	1	0	1	128/64	04D0000–04DFFFF
SA78	0	0	1	1	1	0	128/64	04E0000–04EFFFF
SA79	0	0	1	1	1	1	128/64	04F0000–04FFFFF
SA80	0	1	0	0	0	0	128/64	0500000–050FFFF
SA81	0	1	0	0	0	1	128/64	0510000–051FFFF
SA82	0	1	0	0	1	0	128/64	0520000–052FFFF
SA83	0	1	0	0	1	1	128/64	0530000–053FFFF
SA84	0	1	0	1	0	0	128/64	0540000–054FFFF
SA85	0	1	0	1	0	1	128/64	0550000–055FFFF
SA86	0	1	0	1	1	0	128/64	0560000–056FFFF
SA87	0	1	0	1	1	1	128/64	0570000–057FFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA88	0	1	1	0	0	0	128/64	0580000–058FFFF
SA89	0	1	1	0	0	1	128/64	0590000–059FFFF
SA90	0	1	1	0	1	0	128/64	05A0000–05AFFFF
SA91	0	1	1	0	1	1	128/64	05B0000–05BFFFF
SA92	0	1	1	1	0	0	128/64	05C0000–05CFFFF
SA93	0	1	1	1	0	1	128/64	05D0000–05DFFFF
SA94	0	1	1	1	1	0	128/64	05E0000–05EFFFF
SA95	0	1	1	1	1	1	128/64	05F0000–05FFFFF
SA96	1	0	0	0	0	0	128/64	0600000–060FFFF
SA97	1	0	0	0	0	1	128/64	0610000–061FFFF
SA98	1	0	0	0	1	0	128/64	0620000–062FFFF
SA99	1	0	0	0	1	1	128/64	0630000–063FFFF
SA100	1	0	0	1	0	0	128/64	0640000–064FFFF
SA101	1	0	0	1	0	1	128/64	0650000–065FFFF
SA102	1	0	0	1	1	0	128/64	0660000–066FFFF
SA103	1	0	0	1	1	1	128/64	0670000–067FFFF
SA104	1	0	1	0	0	0	128/64	0680000–068FFFF
SA105	1	0	1	0	0	1	128/64	0690000–069FFFF
SA106	1	0	1	0	1	0	128/64	06A0000–06AFFFF
SA107	1	0	1	0	1	1	128/64	06B0000–06BFFFF
SA108	1	0	1	1	0	0	128/64	06C0000–06CFFFF
SA109	1	0	1	1	0	1	128/64	06D0000–06DFFFF
SA110	1	0	1	1	1	0	128/64	06E0000–06EFFFF
SA111	1	0	1	1	1	1	128/64	06F0000–06FFFFF
SA112	1	1	0	0	0	0	128/64	0700000–070FFFF
SA113	1	1	0	0	0	1	128/64	0710000–071FFFF
SA114	1	1	0	0	1	0	128/64	0720000–072FFFF
SA115	1	1	0	0	1	1	128/64	0730000–073FFFF
SA116	1	1	0	1	0	0	128/64	0740000–074FFFF
SA117	1	1	0	1	0	1	128/64	0750000–075FFFF
SA118	1	1	0	1	1	0	128/64	0760000–076FFFF
SA119	1	1	0	1	1	1	128/64	0770000–077FFFF
SA120	1	1	1	0	0	0	128/64	0780000–078FFFF
SA121	1	1	1	0	0	1	128/64	0790000–079FFFF
SA122	1	1	1	0	1	0	128/64	07A0000–07AFFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)
SA123	1	1	1	0	1	1	128/64	07B0000–07BFFFF
SA124	1	1	1	1	0	0	128/64	07C0000–07CFFFF
SA125	1	1	1	1	0	1	128/64	07D0000–07DFFFF
SA126	1	1	1	1	1	0	128/64	07E0000–07EFFFF
SA127	1	1	1	1	1	1	128/64	07F0000–07FFFFF

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector group protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 5. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). Table 5 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 5. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE #	A22 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Spansion Product		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	01h
Device ID S29GL512N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	7Eh
	Cycle 2										H	H	L	22	23h
	Cycle 3										H	H	H	22	01h
Device ID S29GL256N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	7Eh
	Cycle 2										H	H	L	22	22h
	Cycle 3										H	H	H	22	01h
Device ID S29GL128N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	7Eh
	Cycle 2										H	H	L	22	21h
	Cycle 3										H	H	H	22	01h
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	98h (factory locked), 18h (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	88h (factory locked), 08h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue

using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. The factory offers the option of programming and protecting sectors at the factory prior to shipping the device through the ExpressFlash™ Service. Contact your sales representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Command Sequence" section on page 127 for details.

Advanced Sector Protection

Advanced Sector Protection features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

Persistent Sector Protection is a method that replaces the old 12V controlled protection method.

Password Sector Protection is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Lock Register

The Lock Register consists of 3 bits (DQ2, DQ1, and DQ0). These DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device will abort the Lock Register back to the default 11 state. The programming time of the Lock Register is same as the typical word programming time without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I will toggle until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses.

The Customer Secured Silicon Sector Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, and Password Protection Mode Lock Bit is DQ2 are accessible by all users. Each of these bits are non-volatile. DQ15-DQ3 are reserved and must be 1's when the user tries to program the DQ2, DQ1, and DQ0 bits of the Lock Register. The user is not required to program DQ2, DQ1 and DQ0 bits of the Lock Register at the same time. This allows users to lock the Secured Silicon Sector and then set the device either permanently into Password Protection Mode or Persistent Protection Mode and then lock the Secured Silicon Sector at separate instances and time frames.

- Secured Silicon Sector Protection allows the user to lock the Secured Silicon Sector area

- Persistent Protection Mode Lock Bit allows the user to set the device permanently to operate in the Persistent Protection Mode
- Password Protection Mode Lock Bit allows the user to set the device permanently to operate in the Password Protection Mode

Table 6. Lock Register

DQ15-3	DQ2	DQ1	DQ0
Don't Care	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Dynamically Locked**-The sector is protected and can be changed by a simple command
- **Persistently Locked**-A sector is protected and cannot be changed
- **Unlocked**-The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" are going to be used:

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYB bits are in the "unprotected state". Each DYB is individually modifiable through the DYB Set Command and DYB Clear Command. When the parts are first shipped, all of the Persistent Protect Bits (PPB) are cleared into the unprotected state. The DYB bits and PPB Lock bit are defaulted to power up in the cleared state or unprotected state - meaning the all PPB bits are changeable.

The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPB bits cleared, the DYB bits control whether or not the sector is protected or unprotected. By issuing the DYB Set and DYB Clear command sequences, the DYB bits will be protected or unprotected, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and un-protected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

The DYB bits maybe set or cleared as often as needed. The PPB bits allow for a more static, and difficult to change, level of protection. The PPB bits retain their state across power cycles because they are Non-Volatile. Individual PPB bits are set with a program command but must all be cleared as a group through an erase command.

The PPB Lock Bit adds an additional level of protection. Once all PPB bits are programmed to the desired settings, the PPB Lock Bit may be set to the "freeze state". Setting the PPB Lock Bit to the "freeze state" disables all program and erase commands to the Non-Volatile PPB bits. In effect, the PPB Lock Bit locks the PPB bits into their current state. The only way to clear the PPB Lock Bit to the

"unfreeze state" is to go through a power cycle, or hardware reset. The Software Reset command will not clear the PPB Lock Bit to the "unfreeze state". System boot code can determine if any changes to the PPB bits are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock Bit to disable any further changes to the PPB bits during system operation.

The WP# write protect pin adds a final level of hardware protection. When this pin is low it is not possible to change the contents of the WP# protected sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set and DYB Clear commands for the dynamic sectors switch the DYB bits to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be disabled to the "unfreeze state" by either putting the device through a power-cycle, or hardware reset. The PPB bits can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again to the "freeze state" will lock the PPB bits, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to each sector. If a PPB is programmed to the protected state through the "PPB Program" command, that sector will be protected from program or erase operations will be read-only. If a PPB requires erasure, all of the sector PPB bits must first be erased in parallel through the "All PPB Erase" command. The "All PPB Erase" command will preprogrammed all PPB bits prior to PPB erasing. All PPB bits erase in parallel, unlike programming where individual PPB bits are programmable. The PPB bits have the same endurance as the flash memory.

Programming the PPB bit requires the typical word programming time without utilizing the Write Buffer. During a PPB bit programming and A11 PPB bit erasing sequence execution, the DQ6 Toggle Bit I will toggle until the programming of the PPB bit or erasing of all PPB bits has completed to indicate programming and erasing status. Erasing all of the PPB bits at once requires typical sector erase time. During the erasing of all PPB bits, the DQ3 Sector Erase Timer bit will output a 1 to indicate the erasure of all PPB bits are in progress. When the erasure of all PPB bits has completed, the DQ3 Sector Erase Timer bit will output a 0 to indicate that all PPB bits have been erased. Reading the PPB Status bit requires the initial access time of the device.

Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. When set to the "freeze state", the PPB bits cannot be changed. When cleared to the "unfreeze state", the PPB bits are changeable. There is only one PPB Lock Bit per device. The PPB Lock Bit is cleared to the "un-

freeze state" after power-up or hardware reset. There is no command sequence to unlock or "unfreeze" the PPB Lock Bit.

Configuring the PPB Lock Bit to the freeze state requires approximately 100ns. Reading the PPB Lock Status bit requires the initial access time of the device.

Table 7. Sector Protection Schemes

Protection States			Sector State
DYB Bit	PPB Bit	PPB Lock Bit	
Unprotect	Unprotect	Unfreeze	Unprotected – PPB and DYB are changeable
Unprotect	Unprotect	Freeze	Unprotected – PPB not changeable, DYB is changeable
Unprotect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Unprotect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Unprotect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Unprotect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable

Table 7 contains all possible combinations of the DYB bit, PPB bit, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB bit is set, and the PPB Lock Bit is set, the sector is protected and the protection cannot be removed until the next power cycle or hardware reset clears the PPB Lock Bit to "unfreeze state". If the PPB bit is cleared, the sector can be dynamically locked or unlocked. The DYB bit then controls whether or not the sector is protected or unprotected. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector. The programming of the DYB bit, PPB bit, and PPB Lock Bit for a given sector can be verified by writing a DYB Status Read, PPB Status Read, and PPB Lock Status Read commands to the device.

The Autoselect Sector Protection Verification outputs the OR function of the DYB bit and PPB bit per sector basis. When the OR function of the DYB bit and PPB bit is a 1, the sector is either protected by DYB or PPB or both. When the OR function of the DYB bit and PPB bit is a 0, the sector is unprotected through both the DYB and PPB.

Persistent Protection Mode Lock Bit

Like the Password Protection Mode Lock Bit, a Persistent Protection Mode Lock Bit exists to guarantee that the device remain in software sector protection. Once programmed, the Persistent Protection Mode Lock Bit prevents programming of the Password Protection Mode Lock Bit. This guarantees that a hacker could not place the device in Password Protection Mode. The Password Protection Mode Lock Bit resides in the "Lock Register".

Password Sector Protection

The Password Sector Protection method allows an even higher level of security than the Persistent Sector Protection method. There are two main differences between the Persistent Sector Protection and the Password Sector Protection methods:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock Bit is set to the locked state, or the freeze state, rather than cleared to the unlocked state, or the unfreeze state.
- The only means to clear and unfreeze the PPB Lock Bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a one-time programmable (OTP) region outside of the flash memory. Once the Password Protection Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear and unfreeze the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared to the "unfreezed state", and the PPB bits can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check" after the valid 64-bit password has been entered for the PPB Lock Bit to be cleared to the "unfreezed state". This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Protection Mode Lock Bit

In order to select the Password Sector Protection method, the customer must first program the password. The factory recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Read operations. Once the desired password is programmed in, the customer must then set the Password Protection Mode Lock Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when programming the Password Protection Mode Lock Bit. More importantly, the user must be sure that the password is correct when the Password Protection Mode Lock Bit is programmed. Due to the fact that read operations are disabled, there is no means to read what the password is afterwards. If the password is lost after programming the Password Protection Mode Lock Bit, there will be no way to clear and unfreeze the PPB Lock Bit. The Password Protection Mode Lock Bit, once programmed, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Protection Mode Lock Bit is not erasable. Once Password Protection Mode Lock Bit is

programmed, the Persistent Protection Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Password Read commands. The password function works in conjunction with the Password Protection Mode Lock Bit, which when programmed, prevents the Password Read command from reading the contents of the password on the pins of the device.

Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. The PPB Lock Bit is a volatile bit that reflects the state of the Password Protection Mode Lock Bit after power-up reset. If the Password Protection Mode Lock Bit is also programmed after programming the Password, the Password Unlock command must be issued to clear and unfreeze the PPB Lock Bit after a hardware reset (RESET# asserted) or a power-up reset. Successful execution of the Password Unlock command clears and unfreezes the PPB Lock Bit, allowing for sector PPB bits to be modified. Without issuing the Password Unlock command, while asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a the "freeze state".

If the Password Protection Mode Lock Bit is not programmed, the device defaults to Persistent Protection Mode. In the Persistent Protection Mode, the PPB Lock Bit is cleared to the "unfreeze state" after power-up or hardware reset. The PPB Lock Bit is set to the "freeze state" by issuing the PPB Lock Bit Set command. Once set to the "freeze state" the only means for clearing the PPB Lock Bit to the "unfreeze state" is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Reading the PPB Lock Bit requires a 200ns access time.

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 bytes in length, and uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the Secured Silicon Sector either customer lockable (standard shipping option) or factory locked (contact an AMD sales representative for ordering information). The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the Secured Silicon Sector Indicator Bit permanently set to a "0." The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a "1." Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

The Secured Silicon sector address space in this device is allocated as follows:

Secured Silicon Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the Secured Silicon Sector through a command sequence (see "Write Protect (WP#)"). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: Secured Silicon Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte Secured Silicon sector.

The system may program the Secured Silicon Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See "Command Definitions" .

Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: Secured Silicon Sector Programmed and Protected At the Factory

In devices with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the factory through the ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from the factory with the Secured Silicon Sector permanently locked. Contact your sales representative for details on using the ExpressFlash service.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector group without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector group independently of whether those sector groups were protected or unprotected using the method described in"Advanced Sector Protection" section on page 115. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in "DC Characteristics" section on page 151.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotection". *Note that WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 12 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can

then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8-11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8–11. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact your sales representative for copies of these documents.

Table 8. CFI Query Identification String

Addresses (x16)	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9. System Interface String

Addresses (x16)	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0007h	Typical timeout per single byte/word write 2^N µs
20h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0001h	Max. timeout for byte/word write 2^N times typical
24h	0005h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table I0. Device Geometry Definition

Addresses (x16)	Data	Description
27h	001Ah 0019h 0018h	Device Size = 2^N byte 1A = 512 Mb, 19 = 256 Mb, 18 = 128 Mb
28h 29h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	00xxh 000xh 0000h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) 00FFh, 001h, 0000h, 0002h = 512 Mb 00FFh, 0000h, 0000h, 0002h = 256 Mb 007Fh, 0000h, 0000h, 0002h = 128 Mb
31h 32h 33h 34h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table II. Primary Vendor-Specific Extended Query

Addresses (x16)	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0010h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0100b = 110 nm MirrorBit
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0008h	Sector Protect/Unprotect scheme 0008h = Advanced Sector Protection
4Ah	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	00xxh	WP# Protection 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12 defines the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations–"AC Characteristics" section provides the read parameters, and Figure 11 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 12 shows the address and data requirements. This method is an alternative to that shown in Table 5, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an

address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- Three read cycles at addresses 01h, 0Eh, and 0Fh return the device code.
- A read cycle to an address containing a sector address (SA), and the address 02h on A7–A0 in word mode returns 01h if the sector is protected, or 00h if it is unprotected.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table 12 shows the address and data requirements for both command sequences. See also "Secured Silicon Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 12 shows the address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. ***Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*** Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence of address locations and across sector boundaries. Programming to the same word address multiple times without intervening erases (incremental bit programming) requires a modified programming method. For such application requirements, please contact your

local Spansion representative. Word programming is supported for backward compatibility with existing Flash driver software and for occasional writing of individual words. Use of Write Buffer Programming is strongly recommended for general programming use when more than a few words are to be programmed. The effective word programming time using Write Buffer Programming is much shorter than the single word programming time. **Any word cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 12).

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.)

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

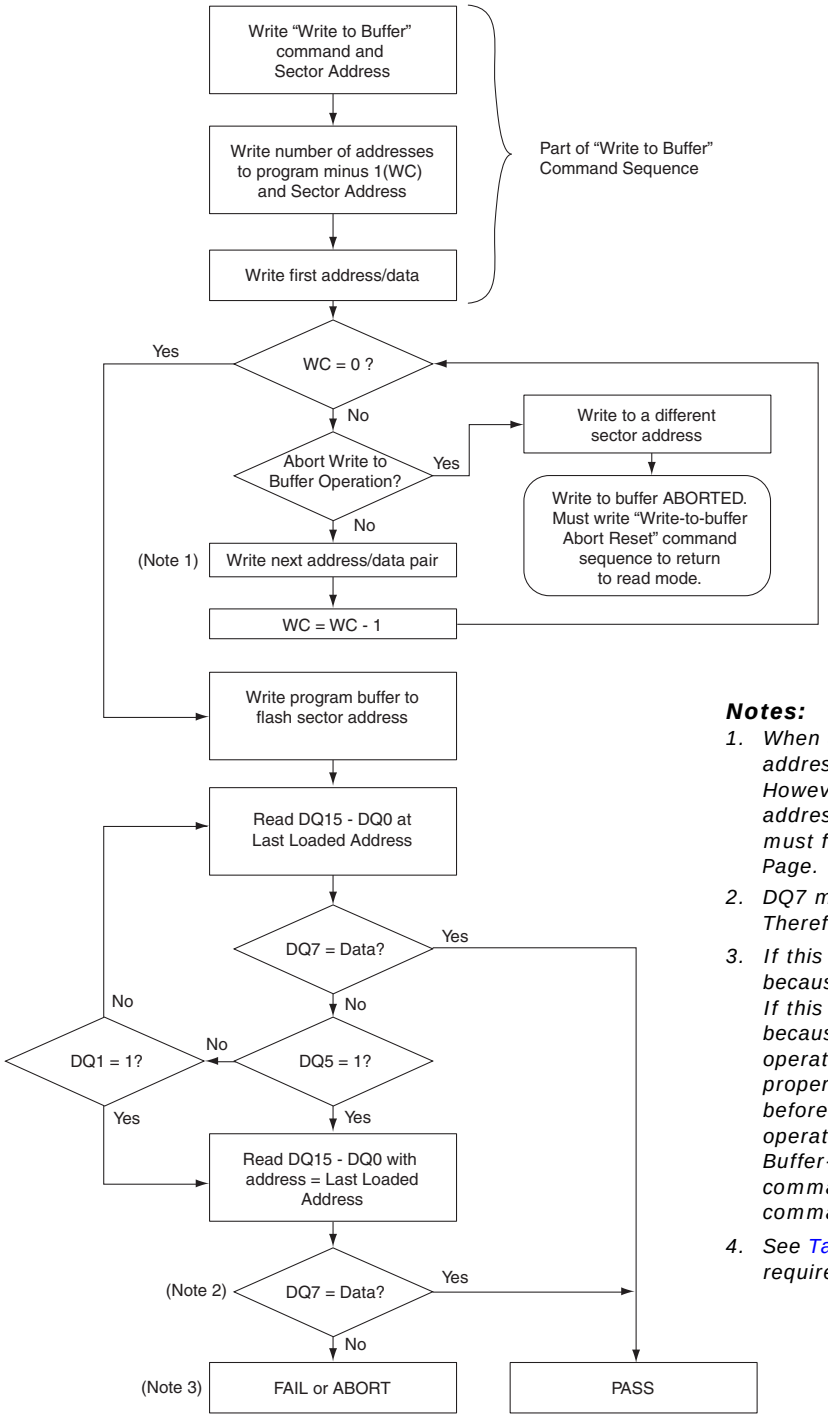
Write buffer programming is allowed in any sequence. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress. This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring incremental bit programming, a modified programming method is required, please contact your local Spansion representative. **Any bit in a write buffer address range cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not*

be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.

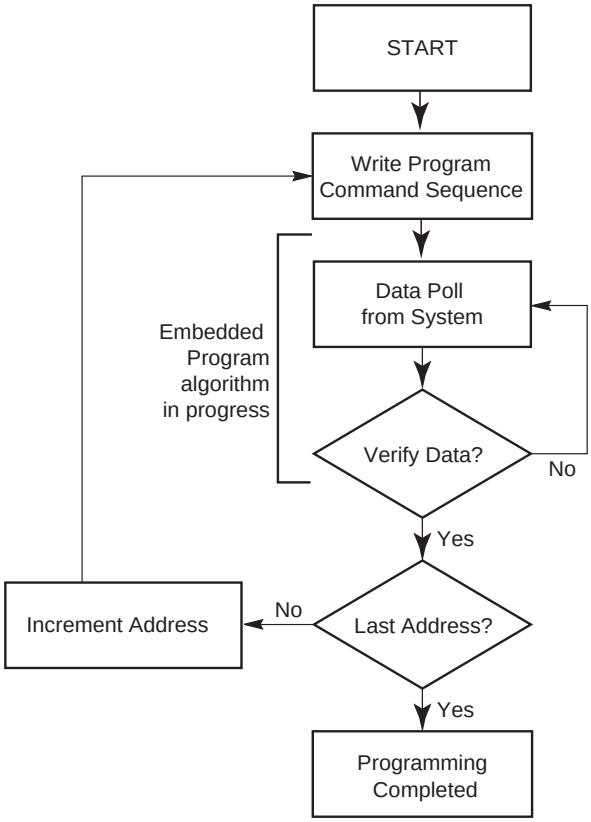
Figure 2 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations–"AC Characteristics" section for parameters, and Figure 14 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Table 12 for command sequences required for write buffer programming.*

Figure I. Write Buffer Programming Operation



Note: *See Table 12 for program command sequence.*

Figure 2. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 μs maximum (5μs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region. *Note that the Secured Silicon Sector autoselect, and CFI functions are unavailable when program operation is in progress.*

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

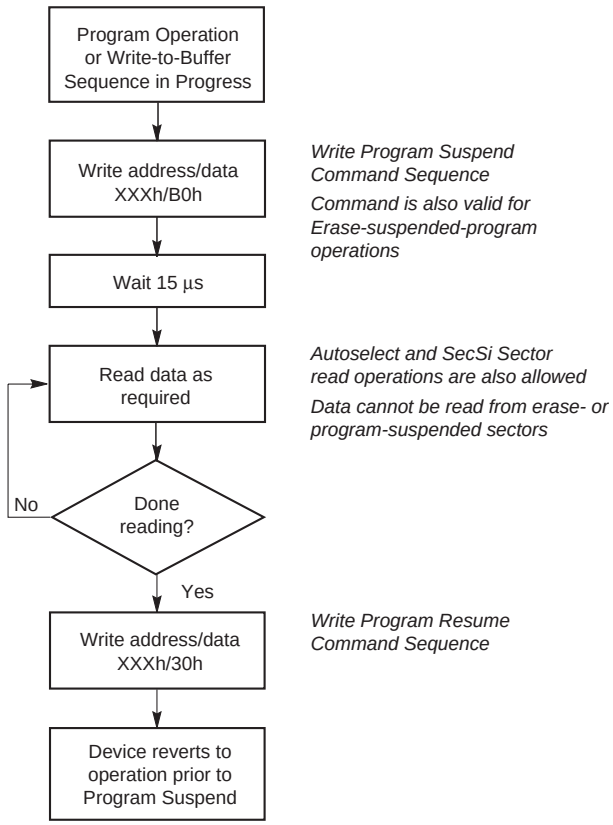


Figure 3. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 12 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored, including erase suspend commands. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. ***Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*** Refer to the "Erase And Programming Performance" section on page 163 in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 12 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

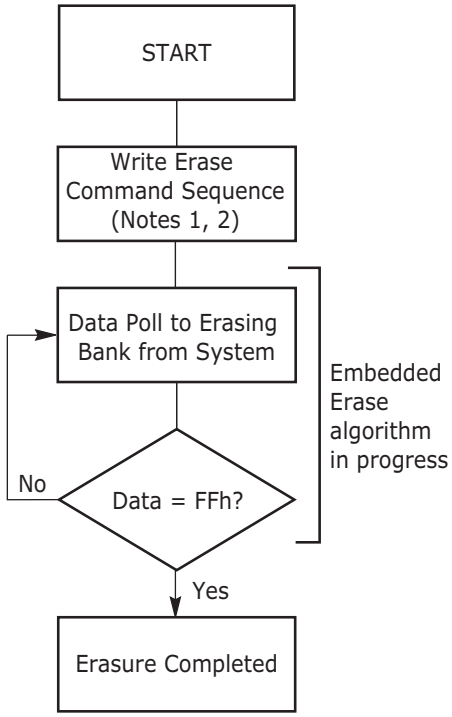
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** ***Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.



Notes:

1. *See Table 12 for program command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the pro-

gram operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Autoselect Mode" section and "Autoselect Command Sequence" section on page 127 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing. It is important to allow an interval of at least 5 ms between Erase Resume and Erase Suspend.

Lock Register Command Set Definitions

The Lock Register Command Set permits the user to one-time program the Secured Silicon Sector Protection Bit, Persistent Protection Mode Lock Bit, and Password Protection Mode Lock Bit. The Lock Register bits are all readable after an initial access delay.

The **Lock Register Command Set Entry** command sequence must be issued prior to any of the following commands listed, to enable proper command execution.

Note that issuing the **Lock Register Command Set Entry** command **disables reads and writes for the flash memory**.

- Lock Register Program Command
- Lock Register Read Command

The **Lock Register Command Set Exit** command must be issued after the execution of the commands to reset the device to read mode. Otherwise the device will hang. If this happens, the flash device must be reset. Please refer to RESET# for more information. It is important to note that the device will be in either Persistent Protection mode or Password Protection mode depending on the mode selected prior to the device hang.

For either the Secured Silicon Sector to be locked, or the device to be permanently set to the Persistent Protection Mode or the Password Protection Mode, the associated Lock Register bits must be programmed. **Note that the Persistent Protection Mode Lock Bit and Password Protection Mode Lock Bit can never be programmed together at the same time. If so, the Lock Register Program operation will abort**.

The Lock Register Command Set Exit command must be initiated to re-enable reads and writes to the main memory.

Password Protection Command Set Definitions

The Password Protection Command Set permits the user to program the 64-bit password, verify the programming of the 64-bit password, and then later unlock the device by issuing the valid 64-bit password.

The **Password Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Password Protection Command Set Entry** command **disabled reads and writes the main memory.**

- **Password Program Command**
- **Password Read Command**
- **Password Unlock Command**

The Password Program command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. There is no special addressing order required for programming the password. **The password is programmed in 8-bit or 16-bit portions. Each portion requires a Password Program Command.**

Once the Password is written and verified, the Password Protection Mode Lock Bit in the "Lock Register" must be programmed in order to prevent verification. The Password Program command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password.

The Password Read command is used to verify the Password. The Password is verifiable only when the Password Protection Mode Lock Bit in the "Lock Register" is not programmed. If the Password Protection Mode Lock Bit in the "Lock Register" is programmed and the user attempts to read the Password, the device will always drive all F's onto the DQ databus.

The lower two address bits (A1–A0) for word mode and (A1–A-1) for by byte mode are valid during the Password Read, Password Program, and Password Unlock commands. **Writing a "1" to any other address bits (A_{MAX}-A2) will abort the Password Read and Password Program commands.**

The Password Unlock command is used to clear the PPB Lock Bit to the "unfreeze state" so that the PPB bits can be modified. The exact password must be entered in order for the unlocking function to occur. **This 64-bit Password Unlock command sequence will take at least 2 µs to process each time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match the password. If another password unlock is issued before the 64-bit password check execution window is completed, the command will be ignored. If the wrong address or data is given during password unlock command cycle, the device may enter the write-to-buffer abort state. In order to exit the write-to-abort state, the write-to-buffer-abort-reset command must be given. Otherwise the device will hang.**

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit to the "unfreeze state". The password is 64 bits long. A1 and A0 are used for matching. Writing the Password Unlock command does not need to be address order specific. An example sequence is starting with the lower address A1-A0=00, followed by A1-A0=01, A1-A0=10, and A1-A0=11 if the device is configured to operate in word mode.

Approximately 2 µs is required for unlocking the device after the valid 64-bit password is given to the device. It is the responsibility of the microprocessor to keep track of the entering the portions of the 64-bit password with the Password Unlock command, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to re-lock the device into the Password Protection Mode, the PPB Lock Bit Set command can be re-issued.

The **Password Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode. Otherwise the device will hang.
Note that issuing the **Password Protection Command Set Exit command re-enables reads and writes for the main memory.**

Non-Volatile Sector Protection Command Set Definitions

The Non-Volatile Sector Protection Command Set permits the user to program the Persistent Protection Bits (PPB bits), erase all of the Persistent Protection Bits (PPB bits), and read the logic state of the Persistent Protection Bits (PPB bits).

The **Non-Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Non-Volatile Sector Protection Command Set Entry** command **disables reads and writes for the main memory**.

- PPB Program Command

The PPB Program command is used to program, or set, a given PPB bit. Each PPB bit is individually programmed (but is bulk erased with the other PPB bits). The specific sector address (A24-A16 for S29GL512N, A23-A16 for S29GL256N, A22-A16 for S29GL128N) is written at the same time as the program command. If the PPB Lock Bit is set to the "freeze state", the PPB Program command will not execute and the command will time-out without programming the PPB bit.

- All PPB Erase Command

The All PPB Erase command is used to erase all PPB bits in bulk. There is no means for individually erasing a specific PPB bit. Unlike the PPB program, no specific sector address is required. However, when the All PPB Erase command is issued, all Sector PPB bits are erased in parallel. If the PPB Lock Bit is set to "freeze state", the ALL PPB Erase command will not execute and the command will time-out without erasing the PPB bits.

The device will preprogram all PPB bits prior to erasing when issuing the All PPB Erase command. Also note that the total number of PPB program/erase cycles has the same endurance as the flash memory array.

- PPB Status Read Command

The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device. This requires an initial access time latency.

The **Non-Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Non-Volatile Sector Protection Command Set Exit** command **re-enables reads and writes for the main memory**.

Global Volatile Sector Protection Freeze Command Set

The Global Volatile Sector Protection Freeze Command Set permits the user to set the PPB Lock Bit and reading the logic state of the PPB Lock Bit.

The **Global Volatile Sector Protection Freeze Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Reads and writes from the main memory are not allowed.

- PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock Bit to the "freeze state" if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set to the "freeze state", it cannot be cleared unless the device is taken through a power-on clear (for Persistent Protection Mode) or the Password Unlock command is executed (for Password Protection Mode). If the Password Protection Mode Lock Bit is programmed, the PPB Lock Bit status is reflected as set to the "freeze state", even after a power-on reset cycle.

- PPB Lock Bit Status Read Command

The programming state of the PPB Lock Bit can be verified by executing a PPB Lock Bit Status Read command to the device.

The **Global Volatile Sector Protection Freeze Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB) to the "protected state", clear the Dynamic Protection Bit (DYB) to the "unprotected state", and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Volatile Sector Protection Command Set Entry** command **disables reads and writes from main memory**.

- DYB Set Command
- DYB Clear Command

The DYB Set and DYB Clear commands are used to protect or unprotect a DYB for a given sector. The high order address bits are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYB bits are modifiable at any time, regardless of the state of the PPB bit or PPB Lock Bit. The DYB bits are cleared to the "unprotected state" at power-up or hardware reset.

—DYB Status Read Command

The programming state of the DYB bit for a given sector can be verified by writing a DYB Status Read command to the device. This requires an initial access delay.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Volatile Sector Protection Command Set Exit command re-enables reads and writes to the main memory**.

Secured Silicon Sector Entry Command

The Secured Silicon Sector Entry command allows the following commands to be executed

- Read from Secured Silicon Sector
- Program to Secured Silicon Sector

Once the Secured Silicon Sector Entry Command is issued, the Secured Silicon Sector Exit command has to be issued to exit Secured Silicon Sector Mode.

Secured Silicon Sector Exit Command

The Secured Silicon Sector Exit command may be issued to exit the Secured Silicon Sector Mode.

Command Definitions

Table 12. S29GL512N, S29GL256N, S29GL128N Command Definitions, x16

Command (Notes)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID	4	555	AA	2AA	55	555	90	X01	227E	X0E	Note 17	X0F	Note 17
	Sector Protect Verify	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
										XX01				
	Secure Device Verify (9)	4	555	AA	2AA	55	555	90	X03	Note 10				
CFI Query (11)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash (confirm)		1	SA	29										
Write-to-Buffer-Abort Reset (16)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (12)		2	XXX	A0	PA	PD								
Unlock Bypass Sector Erase (12)		2	XXX	80	SA	30								
Unlock Bypass Chip Erase (12)		2	XXX	80	XXX	10								
Unlock Bypass Reset (13)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend (14)		1	XXX	B0										
Erase Resume/Program Resume (15)		1	XXX	30										
Sector Command Definitions														
Secured Silicon SEctor	Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88						
	Secured Silicon Sector Exit (18)	4	555	AA	2AA	55	555	90	XX	00				
Lock Register Command Set Definitions														
Lock Register	Lock Register Command Set Entry	3	555	AA	2AA	55	555	40						
	Lock Register Bits Program (22)	2	XXX	A0	XXX	Data								
	Lock Register Bits Read (22)	1	00	Data										
	Lock Register Command Set Exit (18, 23)	2	XXX	90	XXX	00								
Password Protection Command Set Definitions														

Command (Notes)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Password	Password Protection Command Set Entry	3	555	AA	2AA	55	555	60						
	Password Program (20)	2	XXX	A0	PWA x	PWD x								
	Password Read (19)	4	XXX	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3				
	Password Unlock (19)	7	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			00	29										
	Password Protection Command Set Exit (18, 23)	2	XXX	90	XXX	00								
Non-Volatile Sector Protection Command Set Definitions														
PPB	Nonvolatile Sector Protection Command Set Entry	3	555	AA	2AA	55	555	C0						
	PPB Program (24, 25)	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read (25)	1	SA	RD (0)										
	Non-Volatile Sector Protection Command Set Exit (18)	2	XXX	90	XXX	00								
Global Non-Volatile Sector Protection Freeze Command Set Definitions														
PPB Lock Bit	Global Non-Volatile Sector Protection Freeze Command Set Entry	3	555	AA	2AA	55	555	50						
	PPB Lock Bit Set (25)	2	XXX	A0	XXX	00								
	PPB Lock Status Read (25)	1	XXX	RD (0)										
	Global Non-Volatile Sector Protection Freeze Command Set Exit (18)	2	XXX	90	XXX	00								
Volatile Sector Protection Command Set Definitions														
DYB	Volatile Sector Protection Command Set Entry	3	555	AA	2AA	55	555	E0						
	DYB Set (24, 25)	2	XXX	A0	SA	00								
	DYB Clear (25)	2	XXX	A0	SA	01								
	DYB Status Read (25)	1	SA	RD (0)										
	Volatile Sector Protection Command Set Exit (18)	2	XXX	90	XXX	00								

Legend:

X = Don't care

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A_{max}–A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same write buffer page as PA.

WC = Word Count is the number of write buffer locations to load minus 1.

PWD = Password

PWD_x = Password word0, word1, word2, and word3.

DATA = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle, and the 4th, 5th, and 6th cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15-DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A_{MAX}:A16 are don't cares for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth, fifth, and sixth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.*
10. *The data value for DQ7 is "1" for a serialized and protected OTP region and "0" for an unserialized and unprotected Secured Silicon Sector region. See "Secured Silicon Sector Flash Memory Region" for more information. For S29GLxxxNH: XX18h/18h = Not Factory Locked. XX98h/98h = Factory Locked. For S29GLxxxNL: XX08h/08h = Not Factory Locked. XX88h/88h = Factory Locked.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock-Bypass command is required prior to the Unlock-Bypass-Program command.*
13. *The Unlock-Bypass-Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
14. *The system may read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
16. *Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. NOTE: the full command sequence is required if resetting out of ABORT while using Unlock Bypass Mode.*
17. *S29GL512NH/L = 2223h/23h, 2201h/01h; S29GL256NH/L = 2222h/22h, 2201h/01h; S29GL128NH/L = 2221h/21h, 2201h/01h.*
18. *The Exit command returns the device to reading the array.*
19. *Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
20. *For PWDx, only one portion of the password can be programmed per each "A0" command.*
21. *The All PPB Erase command embeds programming of all PPB bits before erasure.*
22. *All Lock Register bits are one-time programmable. Note that the program state = "0" and the erase state = "1". Also note that of both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation will abort and return the device to read mode. Lock Register bits that are reserved for future use will default to "1's". The Lock Register is shipped out as "FFFF's" before Lock Register Bit program execution.*
23. *If any of the Entry command was initiated, an Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
24. *If ACC = V_{HH}, sector protection will match when ACC = V_{IH}*
25. *Protected State = "00h", Unprotected State = "01h".*

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 13 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

Note that all Write Operation Status DQ bits are valid only after 4 µs delay.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

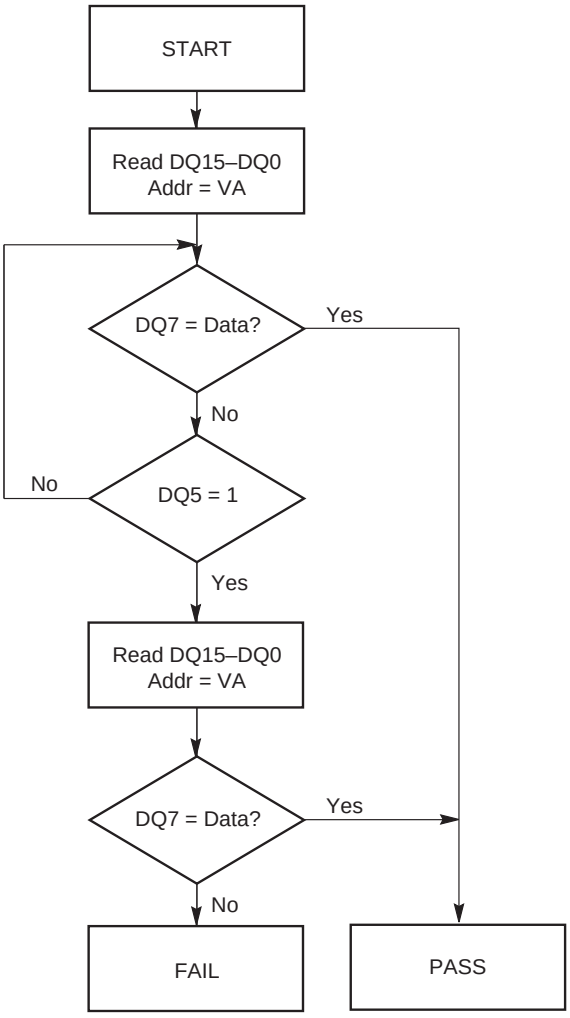
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 13 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 17 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 13 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

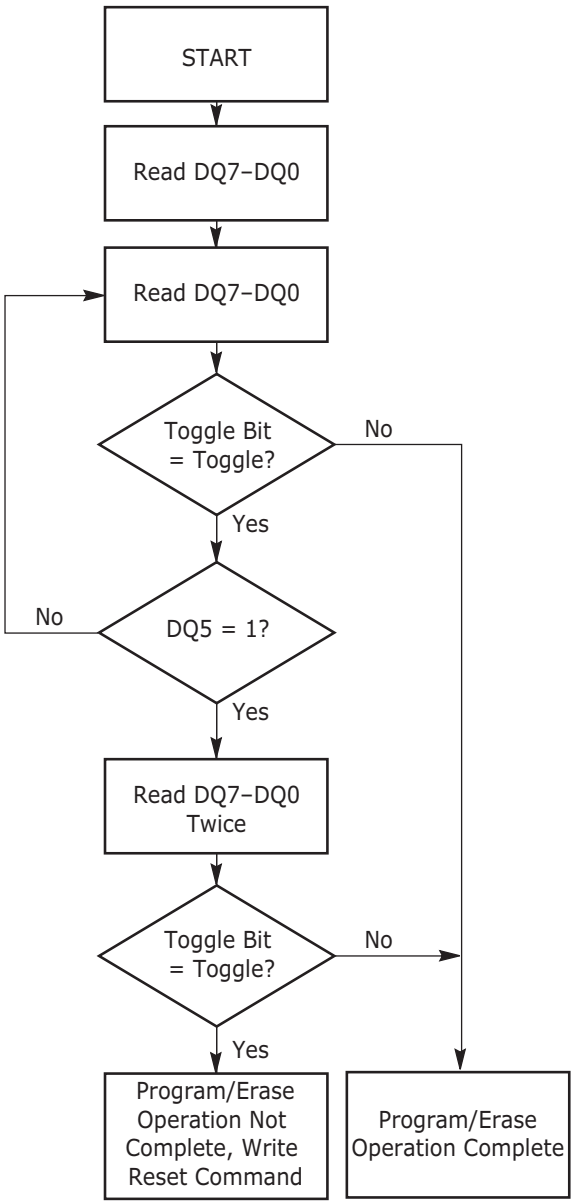
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 13 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 18 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 19 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note:
The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.

Figure 6. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the

read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 13 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the RY/BY#: Ready/Busy# subsection. Figure 18 shows the toggle bit timing diagram. Figure 19 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 and Figure 19 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure,

the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 13 shows the status of DQ3 relative to the other status bits.

DQI: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

Table I3. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to '1' when the device has aborted the write-to-buffer operation.*

Absolute Maximum Ratings

Storage Temperature, Plastic Packages . . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . . −65°C to +125°C

Voltage with Respect to Ground:

- V_{CC} (Note 1) . . . . . −0.5 V to +4.0 V
- V_{IO} . . . . . −0.5 V to +4.0 V
- A9, OE#, and ACC (Note 2) . . . . . −0.5 V to +12.5 V
- All other pins (Note 1) . . . . . −0.5 V to V_{CC} + 0.5V
- Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, and ACC is –0.5 V. During voltage transitions, A9, OE#, and ACC may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9, OE#, and ACC is +12.5 V which may overshoot to +14.0V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

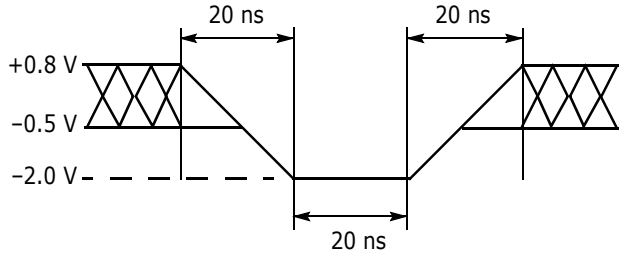


Figure 7. Maximum Negative Overshoot Waveform

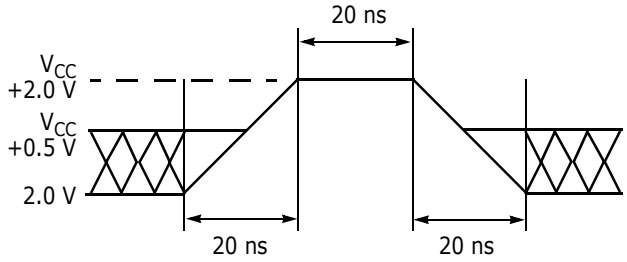


Figure 8. Maximum Positive Overshoot Waveform

Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . −40°C to +85°C

Supply Voltages

V_{CC} . . . . . +2.7 V to +3.6 V or +3.0V to 3.6V

V_{IO} (Note 2) . . . . . +1.65V to 1.95V or VCC

Notes:

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*
2. *See "Product Selector Guide" section on page 80.*

DC Characteristics

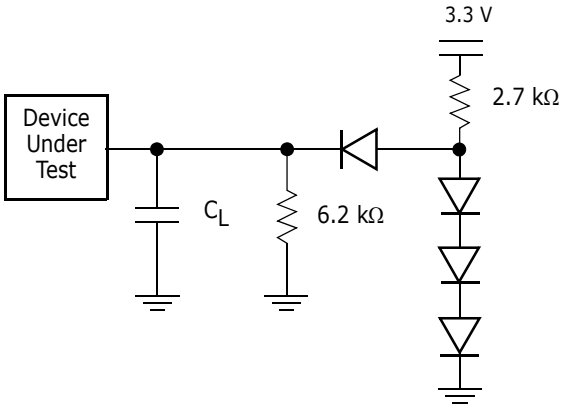
CMOS Compatible-S29GLI28N, S29GL256N, S29GL5I2N

Parameter Symbol	Parameter Description (Notes)	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current (1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			WP/ACC: ±2.0 Others: ±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V			35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (1)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CCmax}$, *f* = 5 MHz		30	50	mA
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CCmax}$, f = 10 MHz		60	90	
I_{CC2}	V_{CC} Intra-Page Read Current (1)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CCmax}$ f = 10 MHz		1	10	mA
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CCmax}$, f=33 MHz		5	20	
I_{CC3}	V_{CC} Active Erase/Program Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CCmax}$		50	80	mA
I_{CC4}	V_{CC} Standby Current	CE#, RESET# = V_{SS} ± 0.3 V, OE# = V_{IH}, $V_{CC} = V_{CCmax}$ $V_{IL} = V_{SS}$ + 0.3 V/-0.1V		1	5	mA
I_{CC5}	V_{CC} Reset Current	$V_{CC} = V_{CCmax}$; $V_{IL} = V_{SS}$ + 0.3 V/-0.1V, RESET# = V_{SS} ± 0.3 V		1	5	µA
I_{CC6}	Automatic Sleep Mode (4)	$V_{CC} = V_{CCmax}$ $V_{IH} = V_{CC}$ ± 0.3 V, $V_{IL} = V_{SS}$ + 0.3 V/-0.1V, WP#/A_{CC} = V_{IH}		1	5	µA
I_{ACC}	ACC Accelerated Program Current	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CCmax}$, WP#/ACC = V_{IH}	WP#/ACC pin	10	20	mA
			V_{CC} pin	50	80	
V_{IL}	Input Low Voltage (5)		–0.1		0.3 x V_{IO}	V
V_{IH}	Input High Voltage (5)		0.7 x V_{IO}		V_{IO} + 0.3	V
V_{HH}	Voltage for ACC Erase/Program Acceleration	V_{CC} = 2.7 –3.6 V	11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V	11.5		12.5	V
V_{OL}	Output Low Voltage (5)	I_{OL} = 100 µA			0.15 x V_{IO}	V
V_{OH}	Output High Voltage (5)	I_{OH} = -100 µA	0.85 x V_{IO}			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (3)		2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.*
3. *Not 100% tested.*
4. *Automatic sleep mode enables the lower power mode when addresses remain stable tor t_{ACC} + 30 ns.*
5. *V_{IO} = 1.65–1.95 V or 2.7–3.6 V*
6. *V_{CC} = 3 V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at 3V.*

Test Conditions



Note: *Diodes are IN3064 or equivalent.*

Figure 9. Test Setup

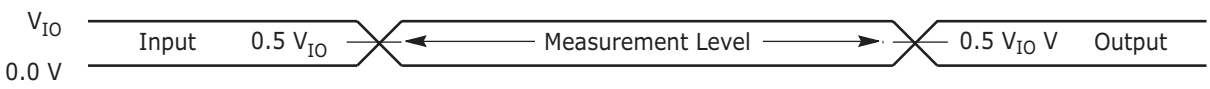
Table 14. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels (See Note)	0.5V_{IO}	V
Output timing measurement reference levels	0.5 V_{IO}	V

Note: *If V_{IO} < V_{CC}, the reference level is 0.5 V_{IO}.*

Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)



Note: *If V_{IO} < V_{CC}, the input measurement reference level is 0.5 V_{IO}.*

Figure 10. Input Waveforms and Measurement Levels

AC Characteristics

Read-Only Operations–S29GLI28N, S29GL256N, S29GL5I2N

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					90	100	110	110	
t_{AVAV}	t_{RC}	Read Cycle Time		$V_{IO} = V_{CC} = 3$ V	Min	90	100	110		ns
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V					110	
t_{AVQV}	t_{ACC}	Address to Output Delay (Note 2)		$V_{IO} = V_{CC} = 3$ V	Max	90	100	110		ns
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V					110	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (Note 3)		$V_{IO} = V_{CC} = 3$ V	Max	90	100	110		ns
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V					110	
	t_{PACC}	Page Access Time			Max	25	25	25	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	25	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
	t_{CEH}	Chip Enable Hold Time	Read		Min	35				ns

Notes:

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}*
3. *OE# = V_{IL}*
4. *See Figure 9 and Table 14 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 90 ns, 100 ns, and 110 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 110 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

AC Characteristics

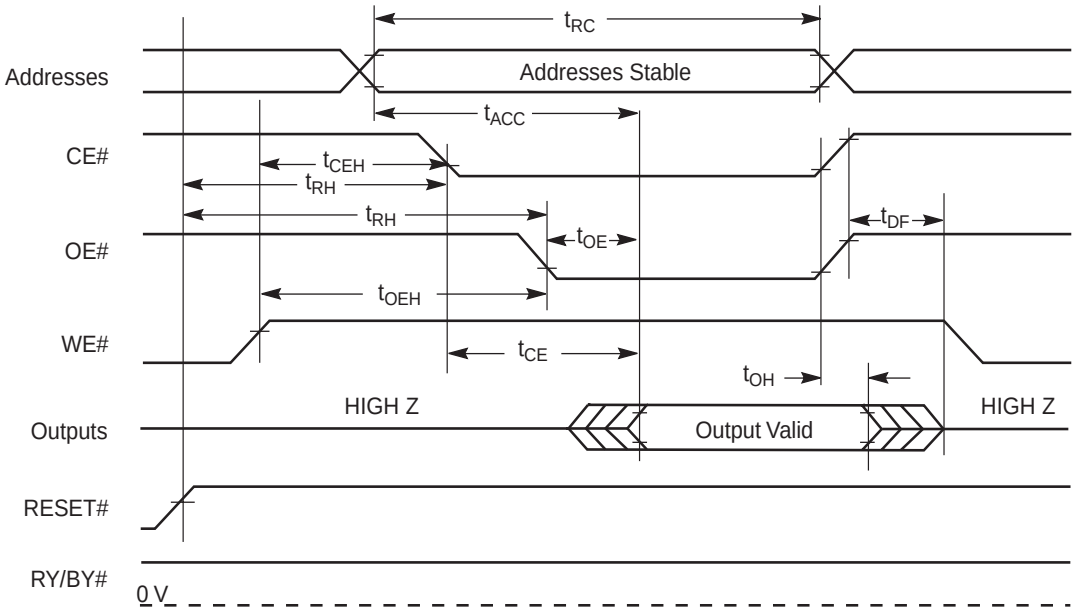
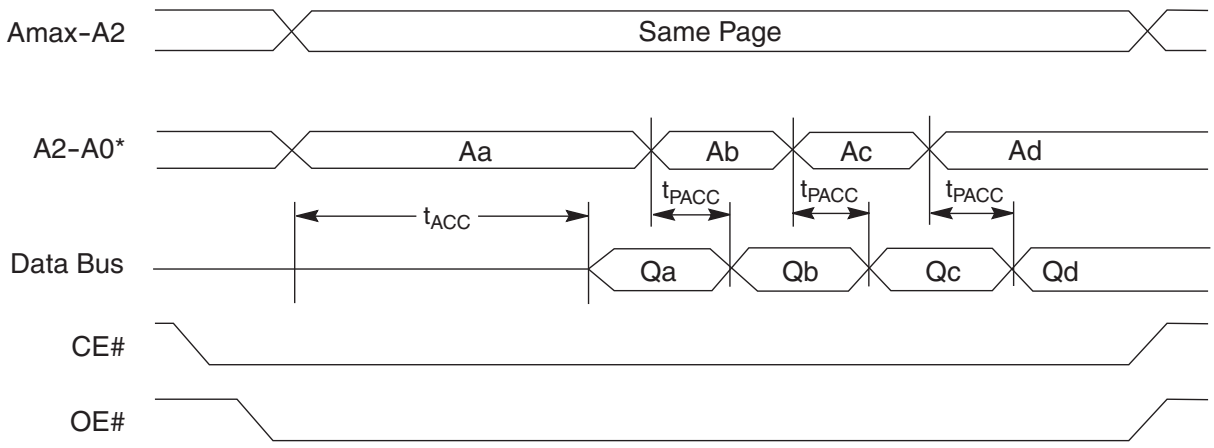


Figure 11. Read Operation Timings



Notes:
1. Figure shows word mode.

Figure 12. Page Read Timings

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description		Speed (Note 2)	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	ns
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Notes:

1. *Not 100% tested. If ramp rate is equal to or faster than 1V/100µs with a falling edge of the RESET# pin initiated, the RESET# pin needs to be held low only for 100µs for power-up.*
2. *Next generation devices may have different reset speeds.*

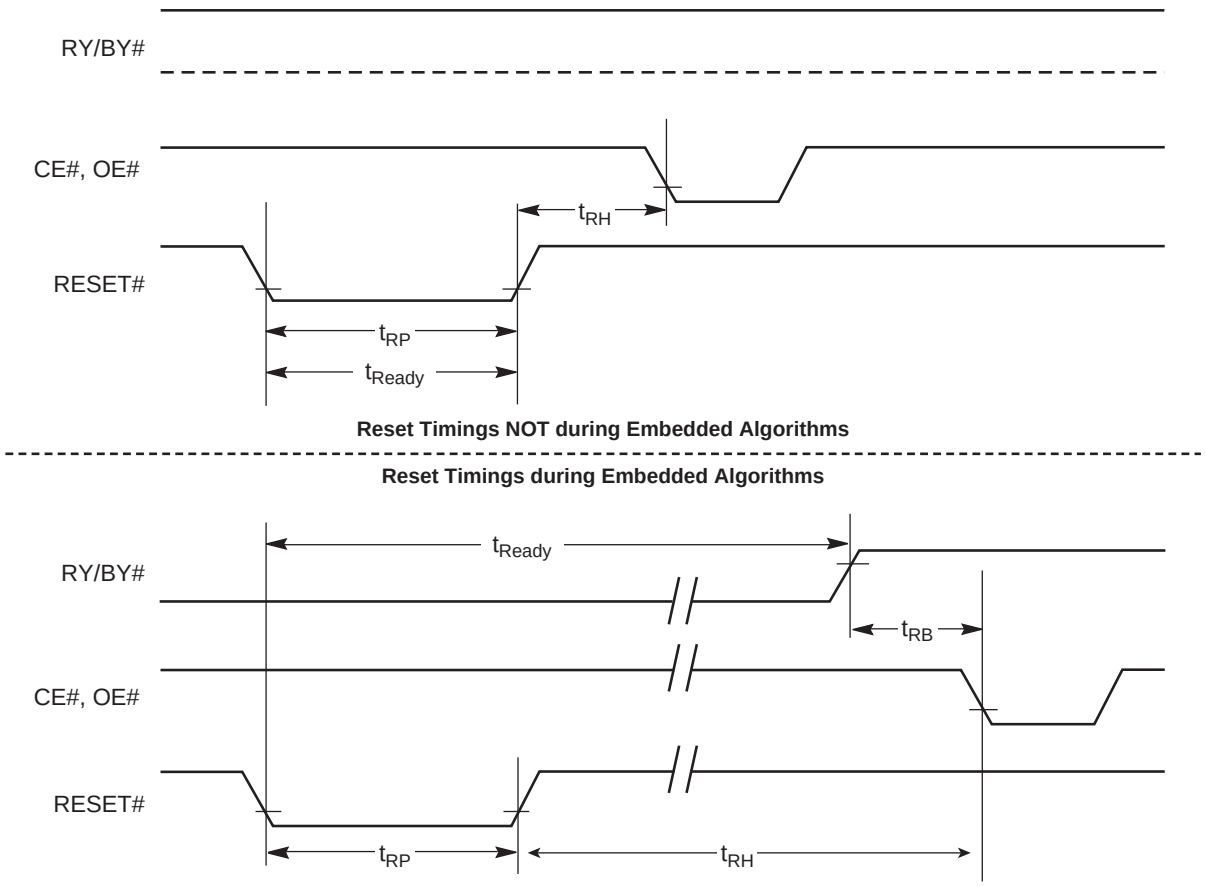


Figure 13. Reset Timings

AC Characteristics

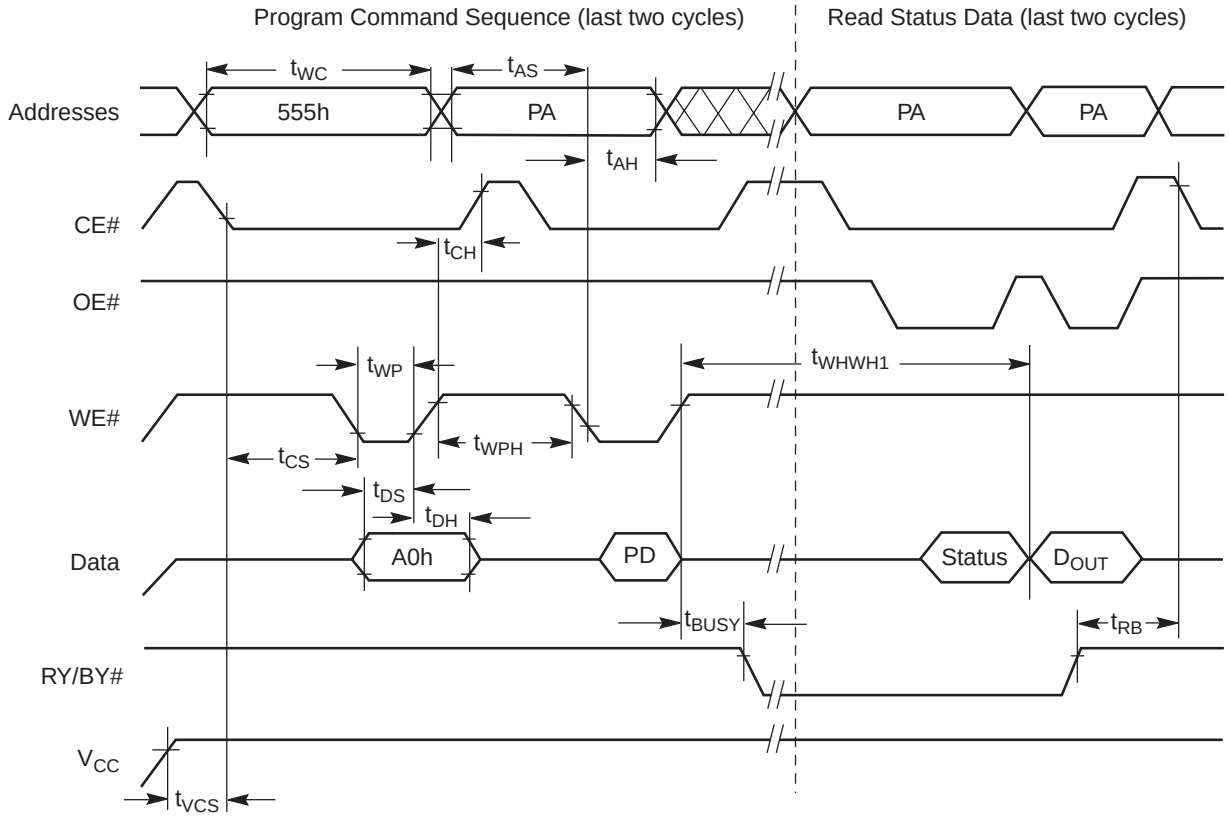
Erase and Program Operations–S29GLl28N, S29GL256N, S29GL5l2N

Parameter					Speed Options				
JEDEC	Std.	Description			90	100	110	110	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	110	110	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45				ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{CEPH}	CE# High during toggle bit polling		Min	20				
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5				sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250				ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				µs
	t_{BUSY}	Erase/Program Valid to RY/BY# Delay		Min	90				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 90 ns, 100 ns, and 110 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 110 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 14. Program Operation Timings

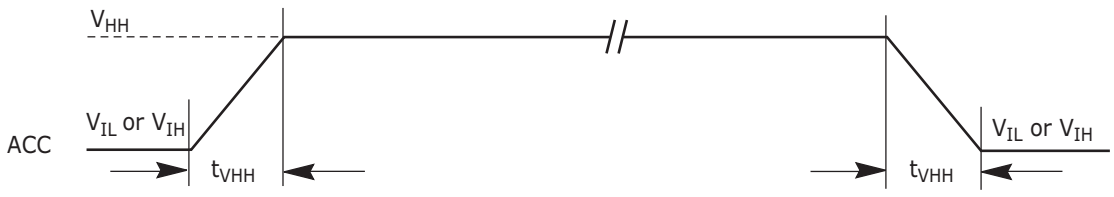
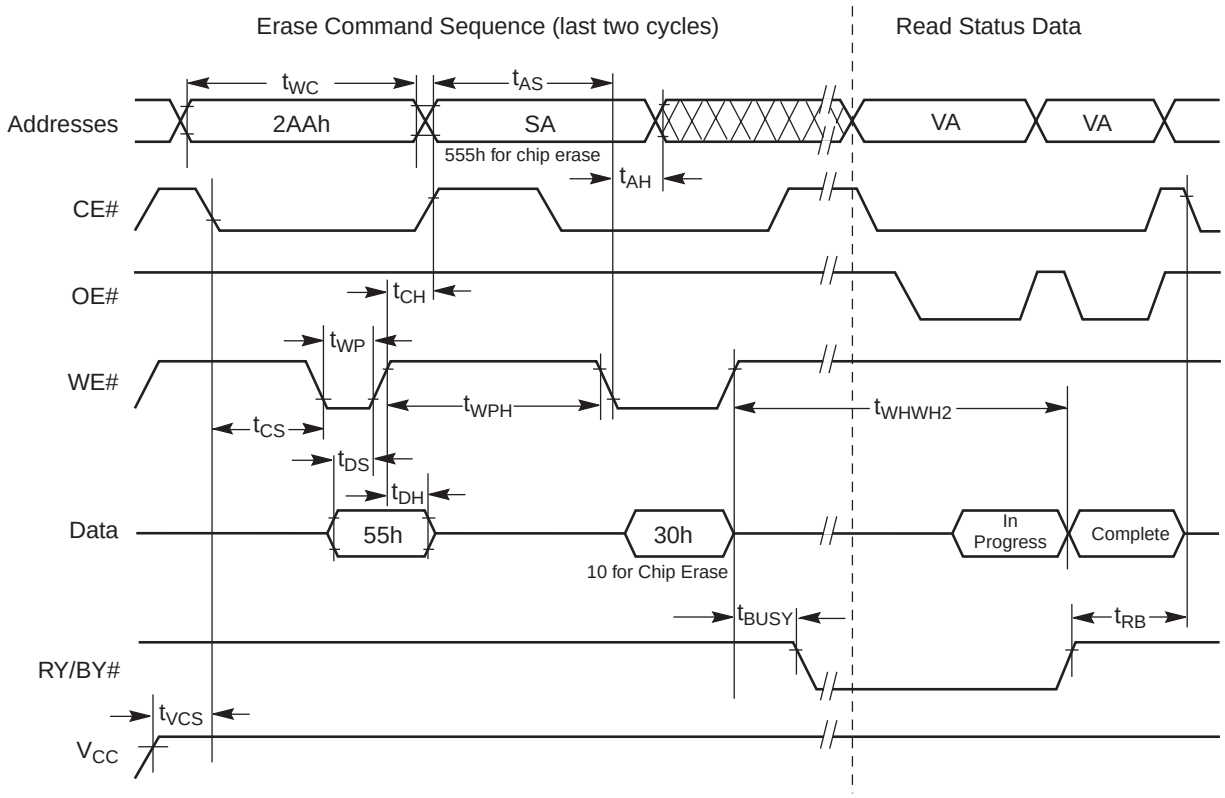


Figure 15. Accelerated Program Timing Diagram

Notes:

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}*
3. *OE# = V_{IL}*
4. *See Figure 9 and Table 14 for test specifications.*

AC Characteristics

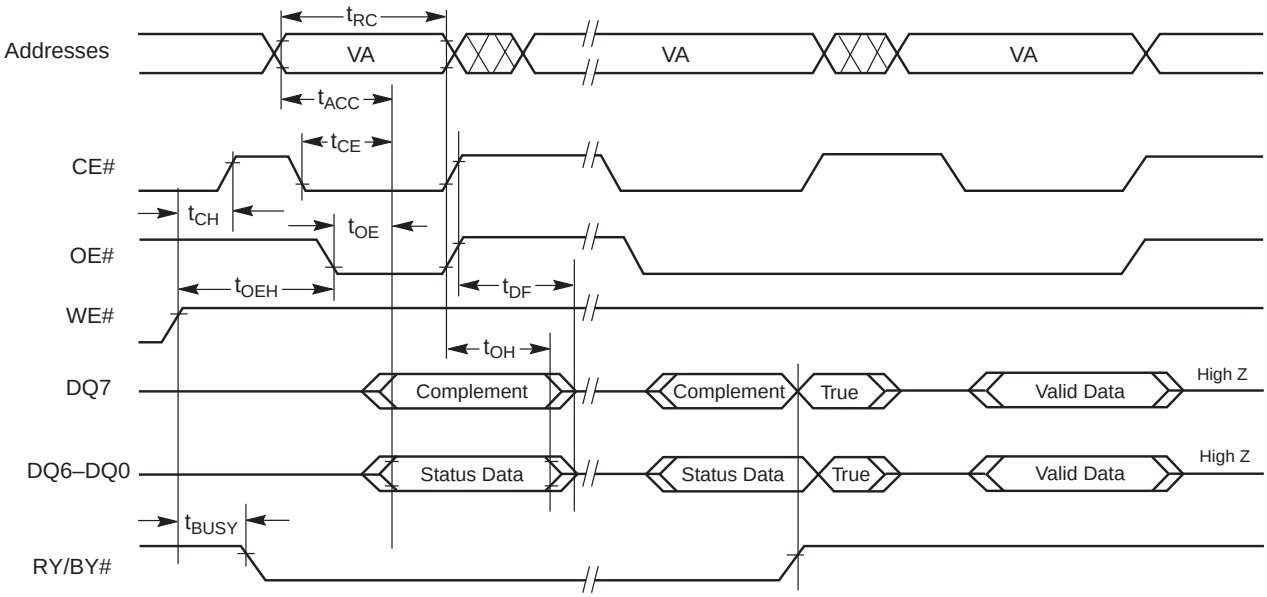


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

Figure 16. Chip/Sector Erase Operation Timings

AC Characteristics

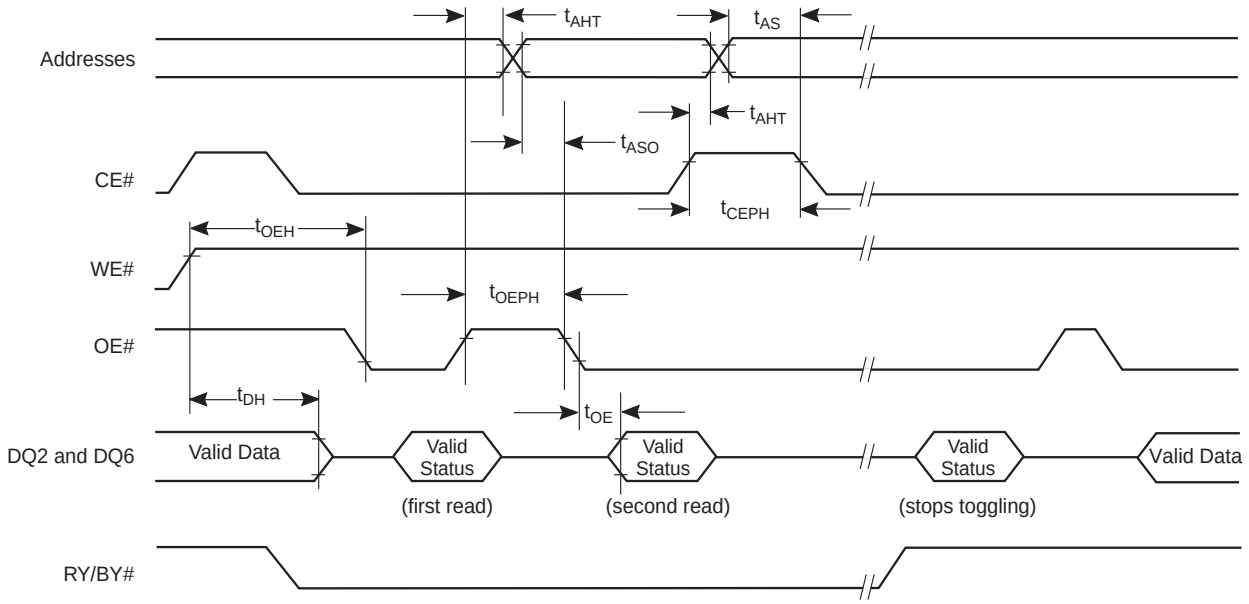


Note:

1. *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*
2. *t_{OE} for data polling is 45 ns when V_{IO} = 1.65 to 2.7 V and is 35 ns when V_{IO} = 2.7 to 3.6 V*

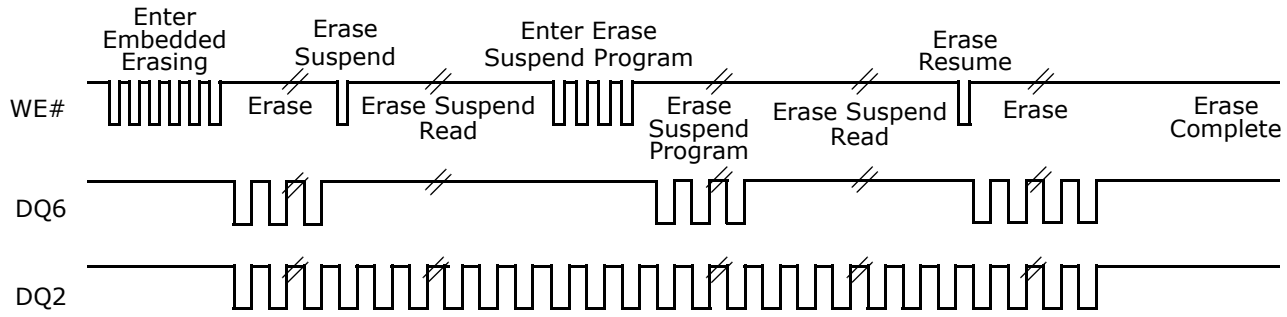
Figure 17. Data# Polling Timings (During Embedded Algorithms)

AC Characteristics



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 18. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 19. DQ2 vs. DQ6

AC Characteristics

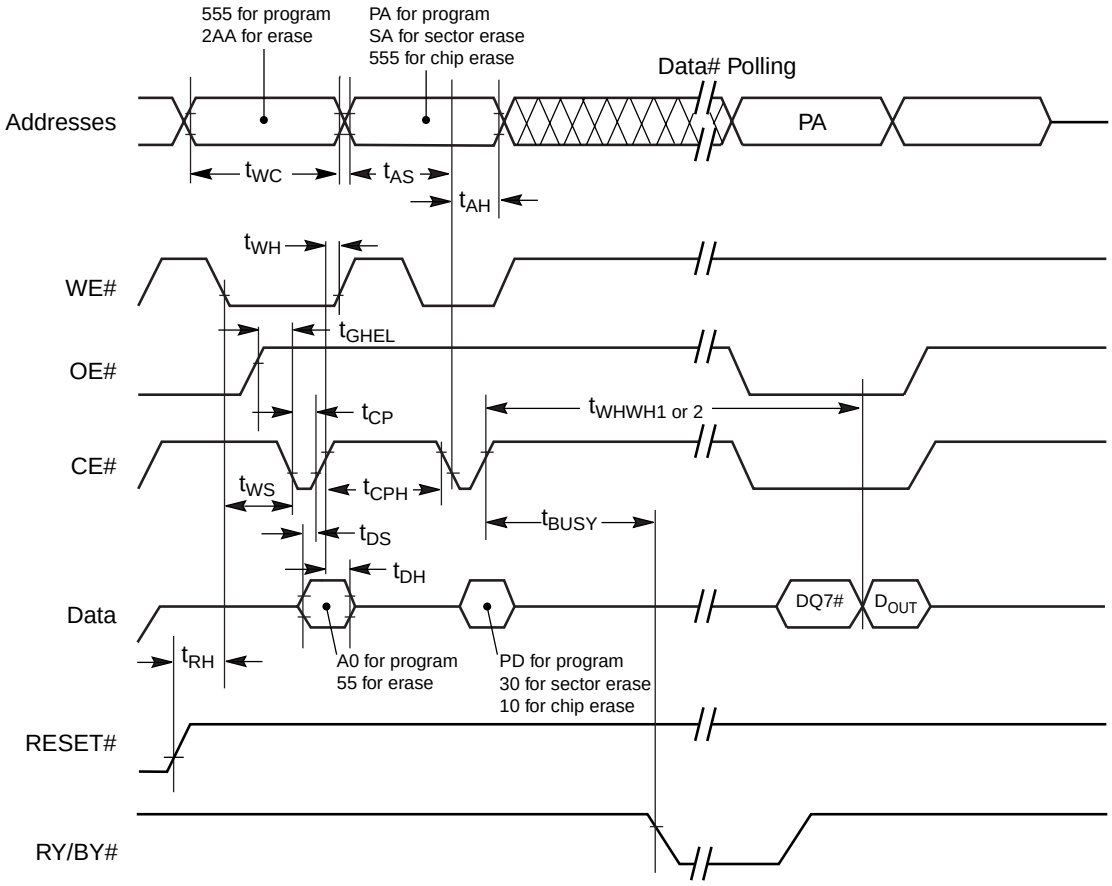
Alternate CE# Controlled Erase and Program Operations- S29GLI28N, S29GL256N, S29GL5I2N

Parameter					Speed Options				
JEDEC	Std.	Description			90	100	110	110	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	110	110	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	T_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45				ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{CEPH}	CE# High during toggle bit polling		Min	20				ns
	t_{OEPH}	OE# High during toggle bit polling		Min	20				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5				sec

Notes:

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 90 ns, 100ns, and 110 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 110 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 20. Alternate CE# Controlled Write (Erase/Program) Operation Timings

Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 5)
Chip Erase Time	S29GL128N	64	256	sec	
	S29GL256N	128	512		
	S29GL512N	256	1024		
Total Write Buffer Programming Time (Note 3)		240		µs	Excludes system level overhead (Note 6)
Total Accelerated Effective Write Buffer Programming Time (Note 3)		200		µs	
Chip Program Time	S29GL128N	123		sec	
	S29GL256N	246			
	S29GL512N	492			

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 10,000 cycles, checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 16-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 12 for further information on command definitions.*

TSOP Pin and BGA Package Capacitance

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			BGA	3.9	4.7	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

pSRAM Type 2

16Mb (1Mb Word x 16-bit)
32Mb (2Mb Word x 16-bit)
64Mb (4Mb Word x 16-bit)

Features

- Process Technology: CMOS
- Organization: x16 bit
- Power Supply Voltage: 2.7~3.1V
- Three State Outputs
- Compatible with Low Power SRAM

Product Information

Density	V_{CC} Range	Standby (ISBI, Max.)	Operating (ICC2, Max.)	Mode
16Mb	2.7-3.1V	80 µA	30 mA	Dual CS
16Mb	2.7-3.1V	80 µA	35 mA	Dual CS and Page Mode
32Mb	2.7-3.1V	100 µA	35 mA	Dual CS
32Mb	2.7-3.1V	100 µA	40 mA	Dual CS and Page Mode
64Mb	2.7-3.1V	TBD	TBD	Dual CS
64Mb	2.7-3.1V	TBD	TBD	Dual CS and Page Mode

Pin Description

Pin Name	Description	I/O
CS1#, CS2	Chip Select	I
OE#	Output Enable	I
WE#	Write Enable	I
LB#, UB#	Lower/Upper Byte Enable	I
A0-A19 (16M) A0-A20 (32M) A0-A21 (64M)	Address Inputs	I
I/O0-I/O15	Data Inputs/Outputs	I/O
V_{CC}/V_{CCQ}	Power Supply	—
V_{SS}/V_{SSQ}	Ground	—
NC	Not Connection	—
DNU	Do Not Use	—

Power Up Sequence

1. Apply power.
2. Maintain stable power (V_{CC} min.=2.7V) for a minimum 200 µs with CS1#=high or CS2=low.

Timing Diagrams

Power Up

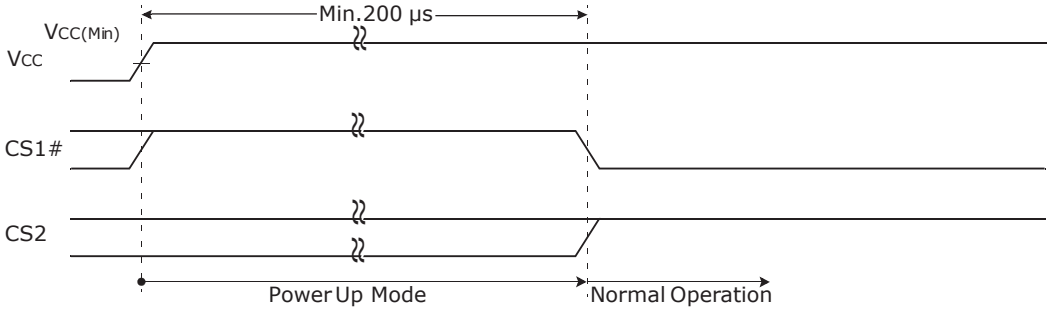


Figure 21. Power Up 1 (CSI# Controlled)

Notes:
1. After V_{CC} reaches V_{CC}(Min.), wait 200 µs with CS1# high. Then the device gets into the normal operation.

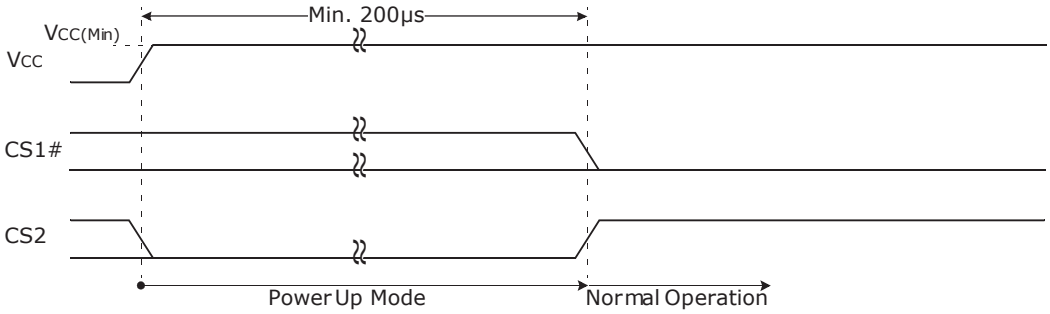


Figure 22. Power Up 2 (CS2 Controlled)

Notes:
1. After V_{CC} reaches V_{CC}(Min.), wait 200 µs with CS2 low. Then the device gets into the normal operation.

Functional Description

Mode	CS1#	CS2	OE#	WE#	LB#	UB#	I/O_{1-8}	I/O_{9-16}	Power
Deselected	H	X	X	X	X	X	High-Z	High-Z	Standby
Deselected	X	L	X	X	X	X	High-Z	High-Z	Standby
Deselected	X	X	X	X	H	H	High-Z	High-Z	Standby
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	Active
Outputs Disabled	L	H	H	H	X	L	High-Z	High-Z	Active
Lower Byte Read	L	H	L	H	L	H	D_{OUT}	High-Z	Active
Upper Byte Read	L	H	L	H	H	L	High-Z	D_{OUT}	Active
Word Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	Active
Lower Byte Write	L	H	X	L	L	H	D_{IN}	High-Z	Active
Upper Byte Write	L	H	X	L	H	L	High-Z	D_{IN}	Active
Word Write	L	H	X	L	L	L	D_{IN}	D_{IN}	Active

Legend:*X = Don't care (must be low or high state).*

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_{IN} , V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_A	-40 to 85	°C

Notes:

1. *Stresses greater than those listed under "Absolute Maximum Ratings" section may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.*

DC Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply Voltage	2.7	2.9	3.1	V
V_{SS}	Ground	0	0	0	
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3 (Note 2)	
V_{IL}	Input Low Voltage	-0.2 (Note 3)	—	0.6	

Notes:

1. *TA=-40 to 85°C, otherwise specified.*
2. *Overshoot: V_{CC}+1.0V in case of pulse width ≤ 20ns.*
3. *Undershoot: -1.0V in case of pulse width ≤ 20ns.*
4. *Overshoot and undershoot are sampled, not 100% tested.*

Capacitance (Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	—	8	pF
C_{OIO}	Input/Output Capacitance	V_{OUT} = 0V	—	10	pF

Note: *This parameter is sampled periodically and is not 100% tested.*

DC and Operating Characteristics

Common

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-1	—	1	µA
Output Leakage Current	I_{LO}	CS1#=V_{IH} or CS2=V_{IL} or OE#=V_{IH} or WE#=V_{IL} or LB#=UB#=V_{IH}, V_{IO}=V_{SS} to V_{CC}	-1	—	1	µA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA	2.4	—	—	V

16M pSRAM

Item	Symbol		Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}		Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	7	mA
	I_{CC2}	Async	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}=V_{IH} or V_{IL}	—	—	30	mA
		Page	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}			35	mA
Standby Current (CMOS)	I_{SB1} (Note 1)		Other inputs=0-VCC 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	80	mA

Notes:

1. *Standby mode is supposed to be set up after at least one active operation after power up. ISB1 is measure after 60ms from the time when standby mode is set up.*

32M pSRAM

Item	Symbol		Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}		Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	7	mA
	I_{CC2}	Async	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}=V_{IH} or V_{IL}	—	—	35	mA
		Page	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}			40	mA
Standby Current (CMOS)	I_{SB1} (Note 1)		Other inputs=0-VCC 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	100	mA

Notes:

1. *Standby mode is supposed to be set up after at least one active operation after power up. ISB1 is measure after 60ms from the time when standby mode is set up.*

64M pSRAM

Item	Symbol		Test Conditions	Min	Typ	Max	Unit
Average Operating Current	I_{CC1}		Cycle time=1µs, 100% duty, I_{IO}=0mA, CS1#≤0.2V, LB#≤0.2V and/or UB#≤0.2V, CS2≥V_{CC}-0.2V, V_{IN}≤0.2V or V_{IN}≥VCC-0.2V	—	—	TBD	mA
	I_{CC2}	Async	Cycle time=Min, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}=V_{IH} or V_{IL}	—	—	TBD	mA
		Page	Cycle time=t_{RC}+3t_{PC}, I_{IO}=0mA, 100% duty, CS1#=V_{IL}, CS2=V_{IH} LB#=V_{IL} and/or UB#=V_{IL}, V_{IN}-V_{IH} or V_{IL}			TBD	mA
Standby Current (CMOS)	I_{SB1} (Note 1)		Other inputs=0-VCC 1. CS1# ≥ V_{CC} - 0.2, CS2 ≥ V_{CC} - 0.2V (CS1# controlled) or 2. 0V ≤ CS2 ≤ 0.2V (CS2 controlled)	—	—	TBD	mA

Notes:

1. *Standby mode is supposed to be set up after at least one active operation after power up. ISB1 is measure after 60ms from the time when standby mode is set up.*

AC Operating Conditions

Test Conditions (Test Load and Test Input/Output Reference)

- Input pulse level: 0.4 to 2.2V
- Input rising and falling time: 5ns
- Input and output reference voltage: 1.5V
- Output load (See Figure 23): CL=50pF

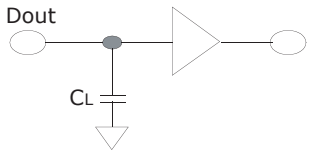


Figure 23. Output Load

Note: *Including scope and jig capacitance.*

ACC Characteristics (Ta = -40°C to 85°C, V_{CC} = 2.7 to 3.1 V)

Symbol		Parameter	Speed Bins		Unit
			70ns		
			Min	Max	
Read	t_{RC}	Read Cycle Time	70	—	ns
	t_{AA}	Address Access Time	—	70	ns
	t_{CO}	Chip Select to Output	—	70	ns
	t_{OE}	Output Enable to Valid Output	—	35	ns
	t_{BA}	UB#, LB# Access Time	—	70	ns
	t_{LZ}	Chip Select to Low-Z Output	10	—	ns
	t_{BLZ}	UB#, LB# Enable to Low-Z Output	10	—	ns
	t_{OLZ}	Output Enable to Low-Z Output	5	—	ns
	t_{HZ}	Chip Disable to High-Z Output	0	25	ns
	t_{BHZ}	UB#, LB# Disable to High-Z Output	0	25	ns
	t_{OHZ}	Output Disable to High-Z Output	0	25	ns
	t_{OH}	Output Hold from Address Change	5	—	ns
	t_{PC}	Page Cycle Time	25	—	ns
	t_{PA}	Page Access Time	—	20	ns
Write	t_{WC}	Write Cycle Time	70	—	ns
	t_{CW}	Chip Select to End of Write	60	—	ns
	t_{AS}	Address Set-up Time	0	—	ns
	t_{AW}	Address Valid to End of Write	60	—	ns
	t_{BW}	UB#, LB# Valid to End of Write	60	—	ns
	t_{WP}	Write Pulse Width	55 (Note 1)	—	ns
	t_{WR}	Write Recovery Time	0	—	ns
	t_{WHZ}	Write to Output High-Z	0	25	ns
	t_{DW}	Data to Write Time Overlap	30	—	ns
	t_{DH}	Data Hold from Write Time	0	—	ns
	t_{OW}	End Write to Output Low-Z	5	—	ns

Notes:

1. t_{WP} (min) = 70ns for continuous write operation over 50 times.

Timing Diagrams

Read Timings

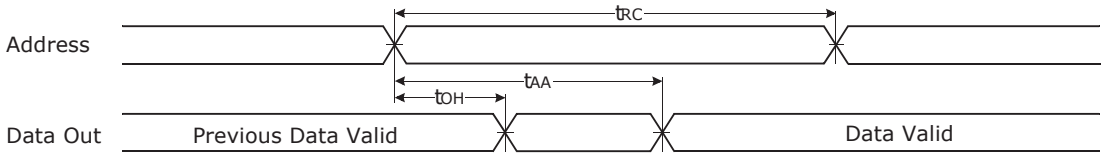


Figure 24. Timing Waveform of Read Cycle(I)

Notes:

1. Address Controlled, CS1# =OE# =V_{IL}, CS2=WE# =V_{IH}, UB# and/or LB# =V_{IL}.

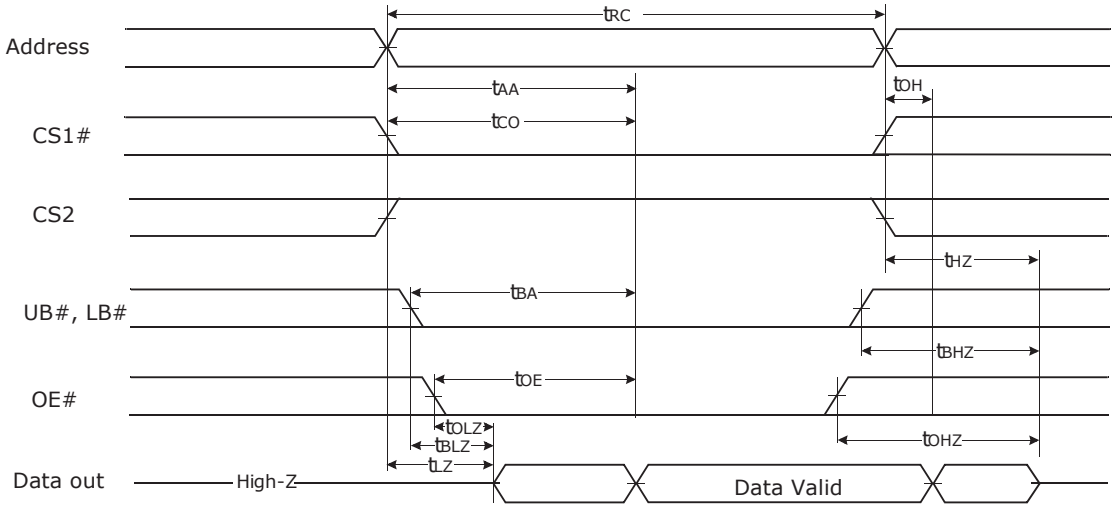


Figure 25. Timing Waveform of Read Cycle(2)

Notes:

1. WE# =V_{IH}.

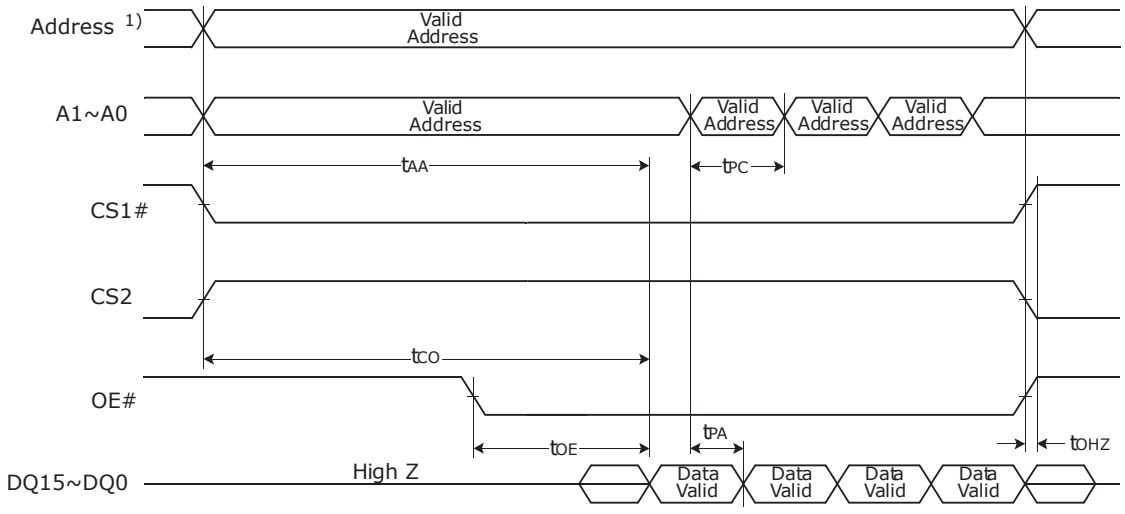


Figure 26. Timing Waveform of Read Cycle(2)

Notes:

1. *16Mb: A2 ~ A19, 32Mb: A2 ~ A20, 64Mb: A2 ~ A21.*

t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

t_{OE}(max) is met only when OE# becomes enabled after t_{AA}(max).

If invalid address signals shorter than min. $T._{RC}$ are continuously repeated for over 4µs, the device needs a normal read timing (t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4µs.

Write Timings

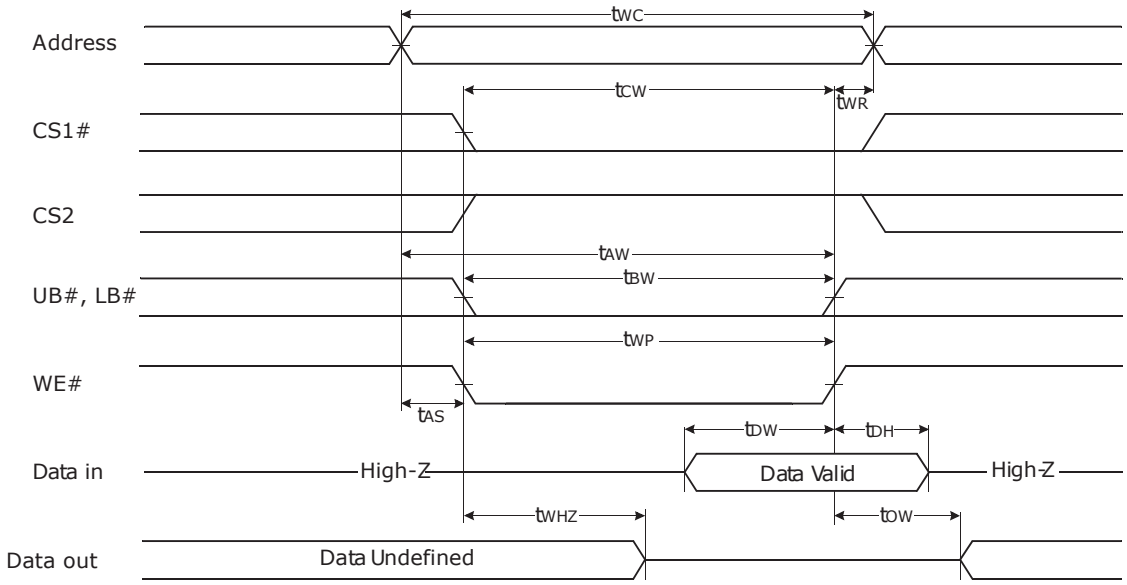


Figure 27. Write Cycle #I (WE# Controlled)

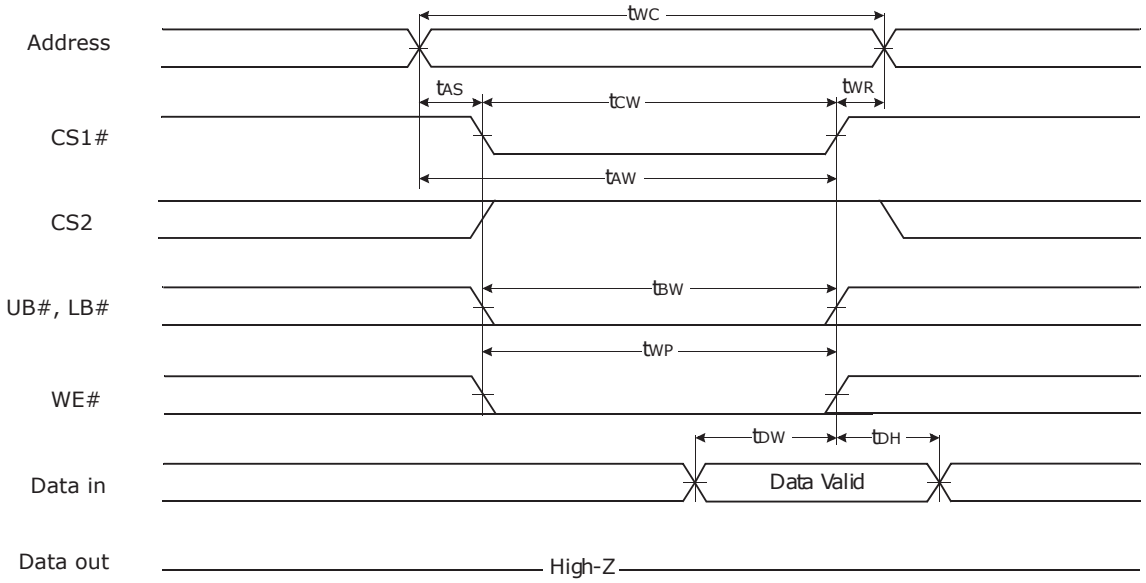


Figure 28. Write Cycle #2 (CSI# Controlled)

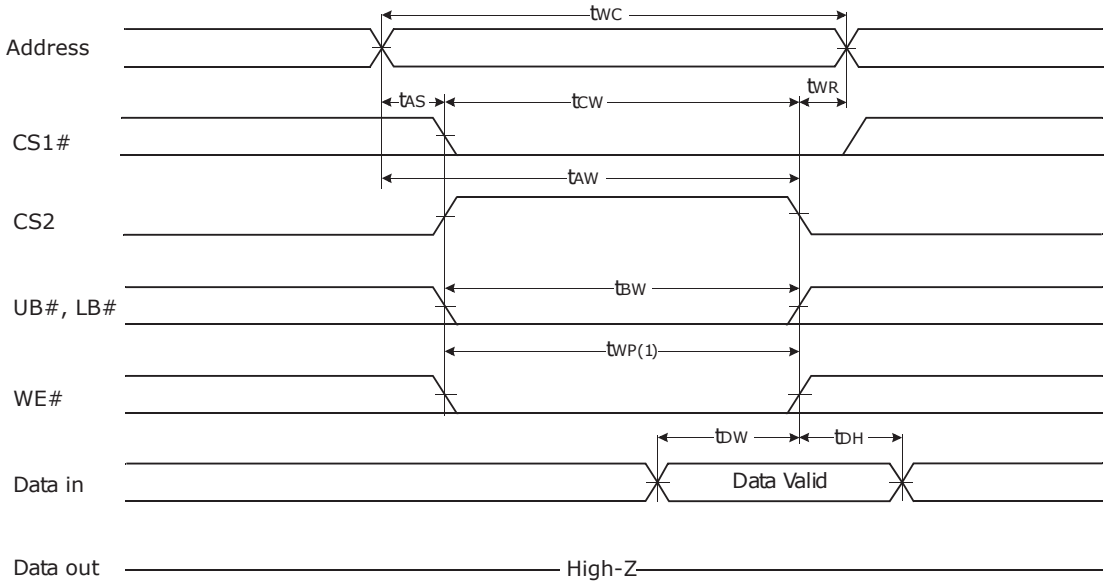


Figure 29. Timing Waveform of Write Cycle(3)(CS2 Controlled)

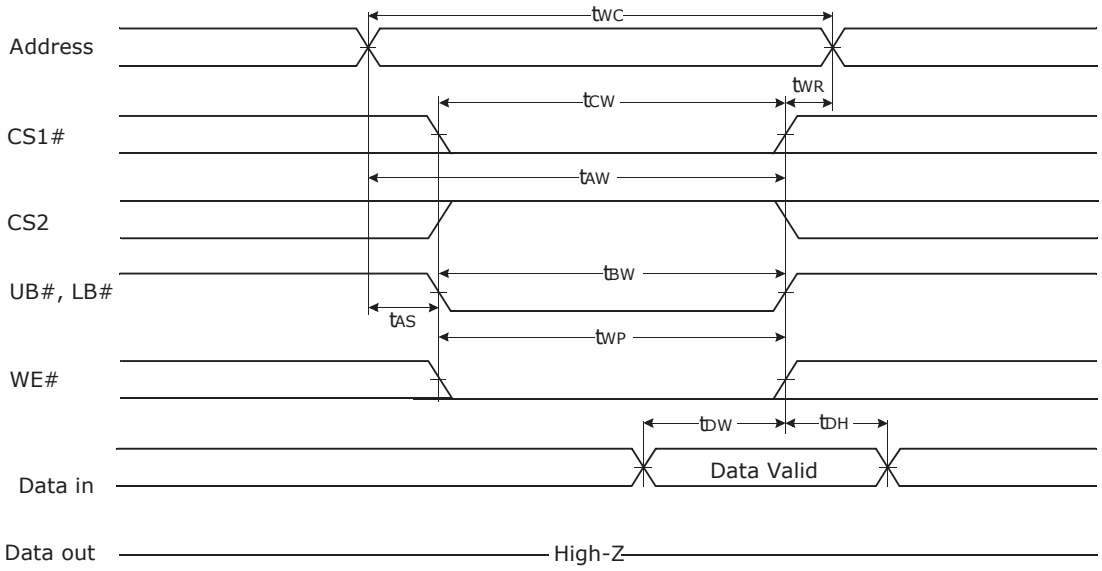


Figure 30. Timing Waveform of Write Cycle(4) (UB#, LB# Controlled)

Notes:

1. *A write occurs during the overlap (t_{WP}) of low CS1# and low WE#. A write begins when CS1# goes low and WE# goes low with asserting UB# or LB# for single byte operation or simultaneously asserting UB# and LB# for double byte operation. A write ends at the earliest transition when CS1# goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*
2. *t_{CW} is measured from the CS1# going low to the end of write.*
3. *t_{AS} is measured from the address valid to the beginning of write.*
4. *t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with CS1# or WE# going high.*

pSRAM Type 6

2M Word by 16-bit Cmos Pseudo Static RAM (32M Density)
4M Word by 16-bit Cmos Pseudo Static RAM (64M Density)

Features

- Single power supply voltage of 2.6 to 3.3 V
- Direct TTL compatibility for all inputs and outputs
- Deep power-down mode: Memory cell data invalid
- Page operation mode:
  - Page read operation by 8 words
- Logic compatible with SRAM R/W ( ) pin
- Standby current
  - Standby = 70 µA (32M)
  - Standby = 100 µA (64M)
  - Deep power-down Standby = 5 µA
- Access Times

	32M 64M
Access Time	70 ns
CE1# Access Time	70 ns
OE# Access Time	25 ns
Page Access Time	30 ns

Pin Description

Pin Name	Description
A_0 to A_{21}	Address Inputs
A0 to A2	Page Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
CE1#	Chip Enable Input
CE2	Chip select Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#,UB#	Data Byte Control Inputs
V_{DD}	Power Supply
GND	Ground
NC	Not Connection

Functional Description

Mode	CE1#	CE2	OE#	WE#	LB#	UB#	Address	I/O_{1-8}	I/O_{9-16}	Power
Read(Word)	L	H	L	H	L	L	X	D_{OUT}	D_{OUT}	I_{DDO}
Read(Lower Byte)	L	H	L	H	L	H	X	D_{OUT}	High-Z	I_{DDO}
Read(Upper Byte)	L	H	L	H	H	L	X	High-Z	D_{OUT}	I_{DDO}
Write(Word)	L	H	X	L	L	L	X	D_{IN}	D_{IN}	I_{DDO}
Write(Lower Byte)	L	H	X	L	L	H	X	D_{IN}	Invalid	I_{DDO}
Write(Upper Byte)	L	H	X	L	H	L	X	Invalid	D_{IN}	I_{DDO}
Outputs Disabled	L	H	H	H	X	X	X	High-Z	High-Z	I_{DDO}
Standby	H	H	X	X	X	X	X	High-Z	High-Z	I_{DDO}
Deep Power-down Standby	H	L	X	X	X	X	X	High-Z	High-Z	I_{DDSD}

Legend:*L = Low-level Input (V_{IL}), H = High-level Input (V_{IH}), X = V_{IL} or V_{IH}, High-Z = High Impedence.*

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{DD}	Power Supply Voltage	-1.0 to 3.6	V
V_{IN}	Input Voltage	-1.0 to 3.6	V
V_{OUT}	Output Voltage	-1.0 to 3.6	V
T_{opr}	Operating Temperature	-40 to 85	°C
T_{strg}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	0.6	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: ESD Immunity: *Spansion Flash memory Multi-Chip Products (MCPs) may contain component devices that are developed by Spansion and component devices that are developed by a third party (third-party components). Spansion components are tested and guaranteed to the ESD immunity levels listed in the corresponding Spansion Flash memory Qualification Database. Third-party components are neither tested nor guaranteed by Spansion for ESD immunity. However, ESD test results for third-party components may be available from the component manufacturer. Component manufacturer contact information is listed in the Spansion MCP Qualification Report, when available. The Spansion Flash memory Qualification Database and Spansion MCP Qualification Report are available from AMD and Fujitsu sales offices.*

DC Recommended Operating Conditions (Ta = -40°C to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage	2.6	2.75	3.3	V
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3 (Note)	
V_{IL}	Input Low Voltage	-0.3 (Note)	—	0.4	

Note: *V_{IH} (Max) V_{DD} = 1.0 V with 10 ns pulse width. V_{IL} (Min) -1.0 V with 10 ns pulse width.*

DC Characteristics (Ta = -40°C to 85°C, VDD = 2.6 to 3.3 V) (See Note 3 to 4)

Symbol	Parameter	Test Condition		Min	Typ.	Max	Unit
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}		-1.0	—	+1.0	µA
I_{LO}	Output Leakage Current	Output disable, V_{OUT} = 0 V to V_{DD}		-1.0	—	+1.0	µA
V_{OH}	Output High Voltage	I_{OH} = - 0.5 mA		2.0	¾	V	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA		—	—	0.4	V
I_{DDO1}	Operating Current	CE1#= V_{IL}, CE2 = V_{IH}, I_{OUT} = 0 mA, t_{RC} = min	ET5UZ8A-43DS	—	—	40	mA
			ET5VB5A-43DS	—	—	50	
I_{DDO2}	Page Access Operating Current	CE1#= V_{IL}, CE2 = V_{IH}, I_{OUT} = 0 mA Page add. cycling, t_{RC} = min		—	—	25	mA
I_{DDS}	Standby Current(MOS)	CE1# = V_{DD} - 0.2 V, CE2 = V_{DD} - 0.2 V	ET5UZ8A-43DS	—	—	70	mA
			ET5VB5A-43DS	—	—	100	µA
I_{DDSD}	Deep Power-down Standby Current	CE2 = 0.2 V		—	—	5	µA

Capacitance (Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: *This parameter is sampled periodically and is not 100% tested.*

AC Characteristics and Operating Conditions

(Ta = -40°C to 85°C, VDD = 2.6 to 3.3 V) (See Note 5 to 11)

Symbol	Parameter	Min	Max	Unit
t_{RC}	Read Cycle Time	70	10000	ns
t_{ACC}	Address Access Time	—	70	ns
t_{CO}	Chip Enable (CE1#) Access Time	—	70	ns
t_{OE}	Output Enable Access Time	—	25	ns
t_{BA}	Data Byte Control Access Time	—	25	ns
t_{COE}	Chip Enable Low to Output Active	10	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{BE}	Data Byte Control Low to Output Active	0	—	ns
t_{OD}	Chip Enable High to Output High-Z	—	20	ns
t_{ODO}	Output Enable High to Output High-Z	—	20	ns
t_{BD}	Data Byte Control High to Output High-Z	—	20	ns

Symbol	Parameter	Min	Max	Unit
t_{OH}	Output Data Hold Time	10	—	ns
t_{PM}	Page Mode Time	70	10000	ns
t_{PC}	Page Mode Cycle Time	30	—	ns
t_{AA}	Page Mode Address Access Time	—	30	ns
t_{AOH}	Page Mode Output Data Hold Time	10	—	ns
t_{WC}	Write Cycle Time	70	10000	ns
t_{WP}	Write Pulse Width	50	—	ns
t_{CW}	Chip Enable to End of Write	70	—	ns
t_{BW}	Data Byte Control to End of Write	60	—	ns
t_{AW}	Address Valid to End of Write	60	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{CEH}	Chip Enable High Pulse Width	10	—	ns
t_{WEH}	Write Enable High Pulse Width	6	—	ns
t_{ODW}	WE# Low to Output High-Z	—	20	ns
t_{OEW}	WE# High to Output Active	0		ns
t_{DS}	Data Set-up Time	30	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{CS}	CE2 Set-up Time	0	—	ns
t_{CH}	CE2 Hold Time	300	—	µs
t_{DPD}	CE2 Pulse Width	10	—	ms
t_{CHC}	CE2 Hold from CE1#	0	—	ns
t_{CHP}	CE2 Hold from Power On	30	—	µs

AC Test Conditions

Parameter	Condition
Output load	30 pF + 1 TTL Gate
Input pulse level	V_{DD} - 0.2 V, 0.2 V
Timing measurements	V_{DD} x 0.5
Reference level	V_{DD} x 0.5
t_R, t_F	5 ns

Timing Diagrams

Read Timings

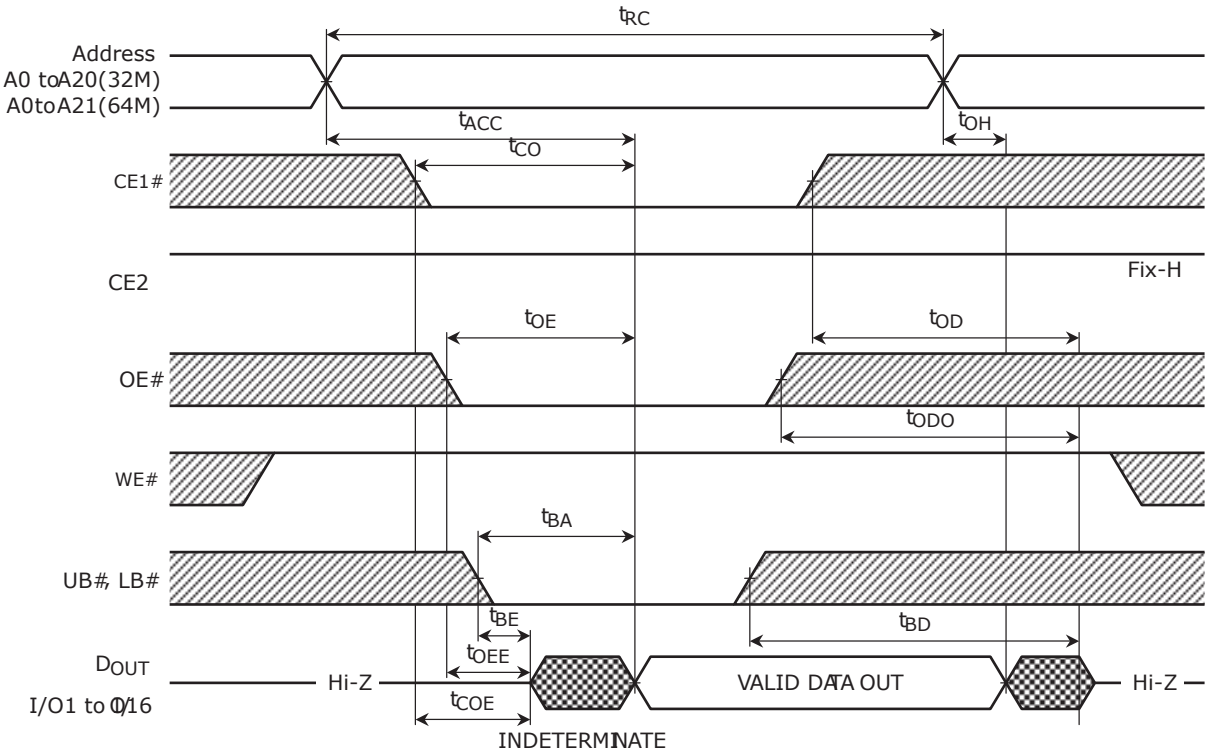


Figure I. Read Cycle

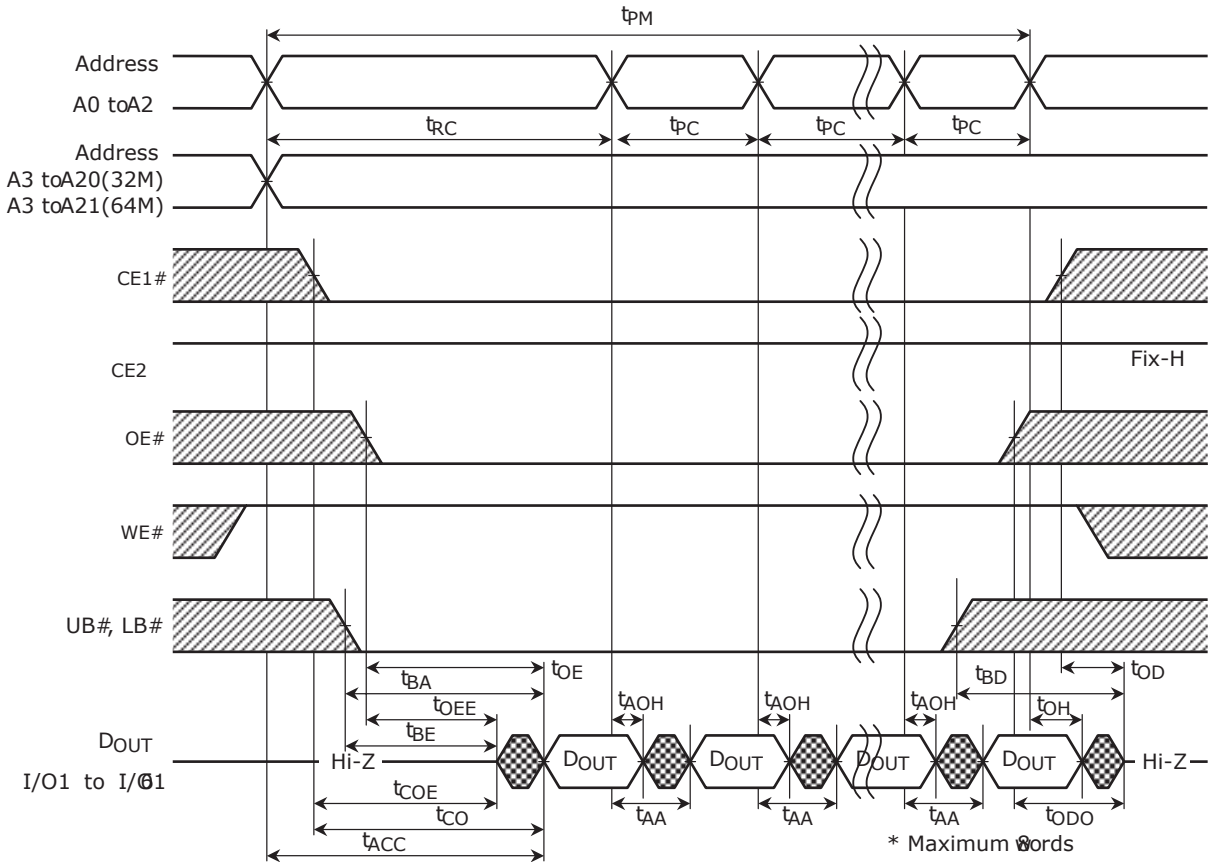


Figure 2. Page Read Cycle (8 Words Access)

Write Timings

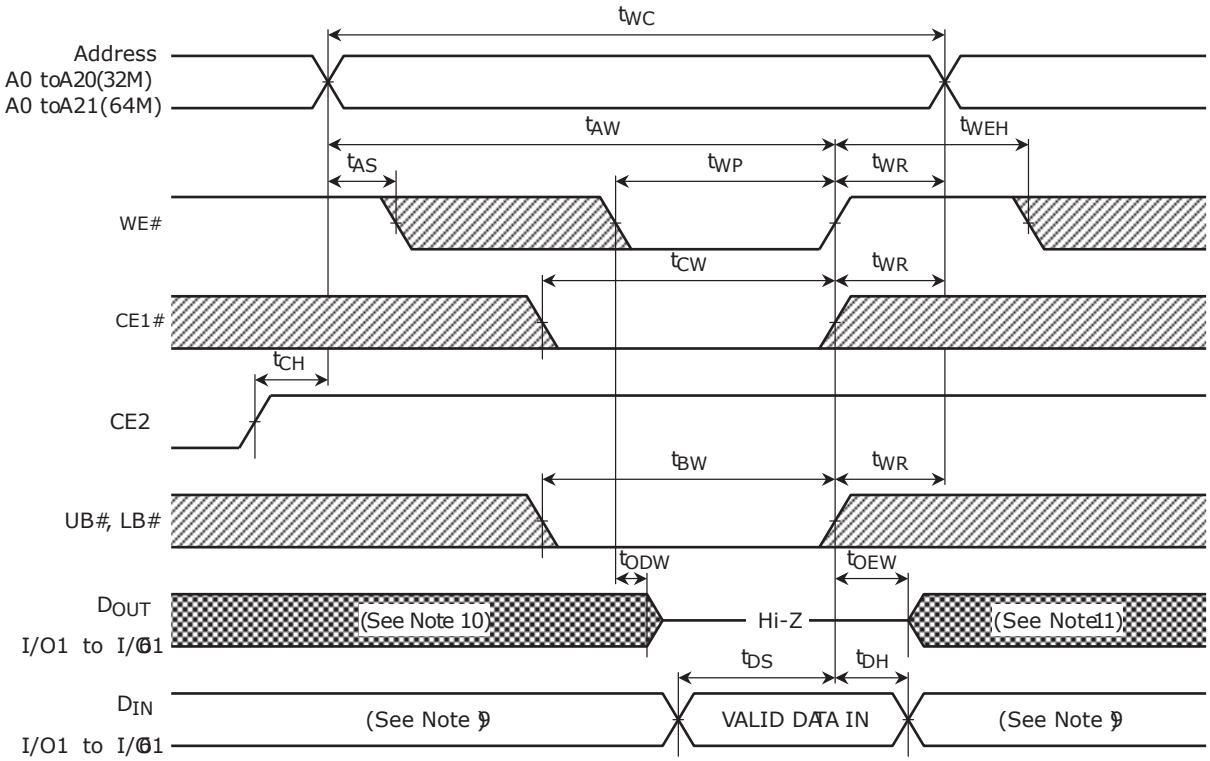


Figure 3. Write Cycle #I (WE# Controlled) (See Note 8)

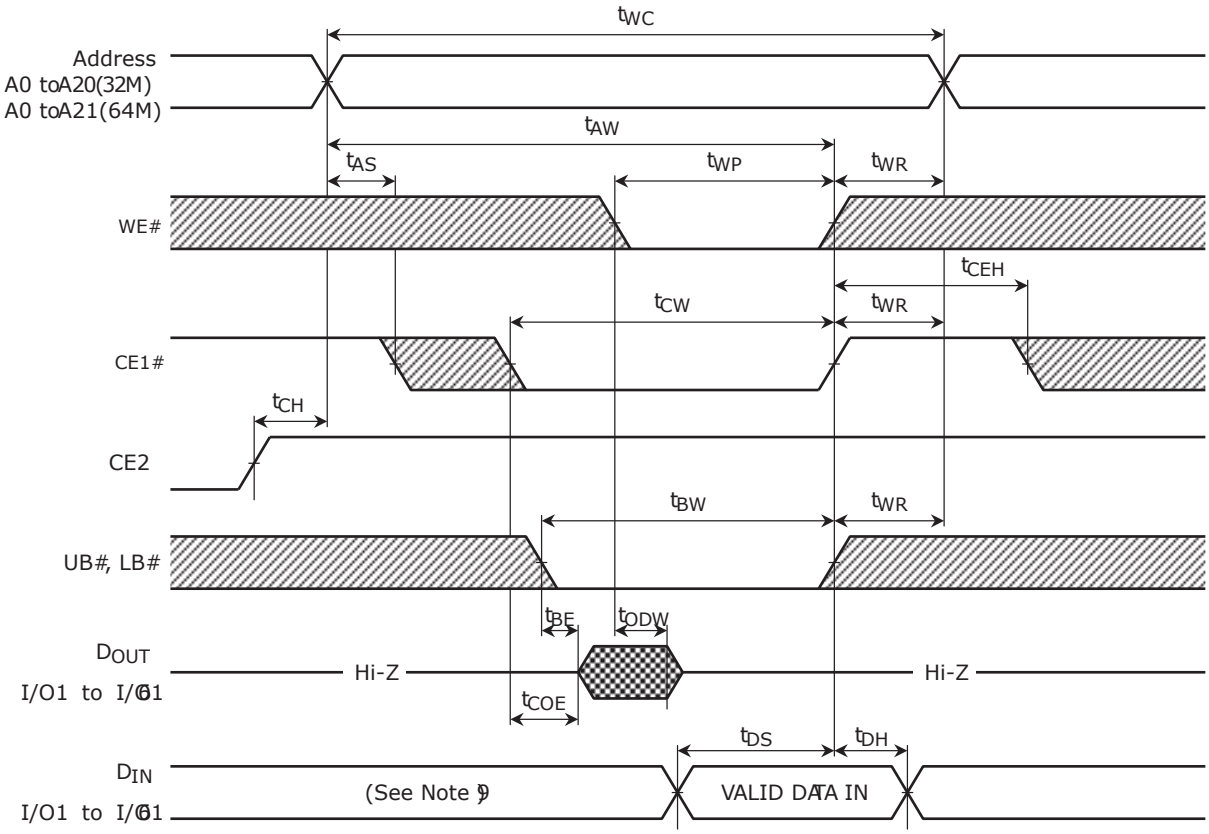


Figure 4. Write Cycle #2 (CE# Controlled) (See Note 8)

Deep Power-down Timing

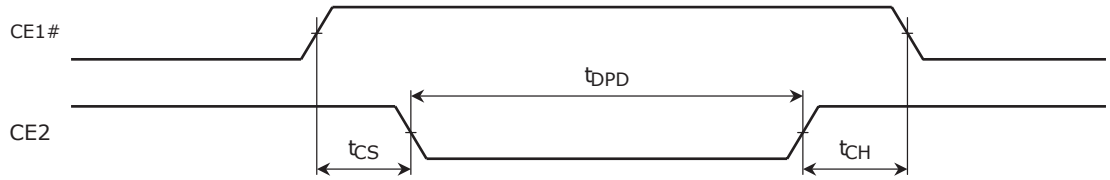


Figure 5. Deep Power Down Timing

Power-on Timing

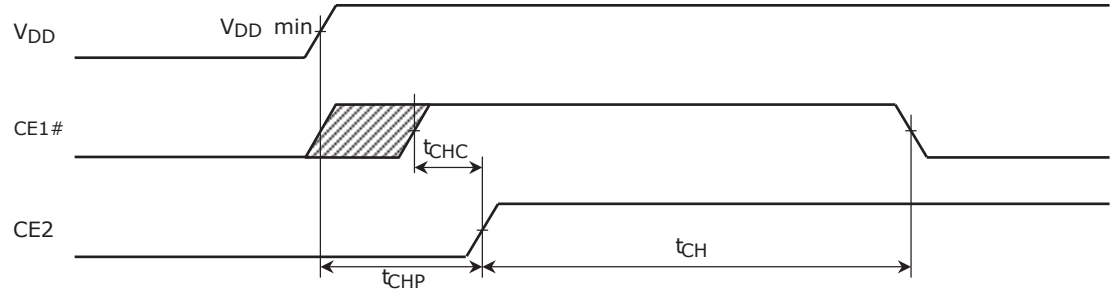


Figure 6. Power-on Timing

Provisions of Address Skew

Read

In case multiple invalid address cycles shorter than t_{RC} min sustain over 10 µs in an active status, at least one valid address cycle over t_{RC} min is required during 10µs.

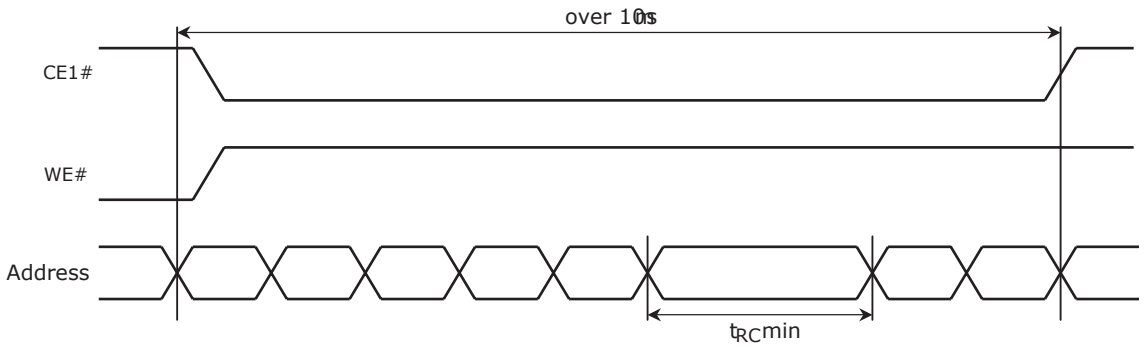


Figure 7. Read

Write

In case multiple invalid address cycles shorter than t_{WC} min sustain over 10 µs in an active status, at least one valid address cycle over t_{WC} min is required during 10 µs.

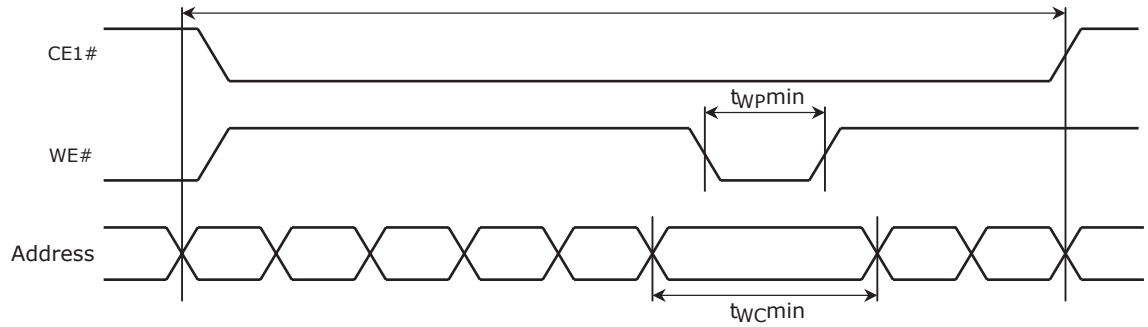


Figure 8. Write

Notes:

1. *Stresses greater than listed under "Absolute Maximum Ratings" section may cause permanent damage to the device.*
2. *All voltages are reference to GND.*
3. *I_{DDO} depends on the cycle time.*
4. *I_{DDO} depends on output loading. Specified values are defined with the output open condition.*
5. *AC measurements are assumed t_R, t_F = 5 ns.*
6. *Parameters t_{OD}, t_{ODO}, t_{BD} and t_{ODW} define the time at which the output goes the open condition and are not output voltage reference levels.*
7. *Data cannot be retained at deep power-down stand-by mode.*
8. *If OE# is high during the write cycle, the outputs will remain at high impedance.*
9. *During the output state of I/O signals, input signals of reverse polarity must not be applied.*
10. *If CE1# or LB#/UB# goes LOW coincident with or after WE# goes LOW, the outputs will remain at high impedance.*
11. *If CE1# or LB#/UB# goes HIGH coincident with or before WE# goes HIGH, the outputs will remain at high impedance.*

Revision Summary

Revision A0 (November 9, 2004)

Initial Release

Revision A1 (January 6, 2005)

Global

Changed text designations from Flash to PL127J.

Pin Connection

Changed Pinout reference.

Block Diagram

Changed pin names on a couple pins.

Changed device designations from Flash to PL127J.

S29GLxxxN_MCP section

Added updated version to this section.

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (I) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Spansion product under development by Spansion LLC. Spansion LLC reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion LLC assumes no liability for any damages of any kind arising out of the use of the information in this document.

Copyright © 2005 Spansion LLC. All rights reserved. Spansion, the Spansion logo, MirrorBit, combinations thereof, and ExpressFlash are trademarks of Spansion LLC. Other company and product names used in this publication are for identification purposes only and may be trademarks of their respective companies.