DATA SHEET

SA2420
Low voltage RF transceiver — 2.45GHz

Product specification 1997 May 23

Philips Semiconductors

PHILIPS

Low voltage RF transceiver — 2.45 GHz SA2420

DESCRIPTION

The SA2420 transceiver is a combined low-noise amplifier, receive mixer, transmit mixer and LO buffer IC designed for high-performance low-power communication systems for 2.4-2.5GHz applications. The LNA has a 2.5dB noise figure at 2.45GHz with 14dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over the -40 to +85°C temperature range. The wide-dynamic-range receive mixer has a 10.9dB noise figure and an input IP3 of +2.8dBm at 2.45GHz. The nominal current drawn from a single 3V supply is 37mA in transmit mode and 22mA in receive mode.

FEATURES

- Low current consumption: 37mA nominal transmit mode and 22mA nominal receive mode
- Fabricated on a high volume, rugged BiCMOS technology
- High system power gain: 22.5dB (LNA + Mixer) at 2.45GHz
- TSSOP24 package
- Excellent gain stability versus temperature and supply voltage
- -10dBm LO input power can be used to drive the mixer
- Operates with either full or half frequency LO
- Wide IF range: 50–500MHz

PIN CONFIGURATION

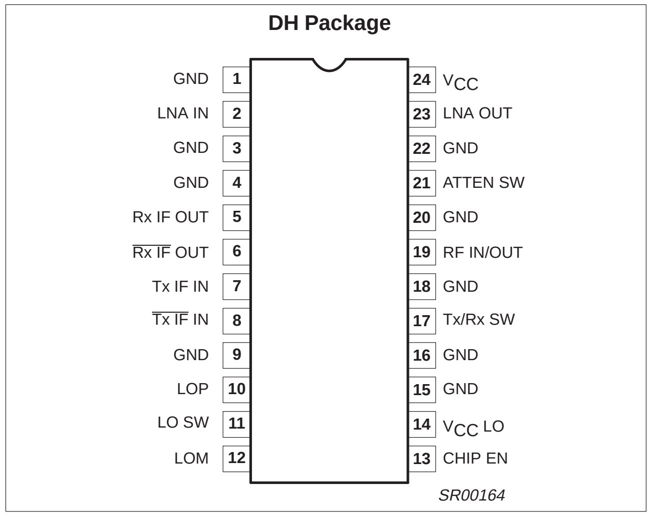

Figure 1. Pin Configuration

APPLICATIONS

- 2.45GHz WLAN front-end (802.11, ISM)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA2420DH	SOT355-1

BLOCK DIAGRAM

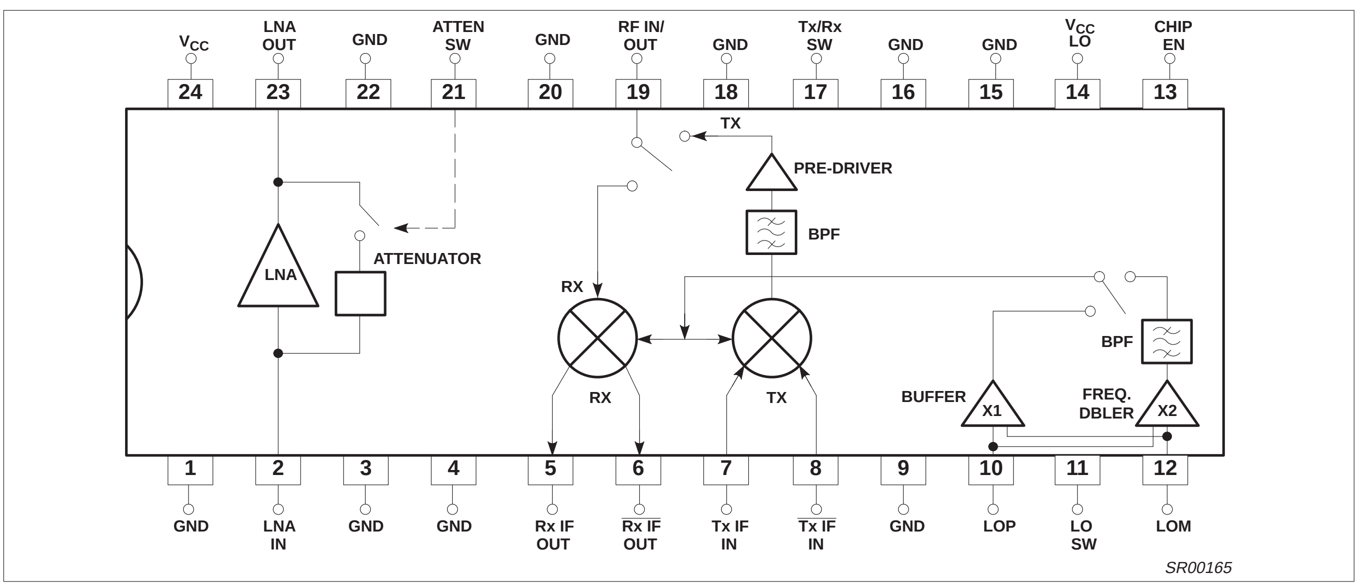

Figure 2. SA2420 Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6	V
V_{IN}	Voltage applied to any pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air) 24-Pin Plastic TSSOP	555	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power (RF/IF/LO pins)	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding these conditions may damage the product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, and absolute maximum ratings may impact product reliability θ_{JA}: 24-Pin TSSOP = 117°C/W
3. IC is protected for ESD voltages for 2000V, excepts pins 10 and 12, which are protected up to 500V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-4σ	TYP	+4σ	MAX	
I_{CCTX}	Supply current, Transmit	LO mode = Hi	25		37		45	mA
I_{CCRX}	Supply current, Receive	LO mode = Hi	15		22		28	mA
$I_{CC\ OFF}$	Power down mode (Tx/Rx SW = Low)	LO mode = Hi, LNA gain = Hi			0		10	μA
$V_{LNA\text{-}IN}$	LNA input voltage	Receive mode			0.855			V
$I_{LNA\text{-}OUT}$	LNA output bias current	Receive mode			4.0			mA
$V_{LO\ 2.1\ GHz}$	LO buffer DC input voltage	LO mode = Hi			2.1			V
$V_{LO\ 1.05\ GHz}$	LO buffer DC input voltage	LO mode = Low			2.1			V
$V_{TX\ IF}$	Tx Mixer input voltage	Transmit mode			1.7			V
$V_{TX\ IFB}$	Tx Mixer input voltage	Transmit mode			1.7			V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; LO_{IN} = -10dBm @ 2.1GHz; f_{RF} = 2.45GHz; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-4σ	TYP	+4σ	MAX	
Low Noise Amplifier (In = Pin 2; Out = 23)								
S_{21}	Amplifier gain	LNA gain = Hi		12.7	14.0	15.3		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	LNA gain = Hi			-0.002			dB/°C
$\Delta S_{21}/\Delta V_{CC}$	Gain V_{CC} drift	LNA gain = Hi			0.3			dB/V
S_{12}	Amplifier reverse isolation	LNA gain = Hi			-22			dB
S_{11}	Amplifier input match[1]	LNA gain = Hi			-8			dB
S_{22}	Amplifier output match[1]	LNA gain = Hi			-8			dB
ISO	Isolation: LO_1 to LNA_{IN}	LO mode = Hi, LNA gain = Hi			-45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Hi			-15			dBm
IP3	Amplifier input third order intercept	f_1 - f_2 = 1MHz, LNA gain = Hi			-3			dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Hi		2.3	2.5	2.7		dB
LNA High Overload Mode								
S_{21}	Amplifier gain	LNA gain = Low		–14.0	-13.3	–12.0		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity	LNA gain = Low			-0.01			dB/°C
$\Delta S_{21}/\Delta V_{CC}$	Gain V_{CC} drift	LNA gain = Low			0.3			dB/V
S_{12}	Amplifier reverse isolation	LNA gain = Low			-16			dB
S_{11}	Amplifier input match[1]	LNA gain = Low			-8			dB
S_{22}	Amplifier output match[1]	LNA gain = Low			-8			dB
ISO	Isolation: LO_1 to LNA_{IN}	LO mode = Hi, LNA gain = Low			-45			dB
P_{-1dB}	Amplifier input 1dB gain compression	LNA gain = Low			+6			dBm
IP3	Amplifier input third order intercept	f_1 - f_2 = 1MHz, LNA gain = Low			17			dBm
NF	Amplifier noise figure (50Ω)	LNA gain = Low			17			dB
Rx Mixer (RF = Pin 19, IF = Pins 5 and 6, LO = Pin 10 or 12, P_{LO} = -10dBm)								
PG_C	Power conversion gain into 50Ω : matched to 50Ω using external balun circuitry.	f_S = 2.45GHz, f_{LO} = 2.1GHz, f_{IF} = 350MHz		7.9	8.5	9.1		dB
$\Delta G_C/\Delta T$	Gain temperature drift				-0.016			dB/°C
$\Delta G_C/\Delta V_{CC}$	Gain V_{CC} drift				0.34			dB/V
S_{11-RF}	Input match at RF (2.45GHz)[1]				-15			dB
NF_M	SSB noise figure (2.45GHz) (50Ω)			10.2	10.9	11.6		dB
P_{-1dB}	Mixer input 1dB gain compression			–11.4	-10.3	–9.2		dBm
IP3	Input third order intercept	f_1 - f_2 = 1MHz		1.7	2.8	3.9		dBm
f_{RF}	RF frequency range[3]		2.4		2.45		2.5	GHz
f_{IF}	IF frequency range[3]		300		350		400	MHz

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	-4σ	TYP	+4σ	MAX	
Rx Mixer Spurious Components ($P_{IN} = P_{-1dB}$)								
$P_{RF\text{-}IF}$	RF feedthrough to IF	C_L = 2pF per side			-35			dBc
$P_{LO\text{-}IF}$	LO feedthrough to IF	C_L = 2pF per side			-35			dBc
Tx Mixer (RF = Pin 19, IF = Pins 7 and 8, LO = Pin 10 or 12, P_{LO} = -10dBm)								
PG_C	Power conversion gain: $R_L = 50\Omega$ $R_S = 50\Omega$	f_S = 2.45GHz, f_{LO} = 2.1GHz, f_{IF} = 350MHz		15.0	17	19.9		dB
$\Delta G_C/\Delta T$	Gain temperature drift				-0.032			dB/°C
$\Delta G_C/\Delta V_{CC}$	Gain voltage drift				0.4			dB/V
$S_{11\text{–}RF}$	Output match at RF (2.45GHz)[1]				-10			dB
NF_M	SSB noise figure (2.45GHz) (50Ω)				13.2			dB
P_{-1dB}	Output 1dB gain compression			1.5	2.9	4.3		dBm
IP3	Output third order intercept	$f_1 - f_2$ = 1MHz		10.1	+11.5	12.9		dBm
f_{RF}	RF frequency range[3]		2.4		2.45		2.5	GHz
f_{IF}	IF frequency range[3]		300		350		400	MHz
Tx Mixer Spurious Components ($P_{OUT} = P_{-1dB}$)								
$P_{IF\text{-}RF}$	IF feedthrough to RF				-29			dBc
$P_{LO\text{-}RF}$	LO feedthrough to RF				-20			dBc
$P_{2LO\text{-}RF}$	2*LO feedthrough to RF				-25			dBc
$P_{IMAGE\text{-}RF}$	Image feedthrough to RF				-0			dBc
LO Buffer: Full and Half Frequency inputs								
P_{LO}	LO drive level (see figure 16)		-10		-7		5	dBm
$S_{11\text{-}LO1}$	Mixer input match (LO = 2.1GHz)	LO mode = Hi			-10			dB
$S_{11\text{-}LO2}$	Mixer input match (LO = 1.05GHz)	LO mode = Low			-10			dB
f_{LO2G}	LO2G frequency range[3]	LO mode = Hi	1.9		2.1		2.3	GHz
f_{LO1G}	LO1G frequency range[3]	LO mode = Low	0.85		1.05		1.25	GHz
Switching[2]								
$t_{Rx\text{-}Tx}$	Receive-to-transmit switching time				1			µs
$t_{Tx\text{-}Rx}$	Transmit-to-Receive switching time				1			µs
$t_{POWER\ UP}$	Chip enable time				1			µs
$t_{PWR\ DWN}$	Chip disable time				1			µs

NOTES:
1. With simple external matching
2. With 50pF coupling capacitors on all RF and IF parts
3. This part has been optimized for the frequency range at 2.4–2.5 GHz. Operation outside this frequency range may yield performance other than specified in this datasheet.

Table 1. Truth Table

Chip-En	TxRx-SW	LNA-SW	LO-SW	Mode	LNA Gain	LO Freq. (Typ)
0	X	X	X	Sleep	N/S	N/S
1	0	1	1	Receive	+14dB	2.1GHz
1	0	0	1	Receive	-8dB	2.1GHz
1	0	1	0	Receive	+14dB	1.05GHz
1	0	0	0	Receive	-8dB	1.05GHz
1	1	X	1	Transmit	N/S	2.1GHz
1	1	X	0	Transmit	N/S	1.05GHz

FUNCTIONAL DESCRIPTION

The SA2420 is a 2.45GHz transceiver front-end available in the TSSOP-24 package. This integrated circuit (IC) consists of a low noise amplifier (LNA) and up- and down-converters. The injection of the local oscillator (LO) signal has two options: 1) direct injection of the LO signal at approximately 2GHz, or 2) injection of an LO signal at approximately 1GHz through an on-chip doubler. The SA2420 functions with a supply voltage range of 3 – 5 V (nominally). There is an enable/disable switch available to power up/down the entire chip in 1µs, typically. This transceiver has several unique features.

The LNA has two operating modes: 1) high gain mode with a gain = +14dB; and 2) low gain mode with a gain <-10dB. The switch for this option is internal and is controlled externally by high and low logic to the pin. When the LNA is switched into the attenuation mode, active matching circuitry (on-chip) is switched in (reducing the number of off-chip components required). To reduce power consumption when the chip is transmitting, the LNA is automatically switched into a “sleep” mode (internally) without the use of external circuitry.

The up and down frequency converters are single-ended at the RF port of the mixers. The up and down converters share the same (RF) pin and use an internal switch for transmitting (up-converting) or receiving (down-converting) modes. The switch is controlled externally by high and low logic states. The RF port is matched to 50Ω and has an input IP3 of +2.8dBm (mixer only). The down-convert mixer is buffered and has open collectors at the pins to allow for matching to common SAW filters. The up-convert mixer has differential inputs (IF port) and single-ended output (RF port), with an input pin to output pin gain of 17dB. The output of the up-converter is designed for a power level = +3dBm (P_{-1dB}). The mixers are fed by the two LO options.

The available LO options are: direct injection (2.1GHz at the pin) or through an on-chip doubler. The doubler has a simple LC bandpass filter (internal) at its output which passes the second harmonic to the mixers. Through an internal switch (controlled externally), either LO can be used depending on the designer’s application. If an application requires the use of a 1.05GHz VCO, then the doubler option would be used to double the frequency (2 × 1.05GHz = 2.1GHz) before being injected into the mixers. For a 2.1GHz VCO, the direct option would be used. With this option, the signal passes through an on-chip buffer and is then injected into the mixers.

Low voltage RF transceiver — 2.45 GHz

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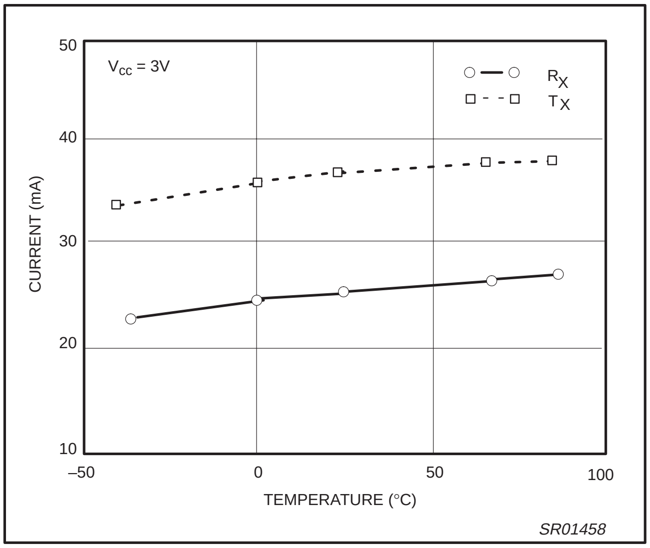


Figure 3. Rx & Tx Currents VS Temperature

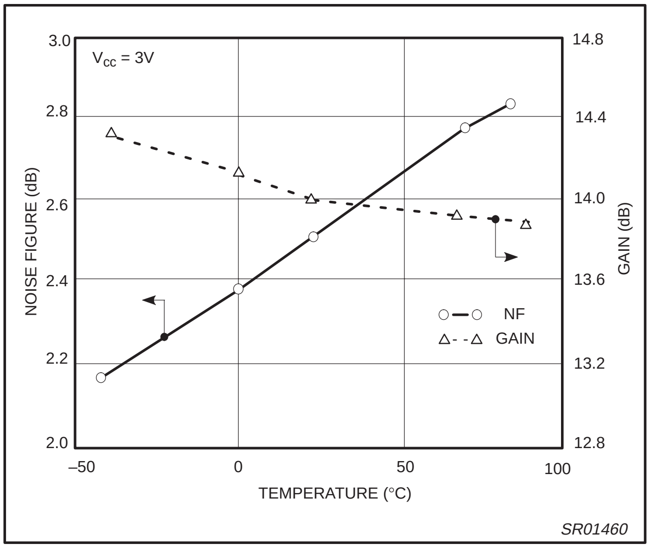


Figure 5. LNA Gain & 50Ω NF VS Temperature

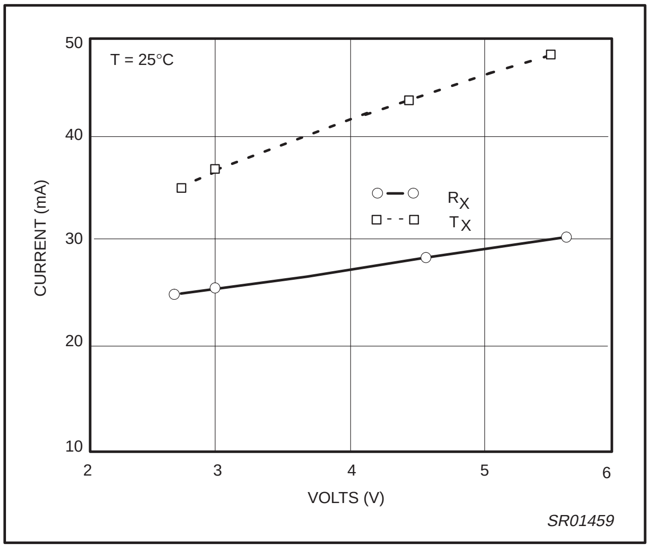


Figure 4. Rx & Tx Currents VS Voltage Supply

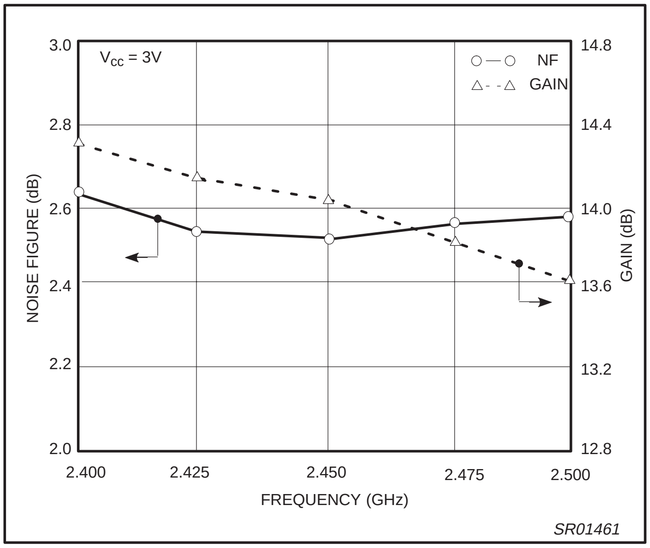


Figure 6. LNA Gain & 50Ω NF VS Frequency

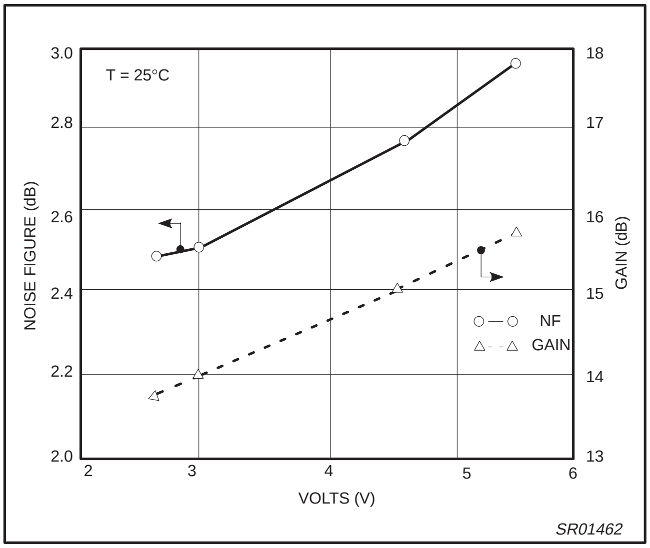


Figure 7. LNA Gain & 50Ω NF VS Supply Voltage

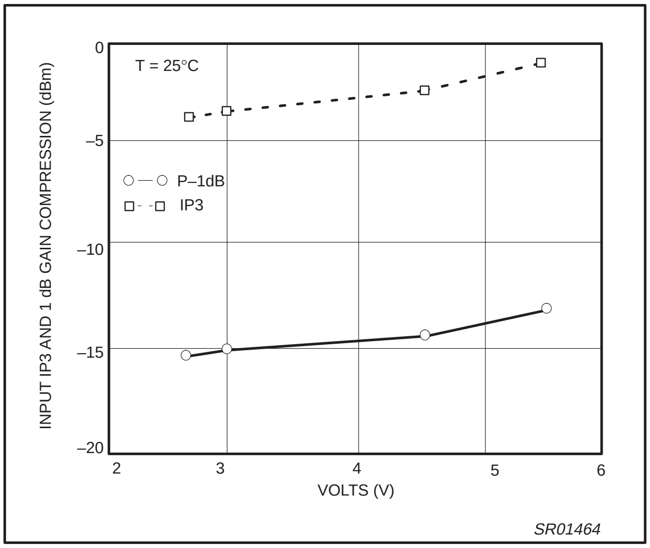


Figure 9. LNA Input IP3 and P–1dB VS Supply Voltage

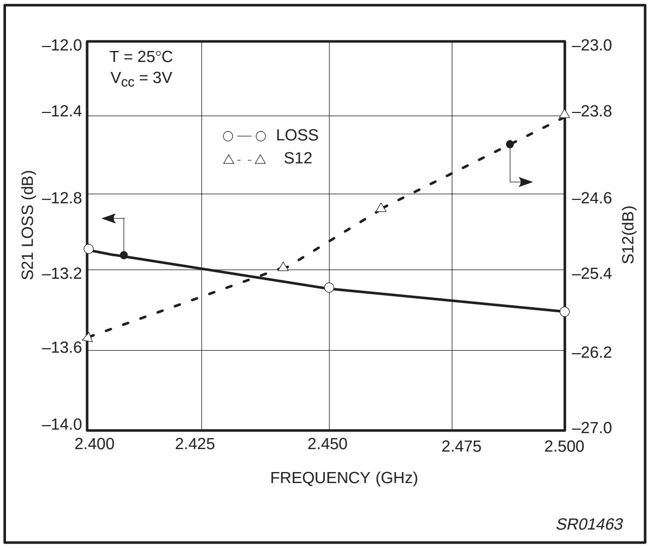


Figure 8. LNA Loss Mode & S12 VS Frequency

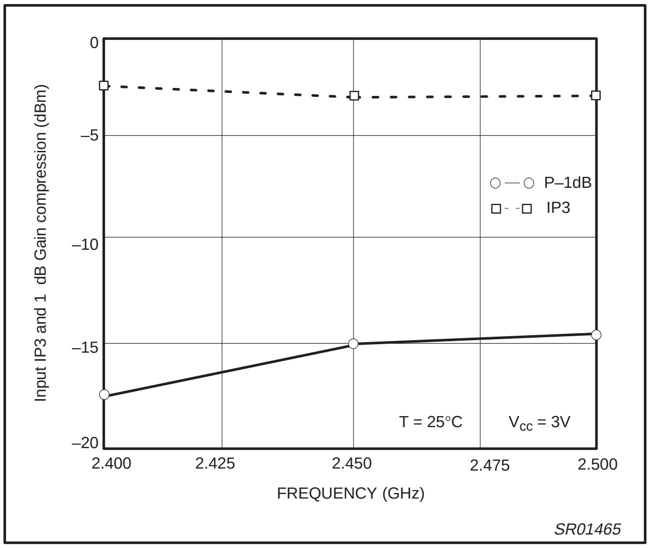


Figure 10. LNA Input IP3 and P–1dB VS Frequency

Low voltage RF transceiver — 2.45 GHz

SA2420

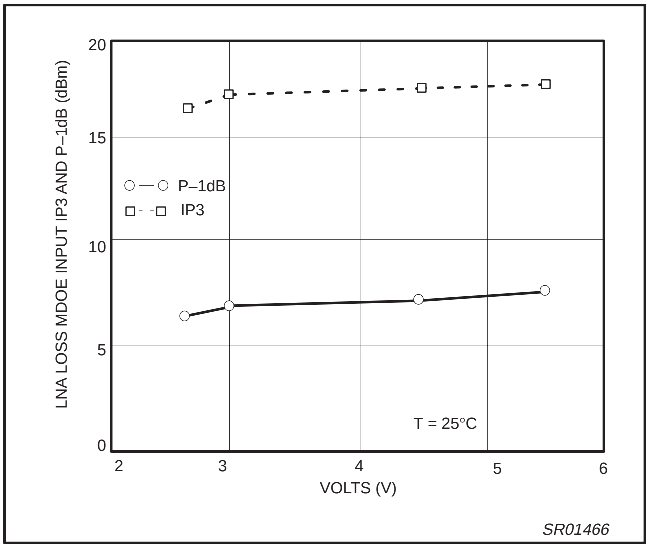


Figure 11. **LNA Loss Mode Input IP3 and P–1dB VS Voltage**

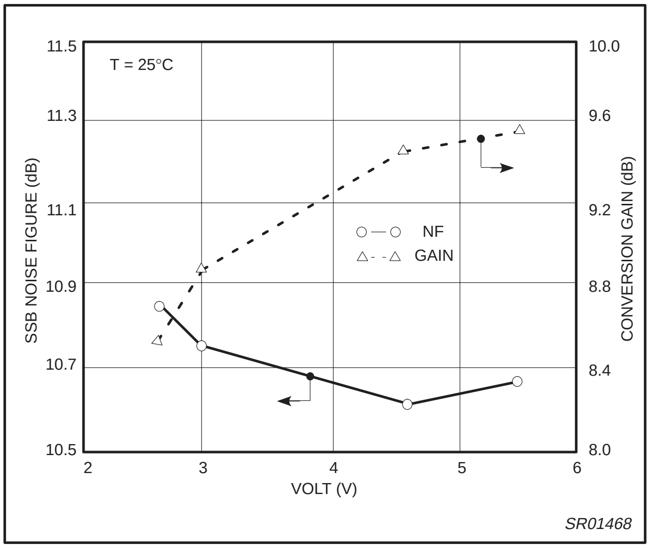


Figure 13. **Rx Mixer Conv. Gain & SSB NF VS Supply Voltage**

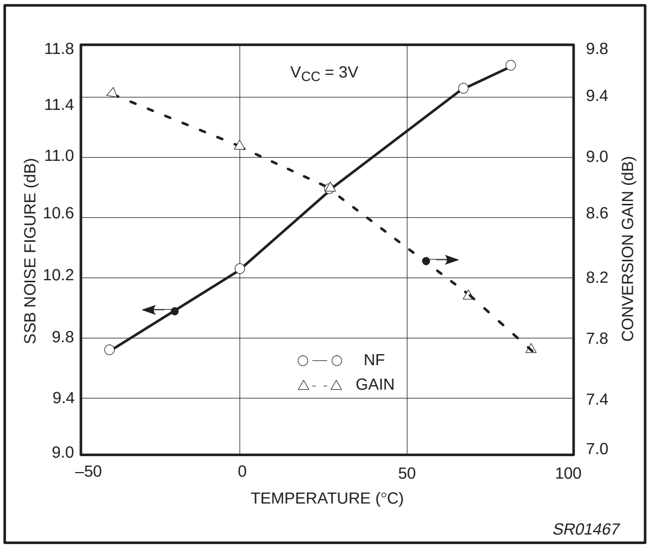


Figure 12. **Rx Mixer Conv. Gain & SSB NF VS Temperature**

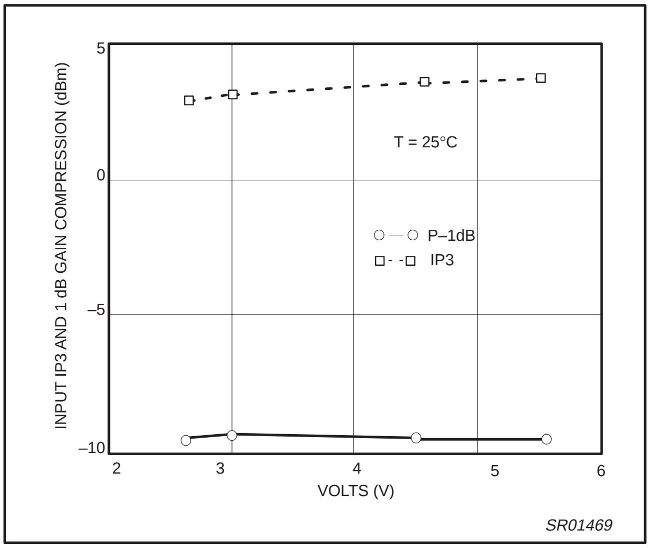


Figure 14. **Rx Mixer Input IP3 and P–1dB VS Supply Voltage**

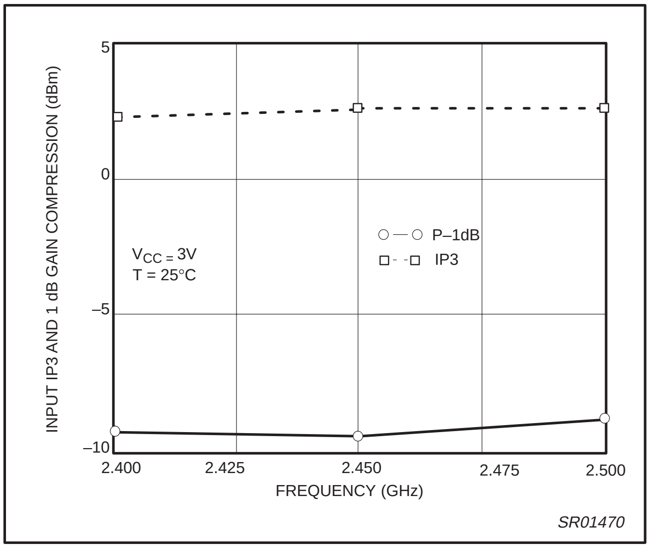


Figure 15. Rx Mixer Output IP3 and P–1dB VS Frequency

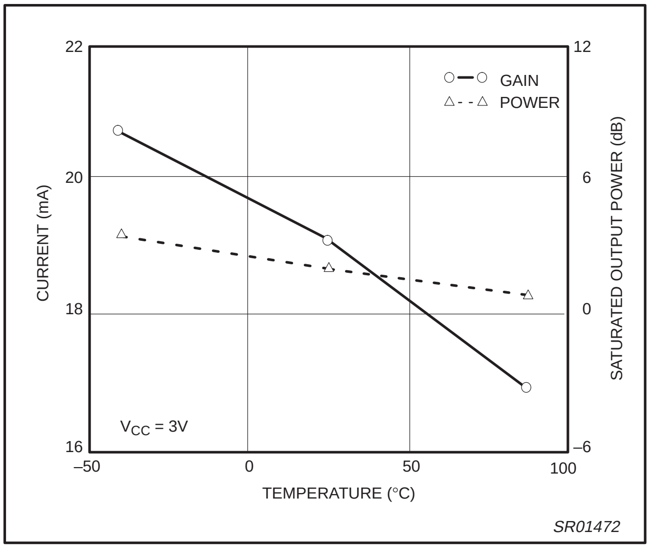


Figure 17. Tx Mx conv. Gain and Output Pwr VS Temp.

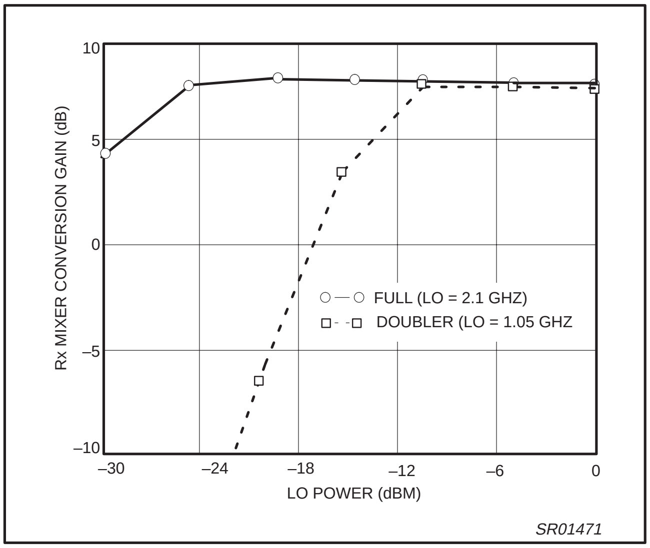


Figure 16. Rx Mixer Conversion Gain VS LO Power

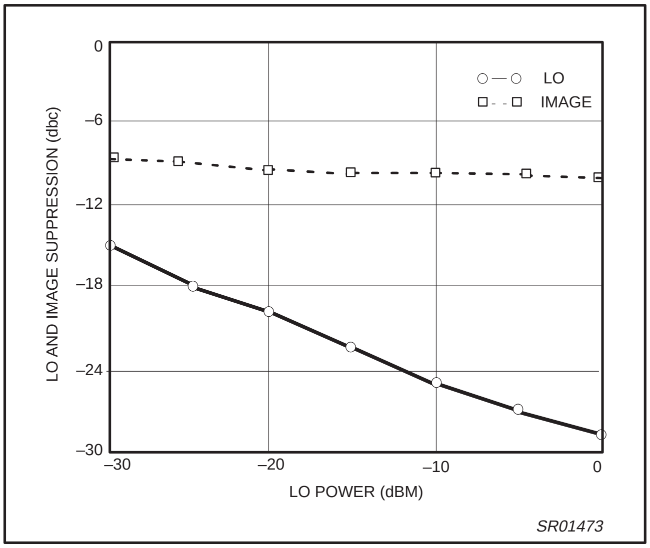


Figure 18. Tx Mixer LO and Image Suppression

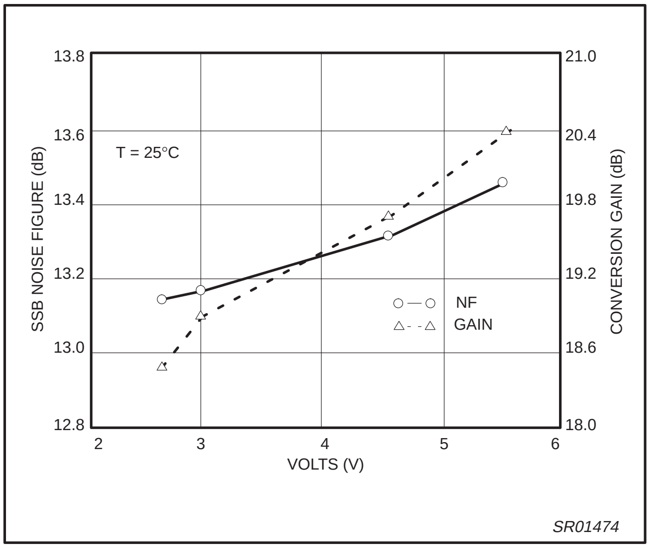


Figure 19. Tx Mixer Gain & NF VS Supply Voltage

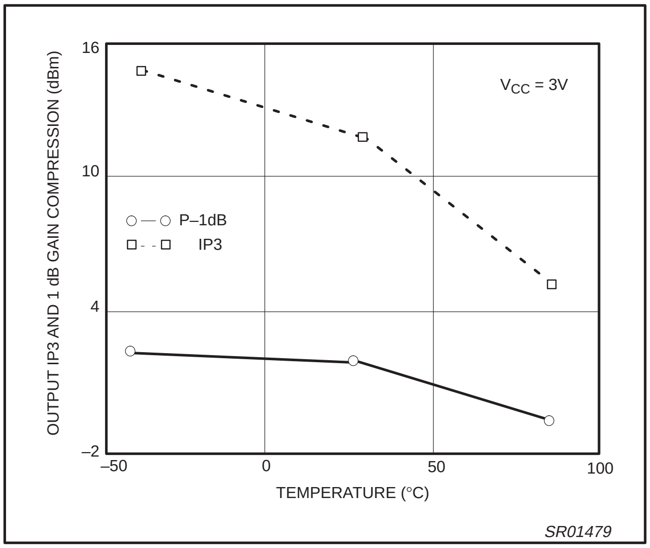


Figure 21. Tx Mixer Output IP3 and P–1dB VS Temperature

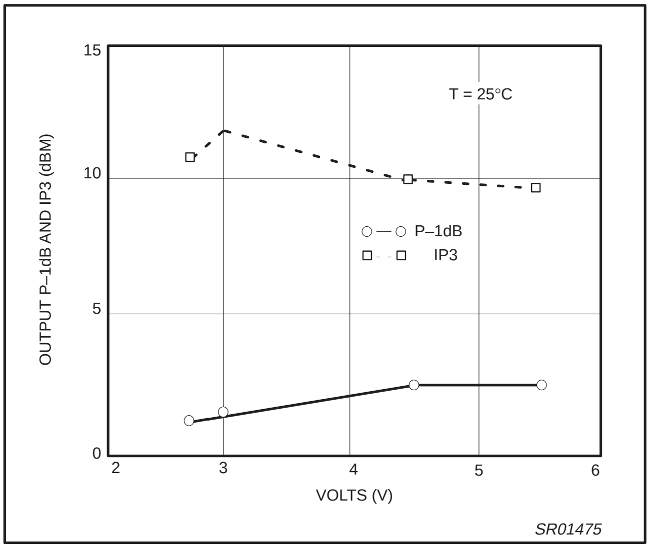


Figure 20. Tx Mixer Output P–1dB and IP3 Vs Voltage

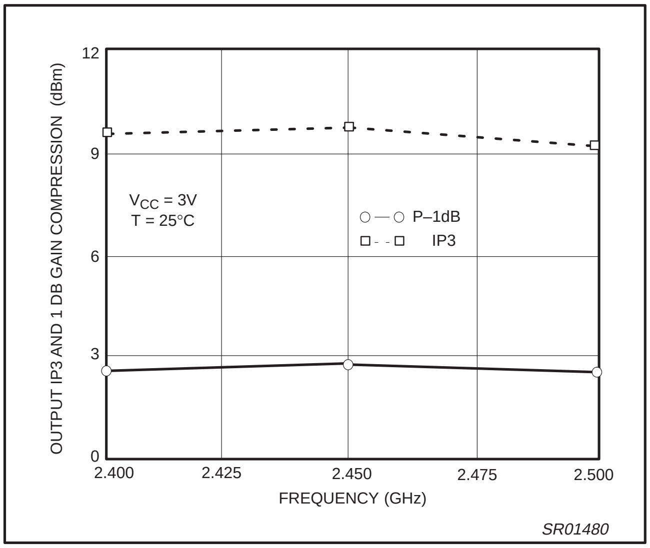


Figure 22. Tx Mixer Output IP3 and P–1dB VS Frequency

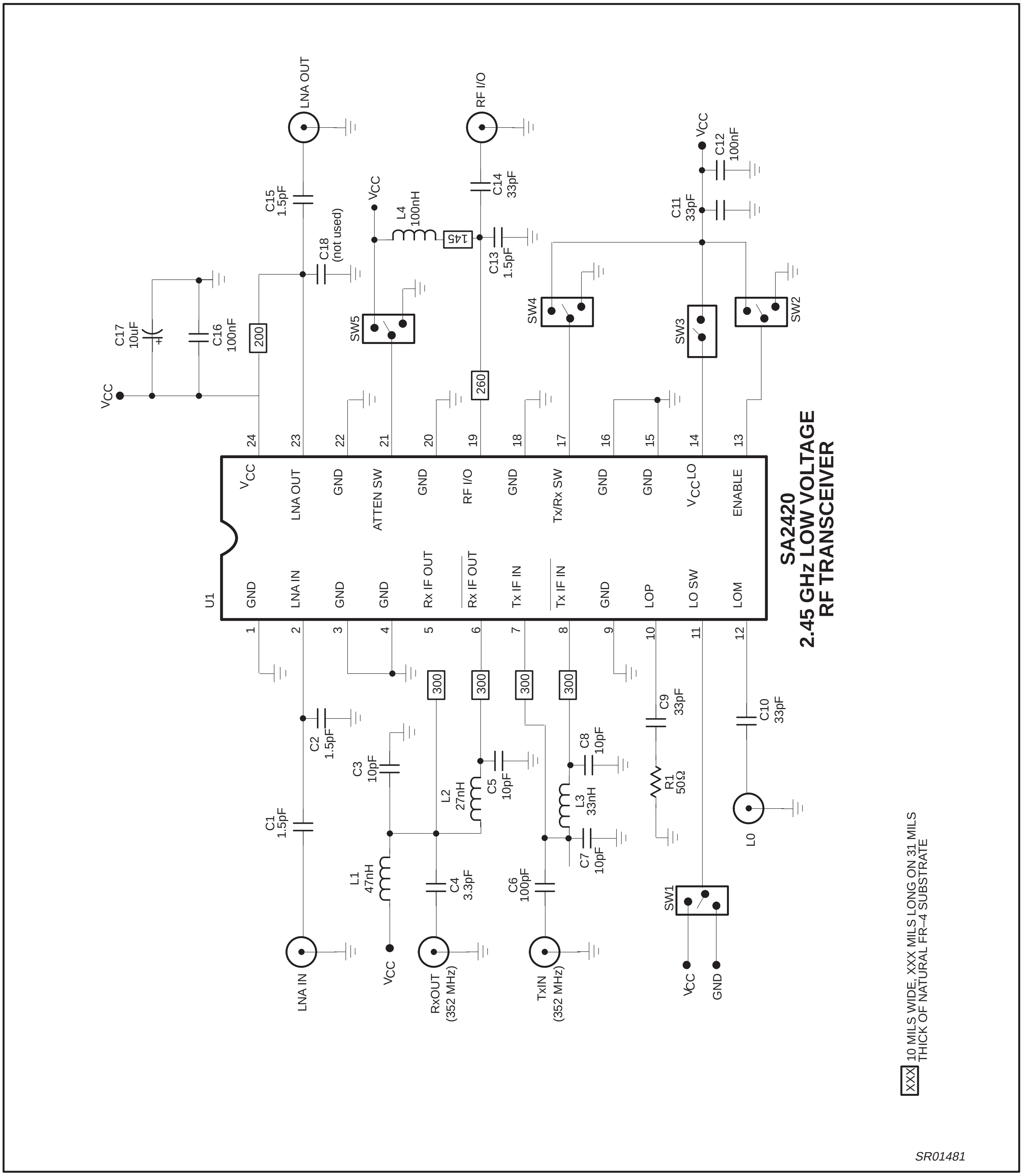

LNA OUT
RF I/O
VCC
C12
100nF
C15
1.5pF
VCC
L4
100nH
145
C14
33pF
C11
33pF
C18
(not used)
C13
1.5pF
C17
10uF
C16
100nF
200
SW5
SW4
SW3
SW2
VCC
260
24
23
22
21
20
19
18
17
16
15
14
13
VCC
LNA OUT
GND
ATTEN SW
GND
RF I/O
GND
Tx/Rx SW
GND
GND
VCCLO
ENABLE
U1
GND
LNA IN
GND
GND
Rx IF OUT
Rx IF OUT
Tx IF IN
Tx IF IN
GND
LOP
LO SW
LOM
1
2
3
4
5
6
7
8
9
10
11
12
SA2420
2.45 GHz LOW VOLTAGE
RF TRANSCEIVER
300
300
300
300
C9
33pF
C10
33pF
C2
1.5pF
C3
10pF
C8
10pF
C5
10pF
L2
27nH
R1
50Ω
L3
33nH
C1
1.5pF
C7
10pF
L0
L1
47nH
C4
3.3pF
C6
100pF
SW1
LNA IN
VCC
RxOUT
(352 MHz)
TxIN
(352 MHz)
VCC
GND
XXX
10 MILS WIDE, XXX MILS LONG ON 31 MILS
THICK OF NATURAL FR–4 SUBSTRATE
SR01481

Figure 23.

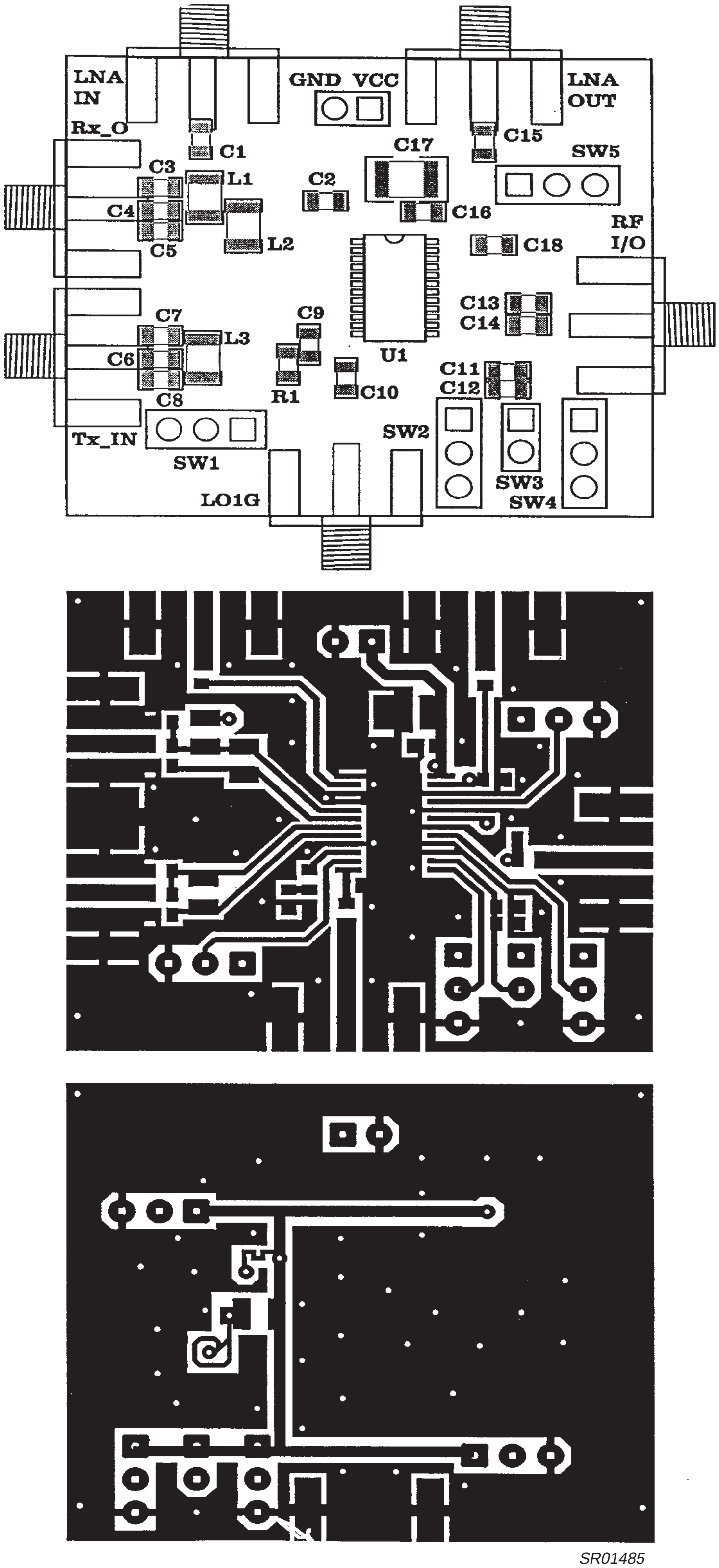
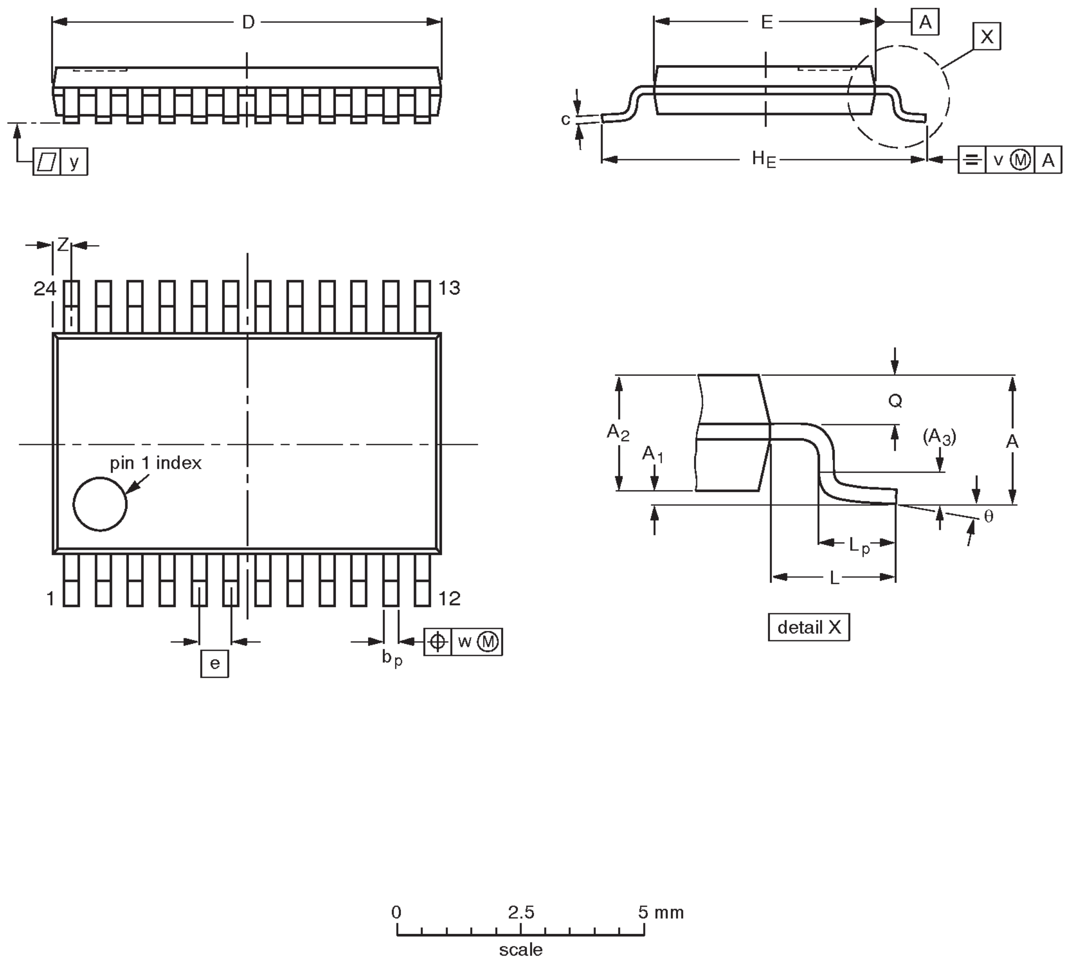


Figure 24. SA2420 RF Transciever

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

NOTES

Low voltage RF transceiver — 2.45GHz SA2420

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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