

## INTEGRATED CIRCUITS

# DATA SHEET



## SAA2013 Adaptive allocation and scaling for PASC coding in DCC systems

Preliminary specification  
File under Integrated Circuits, IC01

May 1994

Philips Semiconductors

**PHILIPS**

## Adaptive allocation and scaling for PASC coding in DCC systems

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### FEATURES

- Wide operating voltage range: 2.7 to 5.5 V
- Low power consumption: 13 mW; 3.0 V
- Low power decode mode: 1 mW; 5.0 V
- Sleep mode for low power and low Electromagnetic Interference (EMI)
- Sophisticated allocation algorithm
- Optimum sound quality
- Three-wire L3 bus microcontroller interface
- Stereo or 2-channel mono recording
- Small surface mounted package (QFP; SOT307).



### GENERAL DESCRIPTION

The SAA2013 performs the adaptive allocation and scaling function in the Precision Adaptive Sub-band Coding (PASC) system. It is not required in playback only applications, and is only used during recording. To complete the PASC processor, a SAA2003 stereo filter and codec is required.

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |                    |          |          |
|-------------|---------|--------------------|----------|----------|
|             | PINS    | PIN POSITION       | MATERIAL | CODE     |
| SAA2013H    | 44      | QFP <sup>(1)</sup> | plastic  | SOT307-2 |

#### Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the "Quality Reference Pocketbook" are followed. The pocketbook can be ordered using the code 9398 510 34011.

# Adaptive allocation and scaling for PASC coding in DCC systems

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## BLOCK DIAGRAM

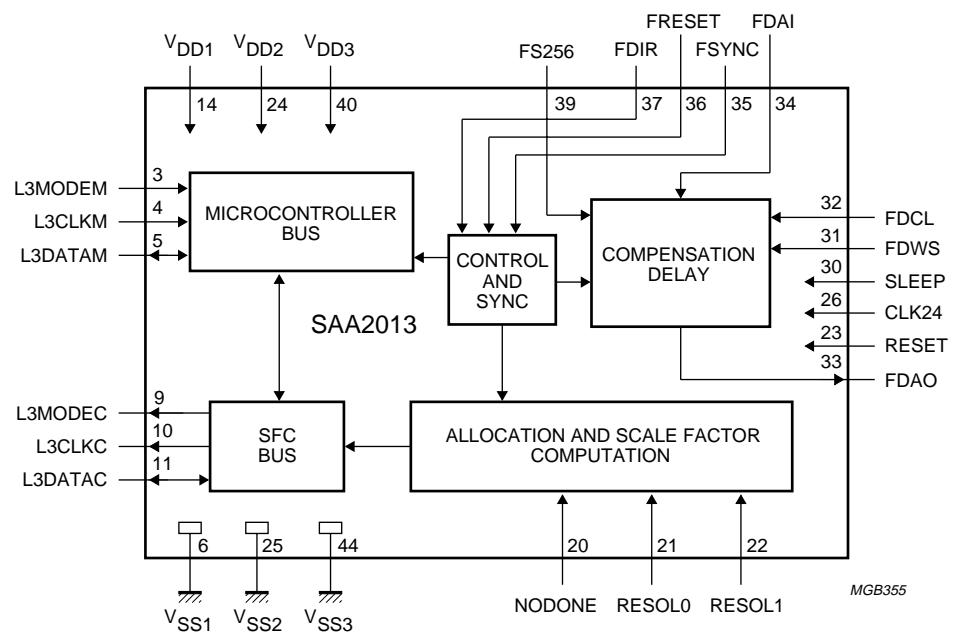


Fig.1 Block diagram.

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## PINNING

| SYMBOL           | PIN | DESCRIPTION  | TYPE |
|------------------|-----|--|------|
| TEST10           | 1   | test input; connect to V <sub>SS</sub>                       | I    |
| TEST11           | 2   | test input; connect to V <sub>SS</sub>                       | I    |
| L3MODEM          | 3   | microcontroller interface mode input                         | I    |
| L3CLKM           | 4   | microcontroller interface clock input                        | I    |
| L3DATAM          | 5   | microcontroller interface data 3-state input/output          | I/O  |
| V <sub>SS1</sub> | 6   | supply ground  | -    |
| TEST12           | 7   | test output; do not connect                                  | O    |
| TEST13           | 8   | test output; do not connect                                  | O    |
| L3MODEC          | 9   | codec interface mode output                                  | O    |
| L3CLKC           | 10  | codec interface clock output                                 | O    |
| L3DATAAC         | 11  | codec interface data 3-state input/output                    | I/O  |
| TEST1            | 12  | test output; do not connect                                  | O    |
| TEST2            | 13  | test output; do not connect                                  | O    |
| V <sub>DD1</sub> | 14  | supply voltage   | -    |
| TEST3            | 15  | test mode input; connect to V <sub>DD</sub>                  | I    |
| TEST4            | 16  | test mode input; connect to V <sub>DD</sub>                  | I    |
| TEST5            | 17  | test input; connect to V <sub>SS</sub>                       | I    |
| TEST6            | 18  | test input; connect to V <sub>SS</sub>                       | I    |
| TEST7            | 19  | test input; connect to V <sub>SS</sub>                       | I    |
| NODONE           | 20  | nodone state selection input; connect to V <sub>DD</sub>     | I    |
| RESOL0           | 21  | resolution selection 0 input                                 | I    |
| RESOL1           | 22  | resolution selection 1 input                                 | I    |
| RESET            | 23  | reset input; active HIGH                                     | I    |
| V <sub>DD2</sub> | 24  | supply voltage   | -    |
| V <sub>SS2</sub> | 25  | supply ground  | -    |
| CLK24            | 26  | 24.576 MHz clock input                                       | I    |
| LOWPWR           | 27  | low power decode select input                                | I    |
| POR              | 28  | power on reset input   | I    |
| TEST8            | 29  | test input; connect to V <sub>SS</sub>                       | I    |
| SLEEP            | 30  | sleep mode select input                                      | I    |
| FDWS             | 31  | filtered data word select                                    | I    |
| FDCL             | 32  | filtered data clock  | I    |
| FDAO             | 33  | filtered data output   | O    |
| FDAI             | 34  | filtered data input  | I    |
| FSYNC            | 35  | sub-band synchronization on filtered I <sup>2</sup> S bus    | I    |
| FRESET           | 36  | reset signal input from SAA2003                              | I    |
| FDIR             | 37  | filtered data direction input                                | I    |
| TEST9            | 38  | test input; connect to V <sub>SS</sub>                       | I    |
| FS256            | 39  | system clock input; 256 × sample frequency (f <sub>s</sub> ) | I    |
| V <sub>DD3</sub> | 40  | supply voltage   | -    |

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| SYMBOL           | PIN | DESCRIPTION   | TYPE |
|------------------|-----|---------------|------|
| n.c.             | 41  | not connected | —    |
| n.c.             | 42  | not connected | —    |
| n.c.             | 43  | not connected | —    |
| V <sub>SS3</sub> | 44  | supply ground | —    |

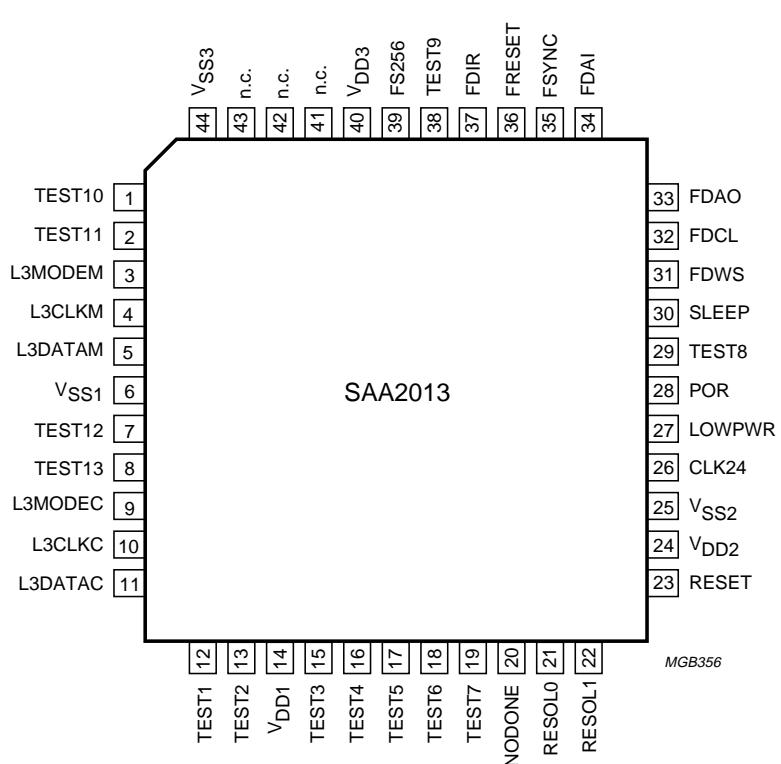


Fig.2 Pin configuration.

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## FUNCTIONAL DESCRIPTION

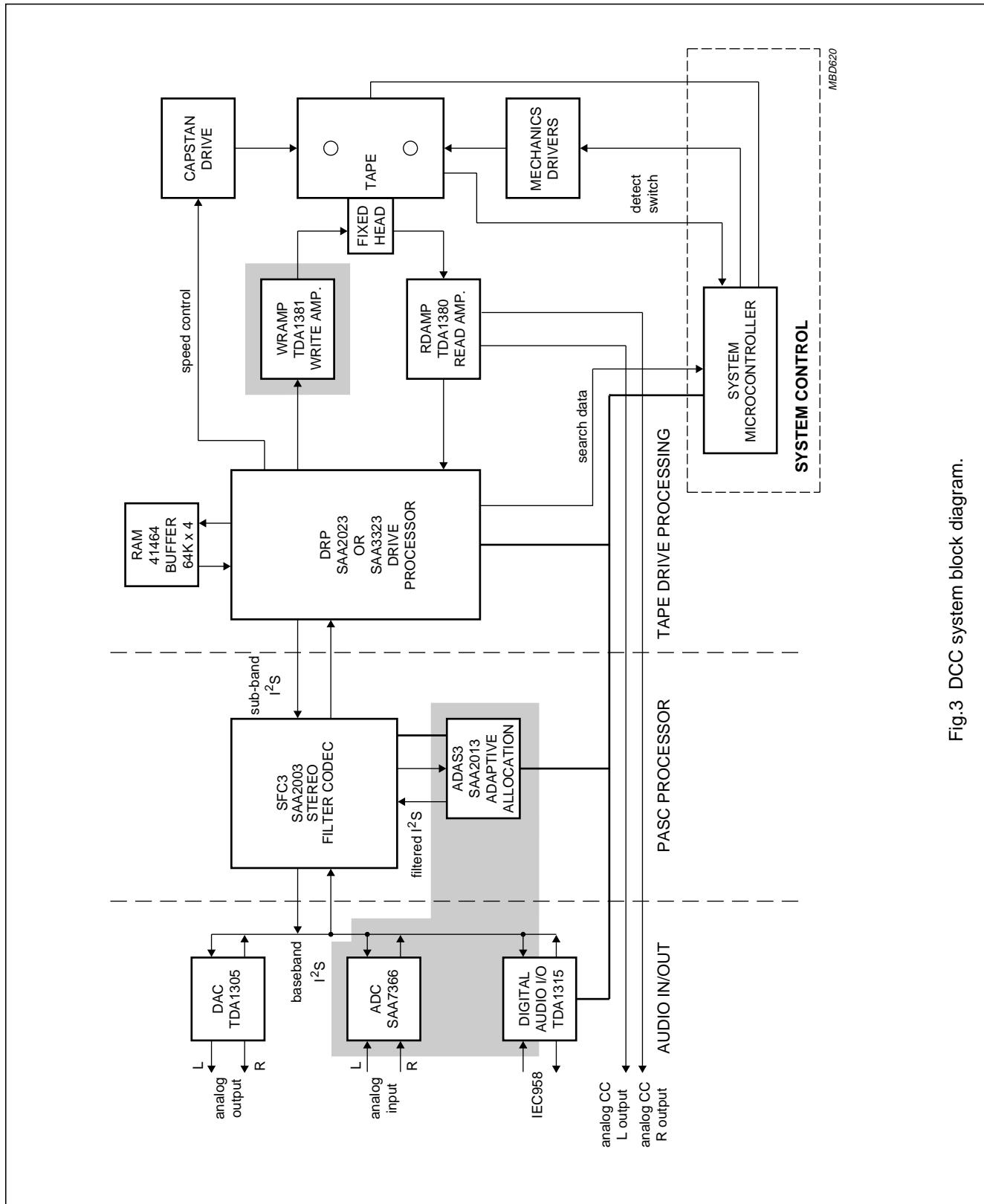


Fig.3 DCC system block diagram.

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### PASC processor

The PASC processor is a dedicated Digital Signal Processor (DSP) engine which efficiently codes digital audio data at a bit rate of 384 kbits/s without affecting the sound quality. This is achieved using an efficient adaptive data notation and by only encoding the audio information which can be heard by the human ear.

The audio data is split into 32 equal sub-bands during encoding. For each of the sub-bands a masking threshold is calculated. The samples from each of the sub-bands are included in the PASC data with an accuracy that is determined by the available bit-pool and by the difference between the signal power and the masking threshold for that sub-band. In decode, the sub-band signals are reconstructed into the full bandwidth audio signal.

The stereo filter codec performs the splitting (encoding) and reconstruction (decoding), including the necessary formatting functions. During encoding, the adaptive allocation and scaling circuit calculates the required accuracy (bit allocation) and scale factors of the sub-band samples.

### Decode/encode control

Selection of decode or encode is controlled using FRESET and FDIR. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal

to determine the operation mode. When FDIR is HIGH, SAA2013 is in decode mode. When FDIR is LOW the SAA2013 is in encode mode. See Fig.4.

### Reset

When used with low-power mode disabled (LOWPWR = V<sub>SS</sub>), and with the SLEEP input LOW, SAA2013 is reset if the RESET pin is held HIGH for at least 5 periods of the CLK24 clock, see Fig.5. SAA2013 defaults to decode mode. When in low-power mode, the RESET pin is disabled.

### Sleep mode

Sleep mode is entered by taking the SLEEP input HIGH with the LOWPWR pin connected to V<sub>SS</sub>; CLK24 and FS256 are stopped internally to the SAA2013, the 3-state buffers will have a high impedance, and outputs will freeze in the same state as just before the sleep mode became active (clocks stopped). To come out of sleep mode, the SLEEP input must be taken LOW again. To clear data present from before sleep was entered, this should be followed by a reset, see Fig.5.

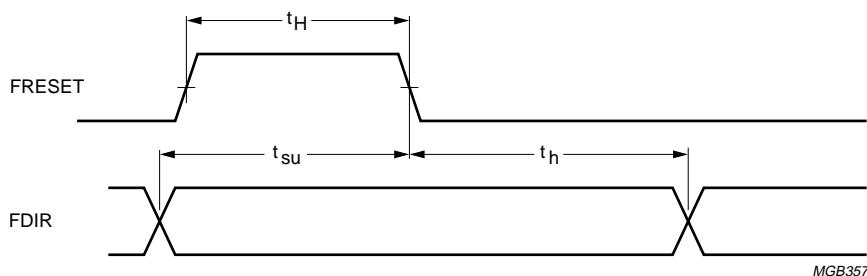


Fig.4 FDIR and FRESET timing.

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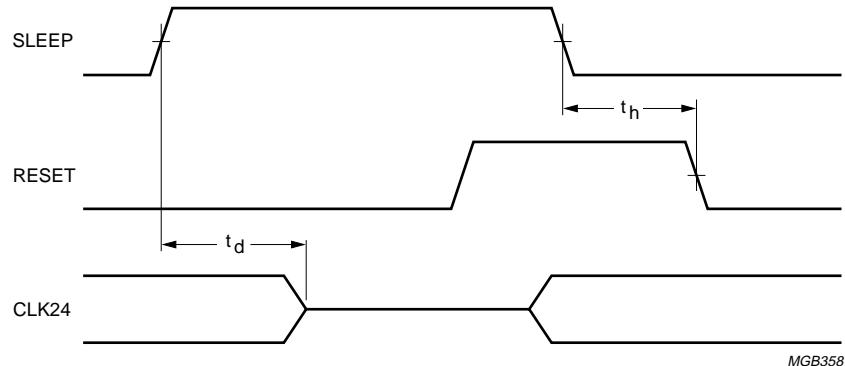


Fig.5 SLEEP and RESET timing.

### Low-power decode mode

Low-power decode mode is made available by connecting the LOWPWR pin to  $V_{DD}$ . With  $LOWPWR = V_{DD}$ , low-power decode mode is entered 9 cycles of CLK24 after the SLEEP input is taken HIGH. In low-power decode mode, the L3 bus connections are connected straight through the SAA2013, which is effectively bypassed. The compensation delay connection between pins FDAI and FDAO is no longer needed by the SAA2003, and CLK24 and FS256 are stopped internally to the SAA2013.

To get out of low-power decode mode, it is necessary to take SLEEP LOW, FDIR LOW, and FRESET HIGH (in a normal application taking FDIR LOW and FRESET HIGH can be achieved by setting SAA2003 into encode mode), SAA2013 then performs an internal reset, and defaults to normal decode mode. The RESET pin does not reset the circuit from low-power decode mode.

### Power-On Reset (POR)

When low-power decode mode is enabled ( $LOWPWR = V_{DD}$ ), a power-on reset circuit is required to ensure that the internal clocks are connected correctly at power-on. A suitable circuit is shown in Fig.6. This circuit will correctly reset the internal clock connection provided that the nominal value of the  $V_{DD}$  supply is reached within 40 ms at power-on.

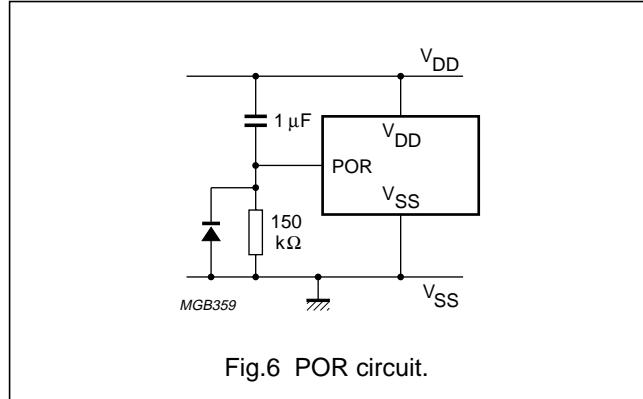


Fig.6 POR circuit.

### Encode mode

In encode mode the SAA2013 receives sub-band filtered samples from SAA2003 on the FDAI pin. The SAA2013 has to collect a complete frame of sub-band data before the allocation and scale factor information can be calculated. So that the allocation and scale factor information is available in the same time frame as the audio samples at the output, the sub-band filtered samples are delayed by 480 FDWS periods.

One FDWS period is equal to  $\frac{1}{f_s}$  where  $f_s$  is the audio sample rate of 32, 44.1 or 48 kHz. The delayed samples are passed to the codec part of SAA2003 on the FDAO pin.

## Adaptive allocation and scaling for PASC coding in DCC systems

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For each sub-band frame, SAA2013 calculates the allocation and scale factor index information required by the SAA2003. In order to synchronize the codec part of SAA2003, SAA2013 frequently requests status information from the codec. It monitors sample frequency, emphasis information and stereo mode, and uses the ready-to-receive bit of the codec to determine when to transfer information.

### Decode mode

In decode the SAA2003 will transfer samples from FDAI to FDAO with a delay of 480 FDWS periods. Settings and status information can be sent to SAA2003 via SAA2013, but the SAA2013 does not itself act on this information. Transfer of this information is automatically synchronized to the ready-to-receive bit of SAA2003 by SAA2013.

### Audio sample resolution section

The SAA2013 is designed for operation with audio input sources of 14, 15, 16 or 18-bit resolution.

For optimum audio performance the bit allocation algorithm of the SAA2013 can be varied to suit the bit resolution of the audio source. This is done with the pins RESOL0 and RESOL1 as shown in Table 1.

**Table 1** Resolution set by pins RESOL0 and RESOL1.

| RESOLUTION | RESOL0 | RESOL1 |
|------------|--------|--------|
| 16 bits    | 0      | 0      |
| 18 bits    | 0      | 1      |
| 14 bits    | 1      | 0      |
| 15 bits    | 1      | 1      |

### Filtered data interface

The filtered data interface signals are given in Table 2.

**Table 2** Filtered data interface signals.

| PIN   | INPUT/OUTPUT | FUNCTION                               | FREQUENCY |
|-------|--------------|--|-----------|
| FDWS  | input        | filtered data interface word select    | $f_s$     |
| FDCL  | input        | filtered data interface bit clock      | $64f_s$   |
| FDAI  | input        | filtered data input                    | —         |
| FDAO  | output       | filtered data output                   | —         |
| FSYNC | input        | filtered data sub-band synchronization | —         |

The filtered data interface transfers sub-band filtered samples between the stereo filter codec SAA2003 and SAA2013. The interface is similar to a normal I<sup>2</sup>S interface, consisting of clock (FDCL), data (FDAI/FDAO) and word select lines (FDWS), except that the samples sent represent signals divided into 32 sub-bands. One frame of data consists of 12 samples from 32 sub-bands for both left and right channels, i.e.: 768 audio samples. Each audio sub-band sample is represented by a 24-bit two's complement number.

The order in which the samples are sent is shown in Table 3.

For two channel mono, the order is the same, but with Channel 1 samples in the place of left and Channel 2 samples in place of right.

**Table 3** Order of samples.

| SUB-BAND | 0  | 0  | 1  | 1  | 2  | 2  | ... | 31 | 31 |
|----------|----|----|----|----|----|----|-----|----|----|
| Channel  | L  | R  | L  | R  | L  | R  | ... | L  | R  |
| Sample   | 0  | 0  | 0  | 0  | 0  | 0  | ... | 0  | 0  |
|          | 1  | 1  | 1  | 1  | 1  | 1  | ... | 1  | 1  |
|          | 2  | 2  | 2  | 2  | 2  | 2  | ... | 2  | 2  |
|          | .  | .  | .  | .  | .  | .  | ... | .  | .  |
|          | .  | .  | .  | .  | .  | .  | ... | .  | .  |
|          | 11 | 11 | 11 | 11 | 11 | 11 | ... | 11 | 11 |

The signal FSYNC is used between each PASC frame to indicate the sending of samples for sub-band 0 (Fig.7).

## Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

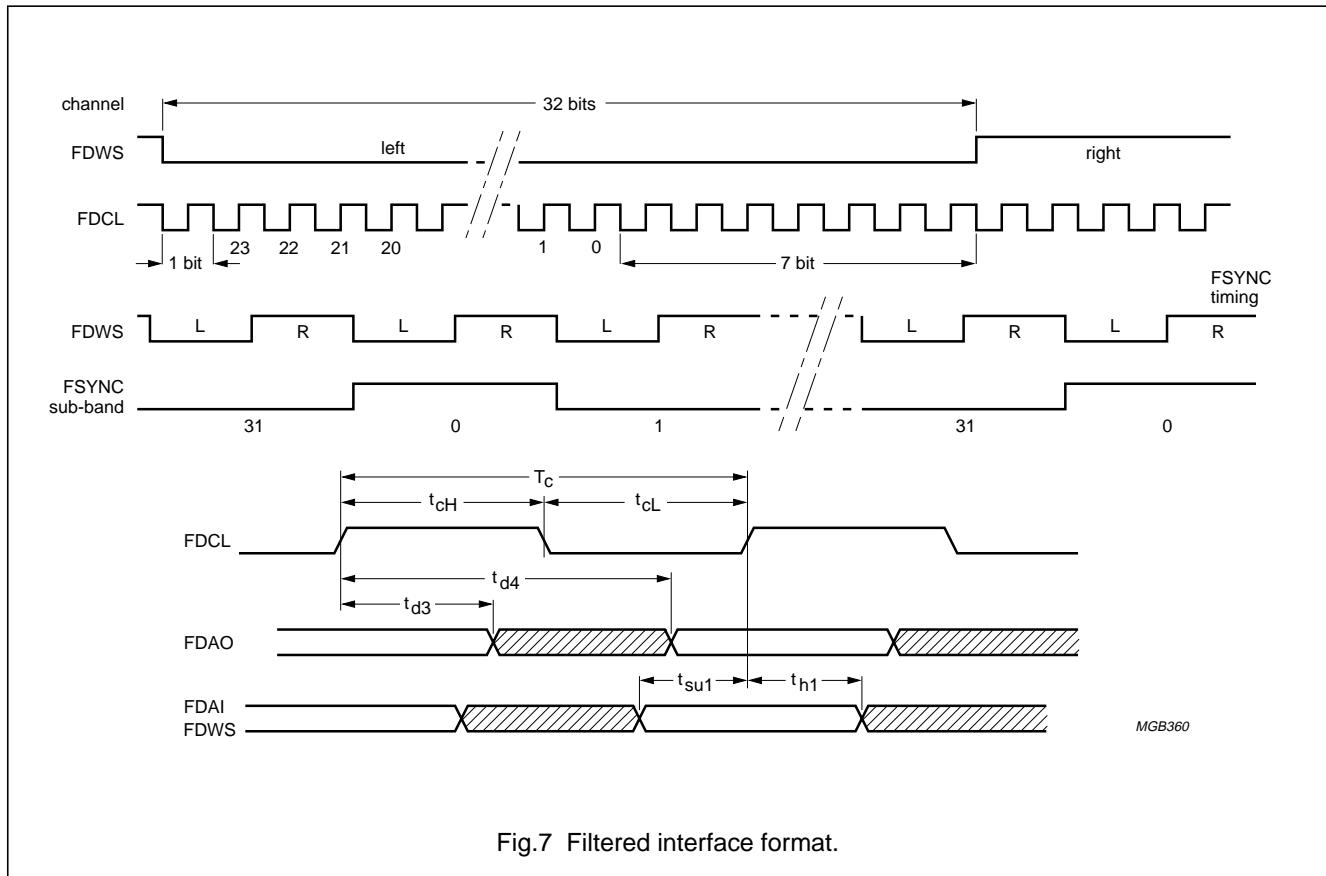


Fig.7 Filtered interface format.

### Control interfaces

Two 3-wire control interfaces are provided (referred to as 'L3' interfaces). One is connected to the system microcontroller (L3MODEM, L3CLKM, L3DATAM where 'M' represents microcontroller), the other to SAA2003 (L3MODEC, L3CLKC, L3DATAC where 'C' represents codec). In general, control data is passed between SAA2003 and the microcontroller via SAA2013. This ensures that the microcontroller is buffered from the time-critical SAA2013 to SAA2003 interface during encode.

The SAA2013 does not interpret the data from the microcontroller interface.

Status information from the codec is interpreted to ensure that SAA2013 quickly acts upon the status of SAA2003.

The L3 bus operation is shown in Fig.8. There are three modes:

1. Address.
2. Data.
3. Halt.

Each interface operates as either a master or a slave, where the master provides L3CLK and L3MODE. For the microcontroller to SAA2013 interface, the microcontroller is the master. For the SAA2013 to SAA2003 interface, SAA2013 is the master.

## Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

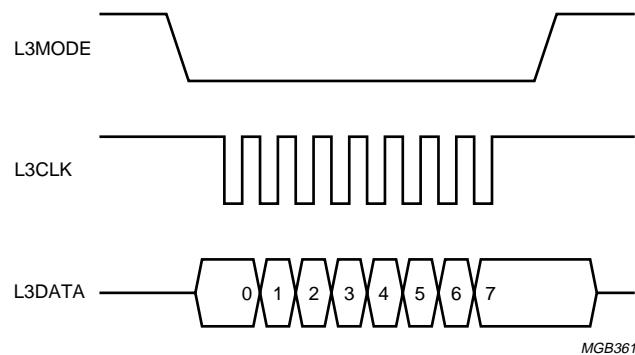


Fig.8 L3 bus operation; address mode.

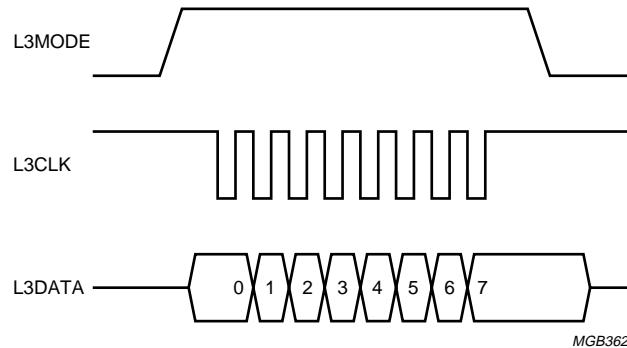


Fig.9 L3 single byte transfer.

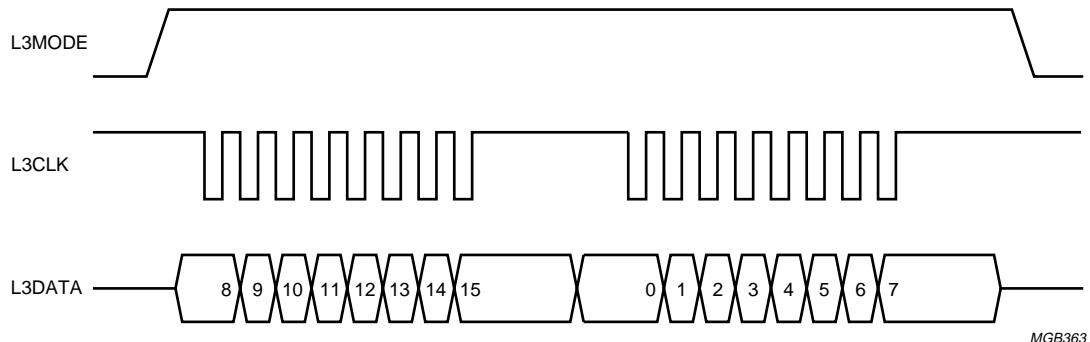


Fig.10 L3 bus two byte transfer.

## Adaptive allocation and scaling for PASC coding in DCC systems

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### ADDRESS MODE

Address mode is entered by the master pulling L3MODE LOW. This causes the L3DATA line to act as an input on the slave, and 8 bits of address data are clocked into the slave. If the slave recognizes the address, it will set-up its internal state based on the 2 Least Significant Bits (LSBs) of the address. The slave then expects to send status data or receive control data.

The addresses for SAA2013 are shown in Table 4.

**Table 4** SAA2013 addresses.

| MSB  | LSB  | L3 OPERATION MODE | FUNCTION               |
|------|------|-------------------|------------------------|
| 0010 | 0000 | WDAT              | extended settings      |
| 0010 | 0001 | RDAT              | allocation information |
| 0010 | 0010 | WCMD              | settings               |
| 0010 | 0011 | RSTAT             | status/peak read       |

The interface may be reset by sending an address of all zeros ('00000000'). This may be used to allow inter-operation with other devices sharing the L3CLK and L3DATA lines (e.g. SAA7345 CD decoder).

### DATA MODE

In data mode, bytes of data are clocked into (e.g. control) or out of (e.g. status) the slave. A single byte transfer is shown in Fig.9. A two byte transfer is shown in Fig.10, between bytes there must be a pause during which the clock remains HIGH.

### HALT MODE

Halt mode consists of pulling L3MODE LOW after sending data. It is used for marking the end of a data transfer mode which does not have an internal bit counter.

### SAA2013 interface modes

The SAA2013 may be used to read and write from or to SAA2003. Information is transferred via a set of transit registers within SAA2013.

### DECODE OPERATION

During decode, the SAA2013 does not perform allocation. Therefore no allocation and scale factor indices are sent to SAA2003. Settings and extended settings may still be sent to SAA2003, and SAA2013 monitors the status of the codec by reading status from it after every occurrence of FSYNC. Peak level data can also be transferred from SAA2003.

### ENCODE OPERATION

In encode, the same information may be sent as for decode, and in addition, allocation/scale factor indices are sent to the codec by SAA2013.

The interface modes are shown in Table 5.

## Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

**Table 5** Interface modes.

| MODE   | ADDRESS |       | INTERFACE MODE    | LENGTH (BITS) | DIRECTION                  |
|--------|---------|-------|-------------------|---------------|----------------------------|
|        | BIT 1   | BIT 0 |                   |               |                            |
| Decode | 0       | 0     | extended settings | 8             | microcontroller to SAA2003 |
|        | 0       | 1     | –                 | –             | –                          |
|        | 1       | 0     | settings          | 16            | microcontroller to SAA2003 |
|        | 1       | 1     | status/peak       | 16 or 48      | SAA2003 to microcontroller |
| Encode | 0       | 0     | extended settings | 8             | microcontroller to SAA2003 |
|        | 0       | 1     | allocation/scale  | 48 × 16       | SAA2013 to SAA2003         |
|        | 1       | 0     | settings          | 16            | microcontroller to SAA2003 |
|        | 1       | 1     | status/peak       | 16 or 48      | SAA2003 to microcontroller |

**PRIORITY**

Each type of transfer has a priority. The priorities are:

1. Allocation/scale/settings (highest priority).
2. Status read.
3. Peak read.
4. Extended settings (lowest priority).

**ALLOCATION AND SCALE FACTOR TRANSFER**

The allocation and scale factor information sent from SAA2013 to SAA2003 during encode has the highest priority. The other types of transfer interleaved with the allocation/scale information.

**SETTINGS TRANSFER**

This is a 16-bit transfer. The microcontroller sends settings to SAA2003. SAA2013 only transfers these without taking notice of the contents. In encode, the settings are held in

the transit registers, and sent next time that allocation is being sent. In decode, settings are sent as soon as possible subject to the RTRC flag from SAA2003.

Before sending settings the microcontroller should read the status of SAA2013 to examine the Ready-To-Receive bit Settings (RTS). After the settings have been received by SAA2013, RTS will be made logic 0, until the settings have been sent to SAA2003. Only after RTS is logic 1 again may the microcontroller send new settings.

**STATUS READ**

Status and peak information may be read from SAA2003 by the microcontroller. The status bits are defined in Table 6.

**Table 6** Status bits.

| BIT         | NAME                        | FUNCTION                            | VALID IN      |
|-------------|-----------------------------|-------------------------------------|---------------|
| B15 to B12  | bit rate index              | bit rate indication                 | encode/decode |
| B11 and B10 | sample frequency indication | 44.1, 48, 32 kHz indication         | encode/decode |
| B9          | RTRS (settings)             | 1 = ready; 0 = not ready            | encode/decode |
| B8          | RTRE (external settings)    | 1 = ready; 0 = not ready            | encode/decode |
| B7 and B6   | MODE                        | sub-band signal mode identification | encode/decode |
| B5          | SYNC                        | synchronization indication          | encode/decode |
| B4          | CLKOK                       | 1 = OK; 0 = not OK                  | encode/decode |
| B3 and B2   | Tr0 and Tr1                 | transparent bits                    | encode/decode |
| B1 and B0   | EMPHASIS                    | emphasis indication                 | encode/decode |

## Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

Since the two bytes of status information are sampled separately, the bytes may result from different sub-band frames.

The only valid bit rate code for the SAA2013 is 1100.

The sample frequency indication is shown in Table 7.

**Table 7** Sample frequency indication.

| BIT 11 | BIT 10 | SAMPLE FREQUENCY  |
|--------|--------|-------------------|
| 0      | 0      | 44.1 kHz; default |
| 0      | 1      | 48.0 kHz          |
| 1      | 0      | 32.0 kHz          |
| 1      | 1      | do not use        |

Ready-to-receive S or E indicates whether the SAA2013 is ready-to-receive new settings or extended settings from the microcontroller. This should be checked before sending new information.

For details of the MODE, SYNC, CLKOK and transparent bits, refer to the "SAA2003 data sheet".

The emphasis indication can be used to apply the correct de-emphasis. In encode SAA2013 will correct the calculated allocation if  $50/15$   $\mu$ s emphasis is applied. When "CCITT J.17" emphasis is applied, the bit allocation remains the same as when no emphasis is applied.

The 2 bytes of the status are 'sampled' at different moments. So the information may not result from the same sub-band frame.

When making repeated status reads (for instance reading the RTRS/RTRE flags before sending settings or extended settings), the microcontroller **must** send an address before each status read, to ensure that the byte counter in the interface is reset to logic 0. If this is not done, then the peak data will be read. Conversely, it is important **not** to send a new address after a status read if the peak data is required.

### PEAK READ

Peak information is read by clocking a further 4 bytes of data after a status read. The data format is shown in Figs 11 and 12. Bits B17 to B31 contain a 15-bit unsigned peak, LSB first, channel indicated by bit B16. Bits B33 to B47 contain a 15-bit unsigned peak, channel indicated by bit B32.

The peak data is delayed by 1 read period. If for example the microcontroller reads peak level data every 50 ms, the peak data sourced by SAA2013 will be 50 ms old. Also it

is possible that peak data may contain an additional delay of 1 column (667  $\mu$ s minimum at 48 kHz, 1 ms maximum at 32 kHz). If the microcontroller attempts to read peak level data with a delay of less than 1 column, the peak level data from the previous reading will be repeated. Normally the microcontroller should allow at least 1 ms between reads. There is also a delay required between peak data words (Fig.13).

If the SAA2013 does not have peak data available (for instance the microcontroller attempts two reads in very quick succession), it will return all peak data bits set to logic 0. The microcontroller can detect if valid peak data has been returned by inspecting bits T16 and T32. If both bits are set to logic 0 the data is not valid.

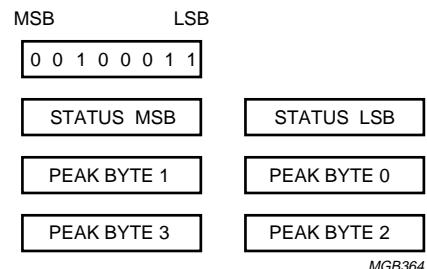


Fig.11 Peak level read format; SAA2013 to microcontroller.

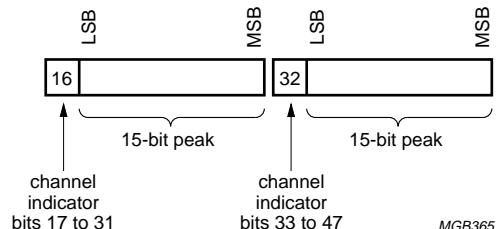


Fig.12 Peak level format.

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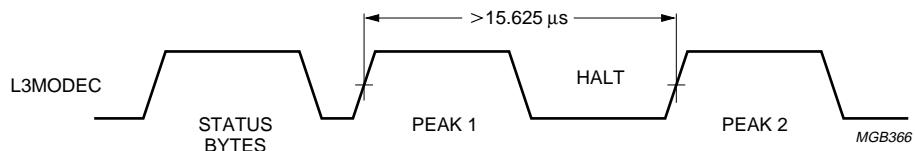


Fig.13 Peak data timing.

### EXTENDED SETTINGS

This is a single byte transfer, valid during decode and encode. The sequence of operations is:

1. Microcontroller reads status from SAA2013, waiting for the flag RTRE to be set.
2. When RTRE is logic 1, the microcontroller writes address bit 0 is logic 0, bit 1 is logic 0.
3. One byte of extended settings is clocked into the transit register (SAA2013).
4. When it is possible (i.e. subject to RTRC being HIGH, and assuming that allocation or status is not waiting), the byte is transferred from the transit register to the SAA2003.

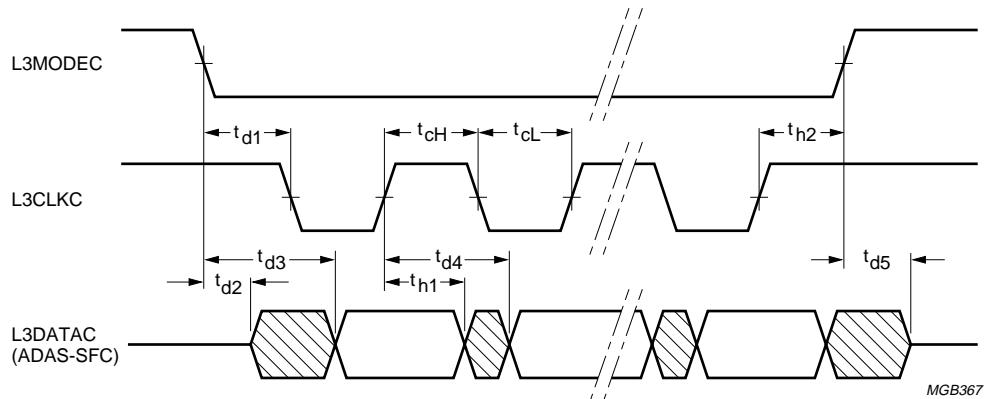


Fig.14 L3 interface timing; SAA2013 to SAA2003 (address mode).

## Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

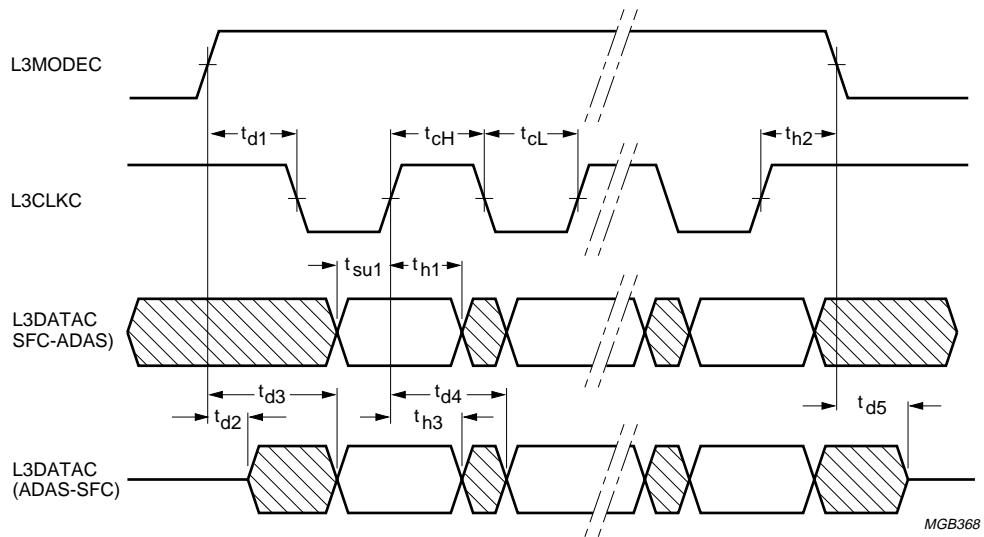


Fig.15 L3 interface timing; SAA2013 to SAA2003 (data mode).

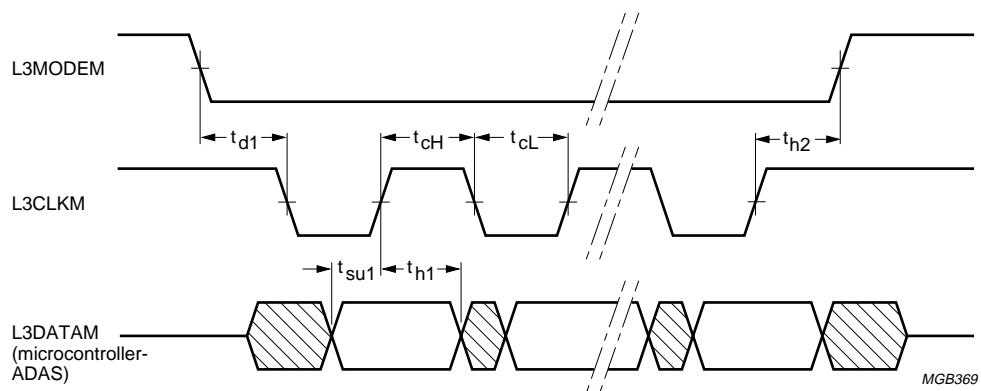


Fig.16 L3 interface timing; microcontroller to SAA2013 (address mode).

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SAA2013

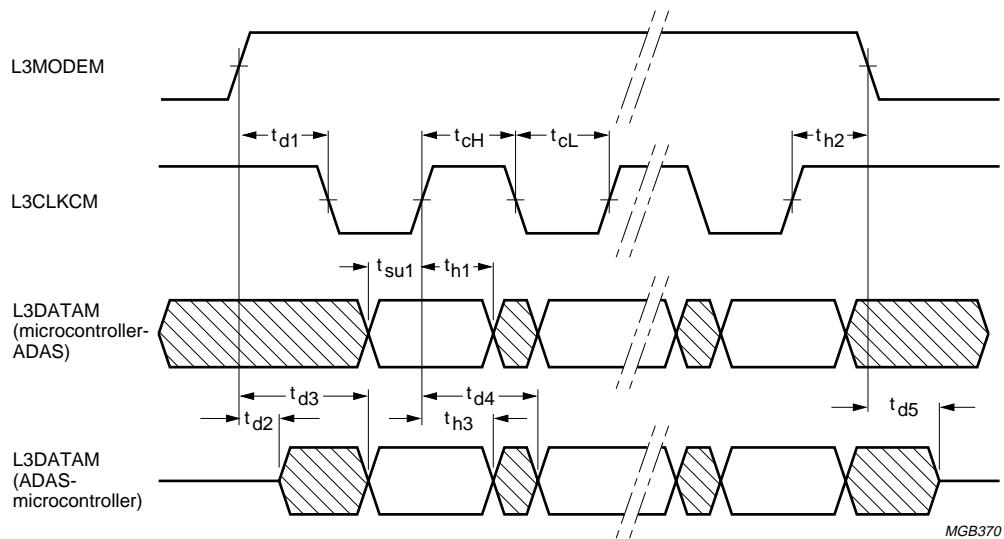


Fig.17 L3 interface timing; microcontroller to SAA2013 (data mode).

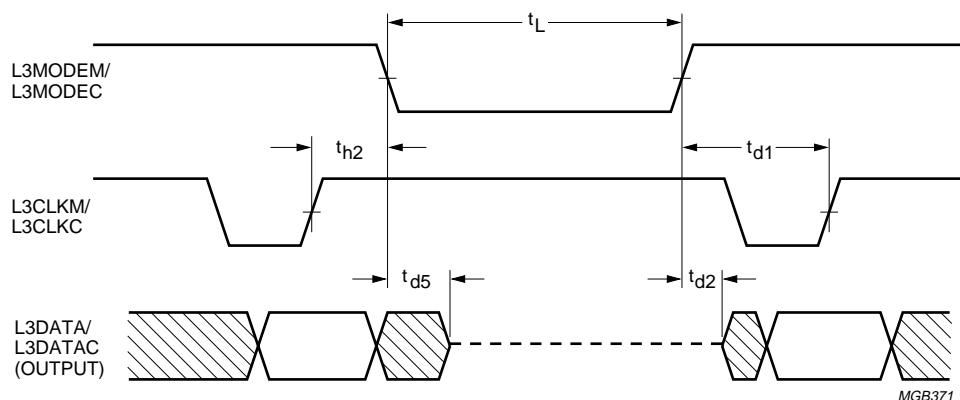


Fig.18 L3 interface timing; microcontroller to SAA2013 and SAA2013 to SAA2003 (halt mode).

## Adaptive allocation and scaling for PASC coding in DCC systems

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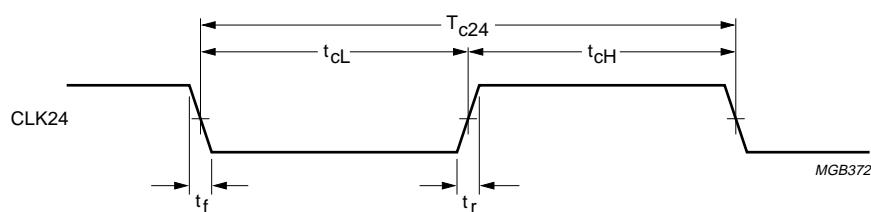


Fig.19 Input timing CLK24.

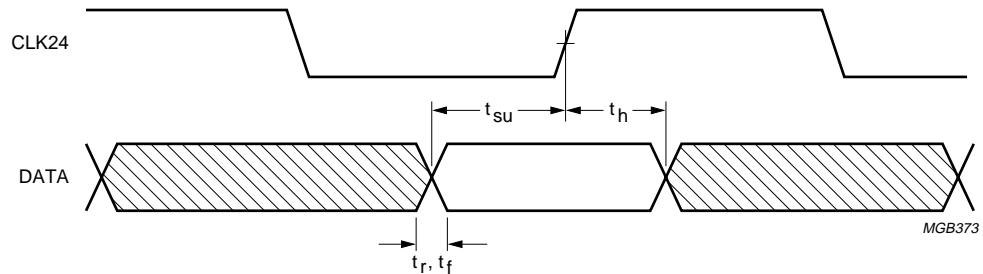


Fig.20 Input signal timing for FSYNC, FRESET, FDIR, FDWS, L3MODEM, L3CLKM, L3DATAM and L3DATAAC.

## Adaptive allocation and scaling for PASC coding in DCC systems

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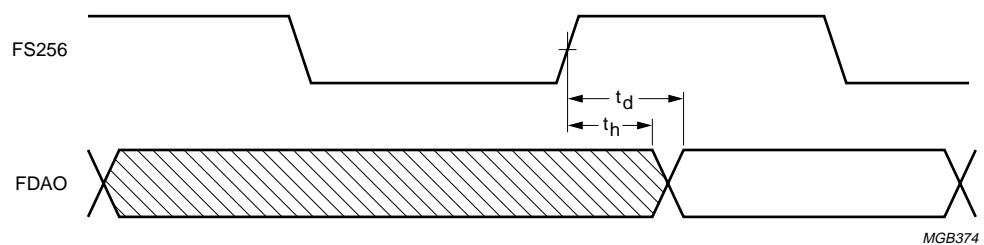


Fig.21 Output signal timing FDAC.

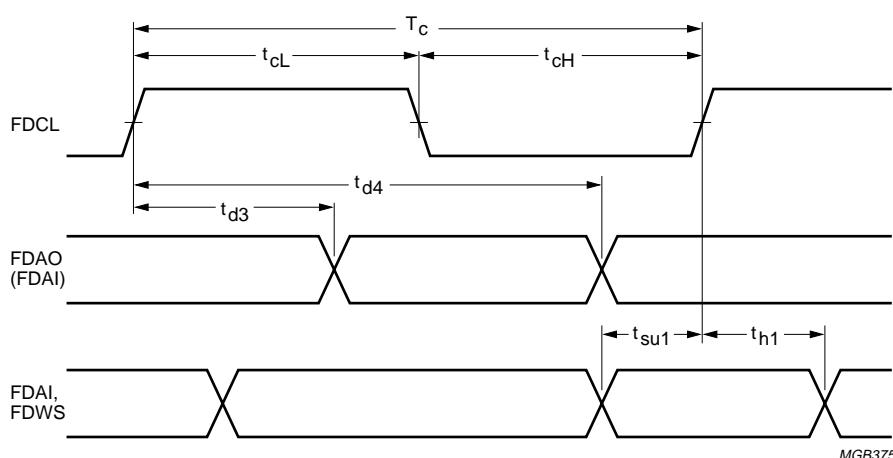


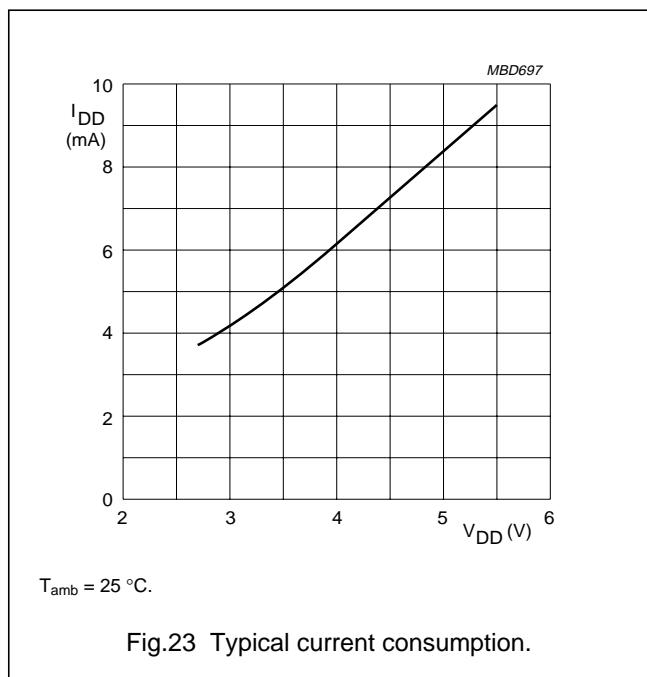
Fig.22 Filtered data interface timing.

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### Current consumption

The typical current consumption is shown in Fig.23.



### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL    | PARAMETER  | CONDITIONS       | MIN.          | MAX.           | UNIT               |
|-----------|--|------------------|---------------|----------------|--------------------|
| $V_{DD}$  | supply voltage   |                  | -0.5          | +6.5           | V                  |
| $V_I$     | input voltage  |                  | -0.5          | $V_{DD} + 0.5$ | V                  |
| $I_I$     | input current  |                  | -             | 20             | mA                 |
| $V_O$     | output voltage   |                  | -0.5          | +6.5           | V                  |
| $I_O$     | output current   |                  | -             | 20             | mA                 |
| $T_{stg}$ | storage temperature  |                  | -65           | +150           | $^{\circ}\text{C}$ |
| $T_{amb}$ | operating ambient temperature  |                  | -40           | +85            | $^{\circ}\text{C}$ |
| $V_{es}$  | electrostatic handling<br>Human Body Model (HBM)<br>Machine Model (MM) | note 1<br>note 2 | -2000<br>-200 | +2000<br>+200  | V                  |

### Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 0  $\Omega$  series resistor.

## Adaptive allocation and scaling for PASC coding in DCC systems

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### CHARACTERISTICS

$V_{DD} = 2.7$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $85$  °C; unless otherwise specified;  $I_{OL}$  and  $I_{OH}$  derated by 75% for  $V_{DD} < 4.5$  V.

| SYMBOL                   | PARAMETER                 | CONDITIONS            | MIN.           | TYP.    | MAX.        | UNIT |
|--------------------------|---------------------------|-----------------------|----------------|---------|-------------|------|
| <b>Supply</b>            |                           |                       |                |         |             |      |
| $V_{DD}$                 | supply voltage            |                       | 2.7            | 5.0     | 5.5         | V    |
| $I_{DD}$                 | supply current            | $V_{DD} = 3.0$ V      | 4              | 5       | 6           | mA   |
|                          |                           | $V_{DD} = 5.0$ V      | 7              | 10      | 12          | mA   |
| $I_{stb}$                | standby current           | $V_{DD} = 5.0$ V      | —              | —       | 400         | µA   |
| <b>Inputs</b>            |                           |                       |                |         |             |      |
| $V_{IL}$                 | LOW level input voltage   |                       | 0              | —       | $0.3V_{DD}$ | V    |
| $V_{IH}$                 | HIGH level input voltage  |                       | $0.7V_{DD}$    | —       | $V_{DD}$    | V    |
| $I_{LI}$                 | input leakage current     | $V_I = 0$ to $V_{DD}$ | -10            | —       | +10         | µA   |
| $C_I$                    | input capacitance         |                       | —              | —       | 10          | pF   |
| <b>Outputs</b>           |                           |                       |                |         |             |      |
| $V_{OL}$                 | LOW level output voltage  | $I_{OL} = 4$ mA       | 0              | —       | 0.4         | V    |
| $V_{OH}$                 | HIGH level output voltage | $I_{OH} = -4$ mA      | $V_{DD} - 0.4$ | —       | $V_{DD}$    | V    |
| $C_L$                    | load capacitance          |                       | —              | —       | 30          | pF   |
| <b>Inputs/outputs</b>    |                           |                       |                |         |             |      |
| $V_{IL}$                 | LOW level input voltage   |                       | 0              | —       | $0.3V_{DD}$ | V    |
| $V_{IH}$                 | HIGH level input voltage  |                       | $0.7V_{DD}$    | —       | $V_{DD}$    | V    |
| $I_{LI}$                 | 3-state leakage current   | $V_I = 0$ to $V_{DD}$ | -10            | —       | +10         | µA   |
| $C_I$                    | input capacitance         |                       | —              | —       | 10          | pF   |
| $V_{OL}$                 | LOW level output voltage  | $I_{OL} = 4$ mA       | 0              | —       | 0.4         | V    |
| $V_{OH}$                 | HIGH level output voltage | $I_{OH} = -4$ mA      | $V_{DD} - 0.4$ | —       | $V_{DD}$    | V    |
| $C_L$                    | load capacitance          |                       | —              | —       | 30          | pF   |
| <b>Clock input CLK24</b> |                           |                       |                |         |             |      |
| $f_i$                    | input frequency           | see Fig.19            | —              | 24.576  | —           | MHz  |
| $t_r$                    | rise time                 |                       | —              | —       | 7           | ns   |
| $t_f$                    | fall time                 |                       | —              | —       | 7           | ns   |
| $t_{cH}$                 | HIGH time                 |                       | 10             | —       | —           | ns   |
| $t_{cL}$                 | LOW time                  |                       | 10             | —       | —           | ns   |
| <b>Clock input FS256</b> |                           |                       |                |         |             |      |
| $f_i$                    | input frequency           | $f_s = 48$ kHz        | —              | 12.288  | —           | MHz  |
|                          |                           | $f_s = 44.1$ kHz      | —              | 11.2896 | —           | MHz  |
|                          |                           | $f_s = 32$ kHz        | —              | 8.192   | —           | MHz  |
| $t_r$                    | rise time                 |                       | —              | —       | 7           | ns   |
| $t_f$                    | fall time                 |                       | —              | —       | 7           | ns   |
| $t_{cH}$                 | HIGH time                 |                       | 35             | —       | —           | ns   |
| $t_{cL}$                 | LOW time                  |                       | 35             | —       | —           | ns   |

## Adaptive allocation and scaling for PASC coding in DCC systems

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| SYMBOL  | PARAMETER                             | CONDITIONS             | MIN.                   | TYP.              | MAX.                   | UNIT |
|---|---------------------------------------|------------------------|------------------------|-------------------|------------------------|------|
| <b>Inputs FSYNC, FRESET, FDIR, FDWS, L3MODEM, L3CLKM, L3DATAM and L3DATAC;<br/>referenced to CLK24 rising edge; see Fig.20; SLEEP = RESET = POR = logic 0</b> |                                       |                        |                        |                   |                        |      |
| $t_{su}$  | set-up time                           |                        | 15                     | —                 | —                      | ns   |
| $t_h$   | hold time                             |                        | 20                     | —                 | —                      | ns   |
| $t_r$   | rise time                             |                        | —                      | —                 | 200                    | ns   |
| $t_f$   | fall time                             |                        | —                      | —                 | 200                    | ns   |
| <b>Inputs FDAI, FDCL, FDWS, FRESET and FDIR; referenced to FS256 rising edge;<br/>SLEEP = RESET = POR = logic 0</b>   |                                       |                        |                        |                   |                        |      |
| $t_{su}$  | set-up time                           |                        | 15                     | —                 | —                      | ns   |
| $t_h$   | hold time                             |                        | 20                     | —                 | —                      | ns   |
| $t_r$   | rise time                             |                        | —                      | —                 | 200                    | ns   |
| $t_f$   | fall time                             |                        | —                      | —                 | 200                    | ns   |
| <b>Output FDAO; referenced to FS256 rising edge; see Fig.21; SLEEP = RESET = POR = logic 0</b>  |                                       |                        |                        |                   |                        |      |
| $t_h$   | hold time                             | $C_L = 7.5 \text{ pF}$ | 0                      | —                 | —                      | ns   |
| $t_d$   | delay time                            | $C_L = 30 \text{ pF}$  | —                      | —                 | 30                     | ns   |
| $t_{d3}$  | output delay time after FDCL<br>HIGH  | see Fig.22             | $2T_{c256} - 10^{(1)}$ | —                 | —                      | ns   |
| $t_{d4}$  | output delay time after FDCL<br>HIGH  | see Fig.22             | —                      | —                 | $3T_{c256} + 60^{(1)}$ | ns   |
| <b>Input FDCL; see Fig.22</b>   |                                       |                        |                        |                   |                        |      |
| $T_c$   | FDCL period                           |                        | 280                    | $4T_{c256}^{(1)}$ | —                      | ns   |
| $t_{cH}$  | FDCL HIGH time                        |                        | $T_{c256} + 35^{(1)}$  | —                 | —                      | ns   |
| $t_{cL}$  | FDCL LOW time                         |                        | $T_{c256} + 35^{(1)}$  | —                 | —                      | ns   |
| <b>Inputs FDAI and FDWS; see Fig.22</b>   |                                       |                        |                        |                   |                        |      |
| $t_{su1}$   | set-up time before FDCL HIGH          |                        | $3T_{c256} + 60^{(1)}$ | —                 | —                      | ns   |
| $t_{h1}$  | hold time after FDCL HIGH             |                        | $T_{c256} + 20^{(1)}$  | —                 | —                      | ns   |
| <b>Input FRESET; see Fig.4</b>  |                                       |                        |                        |                   |                        |      |
| $t_H$   | FRESET HIGH time                      |                        | 1280                   | —                 | —                      | ns   |
| $t_{su}$  | FDIR set-up time before<br>FRESET LOW |                        | 0                      | 210               | —                      | ns   |
| $t_h$   | FDIR hold time after FRESET<br>LOW    |                        | $9T_{c24}^{(2)}$       | 370               | —                      | ns   |
| <b>SLEEP and RESET timing; see Fig.5; LOWPWR = logic 1</b>  |                                       |                        |                        |                   |                        |      |
| $t_h$   | RESET hold time after SLEEP<br>LOW    |                        | $5T_{c24}^{(2)}$       | 210               | —                      | ns   |
| $t_d$   | CLK24 disable after SLEEP<br>HIGH     |                        | $9T_{c24}^{(2)}$       | 370               | —                      | ns   |

## Adaptive allocation and scaling for PASC coding in DCC systems

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| SYMBOL   | PARAMETER   | CONDITIONS                              | MIN. | TYP. | MAX. | UNIT |
|--|---|---|------|------|------|------|
| <b>L3 interface timing; microcontroller to SAA2013</b> |   |   |      |      |      |      |
| ADDRESS MODE; SEE FIG.16                               |   |   |      |      |      |      |
| $t_{d1}$   | L3MODEM LOW to L3CLKM LOW                         |   | 190  | —    | —    | ns   |
| $t_{cH}$   | L3CLKM HIGH time                                  |   | 250  | —    | —    | ns   |
| $t_{cL}$   | L3CLKM LOW time                                   |   | 250  | —    | —    | ns   |
| $t_{su1}$  | L3DATAM input set-up time before L3CLKM HIGH      |   | 190  | —    | —    | ns   |
| $t_{h1}$   | L3DATAM input hold time after L3CLKM HIGH         |   | 30   | —    | —    | ns   |
| $t_{h2}$   | L3CLKM HIGH before L3MODEM HIGH                   |   | 190  | —    | —    | ns   |
| DATA MODE; SEE FIG.17                                  |   |   |      |      |      |      |
| $t_{d1}$   | L3MODEM HIGH to L3CLKM LOW delay time             |   | 190  | —    | —    | ns   |
| $t_{cH}$   | L3CLKM HIGH time                                  |   | 250  | —    | —    | ns   |
| $t_{cL}$   | L3CLKM LOW time                                   |   | 250  | —    | —    | ns   |
| $t_{su1}$  | L3DATAM input set-up time before L3CLKM HIGH      |   | 190  | —    | —    | ns   |
| $t_{h1}$   | L3DATAM input hold time after L3CLKM HIGH         |   | 30   | —    | —    | ns   |
| $t_{h2}$   | L3CLKM HIGH before L3MODEM LOW                    |   | 190  | —    | —    | ns   |
| $t_{d3}$   | L3MODEM HIGH to L3DATAM output valid              |   | —    | —    | 380  | ns   |
| $t_{h3}$   | L3DATAM output hold time after L3CLKM HIGH        |   | 120  | —    | —    | ns   |
| $t_{d4}$   | L3CLKM HIGH to L3DATAM output valid delay time    |   | —    | —    | 360  | ns   |
|  |   | between bits 7 and 8; no halt mode used | —    | —    | 530  | ns   |
| $t_{d2}$   | L3MODEM HIGH to L3DATAM output enabled delay time |   | 0    | —    | 50   | ns   |
| $t_{d5}$   | L3MODEM LOW to L3DATAM output disabled delay time |   | 0    | —    | 50   | ns   |

## Adaptive allocation and scaling for PASC coding in DCC systems

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| SYMBOL                                  | PARAMETER   | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|------------|------|------|------|------|
| HALT MODE; SEE FIG.18                   |   |            |      |      |      |      |
| $t_L$                                   | L3MODEM LOW time                                      |            | 190  | —    | —    | ns   |
| $t_{d1}$                                | L3MODEM HIGH to L3CLKM<br>HIGH delay time             |            | 190  | —    | —    | ns   |
| $t_{h2}$                                | L3CLKM HIGH before<br>L3MODEM LOW                     |            | 190  | —    | —    | ns   |
| $t_{d2}$                                | L3MODEM HIGH to L3DATAM<br>output enabled delay time  |            | 0    | —    | 50   | ns   |
| $t_{d5}$                                | L3MODEM LOW to L3DATAM<br>output disabled delay time  |            | 0    | —    | 50   | ns   |
| L3 interface timing; SAA2013 to SAA2003 |   |            |      |      |      |      |
| ADDRESS MODE; SEE FIG.14                |   |            |      |      |      |      |
| $t_{d1}$                                | L3MODEC LOW to L3CLKC<br>LOW delay time               |            | 190  | —    | —    | ns   |
| $t_{cH}$                                | L3CLKC HIGH time                                      |            | 210  | —    | —    | ns   |
| $t_{cL}$                                | L3CLKC LOW time                                       |            | 210  | —    | —    | ns   |
| $t_{h2}$                                | L3CLKC HIGH time before<br>L3MODEC HIGH               |            | 190  | —    | —    | ns   |
| $t_{d3}$                                | L3MODEC LOW to L3DATAC<br>output valid delay time     |            | —    | —    | 380  | ns   |
| $t_{h1}$                                | L3DATAC output hold time<br>after L3CLKC HIGH         |            | 120  | —    | —    | ns   |
| $t_{d4}$                                | L3CLKC HIGH to L3DATAC<br>output valid delay time     |            | —    | —    | 360  | ns   |
| $t_{d2}$                                | L3MODEC LOW to L3DATAC<br>output enabled delay time   |            | 0    | —    | 50   | ns   |
| $t_{d5}$                                | L3MODEC HIGH to L3DATAC<br>output disabled delay time |            | 0    | —    | 50   | ns   |

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| SYMBOL   | PARAMETER   | CONDITIONS                              | MIN. | TYP. | MAX. | UNIT |
|--|---|---|------|------|------|------|
| DATA MODE; SEE FIG.15                                  |   |   |      |      |      |      |
| $t_{d1}$   | L3MODEC HIGH to L3CLKC LOW  |   | 190  | —    | —    | ns   |
| $t_{cH}$   | L3CLKC HIGH time  |   | 210  | —    | —    | ns   |
| $t_{cL}$   | L3CLKC LOW time   |   | 210  | —    | —    | ns   |
| $t_{su1}$  | L3DATAC input set-up time before L3CLKC HIGH                                    |   | 100  | —    | —    | ns   |
| $t_{h1}$   | L3DATAC input hold time after L3CLKC HIGH                                       |   | 30   | —    | —    | ns   |
| $t_{h2}$   | L3CLKC HIGH time before L3MODEC LOW   |   | 190  | —    | —    | ns   |
| $t_{d3}$   | L3MODEC HIGH to L3DATAC output valid  |   | —    | —    | 380  | ns   |
| $t_{h3}$   | L3DATAC output hold time after L3CLKC HIGH                                      |   | 120  | —    | —    | ns   |
| $t_{d4}$   | L3CLKC HIGH to L3DATAC output valid   | —                                       | —    | 360  | ns   |      |
|  |   | between bits 7 and 8; no halt mode used | —    | —    | 530  | ns   |
| HALT MODE; SEE FIG.18                                  |   |   |      |      |      |      |
| $t_L$  | L3MODEC LOW time  |   | 190  | —    | —    | ns   |
| $t_{d1}$   | L3MODEC HIGH to L3CLKC HIGH delay time  |   | 190  | —    | —    | ns   |
| $t_{h2}$   | L3CLKC HIGH time before L3MODEC LOW   |   | 190  | —    | —    | ns   |
| L3 interface delays in bypassed mode; LOWPWR = logic 1 |   |   |      |      |      |      |
| $t_{pd1}$  | propagation delay from L3MODEM to L3MODEC; L3DATAM to L3DATAC; L3CLKM to L3CLKC |   | —    | —    | 35   | ns   |
| $t_{pd2}$  | propagation delay from L3DATAM to L3DATAC; L3CLKM to L3CLKC                     |   | -20  | —    | +4   | ns   |
| $t_{pd3}$  | propagation delay from L3DATAM to L3DATAC; L3MODEM to L3MODEC                   |   | -20  | —    | +4   | ns   |

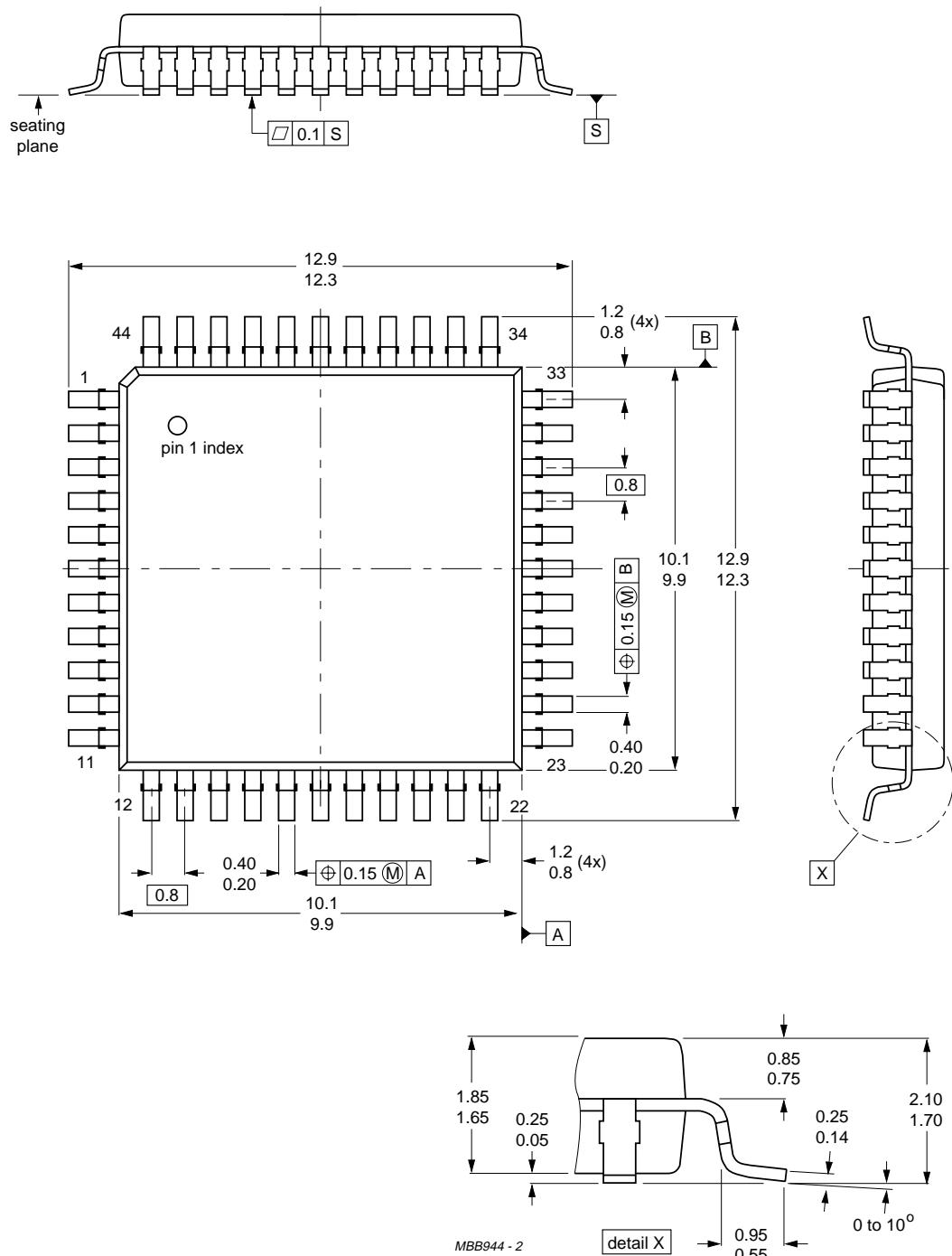
### Notes

1.  $T_{c256}$  is a clock period of FS256.
2.  $T_{c24}$  is a clock period of CLK24.

## Adaptive allocation and scaling for PASC coding in DCC systems

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### PACKAGE OUTLINE



Dimensions in mm.

Fig.24 Plastic quad flat-pack, 44-pin (short) (QFP44SL).

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### **SOLDERING**

#### **Plastic quad flat-packs**

##### **BY WAVE**

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

##### **BY SOLDER PASTE REFLOW**

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be

applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

#### **REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)**

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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### DEFINITIONS

| <b>Data sheet status</b>  |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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**NOTES**

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