INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The SAA3027 is intended for a general purpose (RC-5) infrared remote control system. The device can generate 2048 different commands and utilizes a keyboard with a single-pole switch per key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified later in this publication (see KEY ACTIVITIES).

Features

- Transmitter for 32 x 64 commands
- One transmitter controls 32 systems
- Very low current consumption
- For infrared transmission link
- Transmission by biphase technique
- Short transmission times; speed-up of system reaction time
- LC oscillator; no crystal required
- Input protection
- Test mode facility

QUICK REFERENCE DATA

Supply voltage range	V_{DD}	4,75 to 12,6	V
Input voltage range	V_I	$-0,5$ to $(V_{DD}+0,5)$	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	$-0,5$ to $(V_{DD}+0,5)$	V*
Output current	$\pm I_O$	max. 10	mA
Operating ambient temperature range	T_{amb}	-25 to $+85$	°C

* $V_{DD} + 0,5$ V not to exceed 15 V.

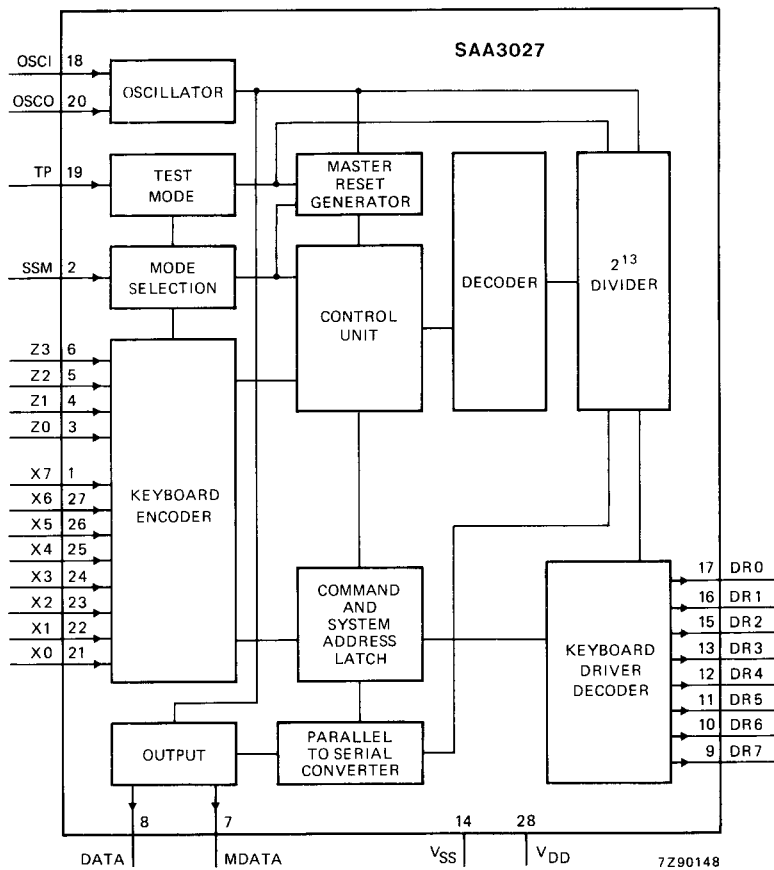## PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).
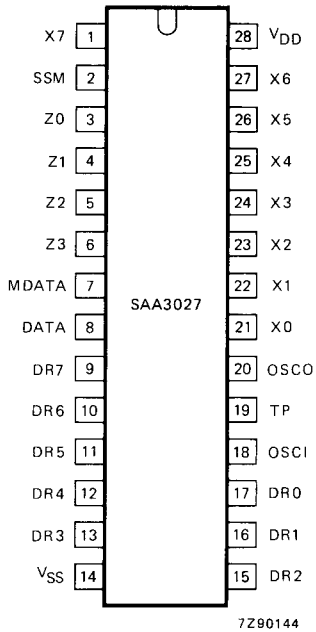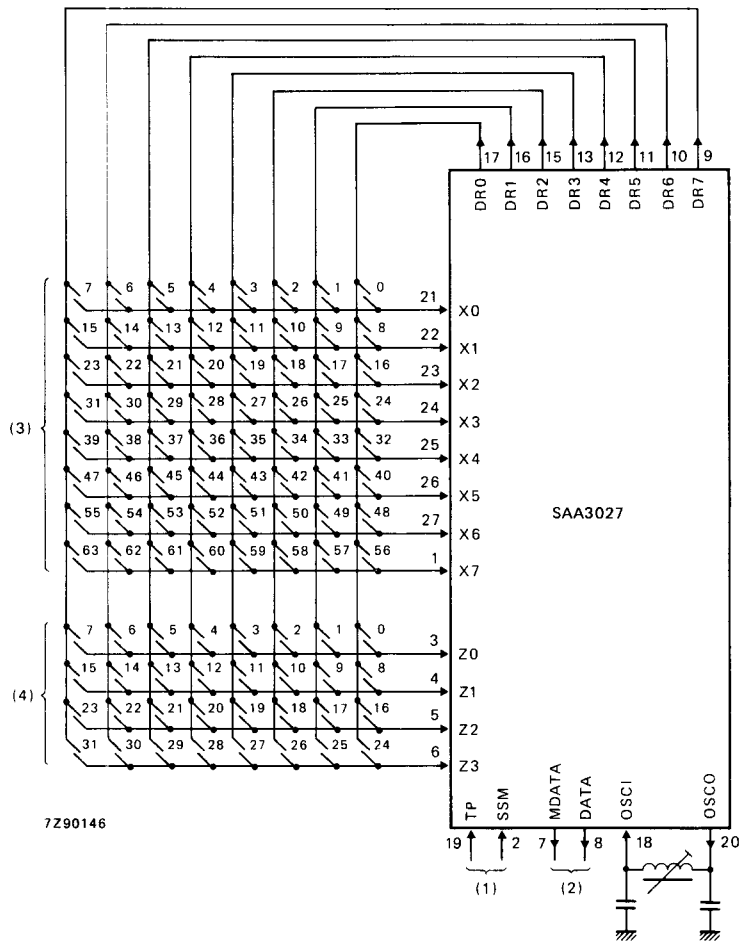
Fig. 1 Block diagram.

Fig. 2 Pinning diagram.

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PINNING

14	V_{SS}	negative supply (ground)
28	V_{DD}	positive supply

21	X0	
22	X1	
23	X2	
24	X3	keyboard command inputs with
25	X4	P-channel pull-up transistors
26	X5	
27	X6	
1	X7	

3	Z0	
4	Z1	keyboard system inputs with
5	Z2	P-channel pull-up transistors
6	Z3	

2	SSM	system mode selection input
19	TP	test pin

18	OSC1	oscillator input
20	OSC0	oscillator output

17	DR0	
16	DR1	
15	DR2	
13	DR3	scan driver outputs with open
12	DR4	drain N-channel transistors
11	DR5	
10	DR6	
9	DR7	

7	MDATA	remote signal outputs
8	DATA	(3-state outputs)

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(1) Programming inputs for operating modes, test mode and reset.
(2) Remote signal outputs.
(3) Keyboard command code matrix 8 x 8.
(4) Keyboard system code matrix 4 x 8.

Fig. 3 Keyboard interconnection.

FUNCTIONAL DECRIPTION

Combined system mode (SSM = LOW)

The X and Z-lines are active HIGH in the quiescent state. Legal key operation either in the X-DR or Z-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the DR-outputs are switched off and two scan cycles are started, switching on the DR-outputs one by one. When a Z or X-input senses a LOW level, a latch-enable signal is fed to the system address or command latches, depending on whether sensing was found in the Z or X-input matrix. After latching a system address number, the device will generate the last command (i.e. all command bits '1') in the chosen system as long as the key is pressed. Latching of a command number causes the device to generate this command together with the system address number stored in the system address latch. Releasing the key will reset the internal action if no data is transmitted at that time. Once the transmission is started, the signal will be finished completely.

Single system mode (SSM = HIGH)

The X-lines are active HIGH in the quiescent state; the pull-up transistors of the Z-lines are switched off and the inputs are disabled. Only legal key operation in the X-DR matrix starts the debounce cycle. When the contact is made for two bit times without interruption, the oscillator-enable signal is latched and the key may be released. Interruption within the two bit times resets the internal action. At the end of the debounce time, the pull-up transistors in the X-lines are switched off, those in the Z-lines are switched on during the first scan cycle. The wired connection in the Z-matrix is then translated into a system address number and stored in the system address latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again, while the transistors in the X-lines are switched on. The second scan cycle produces the command number which, after latching, is transmitted together with the system address number.

Inputs

The command inputs X0 to X7 carry a logical '1' in the quiescent state by means of an internal pull-up transistor. When SSM is LOW, the system inputs Z0 to Z3 also carry a logical '1' in the quiescent state by means of an internal pull-up transistor.

When SSM is HIGH, the transistors are switched off and no current flows via the wired connection in the Z-DR matrix.

Oscillator

OSCI and OSCO are the input/output respectively of a two-pin oscillator. The oscillator is formed externally by one inductor and two capacitors and operates at 72 kHz (typical).

Key-release detection

An extra control bit is added which will be complemented after key-release. In this way the decoder gets an indication that shows if the next code is to be considered as a new command. This is very important for multi-digit entry (e.g. by channel numbers or Teletext/Viewdata pages). The control bit will only be complemented after finishing at least one code transmission. The scan cycles are repeated before every code transmission, so that, even by 'take-over' of key operation during code transmission, the correct system and command numbers are generated.

FUNCTIONAL DESCRIPTION (continued)

Outputs

The output DATA carries the generated information according to the format given in Fig. 4 and Tables 1 and 2. The code is transmitted in biphase; definitions of logical '1' and '0' are given in Fig. 5.

The code consists of four parts:
- Start part formed by 2 bits (two times a logical '1');
- Control part formed by 1 bit;
- System part formed by 5 bits;
- Command part formed by 6 bits.

The output MDATA carries the same information as output DATA but is modulated on a carrier frequency of half the oscillator frequency, so that each bit is presented as a burst of 32 oscillator periods. To reduce power consumption, the carrier frequency has a 25% duty cycle.

In the quiescent state, both outputs are non-conducting (3-state outputs). The scan drivers DR0 to DR7 are of the open drain N-channel type and are conducting in the quiescent state of the circuit. After a legal key operation, a scanning procedure is started so that they are switched into the conducting state one after the other.

Reset action

The circuit will be reset immediately when a key release occurs during:
- debounce time;
- between two codes.

When a key release occurs during scanning of the matrix, a reset action will be accomplished if:
- the key is released while one of the driver outputs is in the low-ohmic '0' state;
- the key is released before detection of that key;
- there is no wired connection in the Z-DR matrix while SSM is HIGH.

Test pin

The test pin TP is an input which can be used for testing purposes.

When LOW, the circuit operates normally.

When HIGH, all pull-up transistors are switched off, the control bit is set to zero and the output data is 2^6 times faster than normal.

When Z2 = Z3 = LOW, the counter will be reset to zero.

KEY ACTIVITIES

Every connection of one X-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating more than one X-input at a time is an illegal keyboard operation and no circuit action is taken (oscillator does not start).

When SSM is LOW, every connection of one Z-input and one DR-output is recognized as a legal keyboard operation and causes the device to generate the corresponding code.

Activating two or more Z-inputs, or Z-inputs and X-inputs, at one time is an illegal keyboard operation and no circuit action is taken.

When SSM is HIGH, a wired connection must be made between a Z-input and a DR-output. If no connection is made, the code is not generated.

When one X or Z-input is connected to more than one DR-output, the last scan signal is considered legal.

The maximum allowable value of the contact series resistance of the keyboard switches is 10 kΩ.

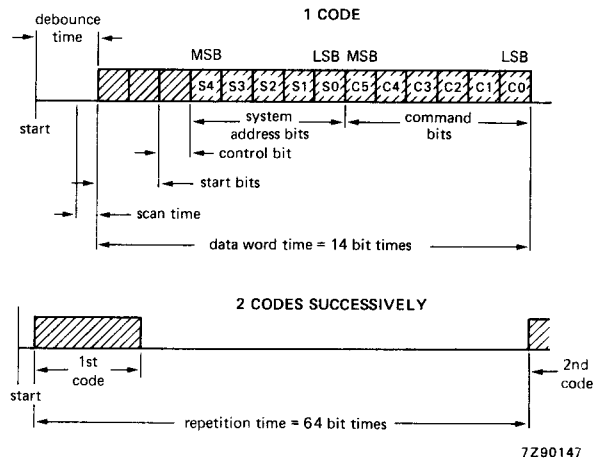*Z2 or Z3 must be connected to V_{DD} to avoid unwanted supply current.*

Fig. 4 DATA output format (RC-5).

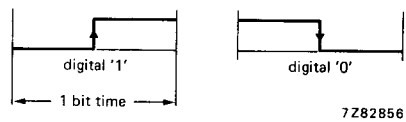Fig. 5 Biphase transmission code; 1 bit time = $2^7 \times T_{OSC}$ = 1,778 ms (typical), where T_{OSC} is the oscillator period time.

Table 1 Command matrix X-DR

code no.	X-lines X.. 0	1	2	3	4	5	6	7	DR-lines DR.. 0	1	2	3	4	5	6	7	command bits C.. 5	4	3	2	1	0
0	•								•								0	0	0	0	0	0
1	•									•							0	0	0	0	0	1
2	•										•						0	0	0	0	1	0
3	•											•					0	0	0	0	1	1
4	•												•				0	0	0	1	0	0
5	•													•			0	0	0	1	0	1
6	•														•		0	0	0	1	1	0
7	•															•	0	0	0	1	1	1
8		•							•								0	0	1	0	0	0
9		•								•							0	0	1	0	0	1
10		•									•						0	0	1	0	1	0
11		•										•					0	0	1	0	1	1
12		•											•				0	0	1	1	0	0
13		•												•			0	0	1	1	0	1
14		•													•		0	0	1	1	1	0
15		•														•	0	0	1	1	1	1
16			•						•								0	1	0	0	0	0
17			•							•							0	1	0	0	0	1
18			•								•						0	1	0	0	1	0
19			•									•					0	1	0	0	1	1
20			•										•				0	1	0	1	0	0
21			•											•			0	1	0	1	0	1
22			•												•		0	1	0	1	1	0
23			•													•	0	1	0	1	1	1
24				•					•								0	1	1	0	0	0
25				•						•							0	1	1	0	0	1
26				•							•						0	1	1	0	1	0
27				•								•					0	1	1	0	1	1
28				•									•				0	1	1	1	0	0
29				•										•			0	1	1	1	0	1
30				•											•		0	1	1	1	1	0
31				•												•	0	1	1	1	1	1

code no.	X-lines X..								DR-lines DR..								command bits C..					
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
32					•				•								1	0	0	0	0	0
33					•					•							1	0	0	0	0	1
34					•						•						1	0	0	0	1	0
35					•							•					1	0	0	0	1	1
36					•								•				1	0	0	1	0	0
37					•									•			1	0	0	1	0	1
38					•										•		1	0	0	1	1	0
39					•											•	1	0	0	1	1	1
40						•			•								1	0	1	0	0	0
41						•				•							1	0	1	0	0	1
42						•					•						1	0	1	0	1	0
43						•						•					1	0	1	0	1	1
44						•							•				1	0	1	1	0	0
45						•								•			1	0	1	1	0	1
46						•									•		1	0	1	1	1	0
47						•										•	1	0	1	1	1	1
48							•		•								1	1	0	0	0	0
49							•			•							1	1	0	0	0	1
50							•				•						1	1	0	0	1	0
51							•					•					1	1	0	0	1	1
52							•						•				1	1	0	1	0	0
53							•							•			1	1	0	1	0	1
54							•								•		1	1	0	1	1	0
55							•									•	1	1	0	1	1	1
56								•	•								1	1	1	0	0	0
57								•		•							1	1	1	0	0	1
58								•			•						1	1	1	0	1	0
59								•				•					1	1	1	0	1	1
60								•					•				1	1	1	1	0	0
61								•						•			1	1	1	1	0	1
62								•							•		1	1	1	1	1	0
63								•								•	1	1	1	1	1	1

Table 2 System matrix Z-DR

system no.	Z-lines Z..				DR-lines DR..								system bits S..				
	0	1	2	3	0	1	2	3	4	5	6	7	4	3	2	1	0
0	•				•								0	0	0	0	0
1	•					•							0	0	0	0	1
2	•						•						0	0	0	1	0
3	•							•					0	0	0	1	1
4	•								•				0	0	1	0	0
5	•									•			0	0	1	0	1
6	•										•		0	0	1	1	0
7	•											•	0	0	1	1	1
8		•			•								0	1	0	0	0
9		•				•							0	1	0	0	1
10		•					•						0	1	0	1	0
11		•						•					0	1	0	1	1
12		•							•				0	1	1	0	0
13		•								•			0	1	1	0	1
14		•									•		0	1	1	1	0
15		•										•	0	1	1	1	1
16			•		•								1	0	0	0	0
17			•			•							1	0	0	0	1
18			•				•						1	0	0	1	0
19			•					•					1	0	0	1	1
20			•						•				1	0	1	0	0
21			•							•			1	0	1	0	1
22			•								•		1	0	1	1	0
23			•									•	1	0	1	1	1
24				•	•								1	1	0	0	0
25				•		•							1	1	0	0	1
26				•			•						1	1	0	1	0
27				•				•					1	1	0	1	1
28				•					•				1	1	1	0	0
29				•						•			1	1	1	0	1
30				•							•		1	1	1	1	0
31				•								•	1	1	1	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range with respect to V_{SS}	V_{DD}	$-0,5$ to $+15$	V
Input voltage range	V_I	$-0,5$ to $(V_{DD}+0,5)$	V*
Input current	$\pm I_I$	max. 10	mA
Output voltage range	V_O	$-0,5$ to $(V_{DD}+0,5)$	V*
Output current	$\pm I_O$	max. 10	mA
Power dissipation output OSCO	P_O	max. 50	mW
Power dissipation per output (all other outputs)	P_O	max. 100	mW
Total power dissipation per package	P_{tot}	max. 200	mW
Operating ambient temperature range	T_{amb}	-25 to $+85$	^oC
Storage temperature range	T_{stg}	-55 to $+150$	^oC

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

* $V_{DD}+0,5$ V not to exceed 15 V.

CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = -25$ to $85\,^{\circ}$C unless otherwise specified

parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
Supply voltage	–	V_{DD}	4,75	–	12,6	V

Supply current
    at $I_O = 0$ mA for all outputs;
    X0 to X7 and Z3 at V_{DD};
    all other inputs at V_{DD} or V_{SS};
    excluding leakage current from
    open drain N-channel outputs;
    $T_{amb} = 25\,^{\circ}$C
	12,6	I_{DD}	–	–	10	μA

Inputs						
Keyboard inputs X and Z with P-channel pull-up transistors						
Input current (each input) at $V_I = 0$ V; TP = SSM = LOW	4,75 to 12,6	$-I_I$	10	–	300	μA
Input voltage HIGH	4,75 to 12,6	V_{IH}	$0,7 \times V_{DD}$	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	$0,3 \times V_{DD}$	V

Input leakage current at $T_{amb} = 25\,^{\circ}$C;
    TP = HIGH;
    $V_I = 12,6$ V
	12,6	I_{IR}	–	–	1	μA

$V_I = 0$ V	12,6	$-I_{IR}$	–	–	1	μA
SSM, TP and OSCI inputs						
Input voltage HIGH	4,75 to 12,6	V_{IH}	$0,7 \times V_{DD}$	–	V_{DD}	V
Input voltage LOW	4,75 to 12,6	V_{IL}	0	–	$0,3 \times V_{DD}$	V
Input leakage current at $T_{amb} = 25\,^{\circ}$C; $V_I = 12,6$ V	12,6	I_{IR}	–	–	1	μA
$V_I = 0$ V	12,6	$-I_{IR}$	–	–	1	μA
Outputs						
DATA, MDATA outputs						
Output voltage HIGH at $-I_{OH} = 0,8$ mA	4,75 to 12,6	V_{OH}	$V_{DD} - 0,6$	–	–	V
Output voltage LOW at $I_{OL} = 0,8$ mA	4,75 to 12,6	V_{OL}	–	–	0,4	V
Output leakage current at: $V_O = 12,6$ V	12,6	I_{OR}	–	–	10	μA
$V_O = 0$ V	12,6	$-I_{OR}$	–	–	20	μA
$T_{amb} = 25\,^{\circ}$C; $V_O = 12,6$ V	12,6	I_{OR}	–	–	1	μA
$V_O = 0$ V	12,6	$-I_{OR}$	–	–	2	μA

| parameter	V_{DD} (V)	symbol	min.	typ.	max.	unit
DR0 to DR7 outputs						
Output voltage LOW ¡ at I_{OL} = 0,35 mA	4,75 to 12,6	V_{OL}	—	--	0,4	V
Output leakage current at V_O = 12,6 V	12,6	I_{OR}	—	--	10	μA
at V_O = 12,6 V; T_{amb} = 25 °C	12,6	I_{OR}	—	--	1	μA
OSCO output						
Output voltage HIGH at $-I_{OH}$ = 0,2 mA; OSCI = V_{SS}	4,75 to 12,6	V_{OH}	$V_{DD}-0,6$	--	—	V
Output voltage LOW at $-I_{OL}$ = 0,45 mA; OSCI = V_{DD}	4,75 to 12,6	V_{OL}	—	--	0,5	V
Oscillator						
Maximum oscillator frequency at C_L = 40 pF (Figs 6 and 7)	4,75	f_{OSCI}	75	72	—	kHz
	6	f_{OSCI}	120	72	—	kHz
	12,6	f_{OSCI}	300	72	—	kHz
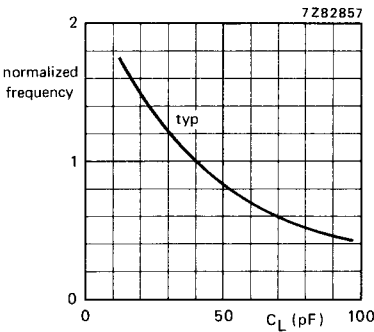
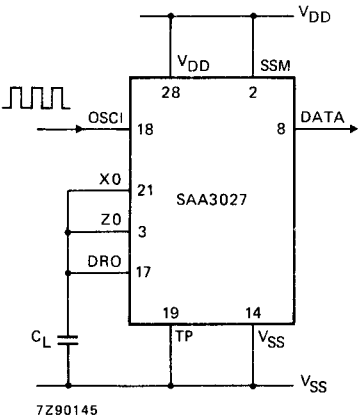Fig. 6 Typical normalized input frequency as a function of the load (keyboard) capacitance.

Fig. 7 Test circuit for measurement of maximum oscillator frequency.