DATA SHEET

SAA3500H
Digital audio broadcast channel decoder

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Digital Audio Broadcast (DAB) full-capacity demodulator and decoder
- Supports DAB transmission modes I, II, III and IV
- Integrated Analog-to-Digital Converter (ADC) for IF input
- Digital mixer with on-chip digital Automatic Frequency Control (AFC) and Automatic Gain Control (AGC)
- Detectors for null symbol, DAB mode and transmitter identification
- On-chip or external synchronization algorithms and control loops
- On-chip timing PLL and DCXO
- Dynamic DAB multiplex reconfiguration supported
- Equal and unequal error protection for up to 64 sub-channels
- Fast information channel buffering
- Simple full capacity output
- Receiver data interface
- Serial output for three sub-channels
- I^2C-bus or L3-bus control interface.

2 APPLICATIONS

- Mobile receivers (FM/DAB car radios)
- Personal Computer add-ons
- Test and measurement equipment
- Portable radios.

3 GENERAL DESCRIPTION

The Philips SAA3500H is a Digital Audio Broadcast (DAB) channel decoder according to the ETSI specification ETS 300 401. The SAA3500H is a successor to the Philips FADIC and SIVIC chip set and provides an IF ADC, digital mixer, full DAB ensemble demodulation and decoding as well as time and frequency synchronization functions. Because of the full-speed Viterbi decoding capacity and a high-speed receiver data output interface, DAB data reception is not limited by the SAA3500H channel decoder.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.0	3.3	3.6	V
$V_{i(max)}$	maximum input voltage	–0.5	–	V_{DD} + 0.5	V
I_{DD}	DC supply current	–	–	180	mA
f_{clk}	clock frequency	–	24576	–	kHz
T_{amb}	ambient temperature	–40	+25	+85	°C
T_{stg}	storage temperature	–65	–	+150	°C

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA3500H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT317-1

6 BLOCK DIAGRAM

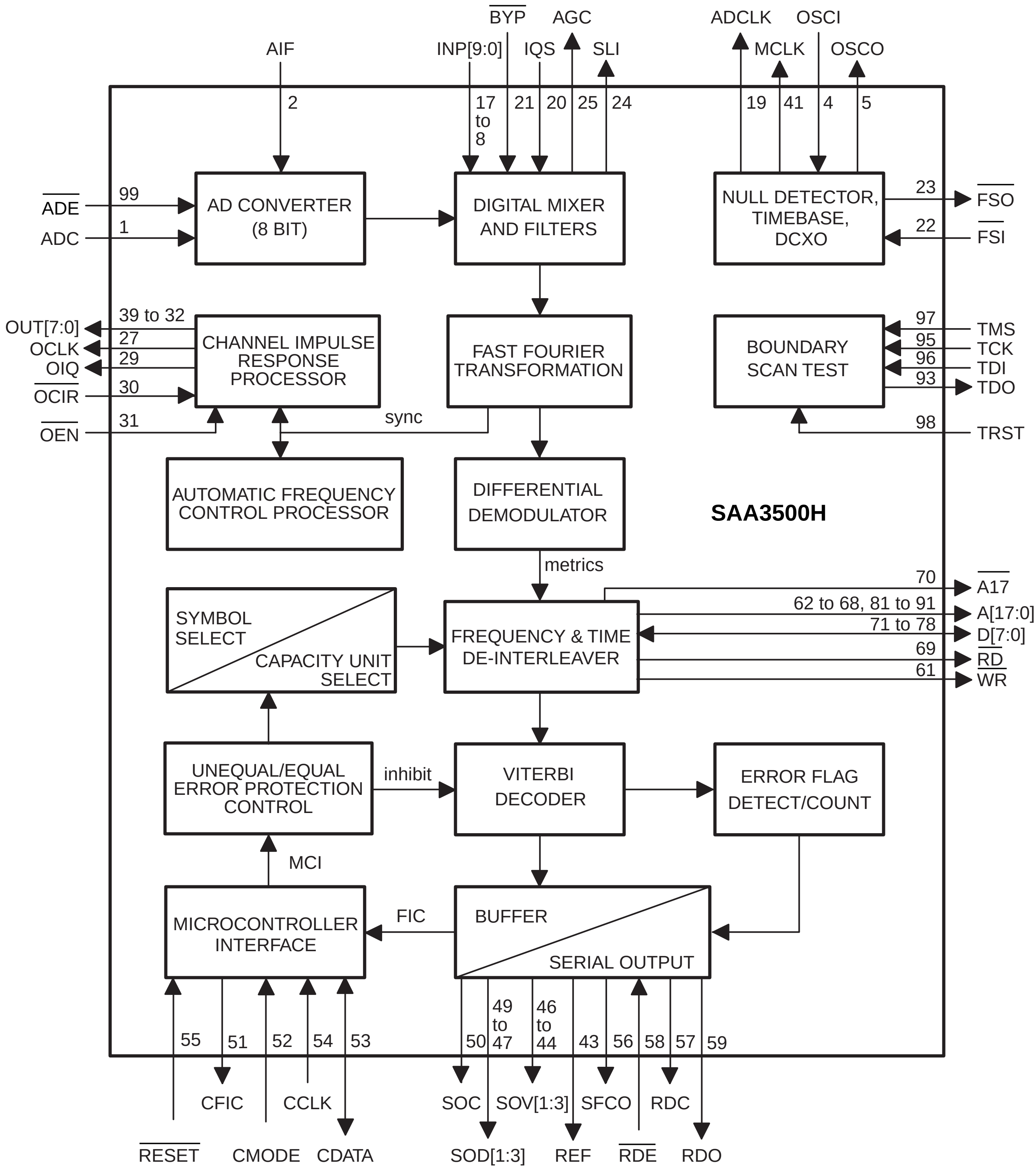


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
ADC	1	input	analog-to-digital converter DC input
AIF	2	input	analog-to-digital converter IF input
V_{SSA}	3	ground	analog supply ground
$\overline{\text{ADE}}$	99	input	analog-to-digital converter enable (active LOW)
V_{DDA}	100	supply	analog voltage supply (+3.3 V)
INP[0:9]	8 to 17	input	2048 kHz IF or baseband digital parallel input data (8 or 10 bits)
ADCLK	19	output	analog-to-digital clock output 8192 kHz if $\overline{\text{BYP}}$ = HIGH, 4096 kHz if $\overline{\text{BYP}}$ = LOW
IQS	20	input	clock signal indicating I or Q baseband data if $\overline{\text{BYP}}$ = LOW; signal for swapping I and Q data bytes if $\overline{\text{BYP}}$ = HIGH
$\overline{\text{BYP}}$	21	input	IF input stage bypass (active LOW)
$\overline{\text{FSI}}$	22	input	frame sync input (LOW indicates DAB null symbol detection)
$\overline{\text{FSO}}$	23	output	null detector/frame sync output (LOW indicates DAB null symbol position)
SLI	24	output	AGC synchronization lock indicator (HIGH if synchronized)
AGC	25	output	AGC level comparator output (HIGH if input sample > reference level, else LOW)
OSCI	4	input	oscillator or system clock input, 24576 kHz
OSCO	5	output	oscillator output
MCLK	41	output	master clock output, 24576 kHz
V_{SS}	7, 18, 26, 40, 60, 80 and 94	supply	digital supply ground
V_{DD}	6, 28, 42 and 79	supply	digital voltage supply (+3.3 V)
TEST	92	input	connect to ground for proper operation
OUT[0:7]	32 to 39	output	baseband or channel impulse response output
OCLK	27	output	output data clock (negative edge indicates new data)
OIQ	29	output	output I or Q select signal if $\overline{\text{OCIR}}$ = HIGH, or frame trigger if $\overline{\text{OCIR}}$ = LOW
$\overline{\text{OCIR}}$	30	input	output select: baseband if $\overline{\text{OCIR}}$ = HIGH, CIR if $\overline{\text{OCIR}}$ = LOW
$\overline{\text{OEN}}$	31	input	output enable (active LOW)
CFIC	51	output	microcontroller interface signal indicating Fast Information Channel (FIC) processing
CMODE	52	input	microcontroller interface mode input (only L3-bus)
CDATA	53	I/O	microcontroller interface serial data I^2C-bus or L3-bus (5 V tolerant)
CCLK	54	input	microcontroller interface clock input I^2C-bus or L3-bus
$\overline{\text{RESET}}$	55	input	chip reset input (active LOW)
A[17:11]	62 to 68	output	address outputs external RAM
A[10:0]	81 to 91	output	address outputs external RAM
$\overline{\text{WR}}$	61	output	write data to RAM (active LOW)
$\overline{\text{RD}}$	69	output	read data from RAM (active LOW)
$\overline{\text{A17}}$	70	output	address bit 17 inverted for second RAM ($128k \times 8$)
D[0:7]	71 to 78	I/O	data input/output external RAM

SYMBOL	PIN	TYPE	DESCRIPTION
SOV3	44	output	serial output valid data 3
SOV2	45	output	serial output valid data 2
SOV1	46	output	serial output valid data 1
SOD3	47	output	serial output data 3
SOD2	48	output	serial output data 2
SOD1	49	output	serial output data 1 (from channel decoder)
SOC	50	output	serial output clock (384 kHz continuous)
REF	43	output	receiver error flag [from Viterbi decoder, for Simple Full Capacity Output (SFCO)]
SFCO	56	output	simple full capacity output (direct from Viterbi decoder)
RDC	57	output	receiver data clock (6144 kHz continuous) or SFCO clock (burst)
$\overline{\text{RDE}}$	58	input	RDI output enable (active LOW)
RDO	59	output	receiver data interface bi-phase output
TDO	93	output	boundary scan test serial output
TCK	95	input	boundary scan test clock input
TDI	96	input	boundary scan test serial input
TMS	97	input	boundary scan test mode select input
TRST	98	input	boundary scan test reset input

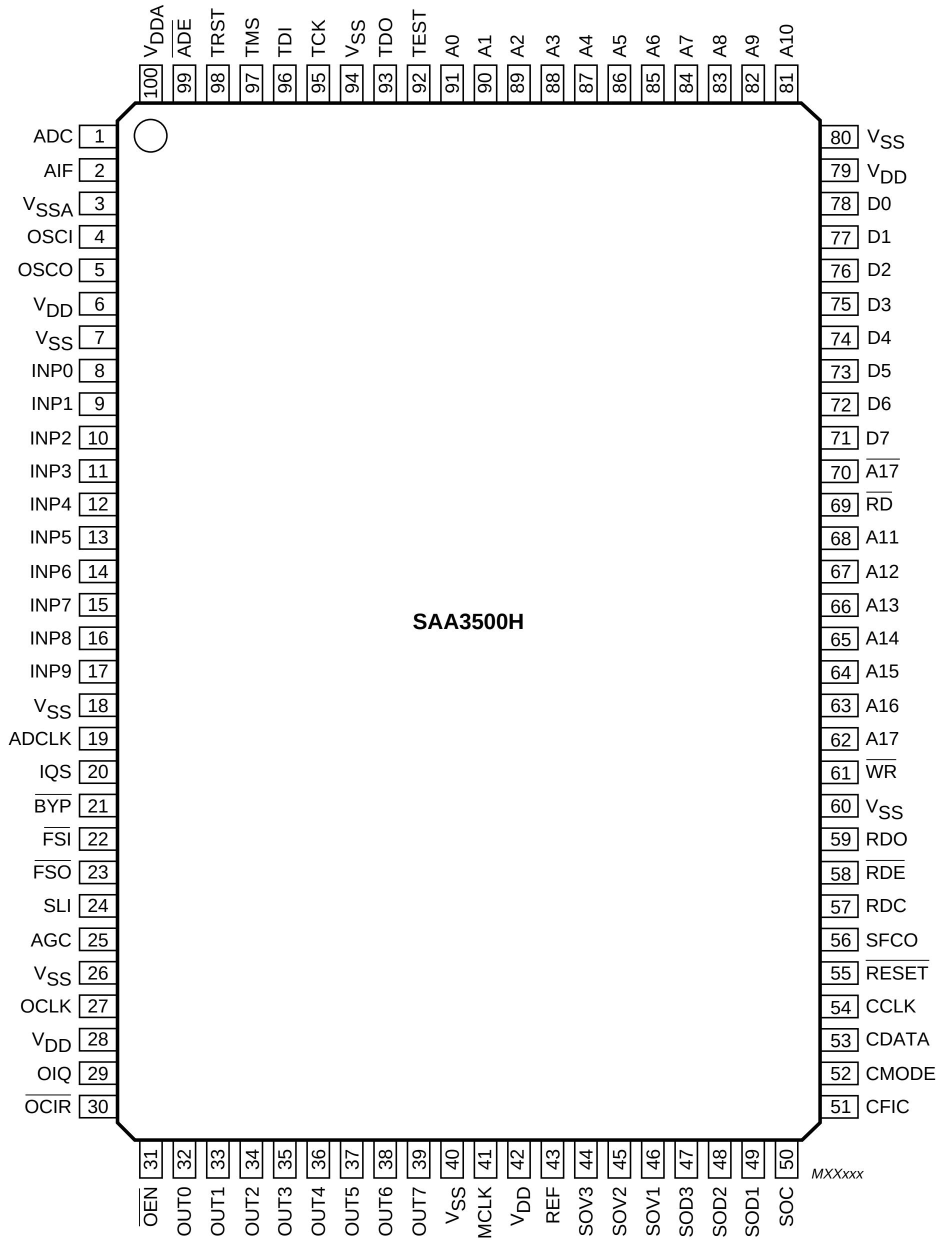


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The 2.048 MHz IF signal is digitized by an 8-bit flash Analog-to-Digital Converter (ADC), which samples at 8.192 MHz. The required input level is limited to a peak-to-peak voltage of 2 V. Due to a fast sample-and-hold circuit sub-sampling is possible, so that all IF frequencies of $N \times 8.192 \pm 2.048$ MHz can be used. If a higher resolution ADC is wanted, an external ADC can be connected.

The digital mixer accepts a 2.048 MHz IF signal at its input and converts it to baseband with In-phase (I) and Quadrature-phase (Q) components. The mixer frequency is adjusted on a DAB frame basis with 1 Hz resolution to prevent performance degradation. The mixer output signals are digitally filtered and subjected to internal Automatic Gain Control (AGC) before entering the subsequent Fast Fourier Transform (FFT) stage.

The output of the digital AGC detectors indicates for each input sample whether the level is below or above the reference input level. By means of external filtering and gain control, the signal can be used to adjust the input signal level of the analog-to-digital converter (external AGC).

The on-chip null detector operates on the digital baseband signal and indicates the coarse position of the DAB null symbol ($\overline{\text{FSO}}$ = LOW), which is used for time base initialization. The spacing of detected null symbols is used to detect the DAB transmission mode.

The time base counts samples on a symbol and a frame basis in order to generate the internal control windows for the FFT and to generate a frame sync signal ($\overline{\text{FSO}}$) during the null symbol. Initialization of the time base is determined by the null detector signal ($\overline{\text{FSI}}$) and the selected DAB mode. After time base initialization the SAA3500H will be in symbol processing mode and the null detector will be deactivated.

The OFDM symbol demodulator applies a real-time FFT and differential demodulation to the baseband signal. The output is quantized to 4-bit metrics for the Viterbi decoder. The position of the FFT window is adjusted on a DAB frame basis in order to avoid Inter-Symbol Interference (ISI).

The FFT result of the reference symbol is processed by the synchronization core, which performs two functions: estimation of the frequency error of the baseband signal, which is needed to adjust the digital mixer (AFC), and calculation of the Channel Impulse Response (CIR) to be used for positioning of the FFT window and the system clock. All timing and frequency control loops are realized in the synchronization core and can be influenced from the control interface.

The Viterbi decoder is preceded by frequency and time de-interleaving of the incoming metrics in external RAM, to distribute burst errors caused by channel fading. Variable rate decoding is done with 3.072 Mb/s decision speed. Output bits are re-encoded and compared to corresponding input bits in order to generate an error flag signal.

Sub-channel selection is done on a Capacity Unit (CU) basis. All standardized Unequal Error Protection (UEP) puncturing schemes for audio and Equal Error Protection (EEP) schemes for data are provided. Up to 64 sub-channels can be selected separately, which means virtually unlimited DAB decoding capabilities.

The output interface provides a full-speed standardized Receiver Data Interface (RDI) for all sub-channel data. This allows to extend every DAB receiver with external decoders for all kind of services. A dedicated interface is provided for the Philips SAA2502H audio source decoder, which completes the DAB receiver.

The system clock of 24.576 MHz, can be generated by an integrated DCXO, which is internally locked to the DAB signal. The clock is available on the MCLK pin to provide a synchronous clock to the MPEG decoder and microcontroller.

The I^2C-bus or L3-bus configurable control interface provides access to Automatic Frequency Control (AFC), Channel Impulse Response (CIR), Fast Information Channel (FIC) and sub-channel selection controls.

9 INTERFACE DESCRIPTION

9.1 Input interface

The input interface can be used in 3 different modes, depending on the bypass ($\overline{\text{BYP}}$) and IQ Select (IQS) pins. Digital input data should be in two's complement format (optionally: offset binary) and synchronized with the ADCLK output signal. Input data are read on the rising edge of ADCLK.

Table 1 Input modes

$\overline{\text{BYP}}$	IQS	DESCRIPTION
0	clk	digital baseband input sampled at 2048 kHz and with I and Q data multiplexed
1	0	digital IF input sampled at 8192 kHz, internal I/Q demodulator
1	1	digital IF input sampled at 8192 kHz, internal I/Q demodulator with I and Q swapped

In case of baseband input the IQ select signal shall indicate whether the current sample is either I or Q data (INP[9:0]).

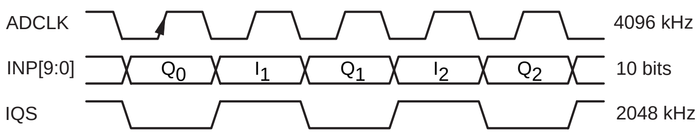


Fig.3 Baseband input signals ($\overline{\text{BYP}}$ = LOW).

Digital IF input is, typically, at a frequency of 2048 kHz. It is possible to apply sub-sampling on a N $\times$ 8.192 $\pm$2.048 MHz (N = 1, 2, 3,...,19) IF signal, but care should be taken with the jitter of the crystal clock, which is proportional to N.

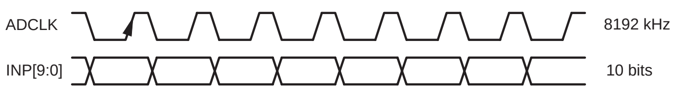


Fig.4 IF input signals [$\overline{\text{BYP}}$ = HIGH, IQS = LOW (no swap) or HIGH (swap)].

To use the on-chip null detector, pins $\overline{\text{FSI}}$ and $\overline{\text{FSO}}$ shall simply be connected to each other.

When using an external null detector, the $\overline{\text{FSI}}$ input shall indicate the position of the null symbol in the baseband signal ($\overline{\text{FSI}}$ = LOW). The negative edge may have a maximum delay of 512 samples with respect to an ideal null detector. The delay compensation can be set via the I^2C/L3 interface (register ATCWinControl). The $\overline{\text{FSI}}$ input provides edge jitter suppression of up to 40 samples starting from the first negative edge. Once the SAA3500H is in symbol processing mode, the $\overline{\text{FSI}}$ signal is ignored. During the null detection state, the Sync Lock Indicator (SLI) will be continuously LOW.

9.2 Memory interface

An external SRAM memory of either 128 or 256 kbytes is required to store the metrics from the data de-interleaver for half (432 CUs) or full (864 CUs) decoding capacity, respectively. The upper address line A17 is available both true and inverted ($\overline{\text{A17}}$) to allow memory extension without an address decoder. 3.3 V RAMs should be used with either an 8 or (2 $\times$) 4-bit data bus and an access time of $\leq$80 ns. Input data are read on the rising edge of $\overline{\text{RD}}$, output data shall be latched on the rising edge of $\overline{\text{WR}}$.

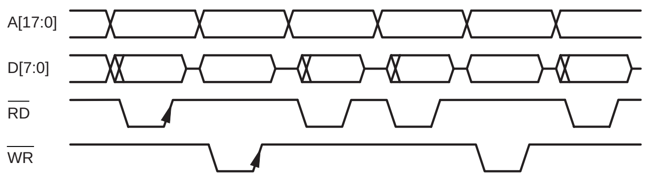


Fig.5 RAM access.

9.3 Parallel output interface

The digital parallel output interface can be used in 3 different modes depending on the $\overline{\text{OCIR}}$ and $\overline{\text{OEN}}$ select pins. Output data shall be latched on the falling edge of OCLK.

Table 2 Parallel output modes
X = don't care.

$\overline{\text{OCIR}}$	$\overline{\text{OEN}}$	DESCRIPTION
0	0	channel impulse response sampled at 64 kHz, OIQ = frame trigger
1	0	baseband sampled at 2048 kHz and with I and Q data multiplexed
X	1	OUT[7:0], OIQ and OCLK disabled

By means of an external digital-to-analog converter, either the CIR or I/Q data can be displayed on an oscilloscope. Digital output data is clocked out on the falling edge of the OCLK output signal. In case of baseband output the OIQ signal indicates, if the current sample is either I or Q data.

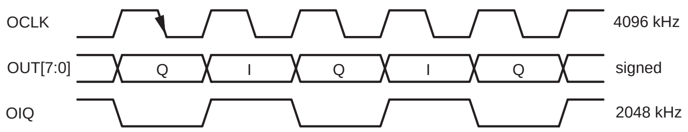


Fig.6 Baseband output signals ($\overline{\text{OCIR}}$ = HIGH, $\overline{\text{OEN}}$ = LOW).

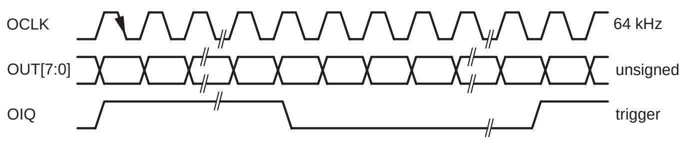


Fig.7 CIR output signals ($\overline{\text{OCIR}}$ = LOW, $\overline{\text{OEN}}$ = LOW).

In the CIR output mode the channel impulse response is clocked out in a burst of N (unsigned) samples at 64 kHz each frame after CIR processing (bit SyncBusy = logic 0). The edges of the frame trigger signal (OIQ) allow to trigger a CIR display either at the start of the symbol or at the start of the symbol guard. In the latter case the CIR peak for a Gaussian channel will be at the left of the display.

9.4 Serial output interface

The serial output interface is intended for transferring up to three sub-channels to the source decoder(s) with a total maximum bit rate of 384 kbit/s. The sub-channels for these outputs should be selected with the appropriate I^2C or L3 commands. The output clock is 384 kHz. Each sub-channel has its own serial data and data valid line, but the clock is common. Serial output data shall be latched on the rising edge of SOC.

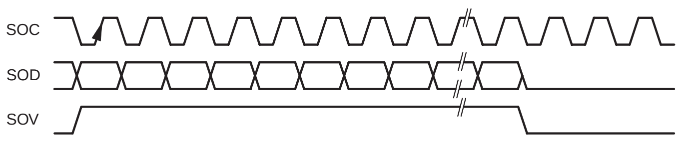


Fig.8 DAB3 serial output.

9.5 Simple full capacity output

This interface provides serial access to all the Viterbi decoder output bits without any formatting. Transmission framing is indicated by the CFIC window, which can also be used to separate the FIC data (CFIC = HIGH) from the Main Service Channel (MSC) data (CFIC = LOW). The bit CFICMode can be used to signal on CFIC the beginning of the selected sub-channels (CFICMode = logic 0). The clock is a 3072 kHz burst clock, activated for each new output bit. Accompanied with the data is the error flag, obtained by re-encoding the Viterbi output bits and comparison with the corresponding Viterbi decoder input bits (REF = HIGH for error bit).

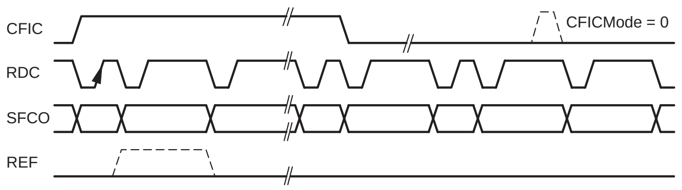


Fig.9 Simple full capacity output (CFICMode = logic 1).

9.6 RDI output

For external use a bi-phase modulated output (RDO) is provided, which carries all the FIC and MSC data, formatted according to the DAB receiver data interface specification *"EN 50255"*, which is based on the IEC 60958 digital audio interface. Optionally, a clock (6144 kHz) and word select signal (48 kHz) can be provided (instead of SFCO signals). Transmitter Identification Information (TII) is not signalled on this RDI. The FIC however is always signalled, with the Cyclic Redundancy Check (CRC) performed and the Error Check Field containing the resulting CRC (normally 0). Selected sub-channels will be directed to the RDI interface in the extended capacity mode (22 bits for MSC), but the number of RDI frames and the reliability are not signalled (i.e., set to all logic 0s and all logic 1s, respectively).

Fig.10 RDI output (normal mode, $\overline{\text{RDE}}$ = LOW).

In case SFCO data output is not desired, a particular ‘RDI plus’ mode can be selected, which provides a continuous 6144 kHz clock on RDC, synchronous to the bi-phase RDI data and accompanied by a fixed word select signal, to allow RDI source reception without an extra clock recovery circuit. Output data shall be latched on the rising edge of RDC.

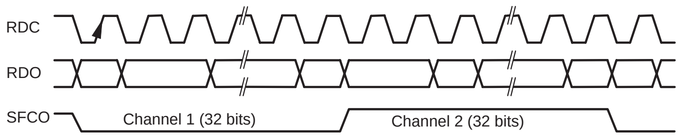


Fig.11 RDI output (RDI plus mode, $\overline{\text{RDE}}$ = LOW).

9.7 Microcontroller interface

The microcontroller interface of the SAA3500H operates in one of two distinct modes of operation: I^{2}C-bus or L3-bus. Mode setting is determined at initialization, as described in Fig.12. On either control bus data are transferred in 8-bit packets, or bytes.

The interface uses three signals and the function in the L3-bus mode or I^{2}C-bus mode is indicated in Table 3.

Table 3 Control bus modes

SIGNAL	L3-BUS MODE	I^{2}C-BUS MODE	DIRECTION	DESCRIPTION
CDATA	L3DATA	SDA	input/output	microcontroller interface serial data
CCLK	L3CLK	SCL	input	microcontroller interface bit clock
CMODE	L3MODE	none	input	microcontroller interface mode select

During a hard reset of the device, the microcontroller interface mode is determined. As a consequence, the interface cannot be used while the reset signal is asserted. Mandatory action must be taken for correct microcontroller interface start-up at a hard reset, as explained in Fig.12.

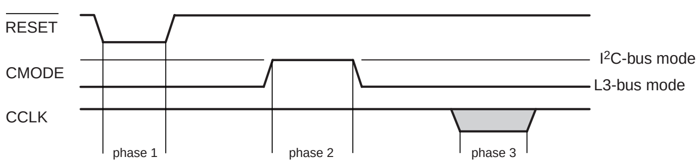


Fig.12 Microcontroller interface initialization procedure.

In phase 1, the level of the CMODE signal determines the microcontroller interface mode, while reset is asserted. CMODE = HIGH defines I²C-bus mode, CMODE = LOW defines L3-bus mode. No transfers can be performed, as CCLK must be HIGH.

In phase 2, which is for L3-bus mode of operation only, it is mandatory to take CMODE HIGH, then LOW again after reset has been de-asserted, to correctly initialize the interface unit. This must occur before any L3-bus transfer (even to or from other devices) is performed. CCLK shall remain HIGH during this phase.

In phase 3, the first transfer can be performed on the microcontroller interface.

Any deviation from these steps may result in undefined behaviour of the microcontroller interface, even with the possibility of disturbing transfers to other devices connected to the control bus.

At a hardware reset, all writeable data items are forced to their default values.

The microcontroller interface provides access to all blocks, which generate or need control information. Selections on the SAA3500H are at the sub-channel level, the required sub-channel parameters should be obtained via the Multiplex Configuration Information (MCI), which is part of the FIC.

The CFIC window from the SAA3500H indicates FIC decoding. FIC data from the I²C/L3 interface will be invalid, if CFIC = HIGH. It is therefore recommended to connect CFIC to a microcontroller interrupt input pin. With regard to the real-time processing requirements, it is highly recommended to use a 16-bit microcontroller.

9.7.1 I²C-BUS MODE

The implemented I²C-bus interface is of the 400 kbit/s, 7-bit address type. The CDATA output driver is of the ‘open drain’ type in order to be compliant with the I²C-bus specification. The device address is as follows:

Table 4 I²C-bus device address

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	0	1	0	1	1	R/$\overline{W}$

Bit 7 to bit 1 comprise the 7-bit I²C-bus slave address, while bit 0 indicates the transfer direction of data and acknowledge bits as follows:

Table 5 Read and write operation to the microcontroller in I²C-bus mode

R/$\overline{W}$	FUNCTION	REMARK
0	data from microcontroller to SAA3500H	all acknowledge generated by SAA3500H
1	data from SAA3500H to microcontroller	acknowledge for data generated by microcontroller

Fundamentals of the I²C-bus interface protocol are shown in Fig.13.

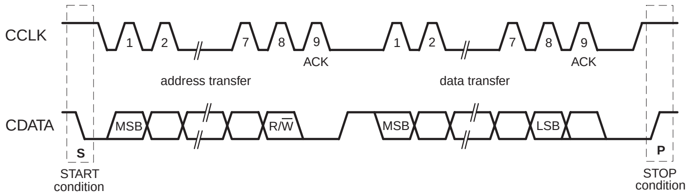


Fig.13 I²C-bus data transfer example.

For full details of the I²C-bus interface specification, please, refer to the I²C-bus specification (http://www.semiconductors.com/handbook/various_38.html), which is also available on request.

9.7.2 L3-BUS MODE

The L3-bus device address is composed as follows:

Table 6 L3-bus device address

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	1	1	0	1	1	DOM1[1]	DOM0[1]

Note

1. The ‘Data Operation Mode’ bits DOM1 and DOM0 define the current sub-mode of the microcontroller interface until the next time a device address is received (see Table 7).

Table 7 Read and write operation to the microcontroller in L3-bus mode

DOM1	DOM0	FUNCTION	REMARK
0	0	data from microcontroller to SAA3500H	general purpose data transfer
0	1	data from SAA3500H to microcontroller	general purpose data transfer
1	0	control from microcontroller to SAA3500H	register selection for data transfer
1	1	status from SAA3500H to microcontroller	short device status message

Fundamentals of the L3-bus interface protocol are shown in Fig.14.

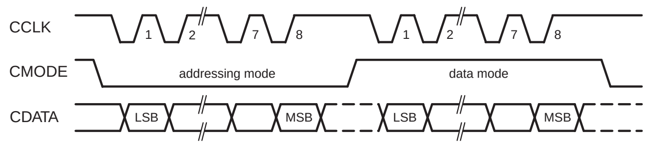


Fig.14 L3-bus command transfer example.

For full details of the L3-bus interface specification, please, refer to the SAA2502H data sheet (order number 9397 750 03068 or at http://www.semiconductors.com/products).

9.7.3 MICROCONTROLLER INTERFACE REGISTERS

Communication between the microcontroller and the SAA3500H is by addressing registers and writing or reading data. All addresses and register contents are in hexadecimal notation.

The following registers are available for the writing of data:

Table 8 Writeable registers

ADDRESS (HEX)	NAME	DESCRIPTION	SETTING AFTER RESET (HEX)
00	Control	control	1F
01	Configuration	configuration	FF
10	CIFCount	CIF count and occurrence change flag	00 00 00
20	CurSubChSel	current sub-channel selection	00 00 00 00
21	NextSubChSel	next sub-channel selection	00 00 00 00
30	SOD1	select sub-channel for serial output SOD1	40
31	SOD2	select sub-channel for serial output SOD2	40
32	SOD3	select sub-channel for serial output SOD3	40
40	AGCExternal	setting of thresholds for external AGC	61 0C
41	AGCInternal	settings of the internal AGC	D0 49
42	AGCFixed	internal AGC switch off and fixed gain setting	00
50	NullDetMargin	null detector margin	40
51	TIIControl	TII main/sub identifier	00 00
60	MixerFreqInput	digital mixer frequency control input	80 00 00
62	CarrierShift	carrier shift by n carrier positions	00
63	AFCGain	AFC loop gain	10
70	ATCWinControl	ATC window control input or FFT window position and null detector delay compensation	96
71	CIRThreshold	CIR detector thresholds, edge and range	02 02
73	ATCGains	ATC loops gains; clock I and P gains and window gain	02 04 20

The following registers are available for the reading of data:

Table 9 Readable registers

ADDRESS (HEX)	NAME	DESCRIPTION	BYTES TO READ
00	Status	internal processing status	1
10	FICErrCount	FIC error count per frame	2
20 to 2B	FICData	FIC data inclusive CRC result	32
51	TIIOutput	TII complex phase values	6
60	AFCLoopOutput	AFC loop output for digital mixer frequency control	3
61	CarrierDev	AFC carrier deviation detector	2
70	ATCWinOutput	ATC window loop output for FFT window position	1
71	ATCDetector	ATC CIR detector output	3
72	ATCClockOutput	ATC clock loop output for external VCXO	1
76	CIRPower	power of CIR response	2

A description of how to use the individual registers is given in a separate application note.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage	note 1	–0.5	+6	V
V_i	input voltage		–0.5	V_{DD} + 0.5	V
I_{DD}	supply current		–	200	mA
I_i	input current		–10	+10	mA
I_o	output current		–10	+10	mA
P_{tot}	total power dissipation		–	650	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	note 2	–300	+300	V
		note 3	–3000	+3000	V

Notes

1. All supply connections must be made to the same external power supply unit.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (‘0 Ω’ is actually 0.75 µH + 10 Ω).
3. Human body model: equivalent to discharging a 100 pF capacitor through a 1500 Ω series resistor.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

12 DC CHARACTERISTICS

V_{DD} = 3.0 to 3.6 V; T_{amb} = –40 to +85 °C; all voltages referenced to ground (V_{SS}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DD(tot)}$	total DC supply voltage	note 1	3.0	3.3	3.6	V
$I_{DD(tot)}$	total DC supply current		–	–	180	mA
Dissipation						
P_{tot}	total power dissipation		–	–	650	mW
Inputs						
CMOS LEVEL INPUT (INP[9:0], $\overline{FSI}$, CCLK AND TCK)						
V_{IH}	HIGH-level input voltage		2.0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$\|I_{LI}\|$	input leakage current	$V_I = 0$ or $V_I = V_{DD}$	–	–	1	μA
C_i	input capacitance		–	5	–	pF
CMOS LEVEL INPUT, PULL-UP ($\overline{BYP}$, CMODE, IQS, $\overline{OCIR}$, $\overline{OEN}$, $\overline{RDE}$, TDI, TMS AND TRST)						
V_{IH}	HIGH-level input voltage		2.0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$R_{pu(VDD)(int)}$	internal pull-up resistor to V_{DD}		16	33	78	kΩ
C_i	input capacitance		–	5	–	pF
CMOS LEVEL INPUT, HYSTERESIS, PULL-UP ($\overline{RESET}$)						
$V_{IH(hys)}$	HIGH-level hysteresis input, rising edge		1.4	–	1.9	V
$V_{IL(hys)}$	LOW-level hysteresis input, falling edge		0.9	–	1.45	V
V_{hys}	hysteresis voltage		0.4	–	0.7	V
$R_{pu(VDD)(int)}$	internal pull-up resistor to V_{DD}		16	33	78	kΩ
C_i	input capacitance		–	5	–	pF
Inputs/outputs						
CMOS LEVEL INPUT, HYSTERESIS, OPEN DRAIN OUTPUT (CDATA)						
$V_{IH(hys)}$	HIGH-level hysteresis input, rising edge		1.4	–	1.9	V
$V_{IL(hys)}$	LOW-level hysteresis input, falling edge		0.9	–	1.45	V
V_{hys}	hysteresis voltage		0.4	–	0.7	V
V_{OL}	LOW-level output voltage	I_{LOAD} = 3 mA	–	–	0.4	V
CMOS LEVEL INPUT, 1.5 mA OUTPUT STAGE (D[7:0])						
V_{IH}	HIGH-level input voltage		2.0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$\|I_{LI}\|$	input leakage current	$V_I = 0$ or $V_I = V_{DD}$	–	–	1	μA
V_{OH}	HIGH-level output voltage	I_{LOAD} = –1.5 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{LOAD} = 1.5 mA	–	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
CMOS LEVEL, 1.5 mA OUTPUT STAGE (A[17:0], $\overline{A17}$, ADCLK, AGC, $\overline{FSO}$, OCLK, OIQ, $\overline{RD}$, SLI, SOD[1:3], SOV[1:3] AND $\overline{WR}$)						
V_{OH}	HIGH-level output voltage	I_{LOAD} = –1.5 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{LOAD} = 1.5 mA	–	–	0.4	V
C_{LOAD}	output load capacitance		–	–	30	pF
CMOS LEVEL, 1.5 mA 3-STATE OUTPUT STAGE, (OUT[7:0])						
V_{OH}	HIGH-level output voltage	I_{LOAD} = –1.5 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{LOAD} = 1.5 mA	–	–	0.4	V
$\|I_{LO}\|$	output leakage current	inactive mode; V_O = 0 or $V_O = V_{DD}$	–	–	1	μA
C_{LOAD}	output load capacitance		–	–	30	pF
CMOS LEVEL, 3 mA OUTPUT STAGE (CFIC, MCLK, RDC, RDO, REF, SFCO, SOC AND TDO)						
V_{OH}	HIGH-level output voltage	I_{LOAD} = –3 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{LOAD} = 3 mA	–	–	0.4	V
C_{LOAD}	output load capacitance		–	–	50	pF

Note

1. All supply connections must be made to the same external power supply unit.

13 AC CHARACTERISTICS

V_{DD} = 3.0 to 3.6 V; T_{amb} = 25 °C; all voltages referenced to ground (V_{SS}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator input (OSC)						
$f_{i(OSC)}$	input frequency	note 1	–	24576	–	kHz
δ_{OSC}	input clock duty factor		40	–	60	%
Reset input ($\overline{RESET}$)						
$t_{CL,RESET}$	reset LOW duration	note 2	60 × T	–	–	ns
Input interface (ADCLK, $\overline{BYP}$, INP[9:0] and IQS)						
BASEBAND INPUT ($\overline{BYP}$ = LOW); see Fig.15						
$T_{cy,ADCLK}$	ADCLK cycle time		–	244	–	ns
$t_{CL,ADCLK}$	ADCLK LOW time		–	122	–	ns
$t_{CH,ADCLK}$	ADCLK HIGH time		–	122	–	ns
$t_{h,INP}$	INP[9:0] hold time		5	–	–	ns
$t_{h,IQS}$	IQS hold time		–	–	80	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF INPUT ($\overline{BYP}$ = HIGH); see Fig.16						
$T_{cy,ADCLK}$	ADCLK cycle time		–	122	–	ns
$t_{CL,ADCLK}$	ADCLK LOW time		–	80	–	ns
$t_{CH,ADCLK}$	ADCLK HIGH time		–	42	–	ns
$t_{h,INP}$	INP[9:0] hold time		5	–	–	ns
$t_{d,INP}$	INP[9:0] delay time		–	–	25	ns
Memory interface ($\overline{A17}$, A[17:0], D[7:0], $\overline{RD}$ and $\overline{WR}$); see Figs 17 and 18						
$T_{cy,A}$	address cycle time		–	326	–	ns
$t_{CL,RD}$	$\overline{RD}$ LOW time		–	163	–	ns
$t_{d,RD}$	$\overline{RD}$ delay time		–	40	–	ns
$t_{h,RD}$	$\overline{RD}$ hold time		–	0	–	ns
$t_{CL,WR}$	$\overline{WR}$ LOW time		–	163	–	ns
$t_{d,WR}$	$\overline{WR}$ delay time		0	40	–	ns
$t_{d,D}$	data delay time		–	0	–	ns
$t_{h,D}$	data hold time		–	–	5	ns
Parallel output interface ($\overline{OCIR}$, OCLK, $\overline{OEN}$, OIQ and OUT[9:0])						
BASEBAND OUTPUT ($\overline{OCIR}$ = HIGH); see Fig.19						
$T_{cy,OCLK}$	OCLK cycle time		–	244	–	ns
$t_{CL,OCLK}$	OCLK LOW time		–	122	–	ns
$t_{CH,OCLK}$	OCLK HIGH time		–	122	–	ns
$t_{su,OUT}$	OUT[7:0] set-up time		–	15	–	ns
$t_{su,OIQ}$	OIQ set-up time		–	17	–	ns
CIR OUTPUT ($\overline{OCIR}$ = LOW); see Fig.20						
$T_{cy,OCLK}$	OCLK cycle time		–	15.6	–	µs
$t_{CL,OCLK}$	OCLK LOW time		–	8.3	–	µs
$t_{CH,OCLK}$	OCLK HIGH time		–	7.3	–	µs
$t_{su,OUT}$	OUT[7:0] set-up time		–	0	–	ns
$t_{su,OIQ}$	OIQ set-up time		–	0	–	ns
Serial output interface (SOC, SOD[3:1] and SOV[3:1]); see Fig.21						
$T_{cy,SOC}$	SOC cycle time		–	2.6	–	µs
$t_{CL,SOC}$	SOC LOW time		–	1.3	–	µs
$t_{CH,SOC}$	SOC HIGH time		–	1.3	–	µs
$t_{h,SOD}$	SOD hold time		–	0	–	ns
$t_{su,SOV}$	SOV set-up time		–	4	–	ns
$t_{h,SOV}$	SOV hold time		–	2	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Simple full capacity output interface (CFIC, RDC, REF and SFCO); see Fig.22						
$t_{CH,CFIC}$	CFIC HIGH time	DAB mode I	–	3.738	–	ms
		DAB mode II	–	0.935	–	ms
		DAB mode III	–	1.246	–	ms
		DAB mode IV	–	1.869	–	ms
$t_{SH,CFIC}$	CFIC strobe HIGH time	bit CFICMode = 0	–	75	–	ns
		bit CFICMode = 1	–	0	–	ns
$t_{su,CFIC}$	CFIC set-up time		–	165	–	ns
$t_{h,CFIC}$	CFIC hold time		–	80	–	ns
$T_{cy,RDC}$	RDC cycle time		325	–	–	ns
$t_{CH,RDC}$	RDC HIGH time		250	–	–	ns
$t_{CL,RDC}$	RDC LOW time		–	75	–	ns
$t_{su,SFCO}$	SFCO set-up time		–	5	–	ns
$t_{su,REF}$	REF set-up time		–	165	–	ns
$t_{h,REF}$	REF hold time		–	–160	–	ns
RDI output interface (RDC, $\overline{\text{RDE}}$, RDO and SFCO)						
NORMAL MODE; see Fig.23						
t_{ONE}	ONE time		–	163	–	ns
t_{ZERO}	ZERO time		–	326	–	ns
RDI PLUS MODE; see Fig.24						
$T_{cy,RDC}$	RDC cycle time		–	163	–	ns
$t_{CH,RDC}$	RDC HIGH time		–	86	–	ns
$t_{CL,RDC}$	RDC LOW time		–	77	–	ns
$T_{cy,SFCO}$	SFCO cycle time		–	20.8	–	µs
$t_{CH,SFCO}$	SFCO HIGH time		–	10.4	–	µs
$t_{CL,SFCO}$	SFCO LOW time		–	10.4	–	µs
$t_{su,SFCO}$	SFCO set-up time		–	4	–	ns
$t_{h,SFCO}$	SFCO hold time		–	0	–	ns
Microcontroller interface						
INITIALIZATION PROCEDURE; see Fig.25						
$t_{CL,RESET}$	$\overline{\text{RESET}}$ LOW time	note 2	$60 \times T$	–	–	ns
$t_{d,RES-MOD}$	delay time from $\overline{\text{RESET}}$ to CMODE	note 2	$10 \times T$	–	–	ns
$t_{CH,CMODE}$	CMODE HIGH time	note 2	$10 \times T$	–	–	ns
$t_{d,MOD-CLK}$	delay time from CMODE to first CCLK	note 2	$10 \times T$	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L3-BUS MICROCONTROLLER TO SLAVE DEVICE; see Figs 26 and 28						
t_{cL}	L3CLK LOW time	note 2	T + 10	–	–	ns
t_{cH}	L3CLK HIGH time	note 2	T + 10	–	–	ns
t_{d1}	L3MODE set-up time before first L3CLK LOW		10	–	–	ns
t_{h1}	L3DATA hold time after L3CLK HIGH		10	–	–	ns
t_{h2}	L3MODE hold time after last L3CLK HIGH		15	–	–	ns
t_{su}	L3DATA set-up time before L3CLK HIGH	note 2	T + 10	–	–	ns
t_L	L3MODE LOW time	note 2	T + 10	–	–	ns
L3-BUS SLAVE DEVICE TO MICROCONTROLLER; see Fig.27						
t_{d2}	L3MODE HIGH to L3DATA enabled time		0	–	20	ns
t_{d3}	L3MODE HIGH to L3DATA stable time		–	–	20	ns
t_{d4}	L3CLK HIGH to L3DATA stable time	note 2	–	–	2T + 30	ns
t_{d5}	L3MODE LOW to L3DATA disabled time		0	–	20	ns
t_{h3}	L3DATA hold time after L3CLK HIGH	note 2	T	–	–	ns
I^2C-BUS INPUTS/OUTPUT (CDATA AND CCLK)						
$t_{f,I2C}$	output fall time		–	–	250	ns
f_{CCLK}	CCLK clock frequency		–	–	400	kHz

Notes

1. In a real application, the clock frequency may vary in a range of ±50 ppm due to timing synchronization.
2. T = 4 × OSC cycle time, i.e., T = 163 ns at f_{osc} = 24.576 MHz.

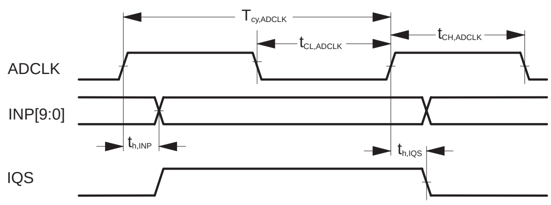


Fig.15 Baseband input timing ($\overline{BYP}$ = LOW).

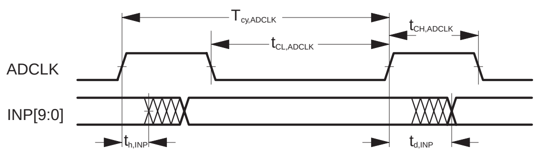


Fig.16 IF input timing [$\overline{BYP}$ = HIGH, IQS = LOW (no swap) or HIGH (swap)].

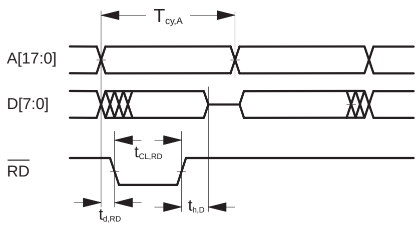


Fig.17 RAM access read timing.

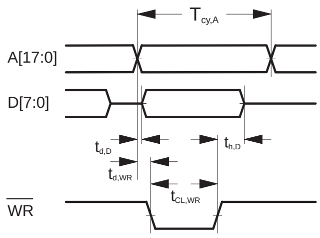


Fig.18 RAM access write timing.

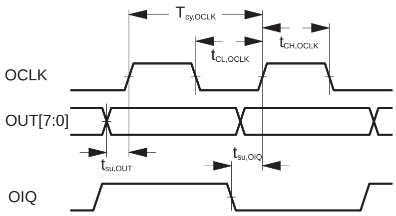


Fig.19 Baseband output timing ($\overline{OCIR}$ = HIGH, $\overline{OEN}$ = LOW).

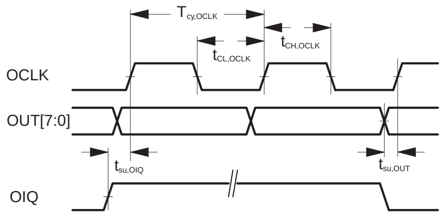


Fig.20 CIR output timing ($\overline{OCIR}$ = LOW, $\overline{OEN}$ = LOW).

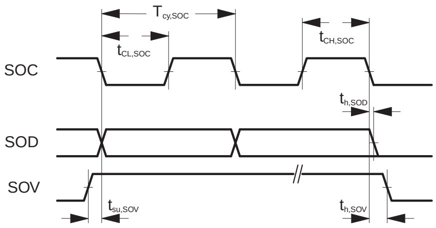


Fig.21 DAB3 serial output timing.

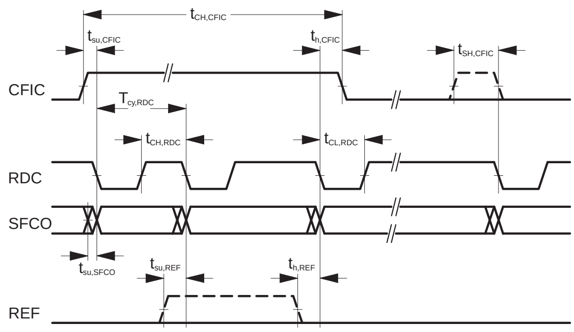


Fig.22 Simple full capacity output timing.

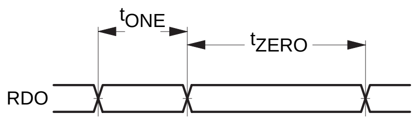


Fig.23 RDI output timing (normal mode, $\overline{RDE}$ = LOW).

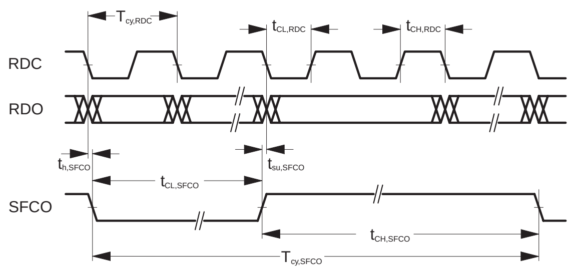


Fig.24 RDI output timing (RDI plus mode, $\overline{RDE}$ = LOW).

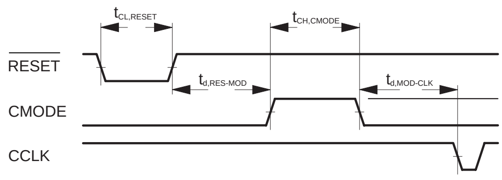


Fig.25 Microcontroller interface initialization timing.

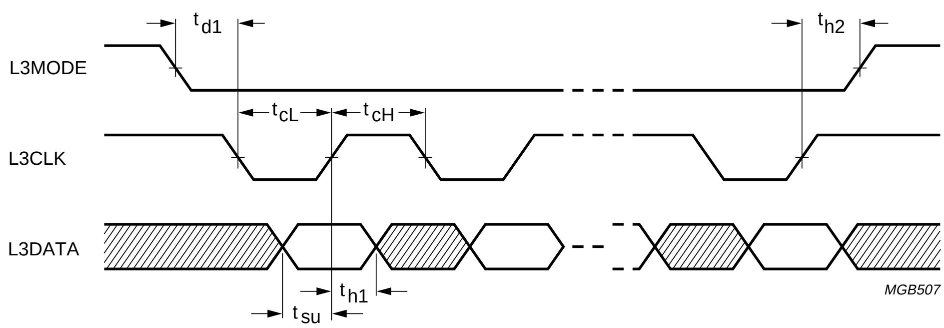


Fig.26 Timing of L3-bus addressing mode.

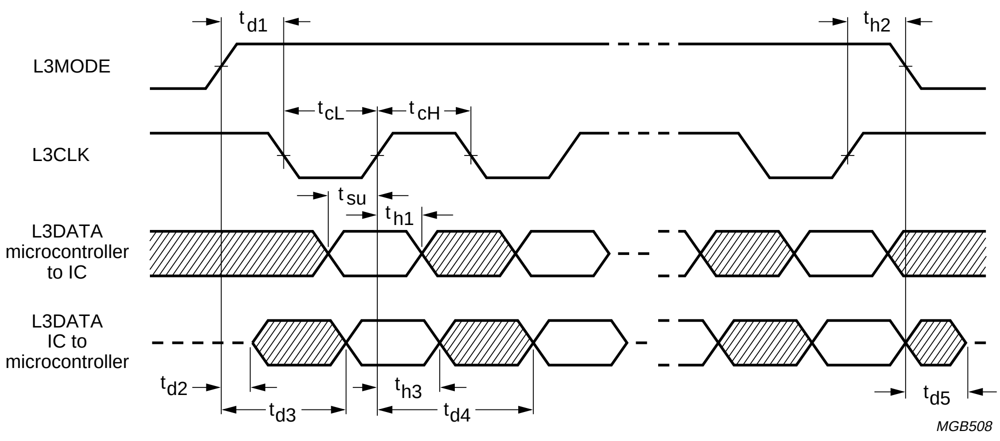


Fig.27 Timing of L3-bus data transfer mode.

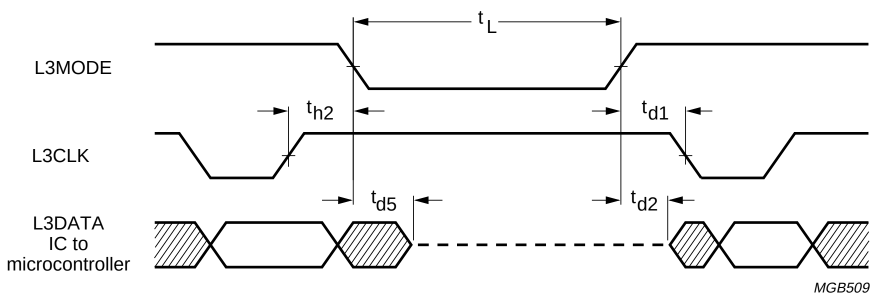


Fig.28 Timing of L3-bus halt mode.

14 APPLICATION INFORMATION

A suggestion for an application block diagram is shown in Fig.29.

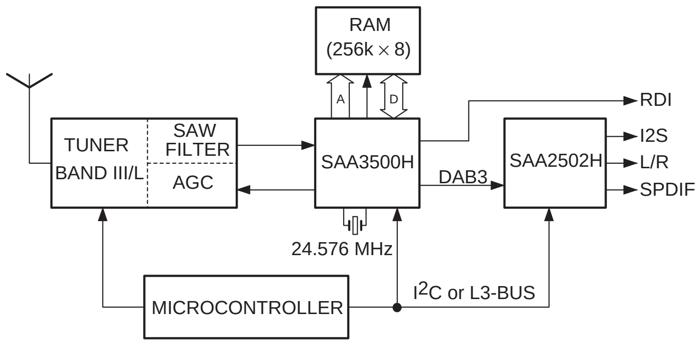


Fig.29 Typical application diagram.

14.1 Clock oscillator

To perform automatic fine tuning of the clock signal, the microcontroller reads data from the SAA3500H and controls an external (VCXO) crystal oscillator. The following requirements should be met by that oscillator:

Table 10 VCXO specification

PARAMETER	VALUE	UNIT
Frequency	24576	kHz
Pull range	±50	ppm
Operating temperature	–40 to +85	°C
Frequency drift with temperature	≤±20	ppm
Tolerance and ageing	≤±10	ppm

14.2 Reset input

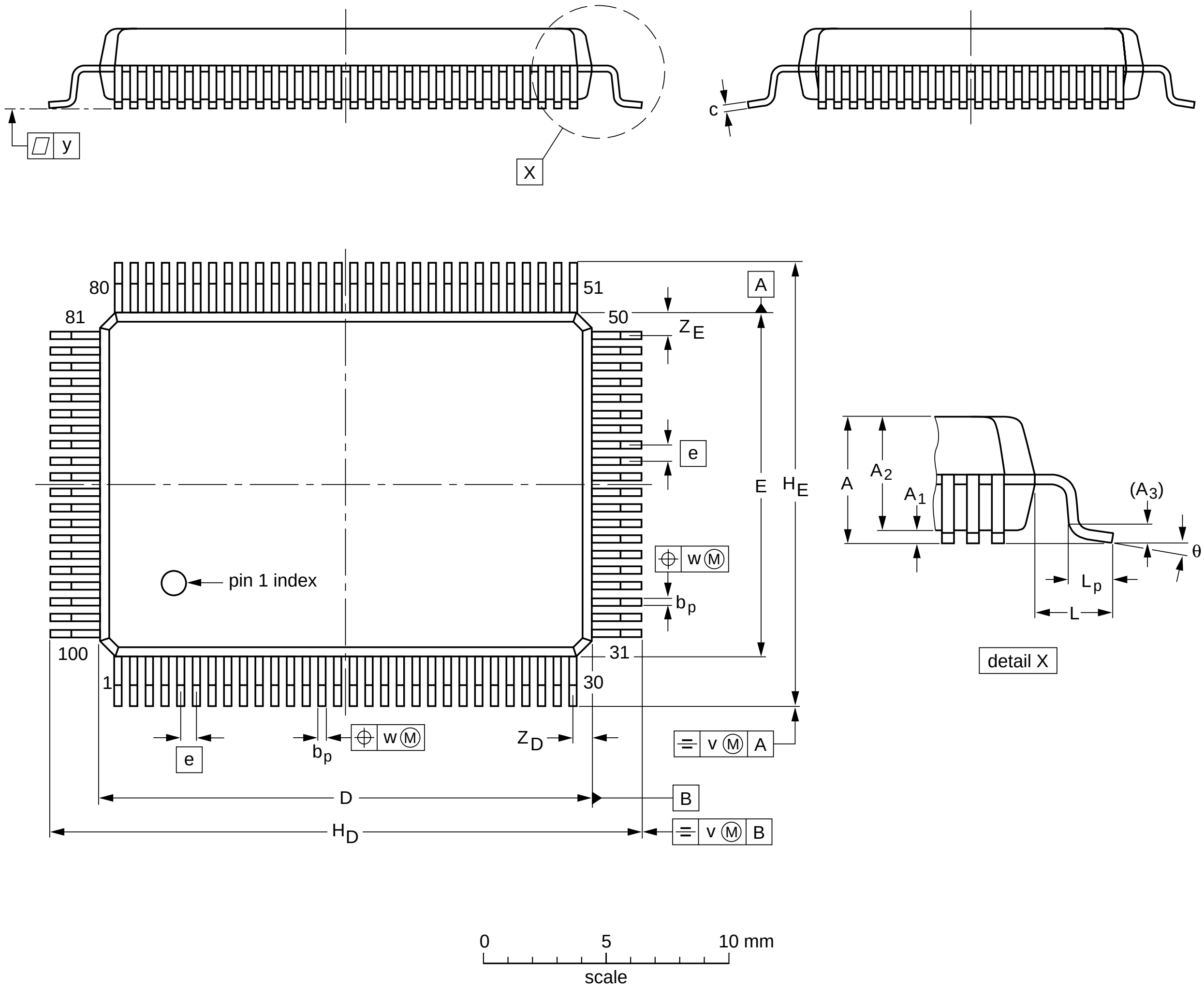
The reset signal is active LOW and should have a minimum duration of 60 clock cycles.

14.3 Boundary scan test interface

For normal operation set TRST LOW, TCK LOW or HIGH, TDI and TMS not connected or HIGH. The boundary scan chain has a length of 84 and a 5-bit instruction code.

15 PACKAGE OUTLINE

QFP100: plastic quad flat package;
100 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT317-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.40 0.25	0.25 0.13	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-1		MO-112				~~97-08-01~~ 99-12-27

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

18 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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