DATA SHEET

SAA4700
VPS dataline processor

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

VPS dataline processor SAA4700

FEATURES

- Adaptive sync slicer with buffered composite sync output VCS
- Adaptive data slicer
- Data rate clock regenerator
- Field selection and line 16 decoding
- Startcode and biphase check
- Data valid output
- Storage of data line information in a 40 bit register bank
- I^2C-bus transmission

GENERAL DESCRIPTION

The SAA4700 is a bipolar integrated circuit designed for use in dataline receivers and incorporates a dataline slicer and decoder. The slicer extracts the dataline signal from the video signal and regenerates the data clock. It also provides signals for the decoder in order to decode the binary data that is transmitted in line 16 of every first field of the composite video signal (video programming signal and video recording programming by Teletext, VPS and VPT systems). The decoded information out of words 5 and 11 to 14 is accessed via the built-in I^2C-bus interface. This information then can be used for programming a video cassette recorder in order to start and stop a recording of a television program at the correct aligned time, regardless of a delay or extension in the transmission time of the required program.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pins 15 and 16)	4.5	5	5.5	V
I_P	total supply current	–	18	23	mA
$V_{i\ CVBS}$	CVBS input signal sync-to-white (peak-to-peak value)	0.5	1	1.4	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA4700	18	DIL	plastic	SOT102 (1)

Note

1. SOT102-1; 1996 December 4.

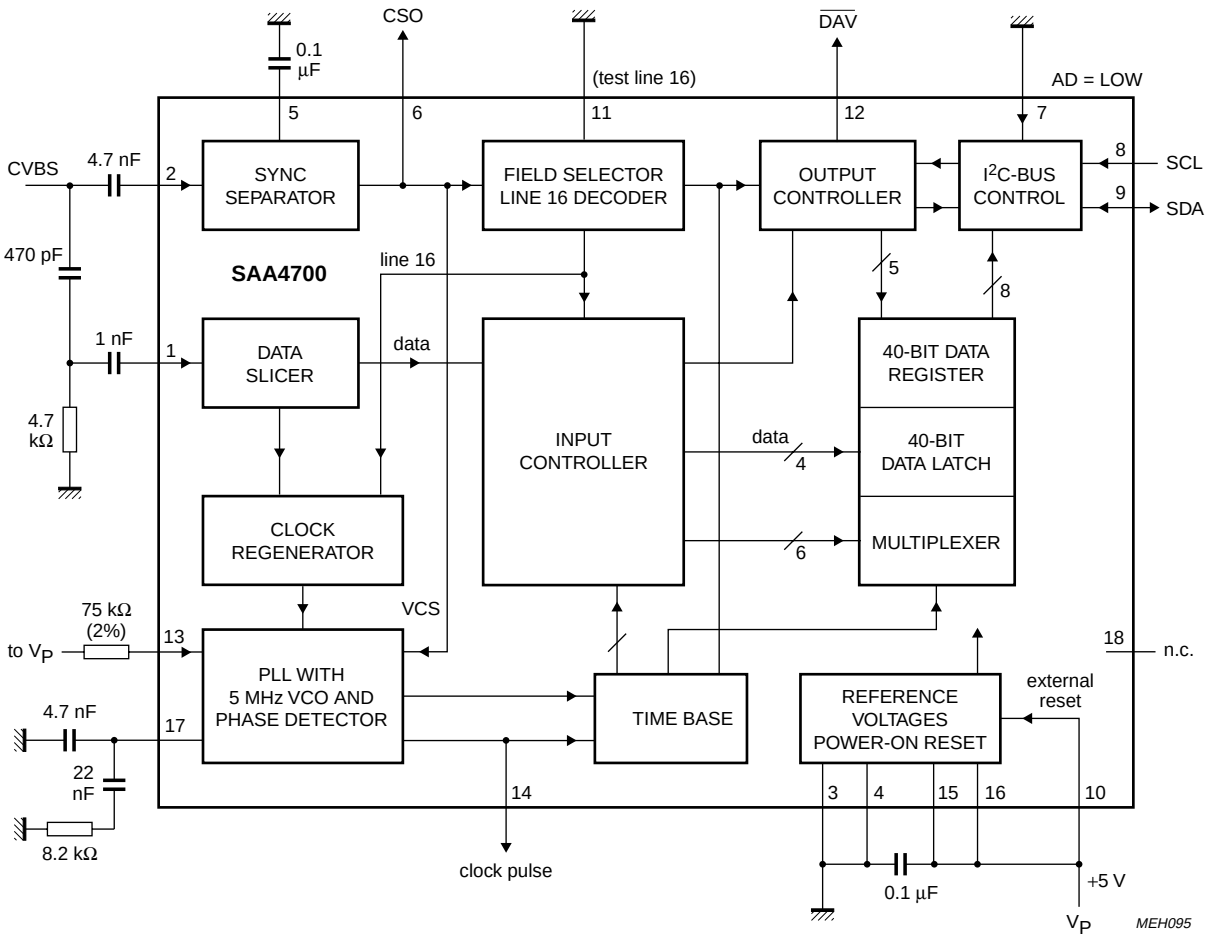


Fig.1 Block diagram and test circuit.

FUNCTIONAL DESCRIPTION

Dataline 16

The information in dataline 16 consists of fifteen 8-bit words; the total information content is shown in Table 1; and the organization of transmitted bytes is shown in Table 2.

Out of the fifteen possible 8-bit words the SAA4700 extracts words 5 and 11 to 14. The contents of these words can be read via the built-in I²C-bus interface. The circuit is fully transparent, thus each bit is transferred without modification with only the sequence of words being changed. Words 11 to 14 are transmitted first followed by word 5.

By evaluating the sliced sync signal the circuit can identify the beginning of dataline 16 in the first field. The dataline decoder stage releases the start code detector. When a correct start code is detected (for timing of start code detection see Fig.3) words 5 and 11 to 14 are decoded, checked for biphase errors and stored in a register bank. If no biphase error has occurred, the contents of the register bank are transferred to a second register bank by the data valid control signal. If the system has been addressed, this transfer will be delayed until the next start or stop condition of the I²C-bus has been received.

The last bit of correct information on the dataline remains available until it is read via the I²C-bus. Once the stored information has been read it is considered to be no longer valid and the internal new data flag is reset. Subsequently, if the circuit is addressed, the only VPS data that will be sent back is ”FFF to F”. The same conditions apply after power-up when no data can be read out. New data is available after reception of another error-free dataline 16.

PINNING

SYMBOL	PIN	DESCRIPTION
CVBS	1	video signal input (CVBS from TV)
SYNC	2	sync amplitude input (CVBS from TV)
GND1	3	analog ground (0 V)
GND2	4	digital ground (0 V)
C_{black}	5	capacitor for black level
CSO	6	composite sync output
AD	7	address set input
SCL	8	I^2C-bus clock line
SDA	9	I^2C-bus data line
$\overline{RS}$	10	reset input active LOW
TP	11	test point for line 16 decoder
$\overline{DAV}$	12	data available output active LOW
R_{osc}	13	oscillator resistor for frequency adjustment
CP	14	test point clock pulse
V_{P1}	15	+5 V supply voltage (digital part)
V_{P2}	16	+5 V supply voltage (analog part)
C_{ph}	17	capacitor of phase detector
n.c.	18	not connected

PIN CONFIGURATION

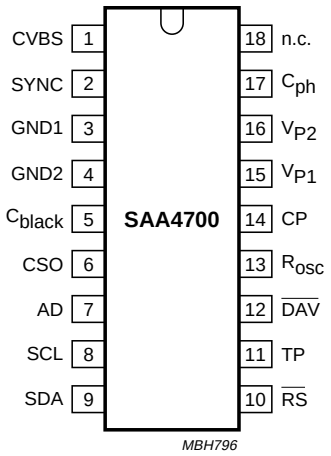


Fig.2 Pin configuration

External reset

The circuit provides an internal power-on reset. When using this facility pin 10 should be connected to V_P or, if external reset (RESET = LOW) is to be used pin 10 should be prepared by connecting pin 10 via a 10 kΩ pull-up resistor to V_P.

Reset forces the following:

- I^2C-bus not to acknowledge
- $\overline{DAV}$ output to go HIGH (pin 12)
- I^2C-bus transfer register to “FFF”

CVBS input

The CVBS signal is applied to the sync separator (pin 2) via a decoupling capacitor and to the data slicer (pin 1) via an RC high-pass filter.

To enable proper storage of the sync value in the decoupling capacitor, the sync generator output resistance should not exceed 1 kΩ.

Black level

The capacitor connected to pin 5 stores the black level value for the adaptive sync slicer.

Composite sync output (CSO)

A composite sync output signal for customer application is provided (pin 6).

$\overline{DAV}$ output

The data available output pin 12 is set LOW after an error free dataline 16 is received. $\overline{DAV}$ returns to HIGH after the beginning of the next first field. If no valid data is available $\overline{DAV}$ remains HIGH. A short duration pulse of 1 µs (Fig.5) is inserted at the beginning of dataline 16; it will ensure that a HIGH-to-LOW transmission occurs which can then be used for triggering.

5 MHz VCO and phase detector

The resistor connected between pin 13 and V_{P2} determines the current into the voltage controlled oscillator. The RC network connected to pin 17 acts as a low-pass filter for the phase detector.

Power supply

To prevent crosscoupling the circuit is provided with separate ground and supply pins for analog and digital parts (pins 3, 4, 15 and 16).

Table 1 Information per word in dataline 16

word number	content
1	run in
2	start code
3	program source identification (binary coded)
4	program source identification (ASCII sequential)
5	sound and VTR control information
6	program/test picture identification
7	internal information exchange
8	address assignment of signal distribution
9	address assignment of signal distribution
10	messages/commands
11 12 13 14	VTR control / information
15	reserve

Table 2 VTR control information of dataline 16

<table>
<tr><td></td><td colspan="9">VTR CONTROL INFORMATION</td></tr>
<tr><td>Word number</td><td>5</td><td colspan="2">11</td><td colspan="2">12</td><td colspan="2">13</td><td colspan="2">14</td></tr>
<tr><td>Bit number</td><td>1 8
X X X X X X X X</td><td colspan="2">0 7
X X X X X X X X</td><td colspan="2">8 15
X X X X X X X X</td><td colspan="2">16 23
X X X X X X X X</td><td colspan="2">24 31
X X X X X X X X</td></tr>
<tr><td>Label binary</td><td rowspan="5">Word 5:
<table><tr><td>Bit1</td><td>Bit2</td><td>Status</td></tr><tr><td>0</td><td>0</td><td>2-channel</td></tr><tr><td>0</td><td>1</td><td>Mono</td></tr><tr><td>1</td><td>0</td><td>Stereo</td></tr><tr><td>1</td><td>1</td><td>2-channel</td></tr><tr><td>Bit3</td><td>Bit4</td><td>Status</td></tr><tr><td>1</td><td>0</td><td>free</td></tr><tr><td>0</td><td>1</td><td>free</td></tr></table></td><td>AD (1)</td><td>Day</td><td>Month</td><td colspan="2">Hour</td><td>Minute</td><td>Nation</td><td>Progr. source</td></tr>
<tr><td></td><td></td><td colspan="7">Special system code</td></tr>
<tr><td>System status code</td><td colspan="6">1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td>NC...NC</td><td>PC...PC</td></tr>
<tr><td>Pause code</td><td colspan="6">1 X 0 0 0 0 0 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1</td><td>NC...NC</td><td>PC...PC</td></tr>
<tr><td>Interrupt code</td><td colspan="6">1 X 0 0 0 0 0 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1</td><td>NC...NC</td><td>PC...PC</td></tr>
</table>

Note

1. address range; NC = nation code; PC = program source code; X = 0 or 1 (bit)

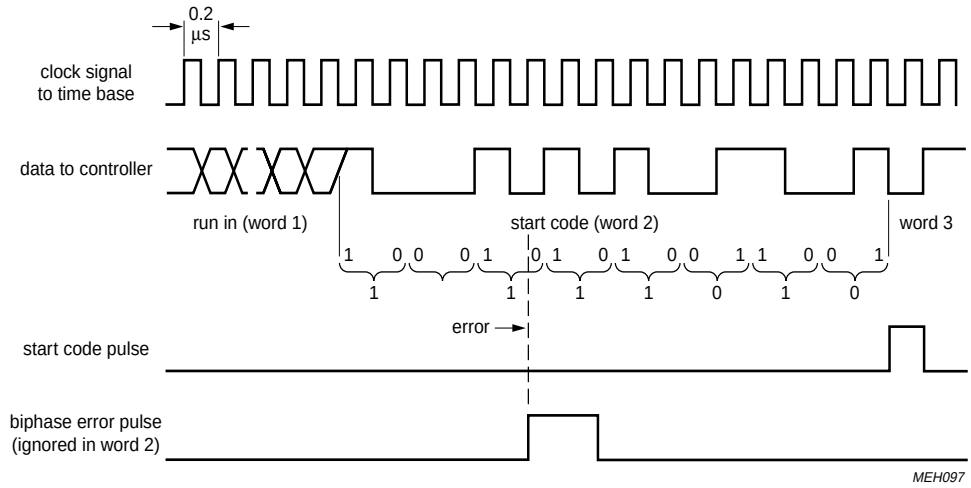


Fig.3 Timing diagram of start code detection.

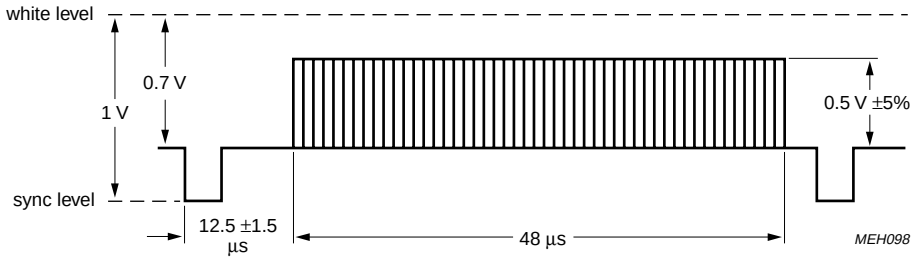


Fig.4 Timing diagram of dataline 16; modulation depth 71.4%.

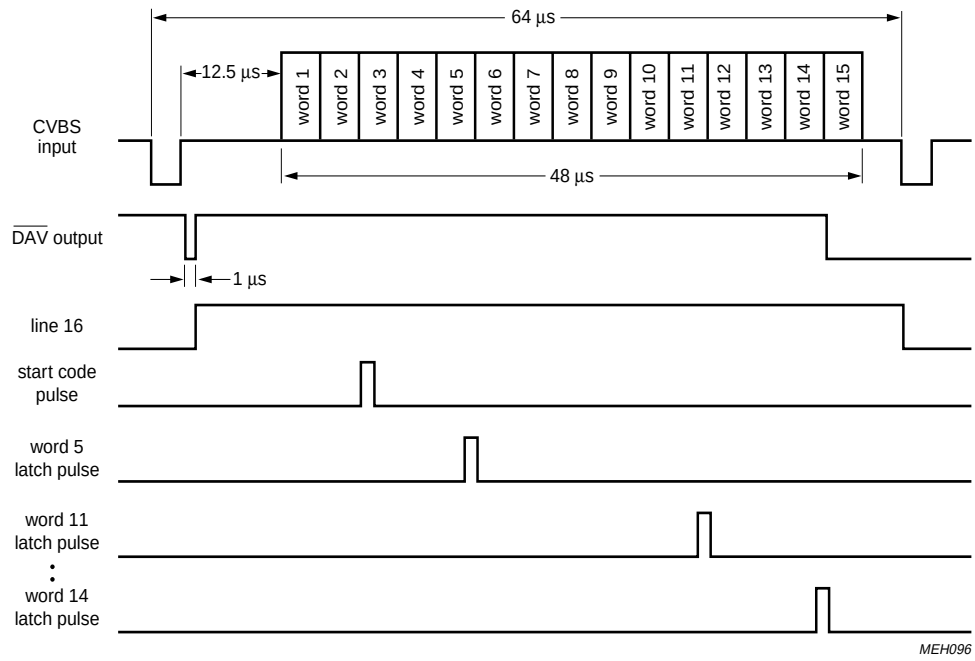


Fig.5 Timing diagram of the data available output and word latch pulses.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 3 and 4 as well as supply pins 15 and 16 tied together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{P1}	supply voltage (pin 15)	–0.5	6.0	V
V_{P2}	supply voltage (pin 16)	–0.5	6.0	V
T_{stg}	storage temperature range	–20	125	°C
T_{amb}	operating ambient temperature range	0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	–	78	K/W

CHARACTERISTICS

$V_{P1} = V_{P2} = 5$ V; $T_{amb} = 25$ °C; CVBS signal according to VPS and VPT standard and measurements taken in Fig.1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{P1}, V_{P2}	supply voltages (pins 15 and 16)		4.5	5	5.5	V
I_P	total supply current	$I_{15} + I_{16}$	–	18	23	mA
CVBS and sync inputs (pins 1 and 2)						
$V_{i\ CVBS}$	CVBS input signal (peak-to-peak value)	sync-to-white note 1; Fig.4	0.5	1	1.4	V
$V_{i\ data}$	data input signal (peak-to-peak value, pin 1)	line 16; Fig.4	250	500	700	mV
$V_{i\ sync}$	sync input signal (peak-to-peak value, pin 2)		100	–	600	mV
R_S	source resistance		–	–	1	kΩ
Composite sync output (pin 6)						
V_{OL}	output voltage LOW		–	–	0.4	V
V_{OH}	output voltage HIGH		2.4	–	–	V
I_{OL}	output current LOW		–	–	200	µA
I_{OH}	output current HIGH		–	–	–500	µA
t_d	sync separator delay time		–	0.3	–	µs
$\overline{\textbf{DAV}}$ **output** (pin 12)		note 2				
V_{OL}	output voltage LOW		–	–	0.4	V
V_{OH}	output voltage HIGH		2.4	–	–	V
I_{OL}	output current LOW		–	–	500	µA
I_{OH}	output current HIGH		–	0.01	1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCL and SDA (pins 8 and 9)						
V_{IL}	input voltage LOW		–	–	1.5	V
V_{IH}	input voltage HIGH		3	–	–	V
I_I	input current	$0.9V_P$	–	–	±10	µA
C_I	input capacitance		–	–	10	pF
$V_{O\ ACK}$	output voltage during acknowledge on pin 9	I_{OL} = 3 mA	–	–	0.4	V
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
$t_{p\ L}$	pulse duration LOW		4.7	–	–	µs
$t_{p\ H}$	pulse duration HIGH		4.0	–	–	µs
SCL	clock frequency		–	–	100	kHz
AD set input (pin 7)		note 2				
V_{IL}	input voltage LOW	address 23H	0	–	0.4	V
V_{IH}	input voltage HIGH	address 21H	2.4	–	V_P	V
RESET input (pin 10)		note 2				
V_{IL}	input voltage LOW	reset active	–	–	0.4	V
V_{IH}	input voltage HIGH	reset non-active	2.4	–	–	V
I_{IL}	input current LOW		–	–	–10	µA
I_{IH}	input current HIGH		–	0.01	1	µA

Notes to the characteristics

1. With standard sync and data amplitude of 68% to 75% black-white.
2. If the open collector output $\overline{DAV}$ is used, a pull-up resistor to V_{P1} is necessary.

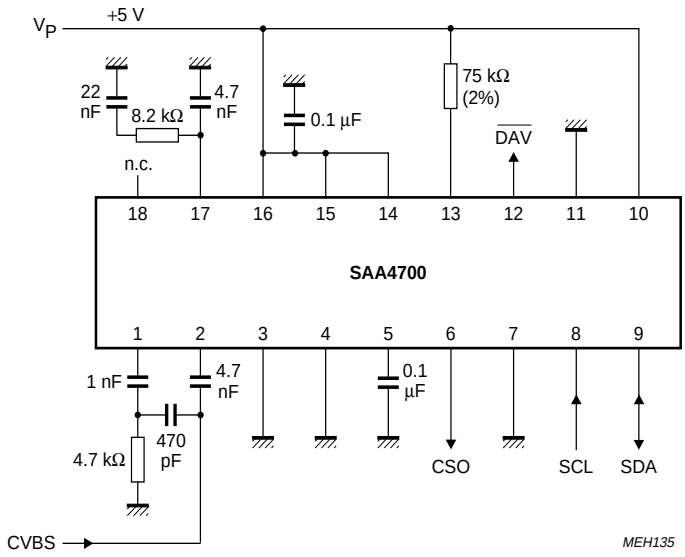


Fig.6 Application circuit.

I²C-BUS FORMAT

S	SLAVE ADDRESS	A	DATA	A	DATA	A	DATA	A	DATA	A	DATA	P

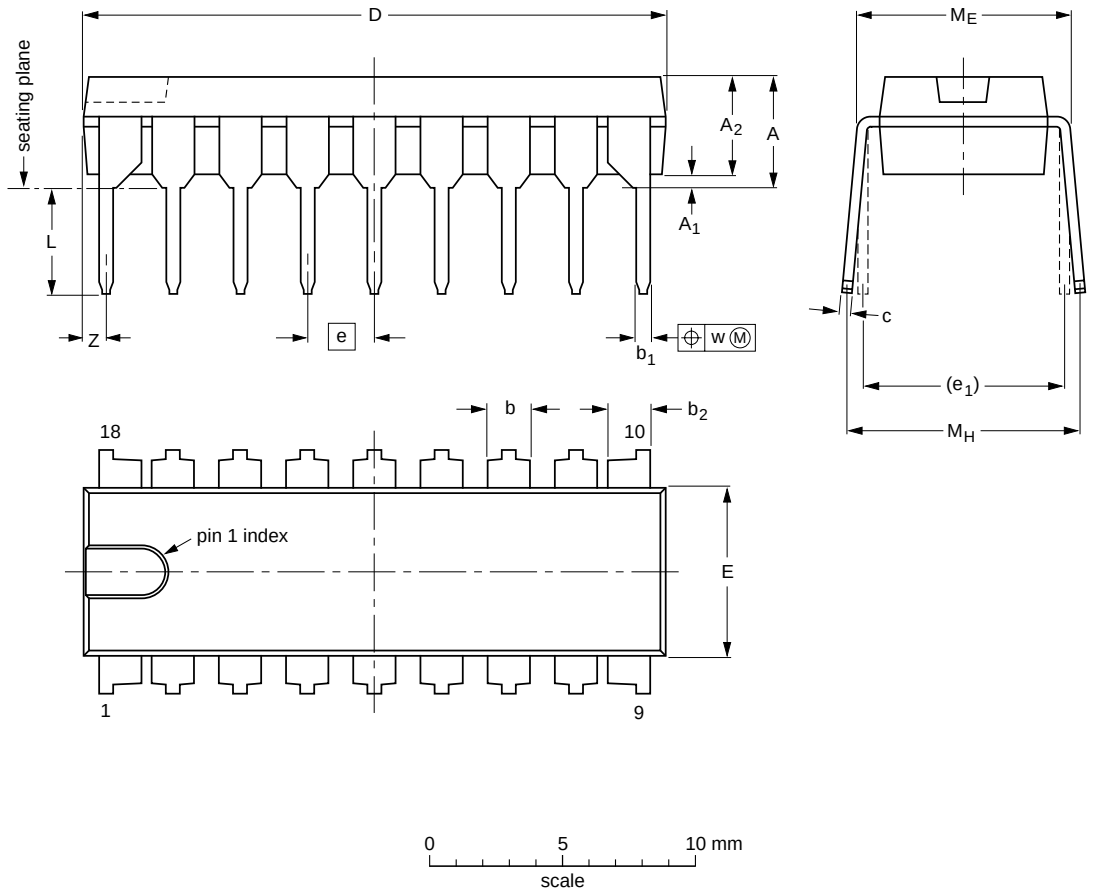
S	=	start condition
SLAVE ADDRESS	=	0010 0001 or 0010 0011 for set input AD = HIGH respectively LOW on pin 7 (the circuit is only a slave transmitter)
A	=	acknowledge, generated by the slave or the master
DATA	=	five data bytes, see words in Table 1
P	=	stop condition respectively non-acknowledge by the microcontroller

Remarks to I²C-bus transmission

- the MSB of each word is transmitted first
- there is no restriction on the number of words to be transmitted, but if more than five words are requested, the following content will be “FF” continuously.
- Normally every dataline transmission has to be ended with STOP condition by non-acknowledge of the controller.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.