# DATA SHEET

# SAA5231
## Teletext video processor

Product specification
File under Integrated Circuits, IC02

November 1986



Philips Semiconductors

PHILIPS

# Teletext video processor SAA5231

## GENERAL DESCRIPTION

The SAA5231 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

### Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 16) | $V_{CC}$ | typ. | 12 | V |
| Supply current (pin 16) | $I_{CC}$ | typ. | 70 | mA |
| Video input amplitude (pin 27) (peak-to-peak value) | | | | |
| pin 2 LOW | $V_{27\text{-}13(p\text{-}p)}$ | typ. | 1 | V |
| pin 2 HIGH | $V_{27\text{-}13(p\text{-}p)}$ | typ. | 2,5 | V |
| Storage temperature range | $T_{stg}$ | | -20 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 | °C |

## PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117); SOT117-1; 1996 November 14

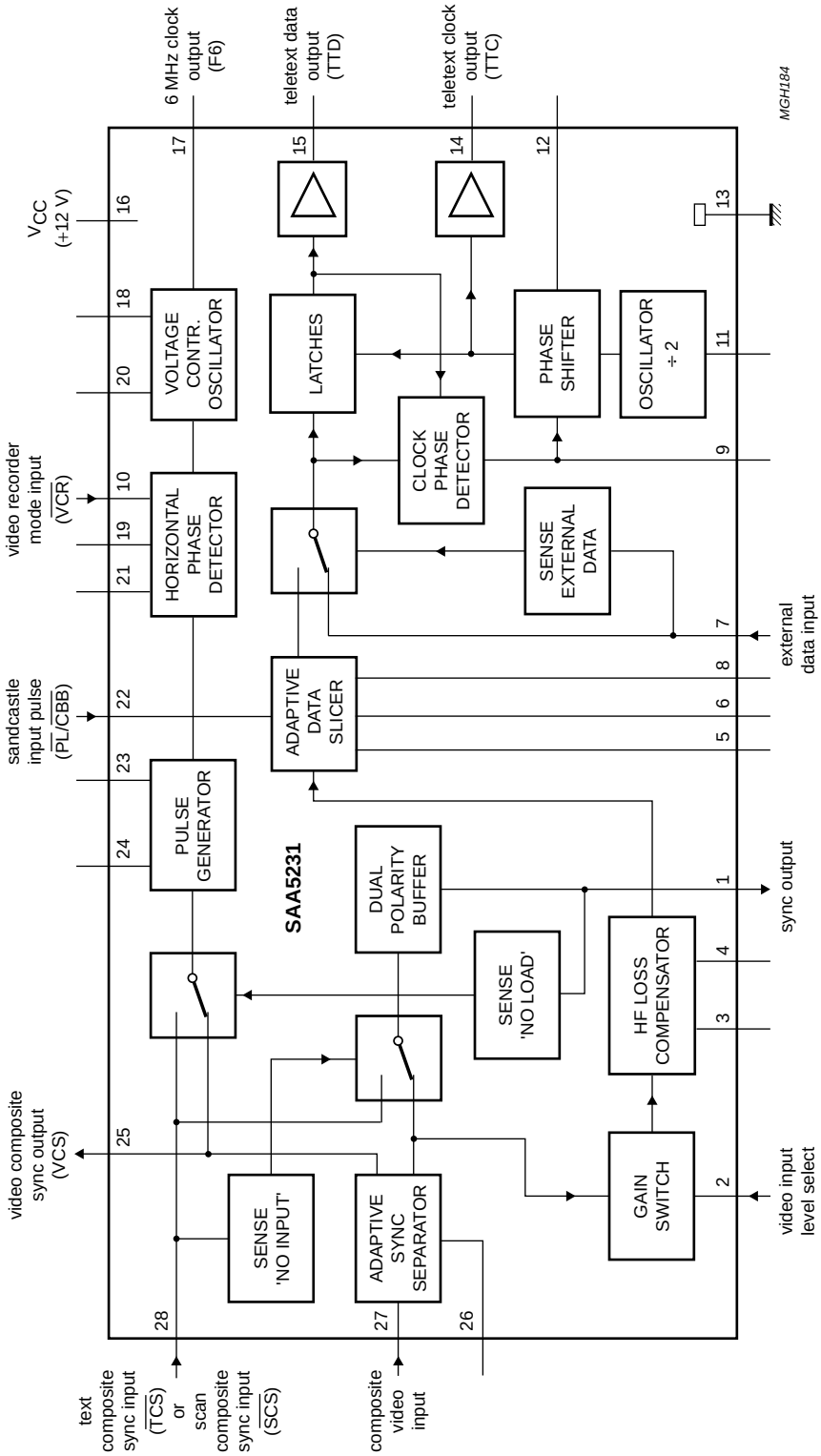



Fig.1 Block diagram.

## PINNING

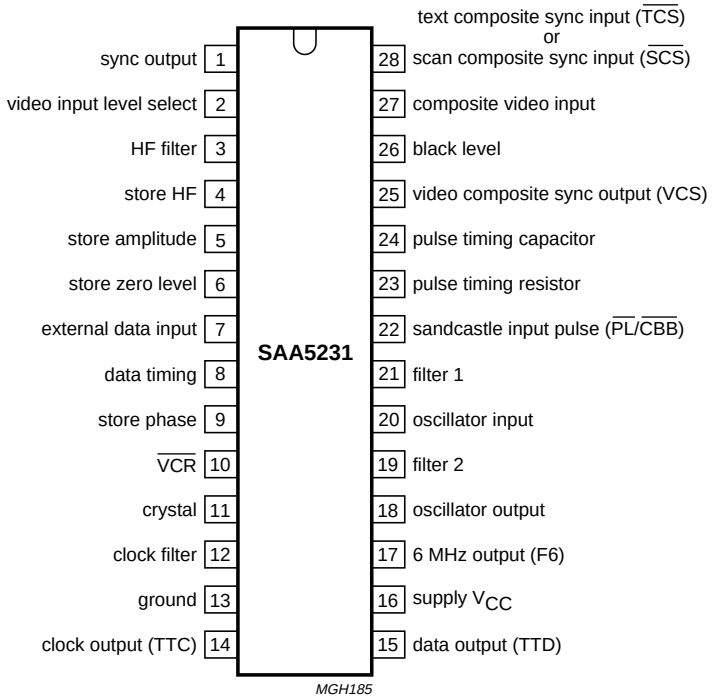



Fig.2 Pinning diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 16) | $V_{CC}$ | max. 13,2 | V |
| Storage temperature range | $T_{stg}$ | − 20 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | 0 to + 70 | °C |

## CHARACTERISTICS

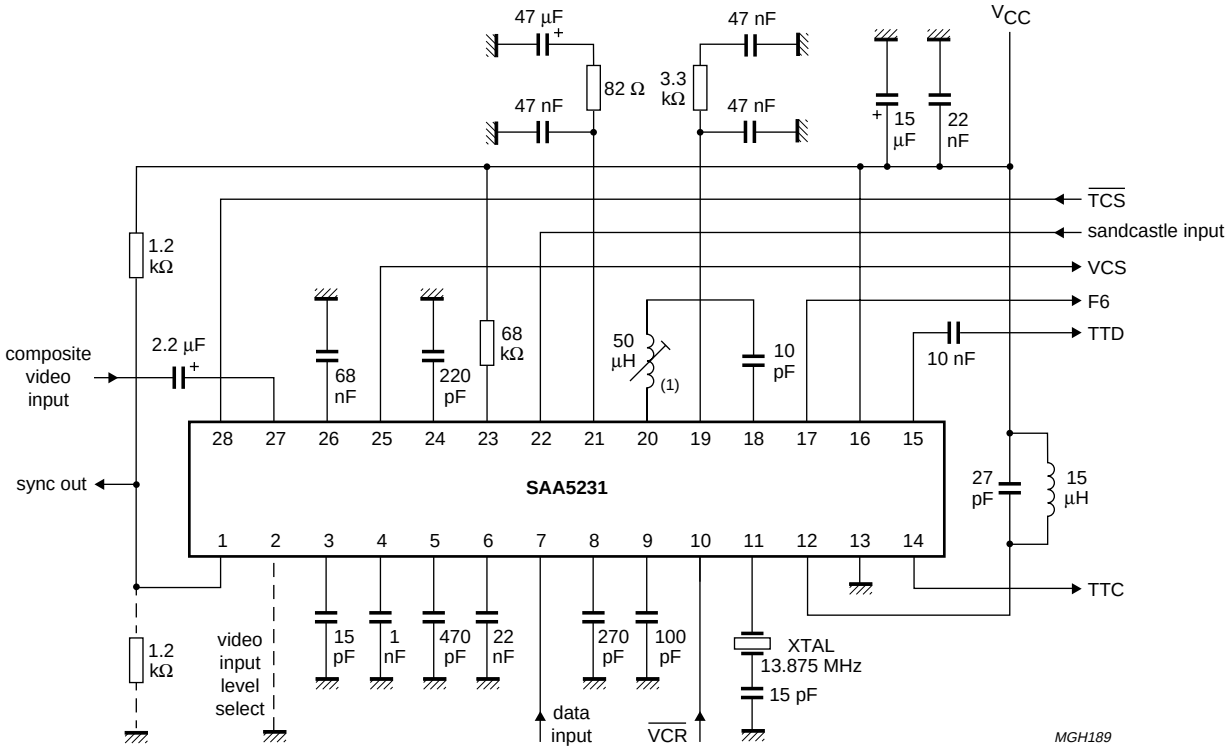
$V_{CC}$ = 12 V; $T_{amb}$ = 25 °C with external components as shown in application circuits unless otherwise stated.

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Supply** (pin 16) | | | | | |
| Supply voltage | $V_{CC}$ | 10,8 | 12,0 | 13,2 | V |
| Supply current | $I_{CC}$ | 50 | 70 | 105 | mA |
| **Video input and sync separator** | | | | | |
| Video input amplitude (sync to white) (peak-to-peak value) | | | | | |
| video input select level LOW (pin 2) | $V_{27\text{-}13(p\text{-}p)}$ | 0,7 | 1 | 1,4 | V |
| video input select level HIGH (pin 2) | $V_{27\text{-}13(p\text{-}p)}$ | 1,75 | 2,5 | 3,5 | V |
| Source impedance | $\lvert Z_s \rvert$ | – | – | 250 | Ω |
| Sync amplitude (peak-to-peak value) | $V_{27\text{-}13(p\text{-}p)}$ | 0,1 | – | 1 | V |
| **Video input level select** | | | | | |
| Input voltage LOW | $V_{2\text{-}13}$ | 0 | – | 0,8 | V |
| Input voltage HIGH | $V_{2\text{-}13}$ | 2,0 | – | 5,5 | V |
| Input current LOW | $I_2$ | 0 | – | –150 | µA |
| Input current HIGH | $I_2$ | 0 | – | 1 | mA |
| **Text composite sync input ($\overline{\text{TCS}}$)** | | | | | |
| Input voltage LOW | $V_{28\text{-}13}$ | 0 | – | 0,8 | V |
| Input voltage HIGH | $V_{28\text{-}13}$ | 2,0 | – | 7,0 | V |
| **Scan composite sync input ($\overline{\text{SCS}}$)** | | | | | |
| Input voltage LOW | $V_{28\text{-}13}$ | 0 | – | 1,5 | V |
| Input voltage HIGH | $V_{28\text{-}13}$ | 3,5 | – | 7,0 | V |
| **Select video sync from pin 1** | | | | | |
| Input current (pin 28) | | | | | |
| at $V_{28}$ = 0 to 7 V | $I_{28}$ | –40 | –70 | –100 | µA |
| at $V_{28}$ = 10 V to $V_{CC}$ | $I_{28}$ | –5 | – | + 5 | µA |
| **Video composite sync output (VCS)** | | | | | |
| Output voltage LOW | $V_{25\text{-}13}$ | 0 | – | 0,4 | V |
| Output voltage HIGH | $V_{25\text{-}13}$ | 2,4 | – | 5,5 | V |
| D.C. output current LOW | $I_{25}$ | – | – | 0,5 | mA |
| D.C. output current HIGH | $I_{25}$ | – | – | –1,5 | mA |
| Sync separator delay time | $t_d$ | 0,25 | 0,35 | 0,40 | µs |

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Dual polarity buffer output** | | | | | |
| $\overline{TCS}$ amplitude (peak-to-peak value) | $V_{1\text{-}13(p\text{-}p)}$ | 0,20 | 0,45 | 0,65 | V |
| Video sync amplitude (peak-to-peak value) | $V_{1\text{-}13(p\text{-}p)}$ | – | – | 1 | V |
| Output current | $I_1$ | – 3 | – | + 3 | mA |
| D.C. output voltage | | | | | |
| $R_L$ to ground (0 V) | $V_{1\text{-}13}$ | 1,0 | 1,4 | 2,0 | V |
| $R_L$ to $V_{CC}$ (12 V) | $V_{1\text{-}13}$ | 9,0 | 10,1 | 11,0 | V |
| **Sandcastle input pulse ($\overline{PL}$/$\overline{CBB}$)** | | | | | |
| Phase lock pulse (PL) | | | | | |
| PL on (LOW) | $V_{22\text{-}13}$ | 0 | – | 3 | V |
| PL off (HIGH) | $V_{22\text{-}13}$ | 3,9 | – | 5,5 | V |
| Blanking pulse (CBB) | | | | | |
| CBB on (LOW) | $V_{22\text{-}13}$ | 0 | – | 0,5 | V |
| CBB off (HIGH) | $V_{22\text{-}13}$ | 1,0 | – | 5,5 | V |
| Input current | $I_{22}$ | –10 | – | + 10 | µA |
| **Phase locked loop (PLL)** | | | | | |
| Phase detector timing | | | | | |
| Pulse duration using composite video | $t_p$ | 2,0 | 2,4 | 2,8 | µs |
| using scan composite sync | $t_p$ | 3,0 | 3,5 | 4,0 | µs |
| time PL must be LOW | | | | | |
| to make VCO run-free | $t_L$ | 100 | – | – | µs |
| **6 MHz clock output (F6)** | | | | | |
| A.C. output voltage (peak-to-peak value) | $V_{17\text{-}13(p\text{-}p)}$ | 1 | 2 | 3 | V |
| A.C. and d.c. output voltage range | $V_{17\text{-}13(max)}$ | 4 | – | 8,5 | V |
| Rise and fall time | $t_r$; $t_f$ | 20 | – | 40 | ns |
| Load capacitance | $C_{17\text{-}13}$ | – | – | 40 | pF |
| **Video recorder mode input ($\overline{VCR}$)** | | | | | |
| VCR-mode on (LOW) | $V_{10\text{-}13}$ | 0 | – | 0,8 | V |
| VCR-mode off (HIGH) | $V_{10\text{-}13}$ | 2,0 | – | $V_{CC}$ | V |
| Input current | $I_{10}$ | –10 | – | +10 | µA |
| **Data slicer** | | | | | |
| Data amplitude of video input (pin 27) | | | | | |
| video input level select LOW (pin 2) | $V_{27\text{-}13}$ | 0,30 | 0,46 | 0,70 | V |
| video input level select HIGH (pin 2) | $V_{27\text{-}13}$ | 0,75 | 1,15 | 1,75 | V |

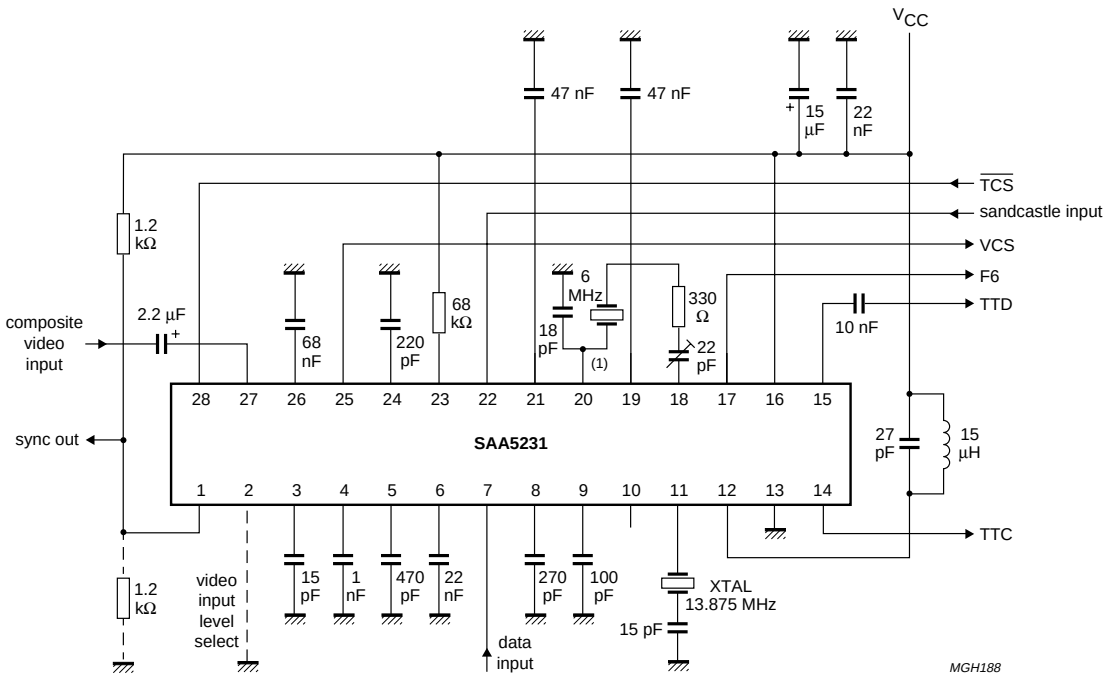
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **Teletext clock output** | | | | | |
| A.C. output voltage (peak-to-peak value) | $V_{14\text{-}13(p\text{-}p)}$ | 2,5 | 3,5 | 4,5 | V |
| D.C. output voltage (centre) | $V_{14\text{-}13}$ | 3,0 | 4,0 | 5,0 | V |
| Load capacitance | $C_L$ | – | – | 40 | pF |
| Rise and fall times | $t_r$; $t_f$ | 20 | 30 | 45 | ns |
| Delay of falling edge relative to other edges of TTD | $t_d$ | –20 | 0 | +20 | ns |
| **Teletext data output** | | | | | |
| A.C. output voltage (peak-to-peak value) | $V_{15\text{-}13(p\text{-}p)}$ | 2,5 | 3,5 | 4,5 | V |
| D.C. output voltage (centre) | $V_{15\text{-}13}$ | 3,0 | 4,0 | 5,0 | V |
| Load capacitance | $C_L$ | – | – | 40 | pF |
| Rise and fall times | $t_r$; $t_f$ | 20 | 30 | 45 | ns |

**APPLICATION INFORMATION**



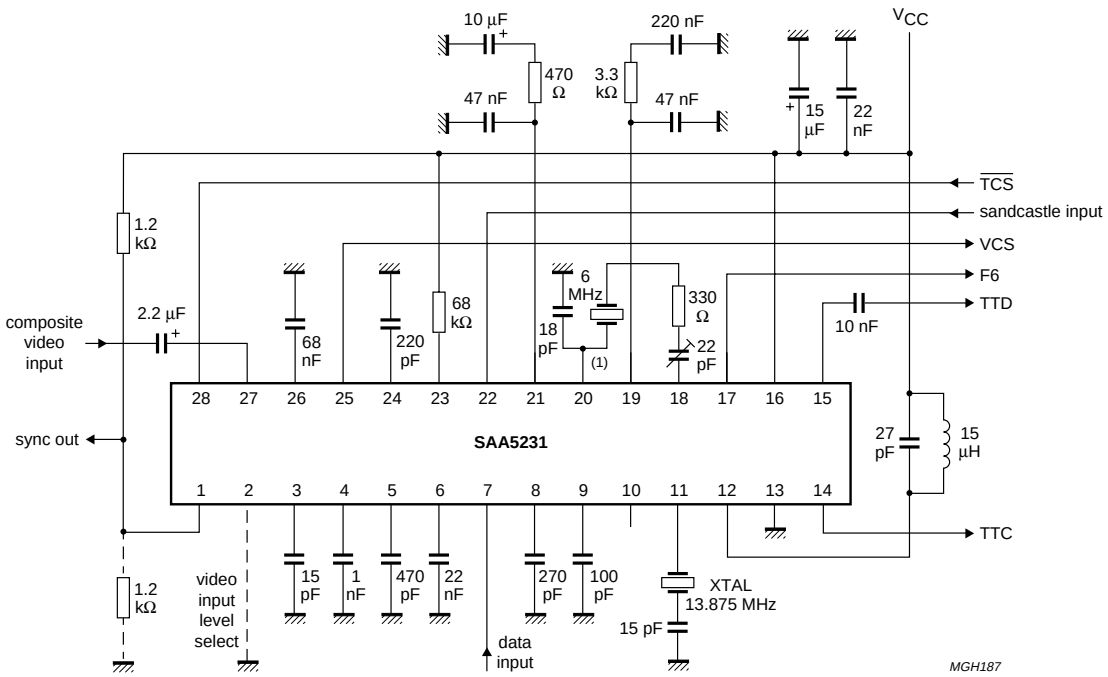

(1) Coil: 50 µH at 1 kHz, $C_o = 4$ pF. Adjust the free-running frequency to 6000 kHz ± 30 kHz.

Fig.3 Application circuit using L/C circuit in PLL.




(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

a. using quartz crystal in PLL




(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

b. using ceramic resonator in PLL.

Fig.4 Application circuit

**Component specifications**

Specifications of some external components in Figs 3, 4a and 4b.

**Quartz crystal** 13,875 MHz; Figs 3, 4a and 4b.

Load resonance frequency (f) 13,875 MHz; adjustment tolerance $\pm 40 \times 10^{-6}$

Load capacitance ($C_L$) 20 pF

Temperature range (T) –20 to +70 °C; frequency tolerance maximum $\pm 30 \times 10^{-6}$

Resonance resistance ($R_r$) typical 10 Ω maximum 60 Ω

Motional capacitance ($C_1$) typical 19 fF

Static parallel capacitance ($C_o$) typical 5 pF

**Fixed inductance** Figs 3, 4a and 4b.

Inductance (L) 15 μH ± 20%

Quality factor (Q) minimum 20

**Variable inductance** Fig. 3

Inductance (L) 50 μH at 1 kHz

Static parallel capacitance ($C_o$) typical 4 pF

**Quartz crystal** Fig. 4a

Preferred type 4322 143 04101

Load resonance frequency (f) 6 MHz; adjustment tolerance $\pm 40 \times 10^{-6}$

Load capacitance ($C_L$) 20 pF

Temperature range (T) –20 to +70 °C; frequency tolerance $\pm 30 \times 10^{-6}$

Resonance resistance ($R_r$) 60 Ω

Motional capacitance ($C_1$) typical 28 fF

Static parallel capacitance ($C_o$) typical 7 pF

**Ceramic resonator;** Fig. 4b

Preferred type KBR 6,0 M, Kyocera

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%

Load capacitance ($C_L$) 20 pF

Temperature range (T) –20 to +70 °C; frequency tolerance maximum ± 0,3%

Resonance resistance ($R_r$) typical 6 Ω

Motional capacitance ($C_1$) typical 9 pF

Static parallel capacitance ($C_o$) typical 60 pF

Ageing (10 years) f maximum ± 0,3%

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.

   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig.4a or Fig.4b.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

15. **Teletext data output (TTD)**

    Data output for CCT.

16. **Supply voltage $V_{CC}$ (+ 12 V typ.)**

17. **Clock output (F6)**

    6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

    A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

    A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

    See pin 18.

21. **Filter 1**

    A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}$/$\overline{CBB}$)**

    This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig.5.

23. **Pulse timing resistor**

    The current for the pulse generator is defined by a 68 Ω resistor connected to this pin.

24. **Pulse timing capacitor**

    The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

    The output signal is for CCT.

26. **Black level**

    The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

    The composite video signal is input via a 2,2 µF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{TCS}$)/Scan composite sync input ($\overline{SCS}$)**

    $\overline{TCS}$ is input from CCT or $\overline{SCS}$ from external sync circuit. $\overline{SCS}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

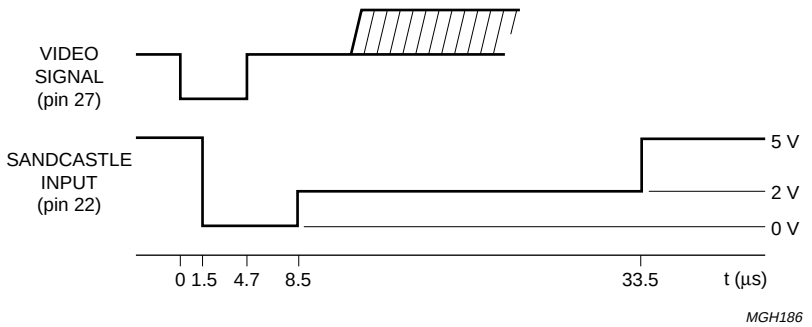
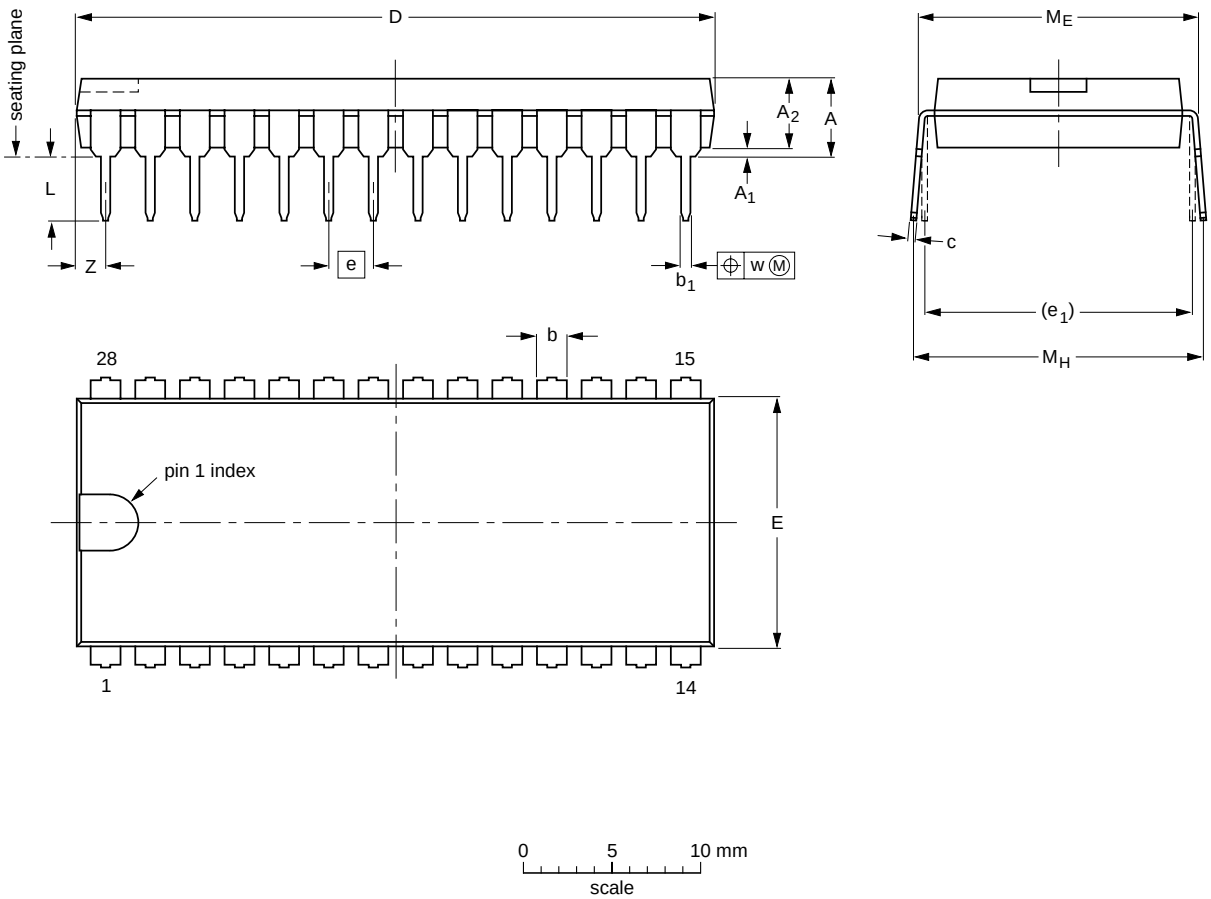



Fig.5 Sandcastle waveform and timing.

## PACKAGE OUTLINE

**DIP28: plastic dual in-line package; 28 leads (600 mil)** **SOT117-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.1 | 0.51 | 4.0 | 1.7<br>1.3 | 0.53<br>0.38 | 0.32<br>0.23 | 36.0<br>35.0 | 14.1<br>13.7 | 2.54 | 15.24 | 3.9<br>3.4 | 15.80<br>15.24 | 17.15<br>15.90 | 0.25 | 1.7 |
| inches | 0.20 | 0.020 | 0.16 | 0.066<br>0.051 | 0.020<br>0.014 | 0.013<br>0.009 | 1.41<br>1.34 | 0.56<br>0.54 | 0.10 | 0.60 | 0.15<br>0.13 | 0.62<br>0.60 | 0.68<br>0.63 | 0.01 | 0.067 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT117-1 | 051G05 | MO-015AH | | | | ~~92-11-17~~<br>95-01-14 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

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