DATA SHEET

SAA7120; SAA7121
Digital Video Encoder (ConDENC)

Preliminary specification
File under Integrated Circuits, IC22

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Philips Semiconductors

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Digital Video Encoder (ConDENC) SAA7120; SAA7121

FEATURES

- Monolithic CMOS 3.3 V (5 V) device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port; input data format Cb-Y-Cr (CCIR 656), SAV and EAV
- Three DACs for Y, C and CVBS, two times oversampled with 10 bit resolution
- Real time control of subcarrier
- Cross colour reduction filter
- Closed captioning encoding and WST- and NABTS-Teletext encoding including sequencer and filter
- Line 23 wide screen signalling encoding
- Fast I²C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal colour bar generator (CBG)
- 2 × 2 bytes in lines 20 (NTSC) for copy guard management system can be loaded via I²C-bus
- Down-mode of DACs
- Controlled rise/fall times of synchronization and blanking output signals
- Macrovision Pay-per-View copy protection system rev.7 and rev.6.1 as option.

  This applies to SAA7120 only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- QFP44 package.

GENERAL DESCRIPTION

The SAA7120; SAA7121 encodes digital YUV video data to an NTSC or PAL CVBS or S-Video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip DACs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
I_{DDA}	analog supply current	–	–	62	mA
I_{DDD}	digital supply current	–	–	38	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C, and CVBS without load (peak-to-peak value)	1.2	1.35	1.45	V
R_L	load resistance	75	–	300	Ω
ILE	LF integral linearity error	–	–	±3	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7120; SAA7121	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 10 × 10 × 1.75 mm	SOT307-2

BLOCK DIAGRAM

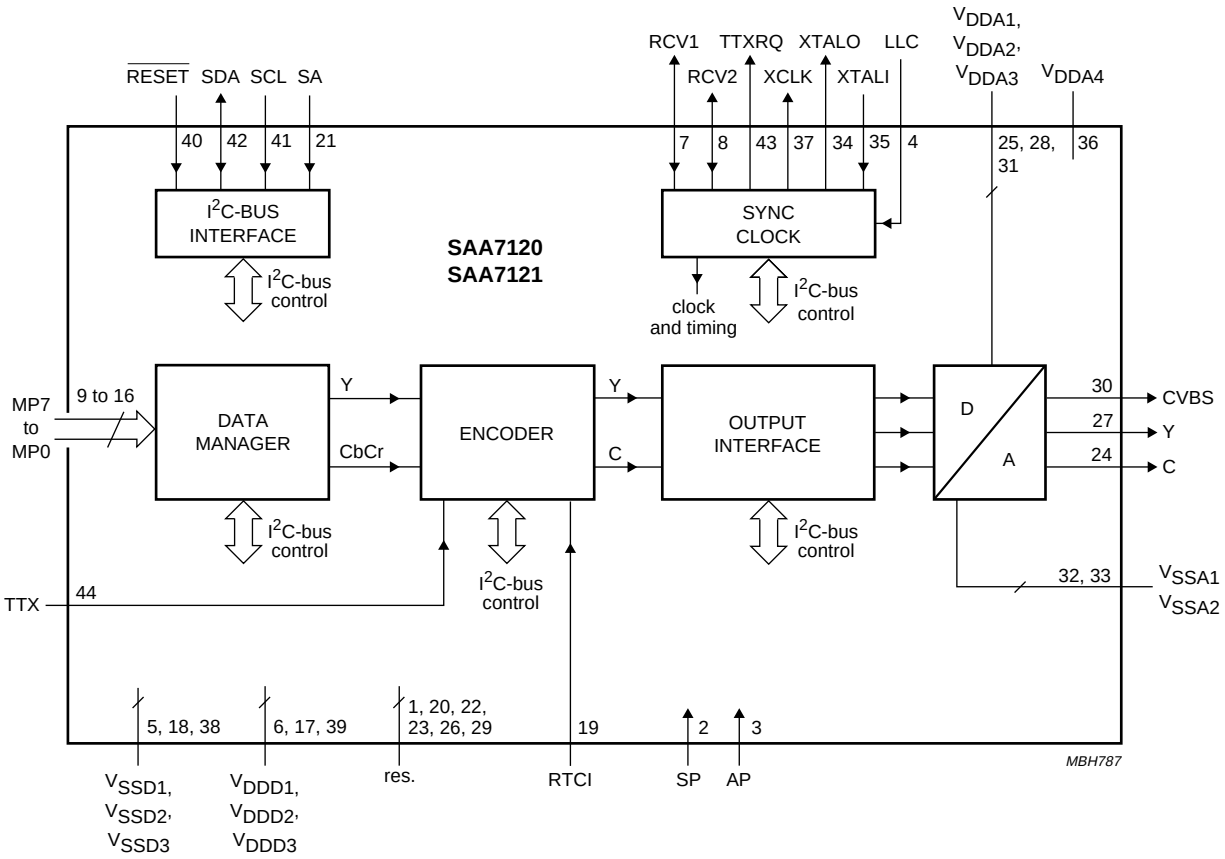


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
res.	1	–	reserved
SP	2	I	test pin; connected to digital ground for normal operation
AP	3	I	test pin; connected to digital ground for normal operation
LLC	4	I	line-locked clock; this is the 27 MHz master clock for the encoder
V_{SSD1}	5	I	digital ground 1
V_{DDD1}	6	I	digital supply voltage 1
RCV1	7	I/O	raster control 1 for video port; this pin receives/provides a VS/FS/FSEQ signal
RCV2	8	I/O	raster control 2 for video port; this pin provides an HS pulse of programmable length or receives an HS pulse
MP7	9	I	MPEG port; it is an input for *"CCIR 656"* style multiplexed Cb Y, Cr data
MP6	10	I	
MP5	11	I	
MP4	12	I	
MP3	13	I	
MP2	14	I	
MP1	15	I	
MP0	16	I	
V_{DDD2}	17	I	digital supply voltage 2
V_{SSD2}	18	I	digital ground 2
RTCI	19	I	Real Time Control input; if the LLC clock is provided by an SAA7111 or SAA7151B, RTCI should be connected to pin RTCO of the decoder to improve the signal quality
res.	20	–	reserved
SA	21	I	the I^2C-bus slave address select input pin; LOW: slave address = 88H, HIGH = 8CH
res.	22	–	reserved
res.	23	–	reserved
C	24	O	analog output of the chrominance signal
V_{DDA1}	25	I	analog supply voltage 1 for the C DAC
res.	26	–	reserved
Y	27	O	analog output of VBS signal
V_{DDA2}	28	I	analog supply voltage 2 for the Y DAC
res.	29	–	reserved
CVBS	30	O	analog output of the CVBS signal
V_{DDA3}	31	I	analog supply voltage 3 for the CVBS DAC
V_{SSA1}	32	I	analog ground 1 for the DACs
V_{SSA2}	33	I	analog ground 2 for the oscillator and reference voltage
XTALO	34	O	crystal oscillator output (to crystal)
XTALI	35	I	crystal oscillator input (from crystal); if the oscillator is not used, this pin should be connected to ground
V_{DDA4}	36	I	analog supply voltage 4 for the oscillator and reference voltage
XCLK	37	O	clock output of the crystal oscillator

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD3}	38	I	digital ground 3
V_{DDD3}	39	I	digital supply voltage 3
$\overline{RESET}$	40	I	reset input, active LOW; after reset is applied, all digital I/Os are in input mode; the I^2C-bus receiver waits for the START condition
SCL	41	I	I^2C-bus serial clock input
SDA	42	I/O	I^2C-bus serial data input/output
TTXRQ	43	O	teletext request output, indicating when bit stream is valid
TTX	44	I	teletext bit stream input

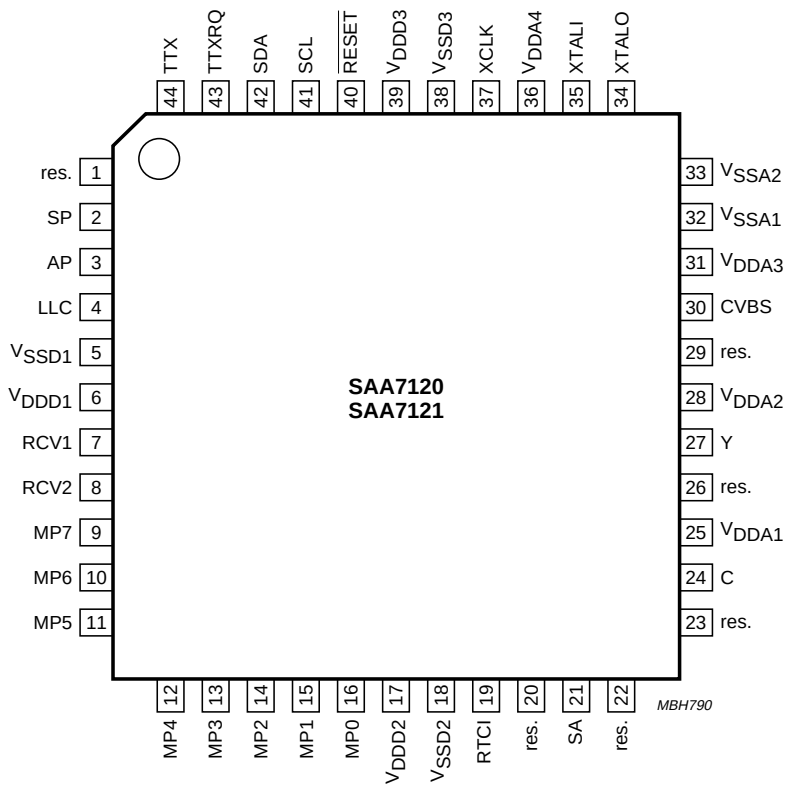


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital video encoder (ConDENC) encodes digital luminance and colour difference signals simultaneously into analog CVBS and S-Video signals. NTSC-M, PAL B/G, and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

The basic encoder function consists of subcarrier generation, colour modulation and the insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"CCIR 624"*.

For ease of analog post-filtering the signals are oversampled twice with respect to the pixel clock prior to digital-to-analog conversion.

The filter characteristics are shown in Figs 3 and 4. The DACs for Y, C, and CVBS have 10-bit resolution.

The 8-bit multiplexed Cb-Y-Cr formats are *"CCIR 656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally when the device is to operate in slave mode.

It is also possible to connect a Philips Digital Video Decoder (SAA7111 or SAA7151B) to the ConDENC. Via pin RTCI, connected to RTCO of a decoder, information concerning the actual subcarrier, PAL-ID and (if used in conjunction with the SAA7111) the subcarrier phase can be inserted.

The ConDENC synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals.

Wide screen signalling data can be loaded via the I^2C-bus. It is inserted into line 23 for 50 Hz field rate standards.

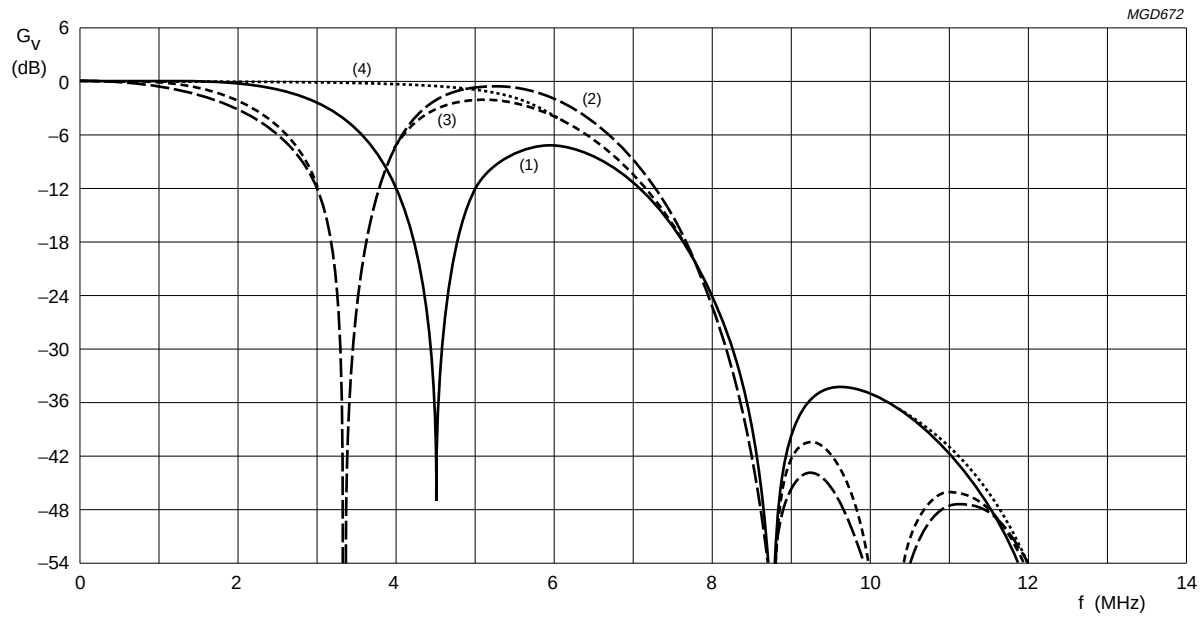
The IC contains closed caption and extended data services encoding (line 21), and supports anti-taping signal generation in accordance with Macrovision.

Possibilities are provided for setting video parameters:

Black and blanking level control

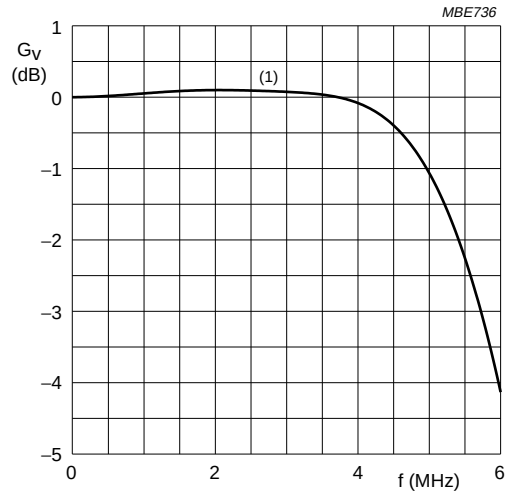
Colour subcarrier frequency

Variable burst amplitude.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 0; CCRS0 = 0.
(4) CCRS1 = 1; CCRS0 = 1.

Fig.3 Luminance transfer characteristic 1.



(1) CCRS1 = 0; CCRS0 = 0.

Fig.4 Luminance transfer characteristic 2.

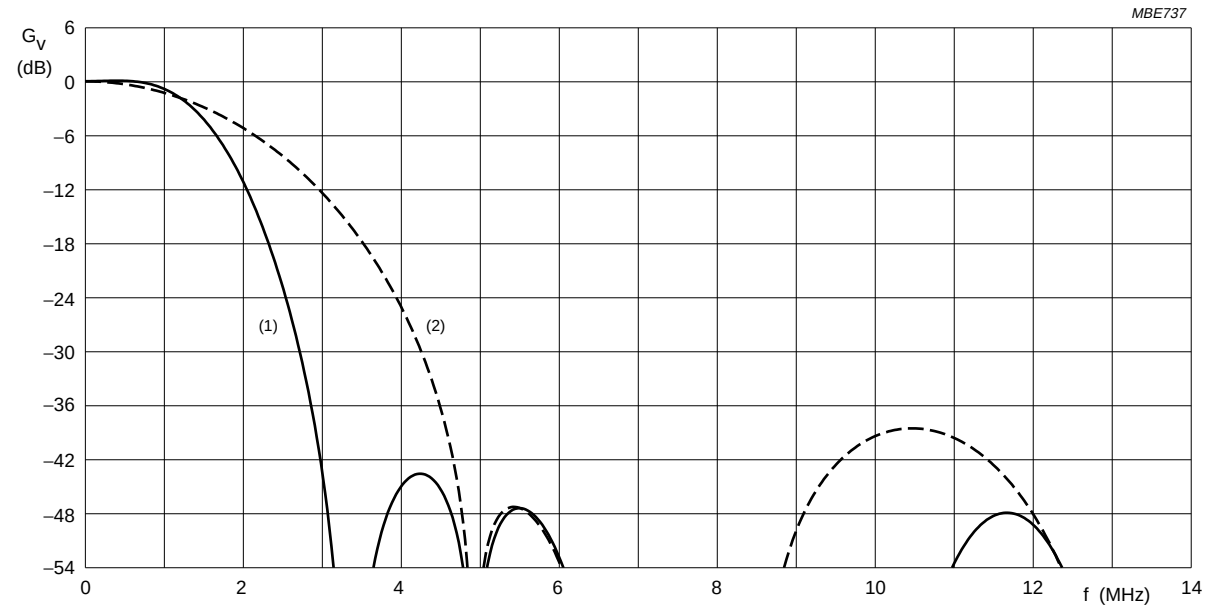
During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the I²C-bus interface to abort a running bus transfer and sets register 3A to 03H, register 61 to 06H, registers 6BH and 6EH to 00H and bit TTX60 to 0. All other control registers are not influenced by a reset.

Encoder

VIDEO PATH

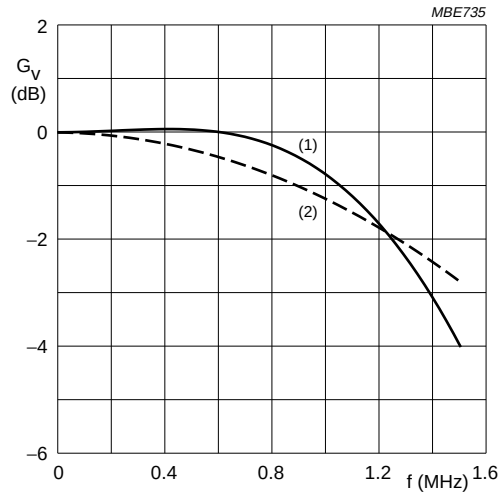
The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (the latter programmable in a certain range to enable different black level set-ups). A fixed synchronization level in accordance with standard composite synchronization schemes is inserted. The inserted blanking level is programmable to allow for manipulations with Macrovision anti-taping. Additional insertion of AGC super-white pulses, programmable in height, is supported.



(1) SCBW = 1.
(2) SCBW = 0.

Fig.5 Chrominance transfer characteristic 1.



(1) SCBW = 1.
(2) SCBW = 0.

Fig.6 Chrominance transfer characteristic 2.

In order to enable easy analog post-filtering, luminance is interpolated from 13.5 MHz data rate to 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. For transfer characteristic of the luminance interpolation filter see Figs 3 and 4.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from 6.75 MHz data rate to 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y and C output. For transfer characteristics of the chrominance interpolation filter see Figs 5 and 6.

The amplitude, beginning and ending of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

TELETEXT INSERTION AND ENCODING

Pin TTX receives a WST- or NABTS-Teletext bitstream sampled at the LLC clock. At each rising edge of output signal TTXRQ a single teletext bit has to be provided after a programmable delay at input pin.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines selectable independently for both fields. The internal insertion window for text is set to 360 (PAL-WST), 296 (NTSC-WST) or 288 (NABTS) teletext bits including clock run-in bits. For protocol and timing see Fig.7.

CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (Line 21).
Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

ANTI-TAPING (SAA7120 ONLY)

For more information contact your nearest Philips Semiconductors sales office.

Data manager

In the data manager, real time arbitration on the data stream to be encoded is performed.

A pre-defined colour look-up table located in this block can be read out in a pre-defined sequence (8 steps per active video line), achieving a colour bar test pattern generator without the need for an external data source. The colour bar function is under software control only.

Output interface/DACs

In the output interface encoded Y and C signals are converted from digital to analog in 10-bit resolution.

Y and C signals are also combined to a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of the DACs can be set together in two groups via software control to minimum output voltage for either purpose.

Synchronization

Synchronization of the ConDENC is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to RCV1 can be influenced by programming the polarity and the on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not to be influenced by RCV1, a horizontal synchronization pulse needs to be supplied at the pin RCV2. Timing and trigger behaviour can also be influenced by RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of ConDENC runs free, thus an arbitrary number of synchronization slopes may be absent, but no additional pulses (with the incorrect phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

Alternatively, the device can be triggered by auxiliary codes in a *"CCIR 656"* data stream at the MP port.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the device can output:

- A Vertical Synchronisation signal (VS) with 3 or 2.5 lines duration, or
- An ODD/EVEN signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 or 8 fields respectively.

On the RCV2 port, the device can provide a horizontal synchronization pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The polarity of both RCV1 and RCV2 is selectable by software control.

The length of a field and the start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

Teletext timing

The teletext timing is shown in Fig.7. t_{FD} is the time needed to interpolate input data TTX and inserting it into the CVBS and Y output signal, such that it appears at t_{TTX} = 10.2 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH-state at output pin TTXRQ, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of outgoing horizontal synchronization pulse.

Time t_{TTXWin} is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbits/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbits/s (World Standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbits/s (NABTS). The insertion window is not opened if the control bit TTXEN is logic 0.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

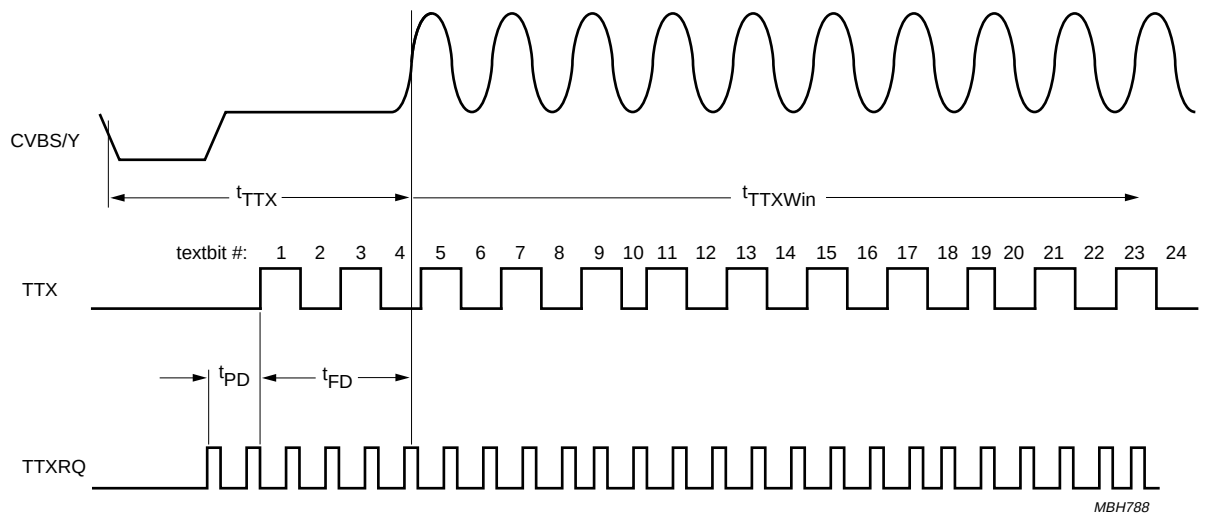


Fig.7 Teletext timing.

Analog output voltages

The analog output voltages are dependent on the open-loop voltage of the operational amplifiers for full-scale conversion (typical value 1.35 V), the internal series resistor (typical value 2 Ω), the external series resistor and the external load impedance.

The digital output signals in front of the DACs under nominal conditions occupy different conversion ranges, as indicated in Table 1 for a $^{100}/_{100}$ colour bar signal.

Values for the external series resistors result in a 75 Ω load.

Input levels and formats

The ConDENC expects digital Y, Cb, Cr data with levels (digital codes) in accordance with *"CCIR 601"* (see Tables 2 and 3).

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 Digital output signals conversion range

CONVERSION RANGE (peak-to-peak) (digits)	
CVBS, SYNC TIP-TO-PEAK CARRIER	**Y (VBS) SYNC TIP-TO-WHITE**
1016	881

Table 2 *"CCIR 601"* signal component levels

COLOUR	SIGNALS		
	Y	**Cb**	**Cr**
White	235	128	128
Yellow	210	16	146
Cyan	170	166	16
Green	145	54	34
Magenta	106	202	222
Red	81	90	240
Blue	41	240	110
Black	16	128	128

I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I²C-bus slave addresses are present:

88H: LOW at pin SA

8CH: HIGH at pin SA.

Tables 5 and 4 summarize the format of the I²C-bus addressing. For more information on how to use the I²C-bus see *"The I²C-bus and how to use it"*, order no. 9398 393 40011. Tables 7 to 42 contain the programming information for the subaddresses. Table 6 summarises this information.

Table 3 8-bit multiplexed format (similar to *"CCIR 601"*)

	BITS							
	0	**1**	**2**	**2**	**4**	**5**	**6**	**7**
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 4 I²C-bus address format; see Table 5

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 5 Explanation of Table 4

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 x or 1 0 0 0 1 1 0 x (1)
ACK	acknowledge, generated by the slave
Subaddress(2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. x is the read/write control bit; write:
   x = logic 0;
   read: x = logic 1, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Table 6 Slave receiver (slave address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BITS[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.
Null	25	0	0	0	0	0	0	0	0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	0	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real time control, Burst start	28	DECCOL	DECFIS	BS5	BS4	BS3	BS2	BS1	BS0
Burst end	29	0	0	BE5	BE4	BE3	BE2	BE1	BE0
Copy guard odd 0	2A	CGO07	CGO06	CGO05	CGO04	CGO03	CGO02	CGO01	CGO00
Copy guard odd 1	2B	CGO17	CGO16	CGO15	CGO14	CGO13	CGO12	CGO11	CGO10
Copy guard even 0	2C	CGE07	CGE06	CGE05	CGE04	CGE03	CGE02	CGE01	CGE00
Copy guard even 1	2D	CGE17	CGE16	CGE15	CGE14	CGE13	CGE12	CGE11	CGE10
Copy guard enable	2E	CGEN1	CGEN0	0	0	0	0	0	0
Null	2F	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	0	0	SYMP	0	0	Y2C	UV2C
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, Real time control, Black level	5D	GAINU8	DECOE	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, Real time control, Blanking level	5E	GAINV8	DECPH	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, Blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	0	0	0	0	0	0	0	0
Standard control	61	0	DOWN	INPI	YGS	0	SCBW	PAL	FISE
RTC enable, Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

REGISTER FUNCTION	SUB ADDRESS	DATA BITS[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
RCV port control	6B	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	SBLBN	0	PHRES1	PHRES0	0	0	FLC1	FLCO
Closed caption, Teletext enable	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV2 output start	70	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
TTX request H start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request H delay	74	TTXHD7	TTXHD6	TTXHD5	TTXHD4	TTXHD3	TTXHD2	TTXHD1	TTXHD0
V-Sync shift	75	0	0	0	0	0	VS_S2	VS_S1	VS_S0
TTX odd request V S	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request V E	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request V S	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request V E	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSB vertical	7C	TTX60	LAL8	0	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	0	0	0	0	0	0	0	0
Disable TTX line	7E	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7F	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13

Note

1. All bits labelled ‘0’ are reserved. They **must** be programmed with logic 0.

Slave Receiver

Table 7 Subaddress 26 and 27

DATA BYTE	LOGIC LEVEL	DESCRIPTION	
WSS	–	wide screen signalling bits:	13 to 11 = reserved 10 to 8 = subtitles 7 to 4 = enhanced services 3 to 0 = aspect ratio
WSSON	0	wide screen signalling output is disabled	
	1	wide screen signalling output is enabled	

Table 8 Subaddress 28 and 29

DATA BYTE	LOGIC LEVEL	DESCRIPTION	REMARKS
BS	–	starting point of burst in clock cycles	PAL : BS = 33 (21H) NTSC : BS = 25 (19H)
BE	–	ending point of burst in clock cycles	PAL : BS = 29 (1DH) NTSC : BS = 29 (1DH)
DECCOL	0	disable colour detection bit of RTCI input	
	1	enable colour detection bit of RTCI input	bit RTCE must be set to 1 (see Fig.10)
DECFIS	0	field sequence as FISE in subaddress 61	
	1	field sequence as FISE bit in RTCI input	bit RTCE must be set to 1 (see Fig.10)

Table 9 Subaddress 2A to 2D

DATA BYTE	DESCRIPTION	REMARKS
CGO0	first byte of Copy guard data, odd field	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of Line 20 encoding format.
CGO1	second byte of Copy guard data, odd field	
CGE0	first byte of Copy guard data, even field	
CGE1	second byte of Copy guard data, even field	

Table 10 Subaddress 2E

DATA BYTE		DESCRIPTION
CCEN1	CCEN0	
0	0	copy guard encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 11 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
UV2C	0	Cb, Cr data are two's complement
	1	Cb, Cr data are straight binary; default after reset
Y2C	0	Y data is two's complement
	1	Y data is straight binary; default after reset
SYMP	0	horizontal and vertical trigger is taken from RCV2 and RCV1 respectively; default after reset
	1	horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP port
CBENB	0	data from input ports is encoded; default after reset
	1	colour bar with fixed colours is encoded

Table 12 Subaddress 5A

DATA BYTE	DESCRIPTION	VALUE	RESULT
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees	3FH	PAL-B/G and data from input ports
		69H	PAL-B/G and data from look-up table
		67H	NTSC-M and data from input ports
		89H	NTSC-M and data from look-up table

Remark: in subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

Table 13 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE	GAINU = –2.17 × nominal to +2.16 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE	GAINU = –2.05 × nominal to +2.04 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Table 14 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with *"CCIR 601"*	white-to-black = 92.5 IRE	GAINV = –1.55 × nominal to +1.55 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE	GAINV = –1.46 × nominal to +1.46 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Table 15 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with *"CCIR 601"*	white-to-sync = 140 IRE[1]	recommended value: BLCKL = 42 (2AH)
		BLCKL = 0	output black level = 34 IRE
		BLCKL = 63 (3FH)	output black level = 54 IRE
		white-to-sync = 143 IRE[2]	recommended value: BLCKL = 35 (23H)
		BLCKL = 0	output black level = 32 IRE
		BLCKL = 63 (3FH)	output black level = 52 IRE
DECOE	real time control	logic 0	disable odd/even field control bit from RTCI
		logic 1	enable odd/even field control bit from RTCI (see Fig.10)

Notes

1. Output black level/IRE = BLCKL × 2/6.29 + 34.0
2. Output black level/IRE = BLCKL × 2/6.18 + 31.7

Table 16 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[1]	recommended value: BLNNL = 46 (2EH)
		BLNNL = 0	output blanking level = 25 IRE
		BLNNL = 63 (3FH)	output blanking level = 45 IRE
		white-to-sync = 143 IRE[2]	recommended value: BLNNL = 53 (35H)
		BLNNL = 0	output blanking level = 26 IRE
		BLNNL = 63 (3FH)	output blanking level = 46 IRE
DECPH	real time control	logic 0	disable subcarrier phase reset bit from RTCI
		logic 1	enable subcarrier phase reset bit from RTCI (see Fig.10)

Notes

1. Output black level/IRE = BLNNL × 2/6.29 + 25.4
2. Output black level/IRE = BLNNL × 2/6.18 + 25.9

Table 17 Subaddress 5F

DATA BYTE	DESCRIPTION
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL
CCRS	select cross colour reduction filter in luminance; see Table 18

Table 18 Logic levels and function of CCRS

CCRS1	CCRS0	DESCRIPTION
0	0	no cross colour reduction; for overall transfer characteristic of luminance see Fig.3
0	1	cross colour reduction #1 active; for overall transfer characteristic see Fig.3
1	0	cross colour reduction #2 active; for overall transfer characteristic see Fig.3
1	1	cross colour reduction #3 active; for overall transfer characteristic see Fig.3

Table 19 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line; default after reset
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component); default after reset
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4); default after reset
YGS	0	luminance gain for white – black 100 IRE; default after reset
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWN	0	DACs for CVBS, Y and C in normal operational mode; default after reset
	1	DACs for CVBS, Y and C forced to lowest output voltage

Table 20 Subaddress 62H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
RTCE	0	no real time control of generated subcarrier frequency
	1	real time control of generated subcarrier frequency through SAA7151B or SAA7111 (timing see Fig.10)

Table 21 Subaddress 62H

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 2.02 × nominal	recommended value: BSTA = 63 (3FH)
		white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 2.82 × nominal	recommended value: BSTA = 45 (2DH)
		white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.90 × nominal	recommended value: BSTA = 67 (43H)
		white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 3.02 × nominal	recommended value: BSTA = 47 (2FH)

Table 22 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = \left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$, rounded up; see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 23 Subaddress 67 to 6A

DATA BYTE	DESCRIPTION	REMARKS
L21O0	first byte of captioning data, odd field	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of Line 21 encoding format.
L21O1	second byte of captioning data, odd field	
L21E0	first byte of extended data, even field	
L21E1	second byte of extended data, even field	

Table 24 Subaddress 6B

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference pulse that is defined by RCV2S and RCV2E, also during vertical blanking Interval); default after reset if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a ‘Composite-Blanking-Not’ signal, for example a reference pulse that is defined by RCV2S and RCV2E, excluding Vertical Blanking Interval, which is defined by FAL and LAL if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port (at bit SYMP = LOW) or from decoded frame sync of “*CCIR 656”* input (at bit SYMP = HIGH); default after reset
	1	horizontal synchronization is taken from RCV2 port (at bit SYMP = LOW)
SRCV1	–	defines signal type on pin RCV1; see Table 25

Table 25 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field; default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0) or eighth field (PAL = 1)
1	1	not applicable	not applicable	–

Table 26 Subaddress 6C and 6D

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or [1727 (FISE = 0)] are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 398H [398H]

Table 27 Subaddress 6D

DATA BYTE	DESCRIPTION
VTRIG	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)

Table 28 Subaddress 6E

DATA BYTE	LOGIC LEVEL	DESCRIPTION
SBLBN	0	vertical blanking is defined by programming of FAL and LAL; default after reset
	1	vertical blanking is forced in accordance with *"CCIR 624"* (50 Hz) or RS170A (60 Hz)
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 29
FLC	–	field length control; see Table 30

Table 29 Logic levels and function of PHRES

DATA BYTE		DESCRIPTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1; default after reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 30 Logic levels and function of FLC

DATA BYTE		DESCRIPTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 31 Subaddress 6F

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CCEN	–	enables individual Line 21 encoding; see Table 32
TTXEN	0	disables teletext insertion
	1	enables teletext insertion
SCCLN	–	selects the actual line, where closed caption or extended data are encoded line = (SCCLN + 4) for M-systems line = (SCCLN + 1) for other systems

Table 32 Logic levels and function of CCEN

DATA BYTE		DESCRIPTION
CCEN1	CCEN0	
0	0	Line 21 encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 33 Subaddress 70 to 72

DATA BYTE	DESCRIPTION
RCV2S	start of output signal on pin RCV2 values above 1715 (FISE = 1) or [1727 (FISE = 0)] are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2S = 11AH [0FDH]
RCV2E	end of output signal on pin RCV2 values above 1715 (FISE = 1) or [1727 (FISE = 0)] are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2E = 694H [687H]

Table 34 Subaddress 73 and 74

DATA BYTE	DESCRIPTION
TTXHS	start of signal on pin TTXRQ see Fig.7
TTXHD	indicates the delay in clock cycles between rising edge of TTXRQ output and valid data on pin TTX minimum value has to be TTXHD = 2

Table 35 Subaddress 75

DATA BYTE	DESCRIPTION
VS_S	Vertical Sync. shift between RCV1 and RCV2 (switched to output) in master mode it is possible to shift H-sync (RCV2; CBLF = 0) against V-sync (RCV1; SRCV1 = 00) standard value: VS_S = 3

Table 36 Subaddress 76, 77 and 7C

DATA BYTE	DESCRIPTION
TTXOVS	first line of occurrence of signal on pin TTXRQ in odd field line = (TTXOVS + 4) for M-systems line = (TTXOVS + 1) for other systems
TTXOVE	last line of occurrence of signal on pin TTXRQ in odd field line = (TTXOVE + 3) for M-systems line = TTXOVE for other systems

Table 37 Subaddress 78, 79 and 7C

DATA BYTE	DESCRIPTION
TTXEVS	first line of occurrence of signal on pin TTXRQ in even field line = (TTXEVS + 4) for M-systems line = (TTXEVS + 1) for other systems
TTXEVE	last line of occurrence of signal on pin TTXRQ in even field line = (TTXEVE + 3) for M-systems line = TTXEVE for other systems

Table 38 Subaddress 7C

DATA BYTE	LOGIC LEVEL	DESCRIPTION
TTX60	0	enables NABTS (FISE = 1) or European TTX (FISE = 0); default after reset
	1	enables World Standard Teletext 60 Hz (FISE = 1)

Table 39 Subaddress 7A to 7C

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M-systems, = FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M-systems, = LAL for other system, measured in lines LAL = 0 coincides with the first field synchronization pulse

Table 40 Subaddress 7E and 7F

DATA BYTE	DESCRIPTION
LINE	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate) this bit mask is effective only, if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE

Slave Transmitter

Table 41 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E

Table 42 No subaddress

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	Version identification of the device. It will be changed with all versions of the device that have different programming models. Current version is 000 binary.
CCRDO	1	Closed caption bytes of the odd field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data has been encoded.
CCRDE	1	Closed caption bytes of the even field have been encoded.
	0	The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data has been encoded.
FSEQ	1	During first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields).
	0	Not first field of a sequence.
O_E	1	During even field.
	0	During odd field.

CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDA}	analog supply voltage		3.1	3.5	V
V_{DDD}	digital supply voltage		3.0	3.6	V
I_{DDA}	analog supply current	note 1	–	62	mA
I_{DDD}	digital supply current	note 1	–	38	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		–0.5	+0.8	V
V_{IH}	HIGH level input voltage (except, SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.3	V
I_{LI}	input leakage current		–	1	µA
C_i	input capacitance	clocks	–	10	pF
		data	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	I_{OL} = 4 mA	–	0.4	V
V_{OH}	HIGH level output voltage (except, SDA, and XTALO)	I_{OH} = 4 mA	V_{DDD} – 4	–	V
I^2C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		–0.5	V_{DDD} + 0.3	V
V_{IH}	HIGH level input voltage		2.3	V_{DDD} + 0.3	V
I_i	input current	V_i = LOW or HIGH	–10	+10	µA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_o	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 2	34	41	ns
δ	duty factor t_{HIGH}/t_{LLC}	note 3	40	60	%
t_r	rise time	note 2	–	5	ns
t_f	fall time	note 2	–	6	ns
Input timing					
$t_{SU;DAT}$	input data set-up time (any pin except SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		6	–	ns
$t_{HD;DAT}$	input data hold time (any pin except SCL, SDA, $\overline{\text{RESET}}$, AP and SP)		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 4	-50×10^{-6}	$+50 \times 10^{-6}$	
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 – 20%	1.5 + 20%	fF
C_0	parallel capacitance (typical)		3.5 – 20%	3.5 + 20%	pF
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_h	output hold time		4	–	ns
t_d	output delay time		–	25	ns
C, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 5	1.20	1.45	V
R_{int}	internal serial resistance		1	3	Ω
R_L	output load resistance		75	300	Ω
B_{-3dB}	output signal bandwidth of DACs		10	–	MHz
ILE	LF integral linearity error of DACs		–	±3	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The data is for both input and output direction.
3. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
4. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
5. For full digital range, without load, V_{DDA} = 3.3 V. The typical voltage swing is 1.35 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

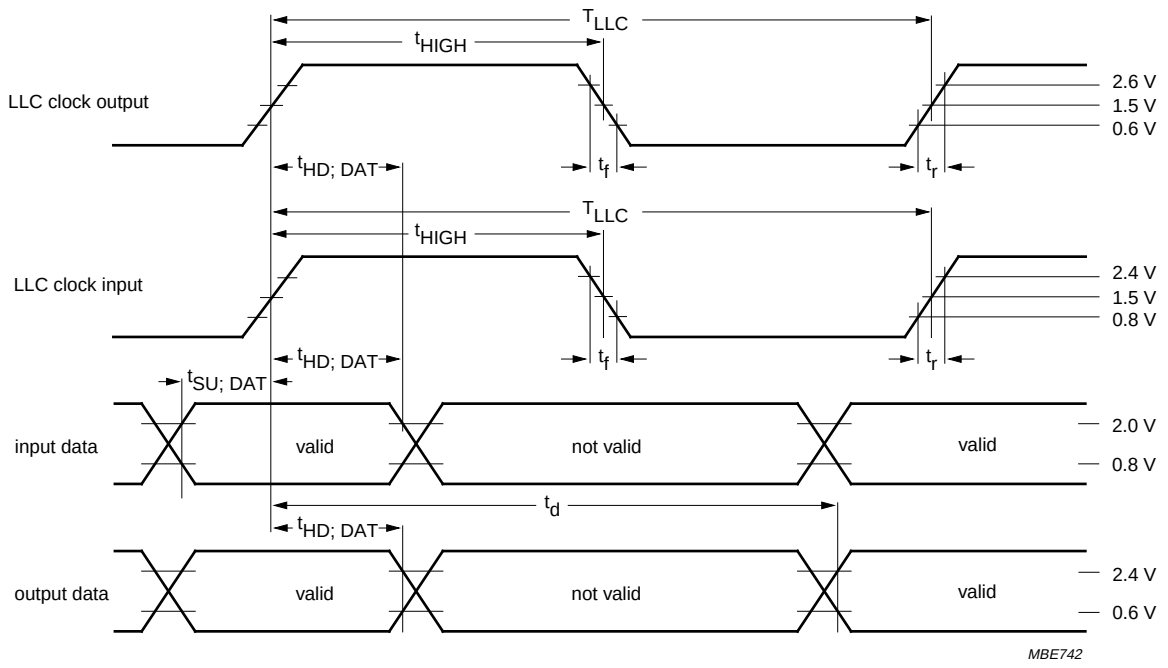
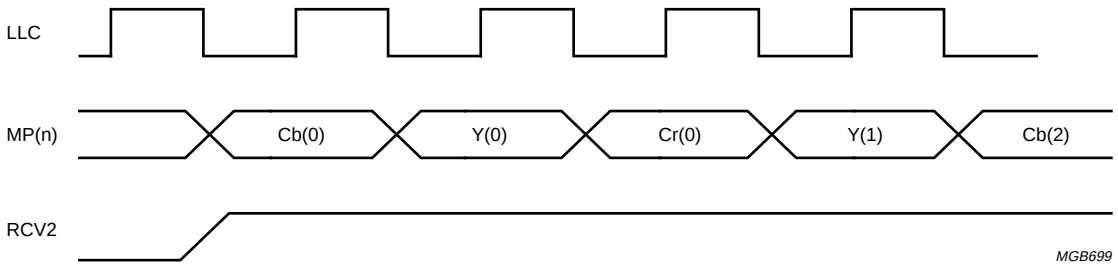
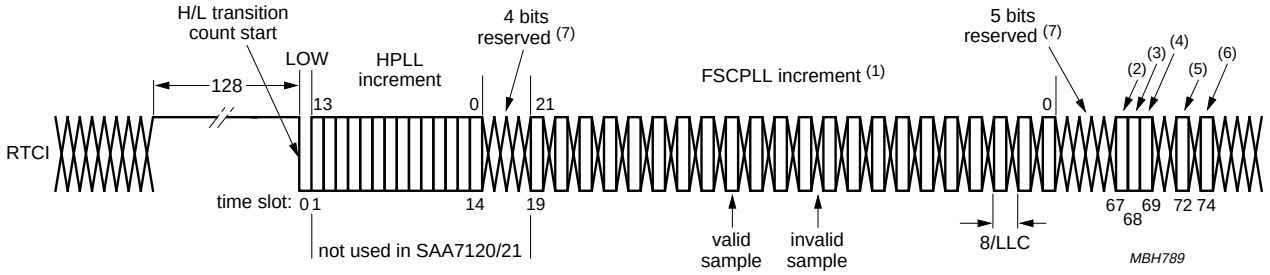


Fig.8 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The phase of the RCV2 signal is programmed to tbf (tbf for 50 Hz) in this example in output mode (RCV2S).

Fig.9 Functional timing.



(1) SAA7111 provides (22:0) bits, resulting in 3 reserved bits before sequence bit.

(2) Sequence bit

PAL: 0 = (R–Y) line normal, 1 = (R–Y) line inverted

NTSC: 0 = no change.

(3) Reset bit: only from SAA7111 decoder.

(4) FISE bit: 0 = 50 Hz, 1 = 60 Hz.

(5) Odd/even bit: odd/even from external.

(6) Colour detection: 0 = no colour detected, 1 = colour detected.

(7) Reserved bits: 232 with 50 Hz systems, 229 with 60 Hz systems.

Fig.10 RTCI timing.

Explanation of RTCI data bits

1. The ConDENC generates the subcarrier frequency out of the FSCPLL increment if enabled (see item 6.).
2. The PAL bit indicates the line with inverted R - Y component of colour difference signal.
3. If the reset bit is enabled (RTCE = 1; DECPH = 1; PHRES = 00), the phase of the subcarrier is reset in each line whenever the reset bit of RTCI input is set to 1.
4. If the FISE bit is enabled (RTCE = 1; DECFIS = 1), the ConDENC takes this bit instead of the FISE bit in subaddress 61H.
5. If the odd/even bit is enabled (RTCE = 1; DECOE = 1), the ConDENC ignores its internally generated odd/even flag and takes the odd/even bit from RTCI input.
6. If the colour detection bit is enabled (RTCE = 1; DECCOL = 1) and no colour was detected (colour detection bit = 0), the subcarrier frequency is generated by the ConDENC. In the other case (colour detection bit = 1) the subcarrier frequency is evaluated out of FSCPLL increment.

   If the colour detection bit is disabled (RTCE = 1; DECCOL = 0), the subcarrier frequency is evaluated out of FSCPLL increment, independent of the colour detection bit of RTCI input.

APPLICATION INFORMATION

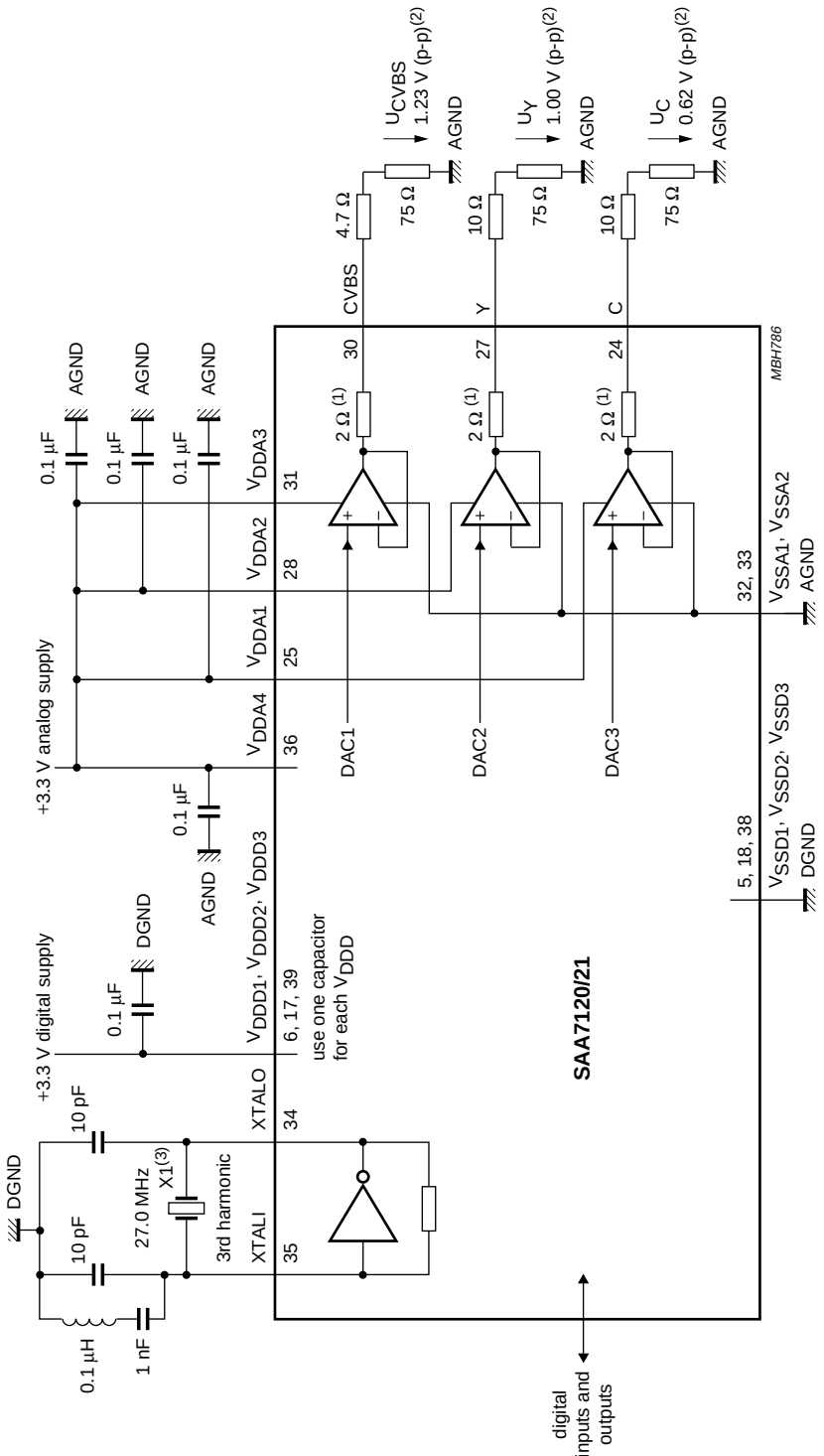
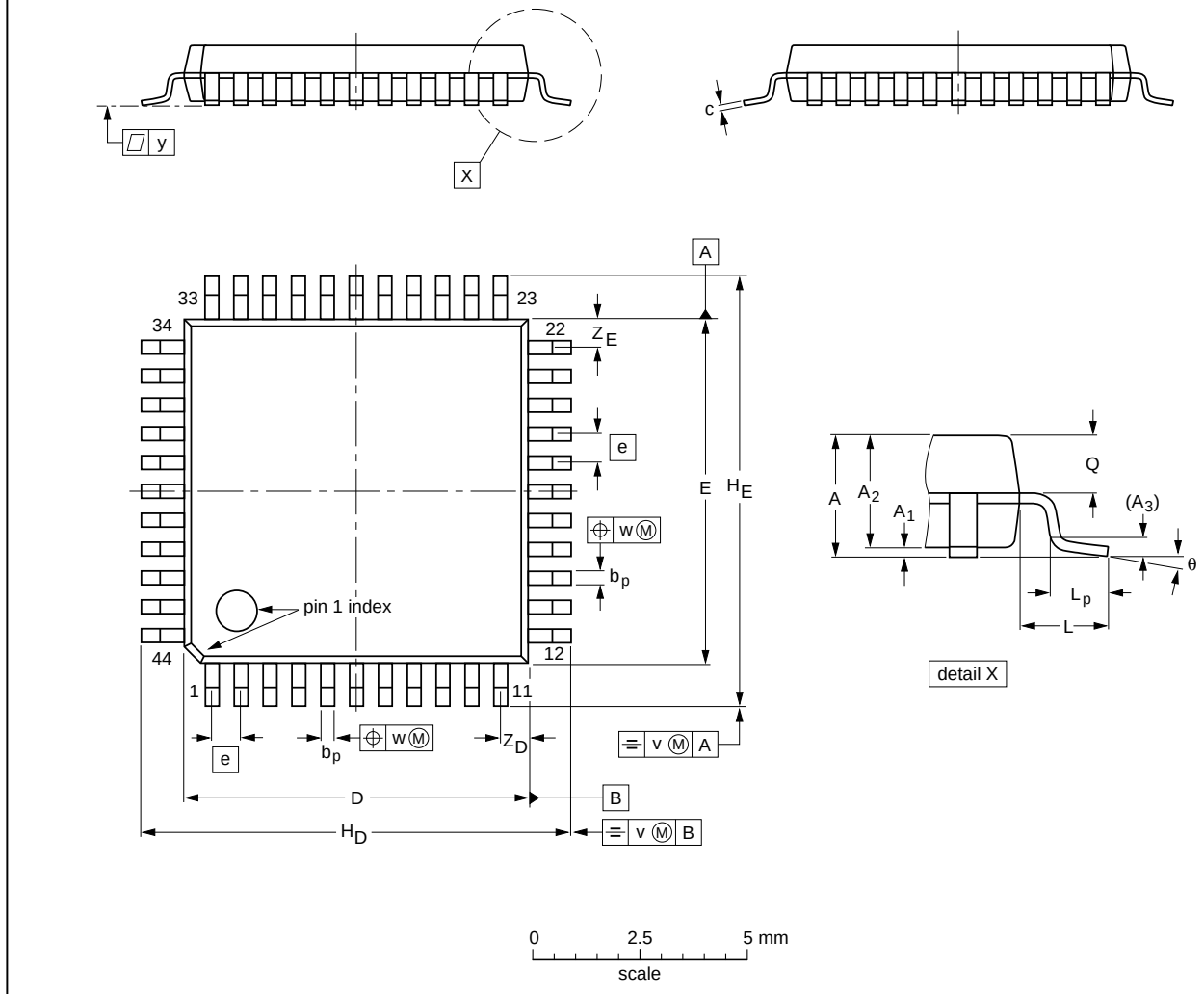


Fig.11 Application environment of ConDENC.

(1) Typical value.
(2) For 100/100 colour bar.
(3) Order no. 4312 065 02341.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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