DATA SHEET

SAA7186
Digital video scaler

Preliminary specification
File under Integrated Circuits, IC22

May 1993

Philips Semiconductors

PHILIPS

CONTENTS

Digital video scaler SAA7186

1 FEATURES

- Scaling of video picture windows down to randomly sized windows
- Processes maximum 1023 pixels per line and 1023 lines per field
- Two-dimensional data processing for improved signal quality of scaled video data and for compression of video data
- 16-bit YUV input data buffer
- Interlace/non-interlace video data processing and field control
- Line memories in Y path and UV path to store two lines, each with $2 \times 768 \times 8$ bit capacity
- Vertical sync processing by scale control
- Non-scaled mode to get full picture or to gate videotext lines
- UV input and output data binary/two's complement
- Switchable RGB matrix and anti-gamma ROMs
- 16-word FIFO register for 32-bit output data
- Output formats: 5-bit and 8-bit RGB, 8-bit YUV or 8-bit monochrome

2 GENERAL DESCRIPTION

The CMOS circuit SAA7186 scales and filters digital video data to randomly sized picture windows. YUV input data in 4:2:2 format are required (SAA7191B source).

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5	5.5	V
$I_{DD\ tot}$	total supply current (inputs LOW, without output load)	-	-	180	mA
V_I	data input level	TTL-compatible			
V_O	data output level	TTL-compatible			
LLC	input clock frequency	-	-	32	MHz
T_{amb}	operating ambient temperature range	0	-	70	°C

4 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7186	100	QFP	plastic	SOT317-2

5 BLOCK DIAGRAM

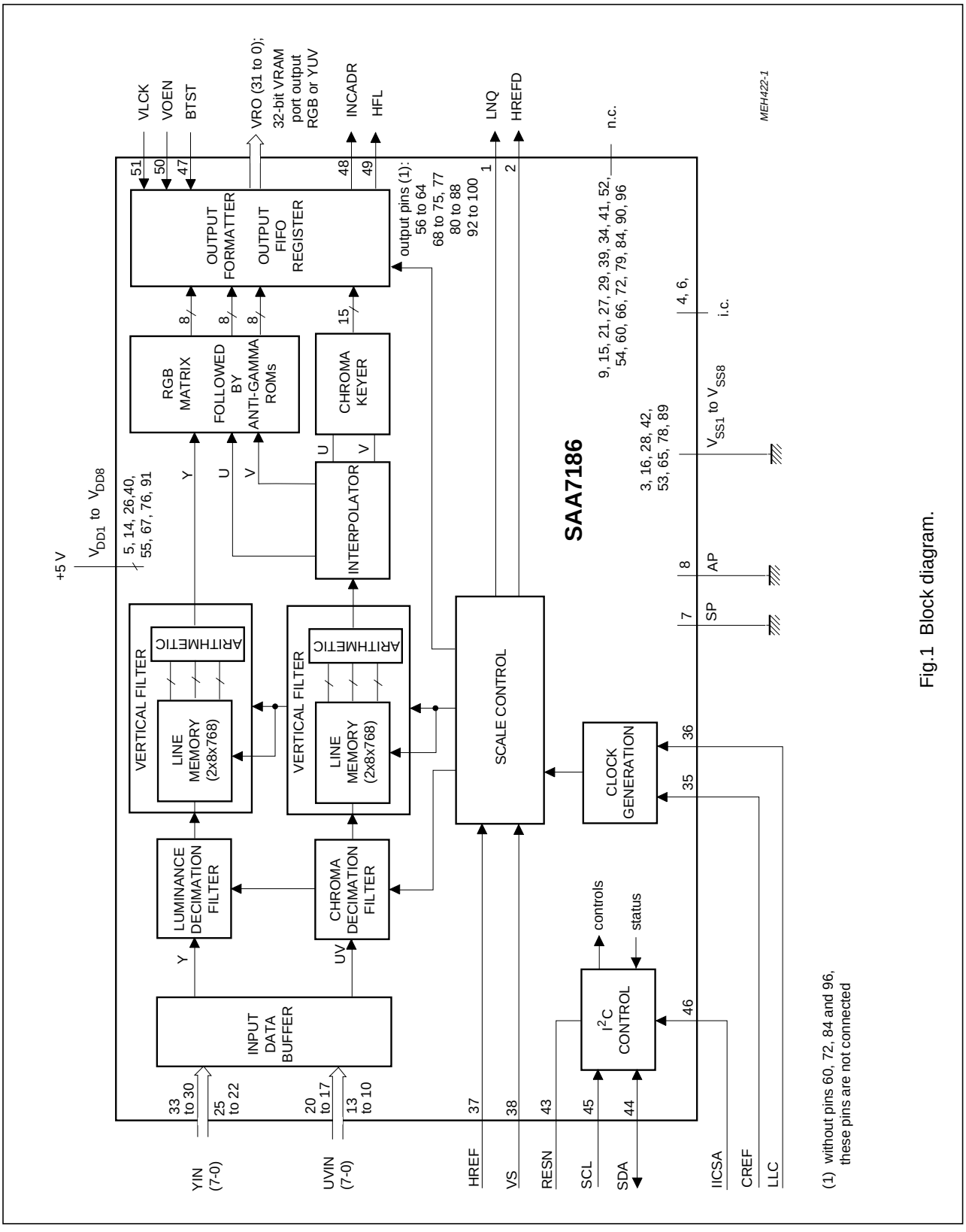


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	STATUS	DESCRIPTION
LNQ	1	O	line qualifier signal; active polarity defined by QPL-bit in “10” (VCLK strobed)
HREFD	2	O	delay-compensated HREF output signal (VCLK strobed)
V_{SS1}	3	–	GND1 (0 V)
i.c.	4	–	internally connected
V_{DD1}	5	–	+5 V supply voltage 1
i.c.	6	–	internally connected
SP	7	I	connected to ground (shift pin for testing)
AP	8	I	connected to ground (action pin for testing)
n.c.	9	–	not connected
UVIN0	10	I	time-multiplexed colour-difference input data (bits 0 to 3)
UVIN1	11	I	
UVIN2	12	I	
UVIN3	13	I	
V_{DD2}	14	–	+5 V supply voltage 2
n.c.	15	–	not connected
V_{SS2}	16	–	GND2 (0 V)
UVIN4	17	I	time-multiplexed colour-difference input data (bits 4 to 7)
UVIN5	18	I	
UVIN6	19	I	
UVIN7	20	I	
n.c.	21	–	not connected
YIN0	22	I	luminance input data (bits 0 to 3)
YIN1	23	I	
YIN2	24	I	
YIN3	25	I	
V_{DD3}	26	–	+5 V supply voltage 3
n.c.	27	–	not connected
V_{SS3}	28	–	GND3 (0 V)
n.c.	29	–	not connected
YIN4	30	I	luminance input data (bits 4 to 7)
YIN5	31	I	
YIN6	32	I	
YIN7	33	I	
n.c.	34	–	not connected
CREF	35	I	clock reference, external sync signal
LLC	36	I	line-locked system clock input signal (twice of pixel rate)
HREF	37	I	horizontal reference, pixel data clock signal (also present during vertical blanking)
VS	38	I	vertical sync input signal (approximately 6 lines long)
n.c.	39	–	not connected
V_{DD4}	40	–	+5 V supply voltage 4

SYMBOL	PIN	STATUS	DESCRIPTION
n.c.	41	–	not connected
V_{SS4}	42	–	GND4 (0 V)
RESN	43	I	reset input (active-LOW for at least 30LLC periods)
SDA	44	I/O	IIC-bus data line
SCL	45	I	IIC-bus clock line
IICSA	46	I	set module address input of IIC-bus (LOW = B8, HIGH = BC)
BTST	47	I	output disable input; HIGH sets all data outputs to high-impedance state
INCADR	48	O	line increment / vertical reset control output line
HFL	49	O	FIFO register half-full flag output
VOEN	50	I	VRAM port output enable input (active-LOW)
VCLK	51	I	FIFO register clock input signal
n.c.	52	–	not connected
V_{SS5}	53	–	GND5 (0 V)
n.c.	54	–	not connected
V_{DD5}	55	–	+5 V supply voltage 5
VRO31	56	O	video output; 32-bit VRAM output port (bits 31 to 28)
VRO30	57	O	
VRO29	58	O	
VRO28	59	O	
n.c.	60	–	not connected
VRO27	61	O	video output; 32-bit VRAM output port (bits 27 to 24)
VRO26	62	O	
VRO25	63	O	
VRO24	64	O	
V_{SS6}	65	–	GND6 (0 V)
n.c.	66	–	not connected
V_{DD6}	67	–	+5 V supply voltage 6
VRO23	68	O	video output; 32-bit VRAM output port (bits 23 to 22)
VRO22	69	O	
VRO21	70	O	video output; 32-bit VRAM output port (bits 21 to 20)
VRO20	71	O	
n.c.	72	–	not connected
VRO19	73	O	video output; 32-bit VRAM output port (bits 19 to 17)
VRO18	74	O	
VRO17	75	O	
V_{DD7}	76	–	+5 V supply voltage 7
VRO16	77	O	video output; 32-bit VRAM output port (bit16)
V_{SS7}	78	–	GND7 (0 V)
n.c.	79	–	not connected

SYMBOL	PIN	STATUS	DESCRIPTION
VRO15	80	O	video output; 32-bit VRAM output port (bits 15 to 12)
VRO14	81	O	
VRO13	82	O	
VRO12	83	O	
n.c.	84	–	not connected
VRO11	85	O	video output; 32-bit VRAM output port (bits 11 to 8)
VRO10	86	O	
VRO9	87	O	
VRO8	88	O	
V_{SS8}	89	O	GND8 (0 V)
n.c.	90	–	not connected
V_{DD8}	91	–	+5 V supply voltage 8
VRO7	92	O	video output; 32-bit VRAM output port (bits 7 to 4)
VRO6	93	O	
VRO5	94	O	
VRO4	95	O	
n.c.	96	–	not connected
VRO3	97	O	video output; 32-bit VRAM output port (bits 3 to 0)
VRO2	98	O	
VRO1	99	O	
VRO0	100	O	

6.1 Pin configuration

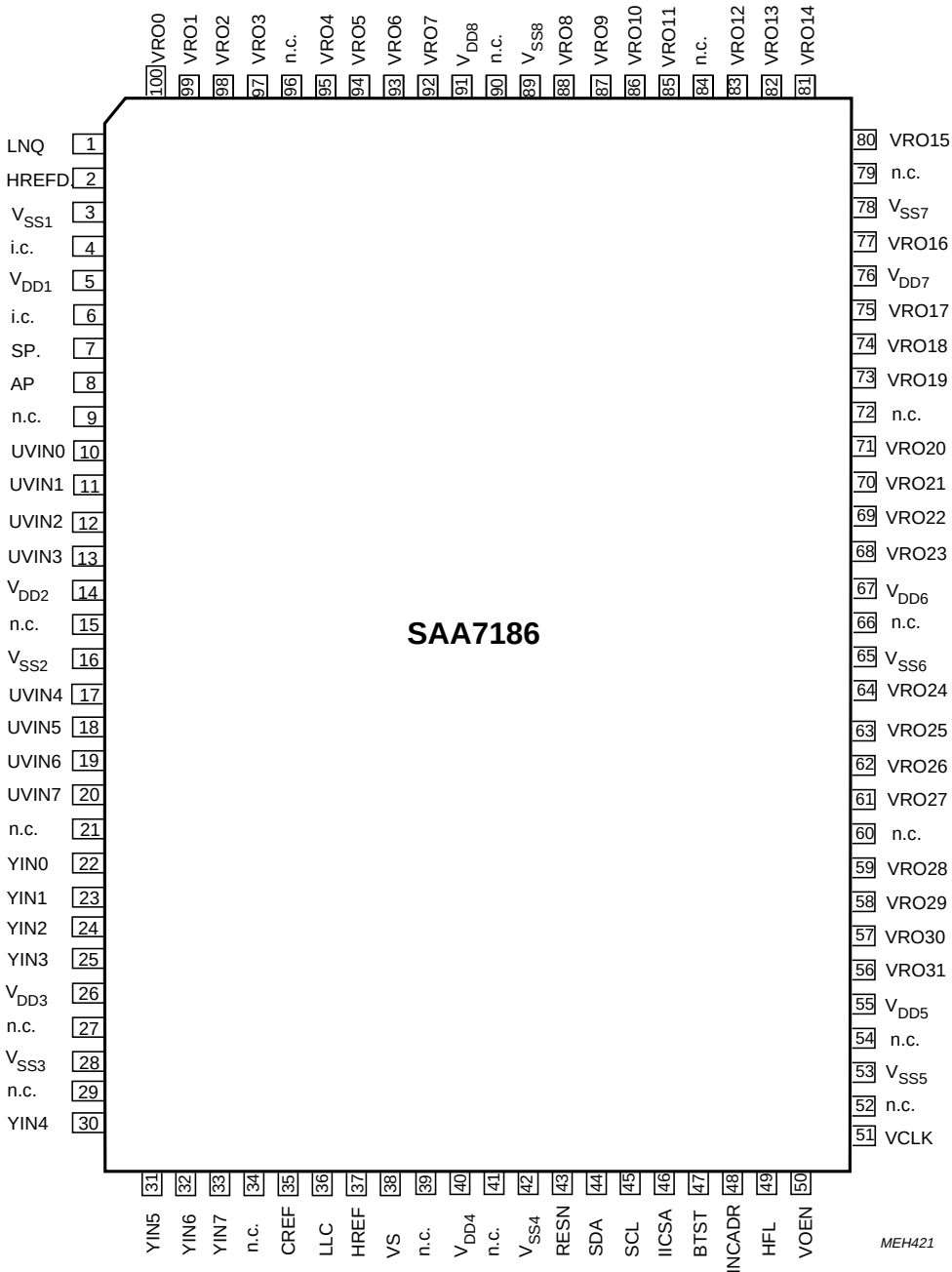


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The input port is output of Philips digital video multistandard decoders (SAA7151B, SAA7191B) or other similar sources.
The SAA7186 input supports the 16-bit YUV 4:2:2 format. The video data from the input port are converted into a unique internal two's complement data stream and are processed in horizontal direction in two separate decimation filters. Then they are processed in vertical direction by the vertical processing unit (VPU).
Chrominance data are interpolated to a 4:4:4 format; a chroma keying bit is generated.
The 4:4:4 YUV data are then converted from the YUV to the RGB domain in a digital matrix. ROM tables in the RGB data path can be used for anti-gamma correction of gamma-corrected input signals.
Uncorrected RGB and YUV signals can be bypassed.
A scale control unit generates reference and gate signals for scaling of the processed video data. After data formatting to the various VRAM port formats, the scaled video data are buffered in the 16 word $\times$ 32-bit output FIFO register. The FIFO output is directly connected to the VRAM output bus VRO(31-0). Specific reference signals support an easy memory interfacing.
All functions of the SAA7186 are controlled via I^2C-bus using 17 subaddresses. The external microcontroller can get information by reading the status register.

7.1 Video input port

The 16-bit YUV input data in 4:2:2 format (Table 1) consist of 8-bit luminance data Y (pins YIN(7-0)) and 8-bit time-multiplexed colour-difference data UV (pins UVIN(7-0)).
The input data are clocked in by the signals LLC and CREF (Fig.3). HREF and VS inputs define the video scan pattern (window).

Sequential input data

- are limited to maximum 768 active pixels per line if the vertical filter is active
- UV can be processed in straight binary and two's complement representation (controlled by TCC)

7.2 Decimation filters

The decimation filters perform accurate horizontal filtering of the input data stream.
Signal characteristics are matched in front of the pixel decimation stage, thus disturbing artifacts, caused by the pixel dropping, are reduced. The signal bandwidth can be reduced in steps of:

2-tap filter = –6 dB at 0.325 pixel rate

3-tap filter = –6 dB at 0.25 pixel rate

4-tap filter = –6 dB at 0.21 pixel rate

5-tap filter = –6 dB at 0.125 pixel rate

9-tap filter = –6 dB at 0.075 pixel rate

The different characteristics are chosen dependent on the defined scaling parameters in an adaptive filter mode (AFS-bit = 1).
The filter characteristics can also be selected independently by control bits HF2 to HF0 at AFS-bit = 0.

7.3 Vertical filters

Y and UV data are handled in separate filters (Fig.1). Each of the two line memories has a capacity of $2 \times 768 \times 8$-bit. Thus two complete video lines of 4:2:2 YUV data can be stored. The VPU is split into two memory banks and one arithmetic unit. The available processing modes, respectively transfer functions, are selectable by the bits VP1 and VP0 if AFS = 0.
An adaptive mode is selected by AFS = 1. Disturbing artifacts, generated by line dropping, are reduced.

Adaptive filter selection (AFS = 1):

SCALING RATIO	FILTER FUNCTION (REFER TO I^2C SECTION)
XD/XS	horizontal
≤1 ≤14/15 ≤11/15 ≤7/15 ≤3/15	bypassed filter 1 filter 6 filter 3 filter 4
YD/YS	vertical
≤1 ≤13/15 ≤4/15	bypassed filter 1 filter 2

7.4 RGB matrix

Y data and UV data are converted after interpolation into RGB data according to CCIR601 recommendation. Data are bypassed in YUV or monochrome modes.

Table 1 4 : 2 : 2 format (pixels per line). The time frames are controlled by the HREF signal.

INPUT	PIXEL BYTE SEQUENCE				
YIN7 YIN6 YIN5 YIN4 YIN3 YIN2 YIN1 YIN0	Ye7 Ye6 Ye5 Ye4 Ye3 Ye2 Ye1 Ye0	Yo7 Yo6 Yo5 Yo4 Yo3 Yo2 Yo1 Yo0	Ye7 Ye6 Ye5 Ye4 Ye3 Ye2 Ye1 Ye0	Yo7 Yo6 Yo5 Yo4 Yo3 Yo2 Yo1 Yo0	Ye7 Ye6 Ye5 Ye4 Ye3 Ye2 Ye1 Ye0
UVIN7 UVIN6 UVIN5 UVIN4 UVIN3 UVIN2 UVIN1 UVIN0	Ue7 Ue6 Ue5 Ue4 Ue3 Ue2 Ue1 Ue0	Ve7 Ve6 Ve5 Ve4 Ve3 Ve2 Ve1 Ve0	Ue7 Ue6 Ue5 Ue4 Ue3 Ue2 Ue1 Ue0	Ve7 Ve6 Ve5 Ve4 Ve3 Ve2 Ve1 Ve0	Ue7 Ue6 Ue5 Ue4 Ue3 Ue2 Ue1 Ue0
Y frame	0	1	2	3	4
UV frame	0		2		4

Note

1. e = even pixel; o = odd pixel

The matrix equations are these considering the digital quantization:

$R = Y + 1.375\ V$

$G = Y - 0.703125\ V - 0.34375\ U$

$B = Y + 1.734375\ U.$

Anti-gamma ROM tables:
ROM tables are implemented at the matrix output to provide anti-gamma correction of the RGB data. A curve for a gamma of 1.4 is implemented

The tables can be used (RTB-bit = 0) to compensate gamma correction for linear data representation of RGB output data.

7.5 Chrominance signal keyer

The keyer generates an alpha signal to achieve a 5-5-5 $+\alpha$ RGB alpha output signal. Therefore, the processed UV data amplitudes are compared with thresholds set via I^2C-bus (subaddresses ”0C to 0F”). A logical “1” signal is generated if the amplitude is inside the specified amplitude range, otherwise a logical “0” is generated.
Keying can be switched off by setting the lower limit higher than the upper limit (“0C or 0E” and “0D or 0F”).

7.6 Scale control and vertical regions

The scale control block SC includes vertical address/sequence counters to define the current position in the input field and to address the internal VPU memories.
To perform scaling, XD of XS pixel selection in horizontal direction and YD of YS line selection in vertical direction are applied. The pixel and line dropping are controlled at the input of the FIFO register. To control the decimation filter function and the vertical data processing in the adaptive mode (AFS = 1), the scaling ratio in horizontal and vertical direction is estimated in the SC block.

The input field can be divided into two vertical regions – the bypass region and the scaling region, which are defined via I^2C-bus by the parameters VS, VC, YO and YS.

Vertical bypass region:

Data are not scaled and independent of I^2C-bits FS1, FS0 the output format is always 8-bit greyscale (monochrome). The SAA7186 outputs all active pixels of a line, defined by the HREF input signal if the vertical bypass region is active. This can be used, for example, to store videotext information in the field memory.

The start line of the bypass region is defined by VS; the number of lines to be bypassed is defined by VC.

Vertical scaling region:

Data is scaled with start at line YO and the output format is selected when FS1, FS0 are valid.
This is the “normal operation” area.

The input/output screen dimensions in horizontal and vertical direction are defined by the parameters

XO, XS and XD for horizontal

YO, YS and YD for vertical.

The circuit processes XS samples of a line. Remaining pixels are ignored if a line is longer than XS. If a line is

shorter than XS, processing is aborted when the falling edge of HREF is detected.

Vertical regions in Fig.4:

- the two regions can be programmed via I²C-bus, whereby regions should not overlap (active region overrides the bypass region).
- the start of a normal active picture depends on video standard and has to be programmed to the correct value.
- the offsets XO and YO have to be set according to the internal processing delays to ensure the complete number of destination pixels and lines (Table 6).
- the scaling parameters can be used to perform a panning function over the video frame/field.

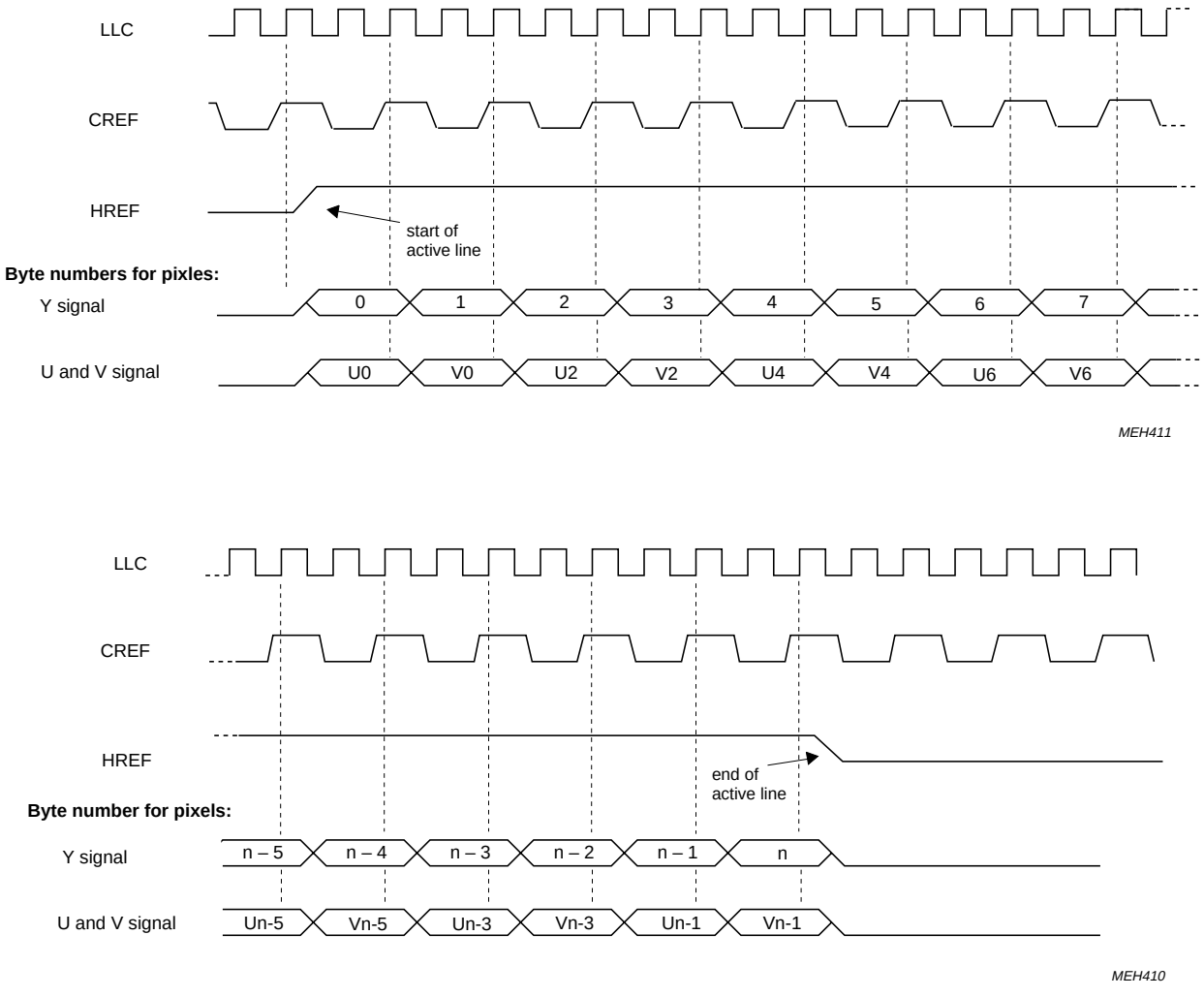


Fig.3 Horizontal and data multiplex timing.

7.7 Output data representation and levels

Output data representation of the YUV data can be modified by bit MCT (subaddress 10).
The DC gain is 1 for YUV input data. The corresponding RGB levels are defined by the matrix equations. The luminance levels are limited according to CCIR 601

16 (239) = black
235 (20) = white
(..) = greyscale luminance levels

if the YUV or monochrome luminance output formats are selected.

The signal levels of the RGB formats are limited in 8-bit to “0” or “255”. For the 5-bit RGB formats a truncation from 8-bit to 5-bit is implemented.

Fill values are inserted dependent on longword position and destination size:

- “0” in RGB formats and for Y two’s complement U, V
- “128” for U, V (straight binary)
- “255” in 8-bit greyscale format

The unused output values of the YUV and greyscale formats can be used for other purposes.

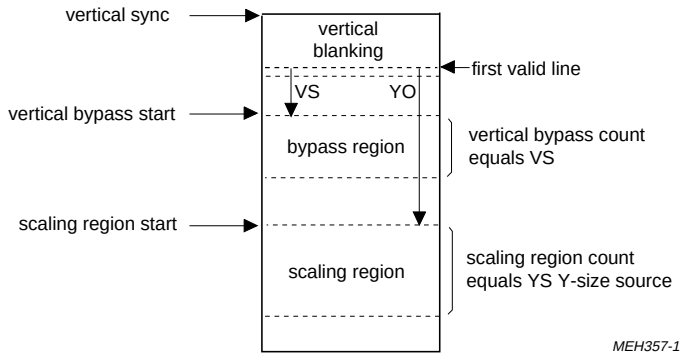


Fig.4 Vertical regions.

Table 2 VRAM port output data formats at **EFE-bit = 0** dependent on FS1 and FS0 bits (set via I^2C-bus)

PIXEL OUTPUT BITS	**FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 32-BIT WORDS**			**FS1 = 0; FS0 = 1 YUV 4:2:2 32-BIT WORDS**			**FS1 = 1; FS0 = 0 YUV 4:2:2 TEST 16-BIT WORDS**			**FS1 = 1; FS0 = 1 8-BIT MONOCHROME 32-BIT WORDS**		
PIXEL ORDER	**n**	**n+2**	**n+4**	**n**	**n+2**	**n+4**	**n**	**n+1**	**n+2**	**n n+1**	**n+4 n+5**	**n+8 n+9**
VRO31	α	α	α	Ye7	Ye7	Ye7	Ye7	Yo7	Ye7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Ye6	Ye6	Ye6	Yo6	Ye6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Ye5	Ye5	Ye5	Yo5	Ye5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Ye4	Ye4	Ye4	Yo4	Ye4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Ye3	Ye3	Ye3	Yo3	Ye3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Ye2	Ye2	Ye2	Yo2	Ye2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Ye1	Ye1	Ye1	Yo1	Ye1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Ye0	Ye0	Ye0	Yo0	Ye0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ue7	Ue7	Ue7	Ve7	Ue7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ue6	Ue6	Ue6	Ve6	Ue6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ue5	Ue5	Ue5	Ve5	Ue5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ue4	Ue4	Ue4	Ve4	Ue4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ue3	Ue3	Ue3	Ve3	Ue3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ue2	Ue2	Ue2	Ve2	Ue2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ue1	Ue1	Ue1	Ve1	Ue1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ue0	Ue0	Ue0	Ve0	Ue0	Yb0	Yb0	Yb0
PIXEL ORDER	**n+1**	**n+3**	**n+5**	**n+1**	**n+3**	**n+5**	**OUTPUTS NOT USED**			**n+2 n+3**	**n+6 n+7**	**n+10 n+11**
VRO15	α	α	α	Yo7	Yo7	Yo7	X	X	X	Yc7	Yc7	Yc7
VRO14	R4	R4	R4	Yo6	Yo6	Yo6	X	X	X	Yc6	Yc6	Yc6
VRO13	R3	R3	R3	Yo5	Yo5	Yo5	X	X	X	Yc5	Yc5	Yc5
VRO12	R2	R2	R2	Yo4	Yo4	Yo4	X	X	X	Yc4	Yc4	Yc4
VRO11	R1	R1	R1	Yo3	Yo3	Yo3	X	X	X	Yc3	Yc3	Yc3
VRO10	R0	R0	R0	Yo2	Yo2	Yo2	X	X	X	Yc2	Yc2	Yc2
VRO9	G4	G4	G4	Yo1	Yo1	Yo1	X	X	X	Yc1	Yc1	Yc1
VRO8	G3	G3	G3	Yo0	Yo0	Yo0	X	X	X	Yc0	Yc0	Yc0
VRO7	G2	G2	G2	Ve7	Ve7	Ve7	X	X	X	Yd7	Yd7	Yd7
VRO6	G1	G1	G1	Ve6	Ve6	Ve6	X	X	X	Yd6	Yd6	Yd6
VRO5	G0	G0	G0	Ve5	Ve5	Ve5	X	X	X	Yd5	Yd5	Yd5
VRO4	B4	B4	B4	Ve4	Ve4	Ve4	X	X	X	Yd4	Yd4	Yd4
VRO3	B3	B3	B3	Ve3	Ve3	Ve3	X	X	X	Yd3	Yd3	Yd3
VRO2	B2	B2	B2	Ve2	Ve2	Ve2	X	X	X	Yd2	Yd2	Yd2
VRO1	B1	B1	B1	Ve1	Ve1	Ve1	X	X	X	Yd1	Yd1	Yd1
VRO0	B0	B0	B0	Ve0	Ve0	Ve0	X	X	X	Yd0	Yd0	Yd0

Note

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels

Table 3 VRAM port output data formats at **EFE-bit = 1** dependent on FS1 and FS0 bits (set via I^2C-bus)

PIXEL OUTPUT BITS	**FS1 = 0; FS0 = 0 RGB 5-5-5 + 1 16-BIT WORDS**			**FS1 = 0; FS0 = 1 YUV 4:2:2 16-BIT WORDS**			**FS1 = 1; FS0 = 0 RGB 8-8-8 24-BIT WORDS**			**FS1 = 1; FS0 = 1 8-BIT MONOCHROME 16-BIT WORDS**		
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO31	α	α	α	Ye7	Yo7	Ye7	R7	R7	R7	Ya7	Ya7	Ya7
VRO30	R4	R4	R4	Ye6	Yo6	Ye6	R6	R6	R6	Ya6	Ya6	Ya6
VRO29	R3	R3	R3	Ye5	Yo5	Ye5	R5	R5	R5	Ya5	Ya5	Ya5
VRO28	R2	R2	R2	Ye4	Yo4	Ye4	R4	R4	R4	Ya4	Ya4	Ya4
VRO27	R1	R1	R1	Ye3	Yo3	Ye3	R3	R3	R3	Ya3	Ya3	Ya3
VRO26	R0	R0	R0	Ye2	Yo2	Ye2	R2	R2	R2	Ya2	Ya2	Ya2
VRO25	G4	G4	G4	Ye1	Yo1	Ye1	R1	R1	R1	Ya1	Ya1	Ya1
VRO24	G3	G3	G3	Ye0	Yo0	Ye0	R0	R0	R0	Ya0	Ya0	Ya0
VRO23	G2	G2	G2	Ue7	Ve7	Ue7	G7	G7	G7	Yb7	Yb7	Yb7
VRO22	G1	G1	G1	Ue6	Ve6	Ue6	G6	G6	G6	Yb6	Yb6	Yb6
VRO21	G0	G0	G0	Ue5	Ve5	Ue5	G5	G5	G5	Yb5	Yb5	Yb5
VRO20	B4	B4	B4	Ue4	Ve4	Ue4	G4	G4	G4	Yb4	Yb4	Yb4
VRO19	B3	B3	B3	Ue3	Ve3	Ue3	G3	G3	G3	Yb3	Yb3	Yb3
VRO18	B2	B2	B2	Ue2	Ve2	Ue2	G2	G2	G2	Yb2	Yb2	Yb2
VRO17	B1	B1	B1	Ue1	Ve1	Ue1	G1	G1	G1	Yb1	Yb1	Yb1
VRO16	B0	B0	B0	Ue0	Ve0	Ue0	G0	G0	G0	Yb0	Yb0	Yb0
PIXEL ORDER	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n**	**n+1**	**n+2**	**n n+1**	**n+2 n+3**	**n+4 n+5**
VRO15	X	X	X	X	X	X	B7	B7	B7	X	X	X
VRO14	X	X	X	X	X	X	B6	B6	B6	X	X	X
VRO13	X	X	X	X	X	X	B5	B5	B5	X	X	X
VRO12	X	X	X	X	X	X	B4	B4	B4	X	X	X
VRO11	X	X	X	X	X	X	B3	B3	B3	X	X	X
VRO10	X	X	X	X	X	X	B2	B2	B2	X	X	X
VRO9	X	X	X	X	X	X	B1	B1	B1	X	X	X
VRO8	X	X	X	X	X	X	B0	B0	B0	X	X	X
VRO7 (2, 3)	α	α	α	α	X	α	α	α	α	α	α	α
VRO6 (3)	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E	O/E
VRO5 (3)	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT	VGT
VRO4 (3)	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT	HGT
VRO3	X	X	X	X	X	X	X	X	X	X	X	X
VRO2 (3)	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF	HRF
VRO1 (3)	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ	LNQ
VRO0 (3)	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ	PXQ

Notes

1. α = keying bit; R, G, B, Y, U and V = digital signals; e = even pixel number; o = odd pixel number; a b c d = consecutive pixels; O/E = odd/even flag
2. YUV 16-bit format: the keying signal α is defined only for YU time steps. The corresponding YV sample has also to be keyed. The α signal in monochrome mode can be used only in the transparent mode (TTR = 1), in this case Ya = Yb.
3. Data valid only when transparent mode active (TTR-bit = 1) and VCLK pin connected to LLC/2 clock rate.

7.8 Output FIFO register and VRAM output port

The output FIFO register is the buffer between the video data stream and the VRAM data input port. Resized video data are buffered and formatted. 32-, 24- and 16-bit video data modes are supported. The various formats are selected by the bits EFE, FS1 and FS0. VRAM port formats are shown in Tables 2 and 3. The FIFO register capacity is 16 word $\times$ 32 bit (for 32-, 24-, or 16-bit video data). The bits LW1 and LW0 can be used to define the position of the first pixel each line in the 32-bit longword formats or to shift the UV sequence to VU in the 16-bit YUV formats (LW1 = 1).

VRAM port inputs are:
VCLK to clock the FIFO register output data and VOEN to enable output data.

VRAM port outputs are:
the HFL flag (half-full flag), the signal INCADR (refer to section “data burst transfer”) and the reference signals for pixel and line selection on outputs VRO(7-0) (only for 24- and 16-bit video data formats refer to “transparent data transfer”).

7.9 VRAM port transfer procedures

Data transfer on the VRAM port can be done asynchronously controlled by outputs HFL, INCADR and input VCLK (data burst transfer with bit TTR = 0).

Data transfer on the VRAM port can be done synchronously controlled by output reference signals on outputs VRO(7-0) and a clock rate of LLC/2 on input VCLK (transparent data transfer with bit TTR = 1 and EFE = 1). The scaling capability of the SAA7186 can be used in various applications.

7.10 Data burst transfer mode

Data transfer on the VRAM port is asynchronously (TTR = 0). This mode can be used for all output formats. Four signals for communication with the external memory are provided.

- HFL flag, the half-full flag of the FIFO output register is raised when the FIFO contains at least 8 data words (HFL = HIGH). By setting HFL = 1, the SAA7186 requests a data burst transfer by the external memory controller, that has to start a transfer cycle within the next 32 LLC cycles for 32-bit longword modes (16 LLC cycles for 16- and 24-bit modes). If there are pixels in the FIFO at the end of a line, which are not transferred, the circuit fills up the FIFO register with “fill pixels” until it is half-full and sets the HFL flag to request a data burst transfer. After transfer is done, HFL is used in combination with INCADR to indicate the line increments (Figures 6 and 7).
- INCADR output signal is used in combination with HFL to control horizontal and vertical address generation for a memory controller. The pulse sequence depends on field formats (interlace/ non-interlace or odd/even fields, Figures 6 and 7) and control bits OF (subaddress 00).

  HFL = 1 at the rising edge of INCADR:

  the end of line is reached, request for line address increment

  HFL = 0 at the rising edge of INCADR:

  the end of field/frame is reached, request for line and pixel addresses reset

  (The distance from the last half-full request HFL to the INCADR pulse may be longer than 64 $\times$ LLC. The HFL state is defined for minimum 4 $\times$ LLC in front of the rising edge of INCADR and minimum 2 $\times$ LLC afterwards.)
- VCLK input signal to clock the FIFO register output data VRO(n). New data are placed on the VRO(n) port with the rising edge of VCLK (Fig.5).
- VOEN input enables output data VRO(n). The outputs are in 3-state mode at VOEN = HIGH. VOEN changes only when VCLK is LOW. If VCLK pulses are applied during VOEN = HIGH, the outputs remain inactive, but the FIFO register accepts the pulses.

7.11 Transparent data transfer mode

Data transfer on the VRAM port can be achieved synchronously (TTR = 1). With a continuous clock rate of LLC/2 on input VCLK, the SAA7186 delivers a continuously processed data stream. Therefore, the extended formats of the VRAM output port have to be selected (bit EFE = 1; Table 3). The reference and gate signals on outputs VRO(6-1) and the LNQ signal are delivered in each field (means scaled and ignored fields). The PXO signal (also VRO0) is only delivered in active fields. The output signals VRO(7-0) can be used to buffer qualified pre-processed RGB or YUV video data (notice: the YUV data are only valid in qualified time slots). Control output signals in Table 3 are:

α	keying signal of the chroma keyer
O/E	odd/even field bit according to the internal field processing
VGT	vertical gate signal, “1” marks the scaling window in vertical direction from YO to (YO + YS) lines, cut by VS.
HGT	horizontal gate signal, “1” marks horizontal direction from XO to (XO + XS) lines, cut by HREF.
HRF	delay compensated horizontal reference signal.
LNQ	line qualifier signal, active polarity is defined by QPL bit.
PXQ	pixel qualifier signal, active polarity is defined by QPP bit.

7.12 Power-on reset

- the FIFO register contents are undefined
- outputs VRO are set to high-impedance state
- output INCADR = HIGH
- output HFL = LOW until the VPE bit is set to “1”
- subaddress “10” is set to 00h and VPE-bit in subaddress “00” is set to zero (Table 4).

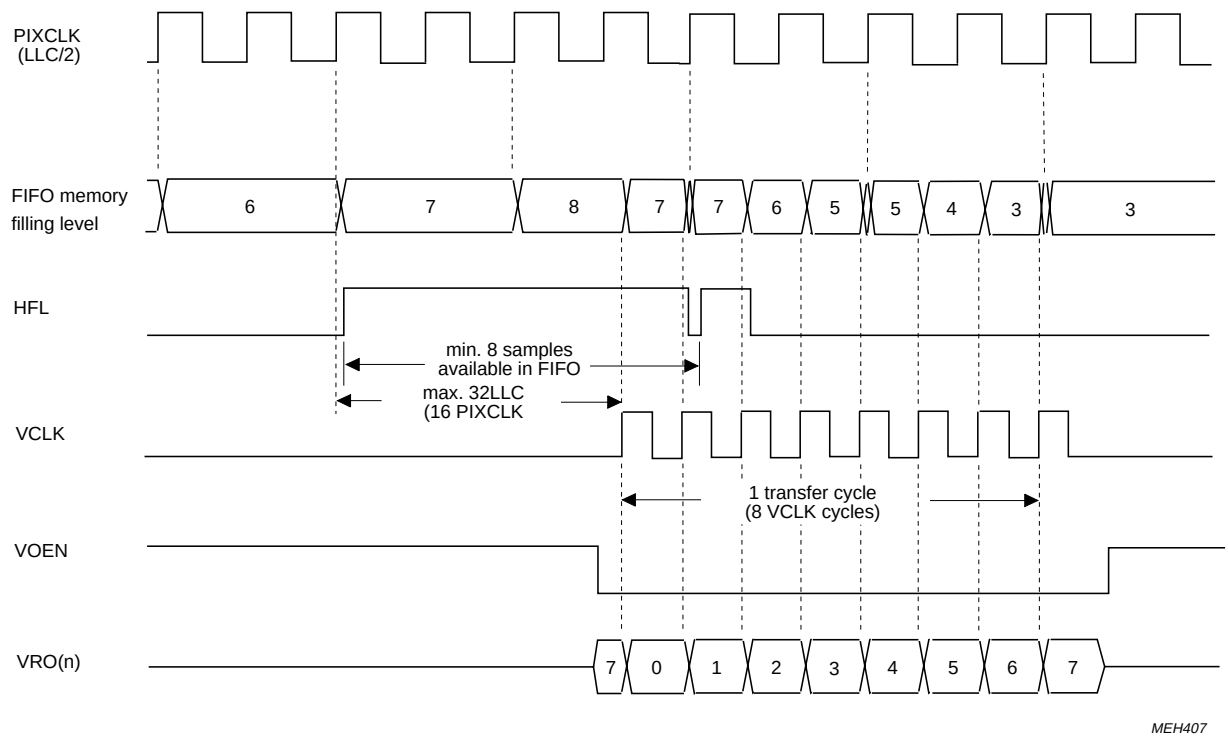


Fig.5 Output port transfer to VRAM at 32-bit data format without scaling. If VCLK cycles occur at VOEN = HIGH, the FIFO register is unchanged, but the outputs VRO(31-0) remain in 3-state position.

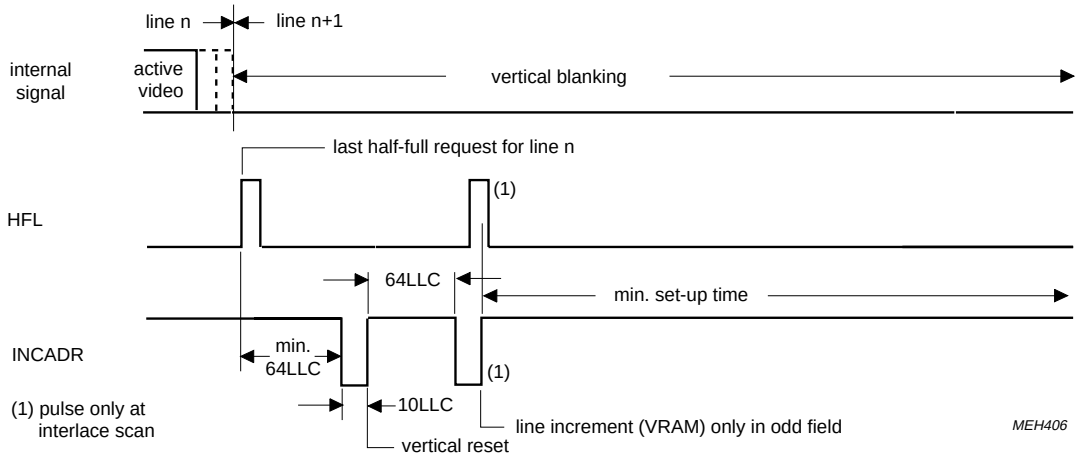


Fig.6 Vertical reset timing to the VRAM.

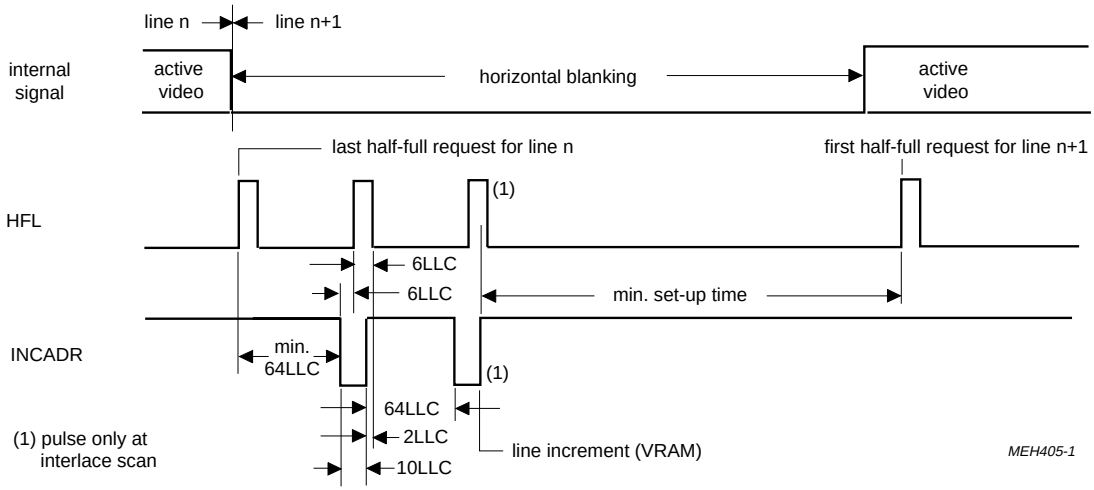


Fig.7 Horizontal increment timing to the VRAM.

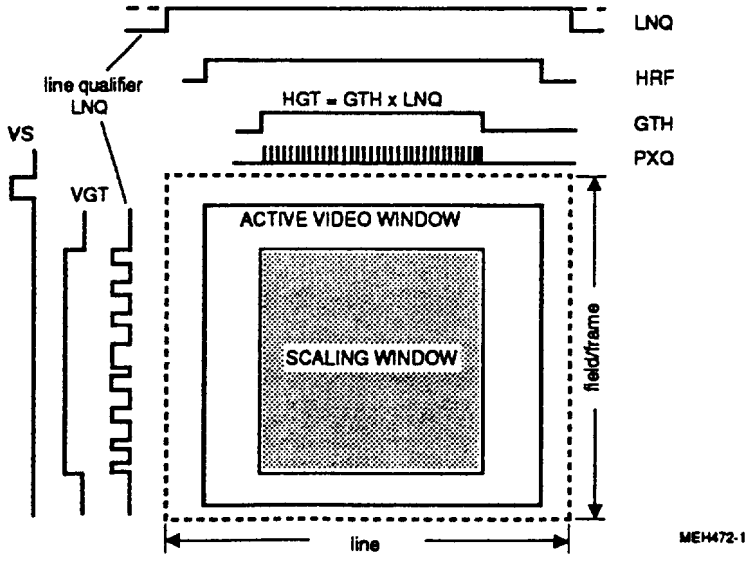


Fig.8 Reference signals for scaling window.

7.13 Field processing

The phase of the field sequence (odd/even dependent on inputs HREF and VS) is detected by means of the falling edge of VS. The current field phase is reported in the status byte by the OEF bit (Table 5). OEF bit can be stable 0 or 1 for non-interlaced input frames or non standard input signals VS and/or HREF (nominal condition for VS and HREF – SAA7191 B with active vertical noise limiter). A free-running odd/even flag is generated for internal field processing if the detection reports a stable OEF bit.

The POE bit (subaddress 0B) can be used to change the polarity of the internal flag (in case of non-standard VS and HREF signals) to control the phase of the free-running flag, and to compensate mis-detections. Thus, the SAA7186 can be used under various VS/HREF timing conditions.

The SAA7186 operates on fields. To support progressive displays and to avoid movement blurring and artifacts, the circuit can process both or single fields of interlaced or non-interlaced input data. Therefore the OF bits can be used. The bits OF1 and OF0 (Table 6) determine the INCADR/HFL generation in “data burst transfer mode”. One of the fields (odd or even) is ignored when OF1 = 1; then no line increment sequence (INCADR/HFL) is generated, the vertical reset pulse is only generated.

With OF1 = OF0 = 0 the circuit supports correct interlaced data storage. Two INCADR/HFL sequences are generated in each qualified line; additionally an INCADR/HFL sequence after the vertical reset sequence of an odd field is generated. Thereby, the scaled lines are automatically stored in the right sequence.

8 OPERATION CYCLE

The operation is synchronized by the input field. The cycle is specified in the flow chart (Fig.9).
The circuit is inactive after power-on reset, VPO is 0 and the FIFO control is set “empty”. The internal control registers are updated with the falling edge of VS signal. The circuit is switched active and waits for a transmission of VS and a vertical reset sequence to the memory controller. Afterwards, the circuit waits for the beginning of a scaling or bypass region. The processing of a current line is finished when a vertical sync pulse appears. The circuit performs a coefficient update and generates a new vertical reset (if it is still active).

Line processing starts when a line is decided to be active, the circuit starts to scale it. Active pixels are loaded into the FIFO register. An HFL flag is generated to initialize a data transfer when eight words are completed. The line end is reached when the programmed pixel number is processed or when a horizontal sync pulse occurs. If there are pixels in the FIFO register, it is filled up until it is half-full to cause a data transfer. Horizontal increment pulses are transmitted after this data transfer.

Remarks:
The SAA7186 will always wait for the HREF/VS pulse before the line increment/vertical reset sequence is performed. After each line/field, the FIFO control is set to empty when INCADR/HFL sequence is transmitted.
No additional actions are necessary if the memory controller has ignored the HFL signal. There is no need to handle overflow/underflow of the FIFO register.

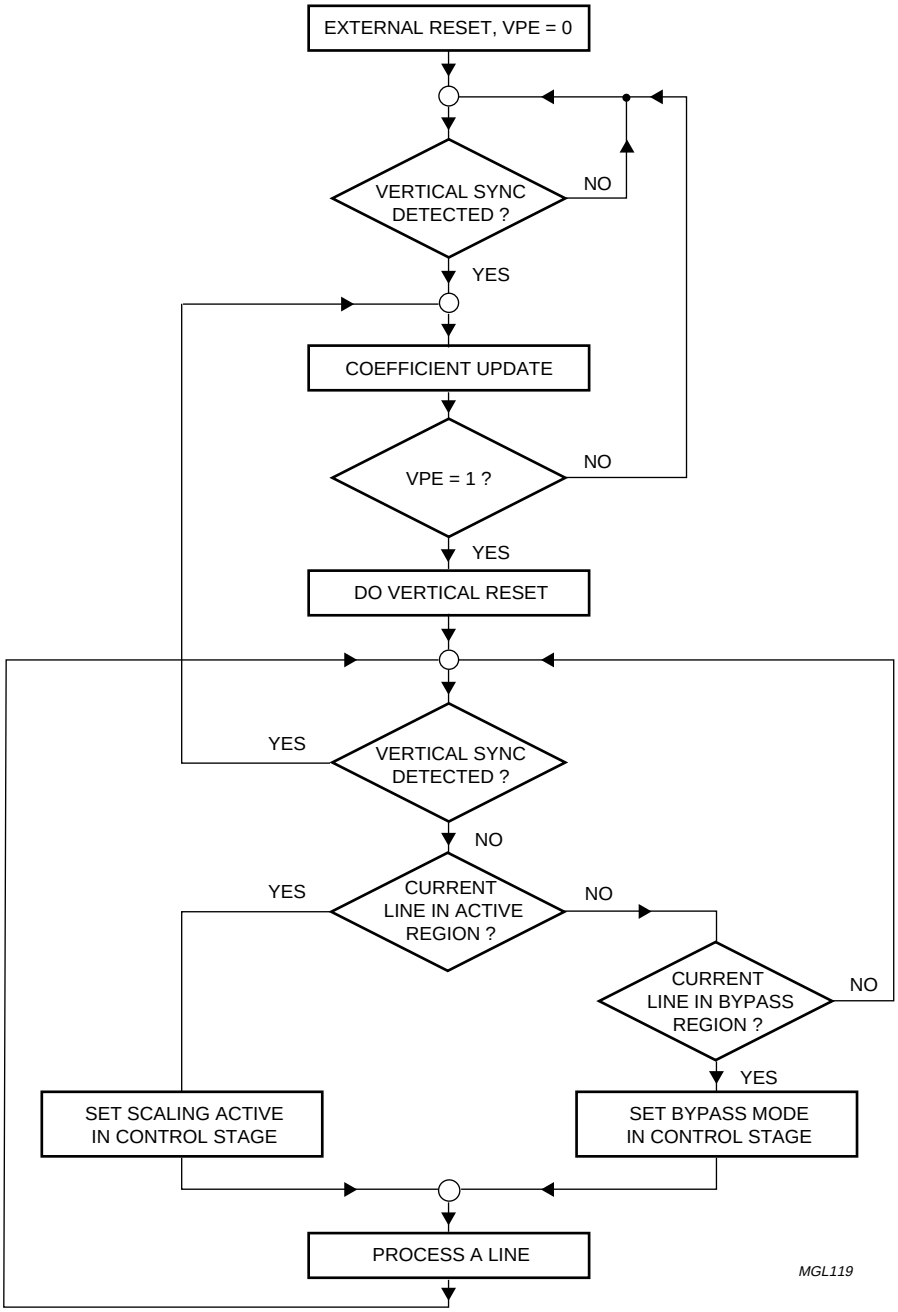


Fig.9 Operation cycle

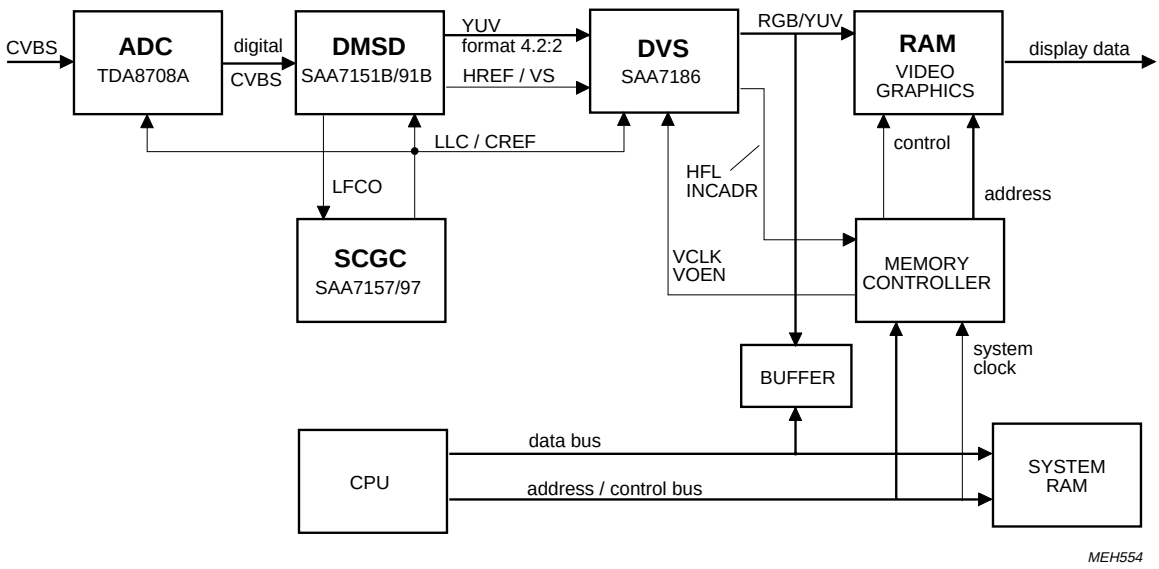


Fig.10 SAA7186 system configuration in Data Burst Transfer Mode (TTR = , VCLK = continuous).

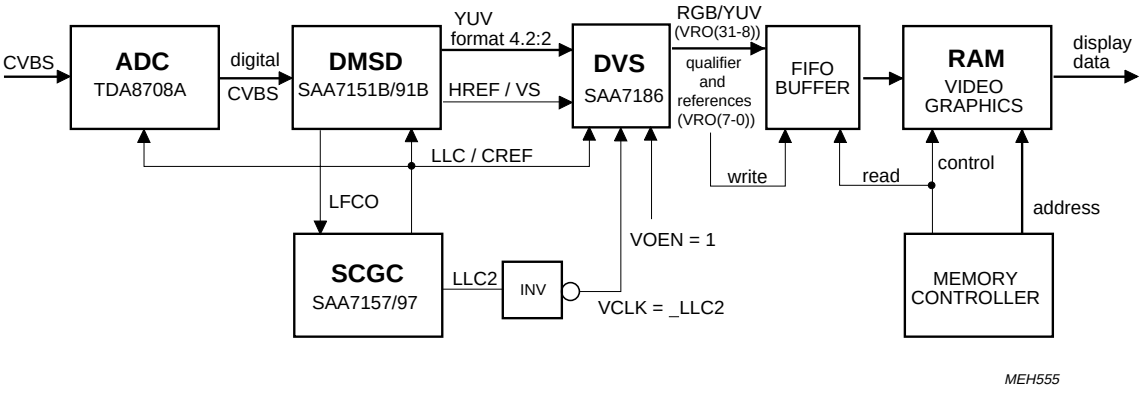


Fig.11 SAA7186 system configuration in Transparent Data Transfer Mode (TTR = 1, EFE = 1, VCLK = continuous (_LLC2)).

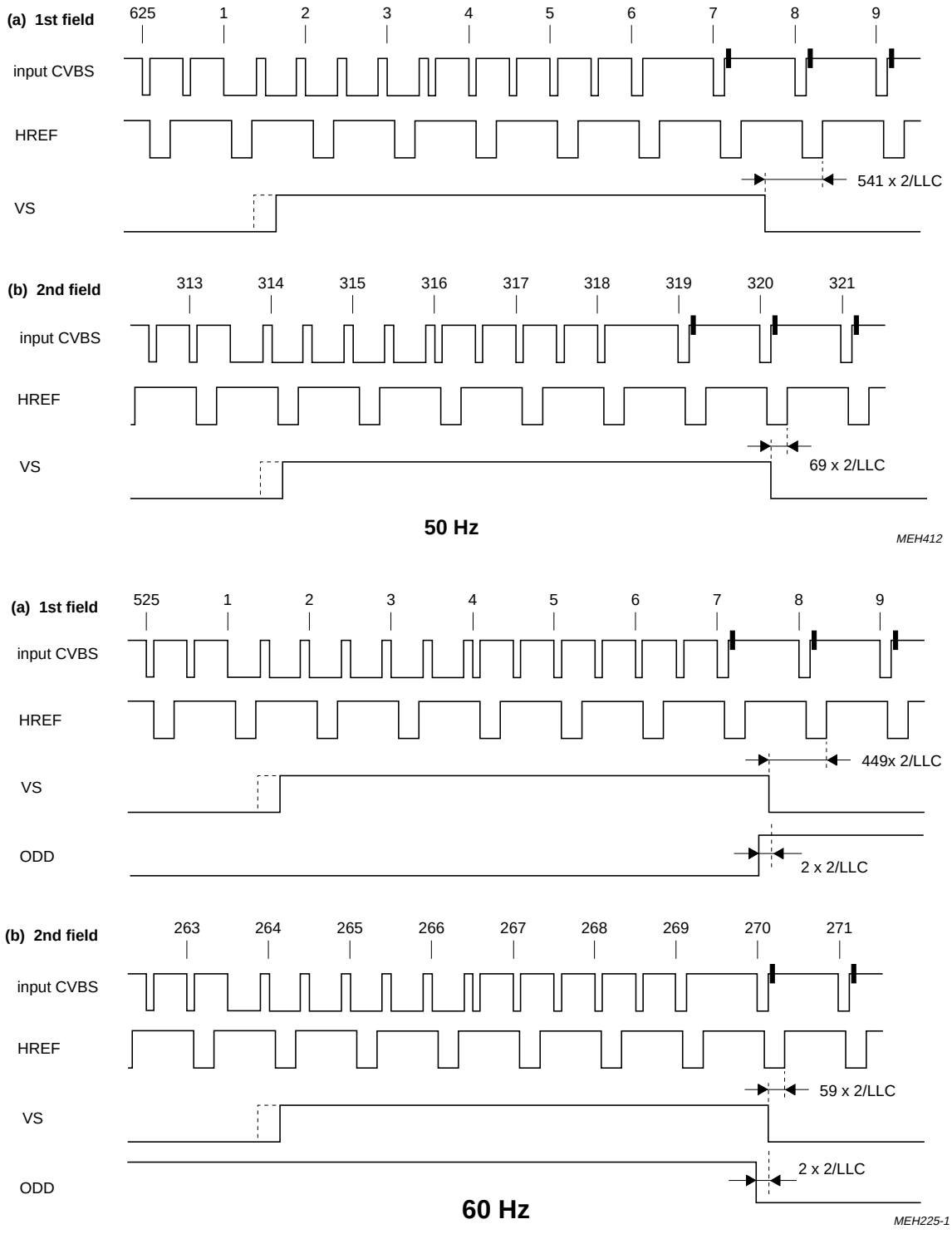


Fig.12 VS timing for video input source SAA7191B.

9 I²C-BUS FORMAT

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA0	A		DATAn	A	P

S	=	start condition
SLAVE ADDRESS	=	1011 100X (IICSA = LOW) or 1011 110X (IICSA = HIGH)
A	=	acknowledge, generated by the slave
SUBADDRESS(1)	=	subaddress byte (Table 4)
DATA	=	data byte (Table 4)
P	=	stop condition
X	=	read/write control bit X = 0, order to write (the circuit is slave receiver) X = 1, order to read (the circuit is slave transmitter)

Note

1. If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Table 4 I^2C-bus; subaddress and data bytes for writing (X in address byte = 0).

FUNCTION	SUBADDRESS	DATA								DF[1]
		D7	D6	D5	D4	D3	D2	D1	D0	
Formats and sequence	00	RTB	OF1	OF0	VPE	LW1	LW0	FS1	FS0	tbf
Output data pixel/line	01	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0	
continued in	04							XD9	XD8	
Input data pixel/line	02	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
continued in	04					XS9	XS8			
Horizontal window start	03	XO7	XO6	XO5	XO4	XO3	XO2	XO1	XO0	
Pixel decimation filter	04	HF2	HF1	HF0	XO8	XS9	XS8	XD9	XD8	
Output data lines/field	05	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0	
continued in	09							YD9	YD8	
Input data lines/field	06	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
continued in	09					YS9	YS8			
Vertical window start	07	YO7	YO6	YO5	YO4	YO3	YO2	YO1	YO0	
AFS/vertical processing	08	AFS	VP1	VP0	YO8	YS9	YS8	YD9	YD8	
Vertical bypass start	09	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0	
continued in	0B				VS8					
Vertical bypass count	0A	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0	
continued in	0B	TCC	0	0	VS8	0	VC8	0	POE	
Chroma keying										
lower limit for V	0C	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	
upper limit for V	0D	VU7	VU6	VU5	VU4	VU3	VU2	VU1	VU0	
lower limit for U	0E	UL7	UL6	UL5	UL4	UL3	UL2	UL1	UL0	
upper limit for U	0F	UU7	UU6	UU5	UU4	UU3	UU2	UU1	UU0	
Byte 10[2]	10	0	0	0	MCT	QPL	QPP	TTR	EFE	
Unused	11 to 1F									

Notes

1. Default register contents fill in by hand
2. Byte 10 is set to 00h after power-on reset.

Table 5 I^2C-bus status byte (X in address byte = 1)

FUNCTION		DATA							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
status byte		ID3	ID2	ID1	ID0	0	0	OEF	SVP

Function of status bits:

ID3 to ID0 Software version of SAA7186 compatible with

ID3	ID2	ID1	ID0	version
0	0	0	1	1

OEF Identification of field sequence dependent on inputs HREF and VS:
0 = even field detected; 1 = odd field detected

SVP State of VRAM port: 0 = inputs HFL and INCADR inactive;
1 = inputs HFL and INCADR active.

Table 6 Function of the register bits of Table 4

"00" RTB	ROM table bypass switch: 0 = anti-gamma ROM active 1 = table is bypassed
OF1 to OF0	Set output field mode: OF1 OF0 field mode DVS process 0 0 both fields for interlaced storage 0 1 both fields for non-interlaced storage 1 0 odd fields only (even fields ignored) for non-interlaced storage 1 1 even fields only (odd fields ignored) for non-interlaced storage
VPE	VRAM port outputs enable: 0 = HFL and INCADR inactive; VRO outputs in 3-state position (HFL = LOW, INCADR = HIGH) 1 = HFL and INCADR enabled; VRO outputs dependent on VOEN
LW1 to LW0	First pixel position in VRO data for FS1 = 0; FS0 = 0 (RGB) and FS1 = 0; FS0 = 1 (YUV): LW1 LW0 31 to 24 23 to 16 15 to 8 7 to 0 0 0 pixel 0 pixel 0 pixel 1 pixel 1) 0 1 pixel 0 pixel 0 pixel 1 pixel 1) EFE = 0, TRR = 0 1 0 black black pixel 0 pixel 0) 1 1 black black pixel 0 pixel 0) First pixel position in VRO data for FS1 = 1; FS0 = 1 (monochrome): LW1 LW0 31 to 24 23 to 16 15 to 8 7 to 0 0 0 pixel 0 pixel 1 pixel 2 pixel 3) 0 1 black pixel 0 pixel 1 pixel 2) EFE = 0, TRR = 0 1 0 black black pixel 0 pixel 1) 1 1 black black black pixel 0) 0 0 pixel 0 pixel 1 X X) EFE = 1, TRR = 0; 0 1 black pixel 0 X X) LW only effects 1 0 pixel 0 pixel 1 X X) greyscale format 1 1 black pixel 0 X X)

<table>
<tr><td>FS1 to FS0</td><td>FIFO output register format select (EFE-bit see “10”):
<table>
<tr><th>EFE</th><th>FS1</th><th>FS0</th><th>output format (Tables 2 and 3)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>RGB 5-5-5 + alpa; 2×16-bit/pixel; 32-bit word length;
RGB matrix on, VRAM output format</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>YUV 4:2:2; 2×16-bit/pixel; 32-bit word length;
RGB matrix off, VRAM output format</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>YUV 4:2:2; video test mode; 1×16-bit/pixel; 16-bit word length;
RGB matrix off, optional output format</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>monochrome mode; 4×8-bit/pixel; 32-bit word length;
RGB matrix off, VRAM output format</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>RGB 5-5-5 + alpa; 1×16-bit/pixel; 16-bit word length;
RGB matrix on, VRAM output + transparent format</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>YUV 4:2:2 + alpa; 1×16-bit/pixel; 16-bit word length;
RGB matrix off, VRAM output + transparent format</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>RGB 8-8-8 + alpa; 1×24-bit/pixel; 24-bit word length;
RGB matrix on, VRAM output + transparent format</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>monochrome mode; 2×8-bit/pixel; 16-bit word length;
RGB matrix off, VRAM output + transparent format</td></tr>
</table></td></tr>
<tr><td>“01 and 04”
XD9 to XD0</td><td>Pixel number per line (straight binary) on output (VRO):
00 0000 0000 to 11 1111 1111 (number of XS pixels as a maximum)</td></tr>
<tr><td>“02 and 04”
XS9 to XS0</td><td>Pixel number per line (straight binary) on inputs (YIN and UVIN):
00 0000 0000 to 11 1111 1111 (number of input pixels per line as maximum)</td></tr>
<tr><td>“03 and 04”
XO8 to XO0</td><td>Horizontal start position (straight binary) of scaling window (take care of active pixel number per line).
start with 1st pixel after HREF rise = 0 0001 0000 to 1 1111 1111 (010 to 1FF)

window start and window end may be cut by internal delay compensated HREF = 0 phase. XO has to be matched to the internal processing delay to get full scaling range</td></tr>
</table>

<table>
<tr><td>“04”
HF2 to HF0</td><td>Horizontal decimation filter (Figures 13 and 14):
<table>
<tr><th>HF2</th><th>HF1</th><th>HF0</th><th>taps</th><th>filter</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>2</td><td>filter 1 (1/2 (1 + z^{-1}))</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>3</td><td>filter 2 (1/4 (1 + $2z^{-1}$ + z^{-2}))</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>5</td><td>filter 3 (1/8 (1 + $2z^{-1}$ + $2z^{-2}$ + $2z^{-3}$ + z^{-4}))</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>9</td><td>filter 4 (1/16 (1 + $2z^{-1}$ + $2z^{-2}$ + $2z^{-3}$ + $2z^{-4}$ + $2z^{-5}$ + $2z^{-6}$ + $2z^{-7}$ + z^{-8}))</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>filter bypassed</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>filter bypassed + delay in Y channel of 1T</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>8</td><td>filter 5 (1/16 (1 + $3z^{-1}$ + $3z^{-2}$ + z^{-3} + z^{-4} + $3z^{-5}$ + $3z^{-6}$ + z^{-7}))</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4</td><td>(1/8 (1 + $3z^{-1}$ + $3z^{-2}$ + z^{-3}))</td></tr>
</table></td></tr>
<tr><td>“05 and 08”
YD9 to YD0</td><td>Line number per output field (straight binary):
00 0000 0000 to 11 1111 1111 (number of YS lines as a maximum)</td></tr>
<tr><td>“06 and 08”
YS9 to YS0</td><td>Line number per input field (straight binary):
00 0000 0000 0 line
11 1111 1111 1023 lines (maximum = number of lines/field – 3)</td></tr>
<tr><td>“07 and 08”
YO8 to YO0</td><td>Vertical start of scaling window. “0” equals 3rd line after rising slope of VS input signal. Take care of active line number per field (straight binary).
0 0000 0000 start with 3rd line after the rising slope of VS
0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B)
1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)</td></tr>
<tr><td>“08”
AFS
VP1 to VP0</td><td>Adaptive filter switch: 0 = off; use VP1, VP0 and HF2 to HF0 bits
1 = on; filter characteristics are selected by the scaler
Vertical data processing
<table>
<tr><th>VP1</th><th>VP0</th><th>processing</th></tr>
<tr><td>0</td><td>0</td><td>bypassed</td></tr>
<tr><td>0</td><td>1</td><td>delay of one line H(z) = z^{-H}</td></tr>
<tr><td>1</td><td>0</td><td>vertical filter 1: (H(z) = 1/2 (1 + z^{-H}))</td></tr>
<tr><td>1</td><td>1</td><td>vertical filter 2: (H(z) = 1/4 (1 + $2z^{-H}$ + z^{-2H}))</td></tr>
</table></td></tr>
<tr><td>“09 and 0B”
VS8 to VS0</td><td>Vertical bypass start, sets begin of the bypass region (straight binary). Scaling region overrides bypass region (YO bits):
0 0000 0000 start with 3rd line after the rising slope of VS
0 0000 0011 start with 1st line after the falling slope of nominal VS (SAA7151B/91B)
1 1111 1111 511 + 3 lines after the rising slope of VS (maximum value)</td></tr>
</table>

"0A and 0B" VC8 to VC0	Vertical bypass count, sets length of bypass region (straight binary): 00 0000 0000 0 line length 11 1111 1111 511 lines length (maximum = number of lines/field – 3)
TCC	Two's complement input data select (U, V): 0 = binary input data 1 = two's complement input data
POE	Polarity, internally detected odd/even flag O/E: 0 = flag unchanged; 1 = flag inverted
"0C" VL7 to VL0	Set lower limit for V colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0D" VU7 to VU0	Set upper limit for V colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0E" UL7 to UL0	Set lower limit for U colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level
"0F" UU7 to UU0	Set upper limit for U colour-difference signal (8 bit; two's complement): 1000 0000 as maximum negative value = –128 signal level 0000 0000 limit = 0 0111 1111 as maximum positive value = +127 signal level

“10” MCT	Monochrome and two’s complement output data select: 0 = inverse greyscale luminance (if greyscale is selected by FS bits) or straight binary U, V data output 1 = non-inverse monochrome luminance (if greyscale is selected by FS bits) or two’s complement U, V data output
QPL	Line qualifier polarity flag : 0 = LNQ is active-LOW (pin 1 and on VRO1, pin 99); 1 = LNQ is active-HIGH
QPP	Pixel qualifier polarity flag : 0 = PXQ is active-LOW (VRO0, pin 100); 1 = PXQ is active-HIGH
TTR	Transparent data transfer: 0 = normal operation (VRAM protocol valid,) 1 = FIFO register transparent (output FIFO in shift register mode)
EFE	Extended formats enable, FS-bits in subaddress “00”

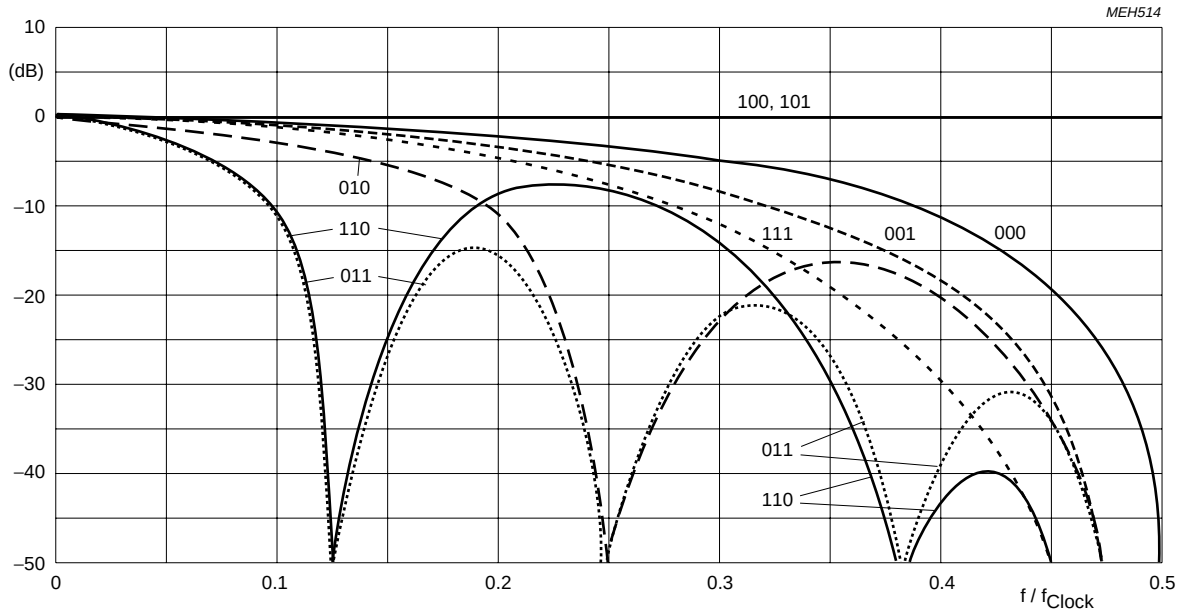


Fig.13 Horizontal frequency characteristic of luminance signal (Y) dependent on HF2 to HF0 bits (subaddress 04).

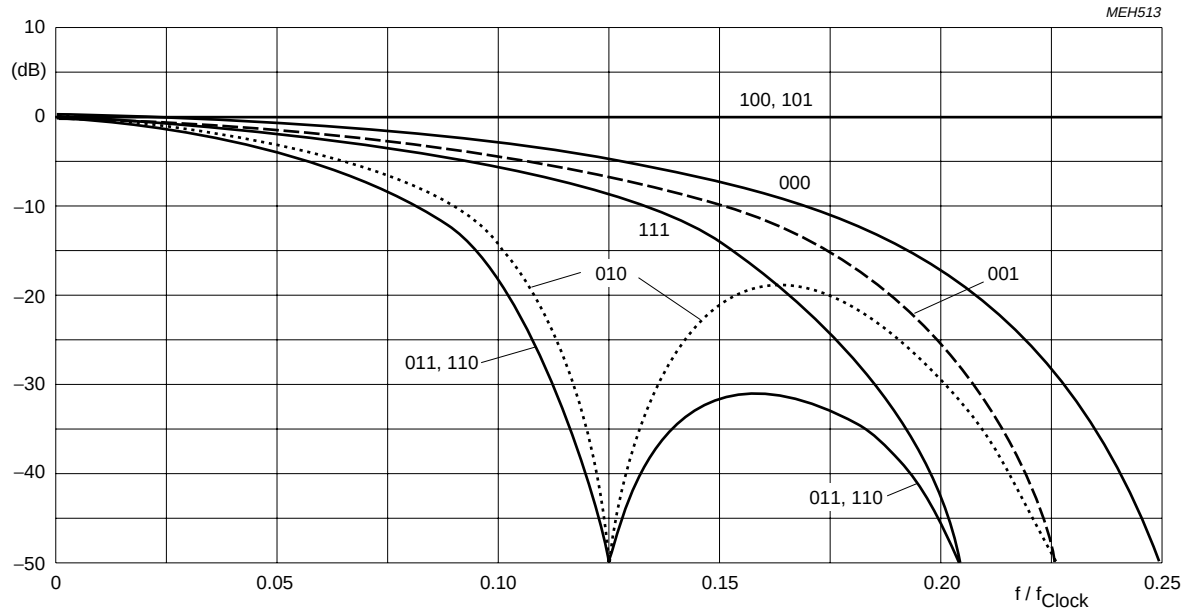


Fig.14 Horizontal frequency characteristic of chrominance signals (UV) without UV interpolation dependent on HF2 to HF0 bits (subaddress 04).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pins 5, 14, 26, 40, 55, 67, 76 and 91)	–0.5	6.5	V
V_I	DC input voltage on all pins	–0.5	V_{DD}	V
I_{DD}	supply current (pins 5, 14, 26, 40, 55, 67, 76 and 91)	–	70	mA
P_{tot}	total power dissipation	0	1	W
T_{stg}	storage temperature range	–65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling(1) for all pins	–	±2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

11 DC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range (pins 5, 14, 26, 40, 55, 67, 76 and 91)		4.5	5	5.5	V
I_P	total supply current ($I_{DD1} + I_{DD2} + I_{DD3} + I_{DD4} + I_{DD5} + I_{DD6} + I_{DD7} + I_{DD8}$)	inputs LOW and outputs without load	–	80	–	mA
Data and control inputs						
$V_{I\,L}$	input voltage LOW		–0.5	–	0.8	V
$V_{I\,H}$	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	$V_{I\,L}$ = 0	–	–	10	µA
C_I	input capacitance	data	–	–	8	pF
		clocks	–	–	10	pF
Data and control outputs						
$V_{O\,L}$	output voltage LOW	note 1	–	–	0.6	V
$V_{O\,H}$	output voltage HIGH	note 1	2.4	–	–	V
3-state outputs						
$I_{O\,off}$	high-impedance output current		–	–	±5	µA
C_O	high-impedance output capacitance		–	–	8	pF
I²C-bus, SDA and SCL (pins 44 and 45)						
$V_{I\,L}$	input voltage LOW		–0.5	–	1.5	V
$V_{I\,H}$	input voltage HIGH		3	–	V_{DD}+0.5	V
$I_{44, 45}$	input current		–	–	±10	µA
I_{ACK}	output current on pin 44	acknowledge	3	–	–	mA
$V_{O\,L}$	output voltage at acknowledge	I_{44} = 3 mA	–	–	0.4	V

12 AC CHARACTERISTICS

V_{DD1} to V_{DD8} = 4.5 to 5.5 V; T_{amb} = 0 to 60 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LLC timing (pin 36)		Fig.11				
t_{LLC}	cycle time		31	–	45	ns
t_p	pulse width (duty factor)	$t_{LLC\,H}$ / t_{LLC}	40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
Input data and CREF timing		Fig.15				
t_{SU}	setup time		11	–	–	ns
t_{HD}	hold time		3	–	–	ns
VCLK timing (pin 51)		Fig.16				
t_{VCLK}	VRAM port clock cycle time	note 2	50	–	200	ns
$t_{p\,L}$, $t_{p\,H}$	LOW and HIGH times	note 3	17	–	–	ns
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
Output data and reference signal timing		Figures 15 and 16				
C_L	load capacitance	VRO outputs	15	–	40	pF
		other outputs	7.5	–	25	pF
t_{OH}	VRO data hold time	C_L = 10 pF; note 4	0	–	–	ns
t_{OHL}	related to LLC (INCADR, HFL)	C_L = 10 pF; note 5	0		–	ns
t_{OHV}	related to VCLK (HFL)	C_L = 10 pF; note 5	0		–	ns
t_{OD}	VRO data delay time	C_L = 40 pF; note 4	–	–	25	ns
t_{ODL}	related to LLC (INCADR, HFL)	C_L = 25 pF; note 5	–	–	60	ns
t_{ODV}	related to VCLK (HFL)	C_L = 25 pF; note 5	–	–	60	ns
t_D	output disable time to 3-state	C_L = 40 pF; note 6	–	–	40	ns
t_E	output enable time from 3-state	C_L = 40 pF; note 6	–	–	40	ns
$t_{HFL\,VOE}$	HFL maximum response time	VRAM port enabled	–	–	810	ns
$t_{HFL\,VCLK}$	HFL maximum response time	HFL set at beginning of VCLK burst	–	–	840	ns

Notes

1. Levels are measured with load circuit. VRO outputs with 1.2 kΩ in parallel to 25 pF at 3 V (TTL load).
2. Maximum t_{VCLK} = 200 ns for test mode only. The applicable maximum cycle time depends on data format, horizontal scaling and input data rate.
3. Measured at 1,5 V level; $t_{p\,L}$ may be unlimited.
4. Timings of VRO refer to the rising edge of VLCK.
5. The timing of INCADR refers to LLC; the rising edge of HFL always refers to LLC. During a VRAM transfer is the falling edge of HFL generated by VCLK. Both edges of HFL refer to LLC during horizontal increment and vertical reset cycles.
6. Asynchronous signals with timing referring to the 1.5 V switching point of VOEN input signal (pin 50).

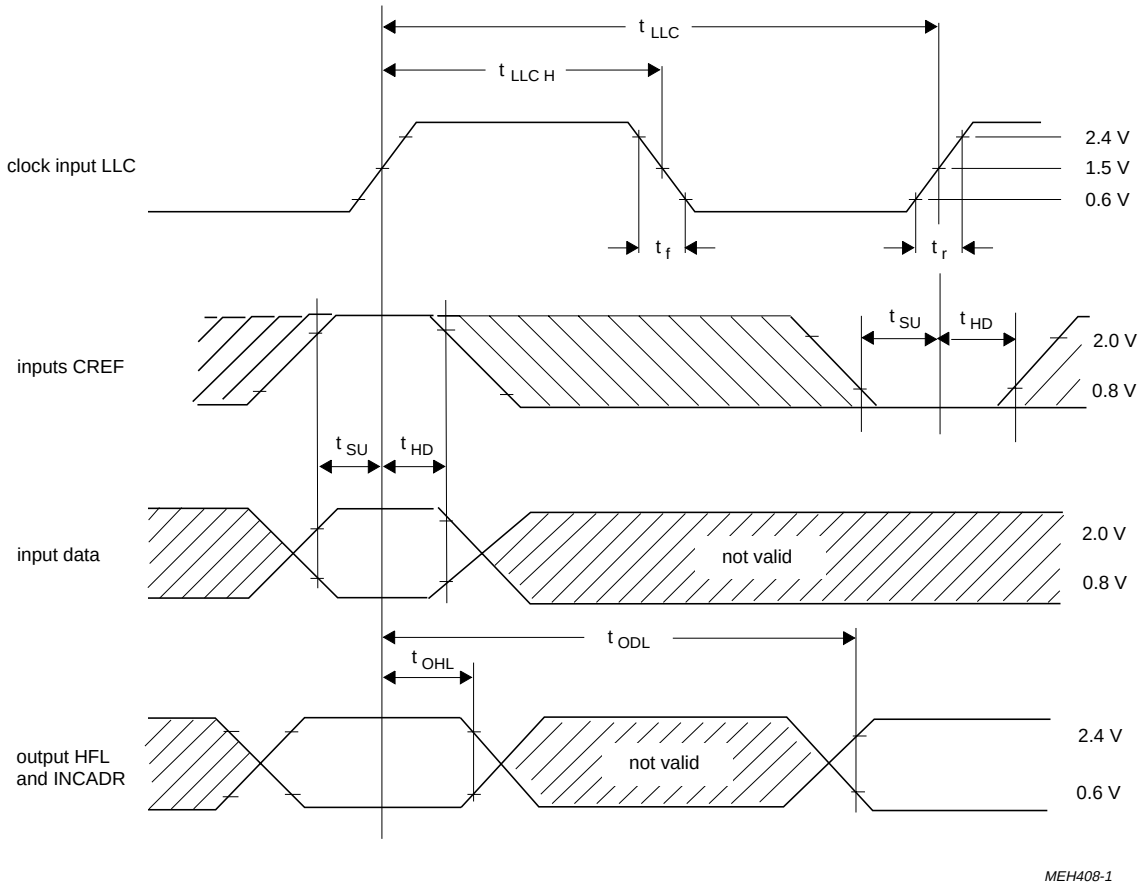


Fig.15 Data input timing (LLC).

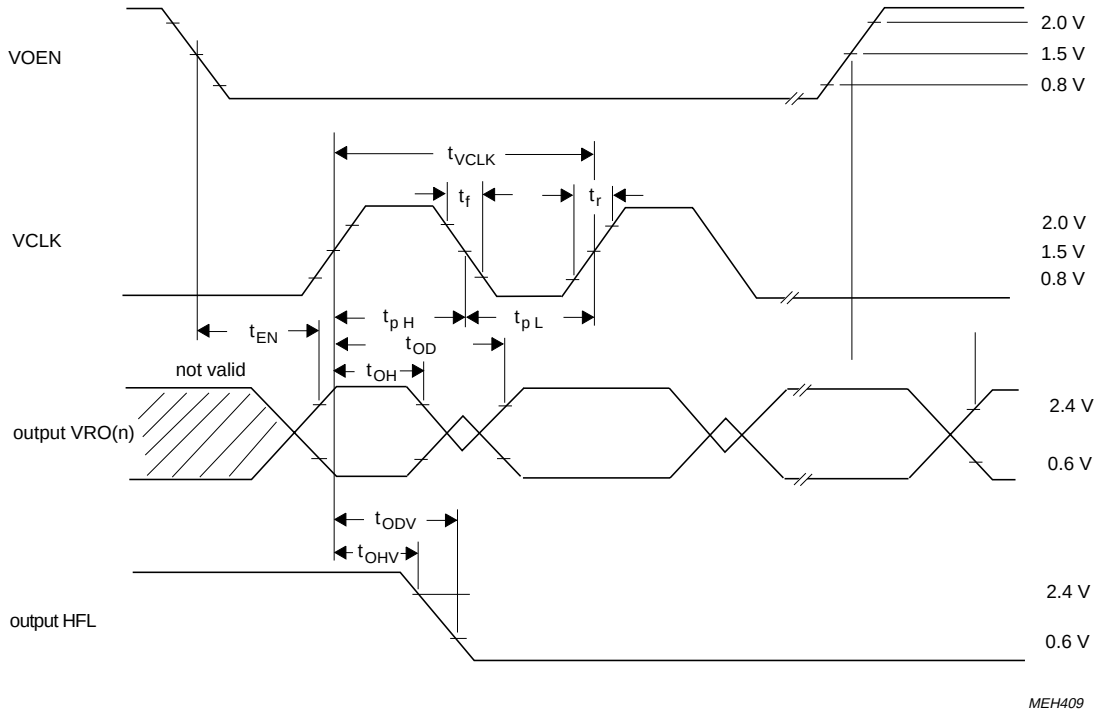


Fig.16 Data output timing (VCLK).

13 PROCESSING DELAYS

PORTS	DELAY IN LLC	REMARKS
YIN to VRO	58	in transparent mode only
UVIN to VRO	58	in transparent mode only
HREF to VRO	58	in transparent mode only

14 PROGRAMMING EXAMPLE

Slave address byte is B8h at pin IICSA = 0 (or BCh at pin IICSA = +5 V).

This example shows the setting via I^2C-bus for the processing of a picture segment at 1:1 horizontal and vertical scale.

Values in brackets [..]:
If no scaling or panning is wanted,
the parameters XD, XS, YD and YS should be set to the maximum value 3FFh.
the parameters XO and YO should be set to the minimum value 000h.
(in this case, HREF and VS from external define the SAA7186 processing window).

SUBADDR. (HEX)	BITS	FUNCTION	VALUE (HEX)	COMMENT
00	RTB, OF(1:0), VPE, LW(1:0), FS(1:0),	ROM table control and field sequence processing; VRAM port enable; output format select	11	(1)
01	XD(7:0)	LSB's output pixel/line	80 [FF]	384 pixels out
02	XS(7:0)	LSB's input pixel/line	80 [FF]	384 pixels in
03	XO(7:0)	LSB's for horizontal window start	10 [00]	1st pixel after HREF = 1
04	HF(2:0), XO(8), XS(9, 8), XD(9, 8)	horizontal filter select and MSB's of subaddresses 01, 02, 03	85 [8F]	horizontal filter bypassed
05	YD(7:0)	LSB's output lines/field	90 [FF]	144 lines out
06	YS(7:0)	LSB's input lines/field	90 [FF]	144 lines in
07	YO(7:0)	LSB's vertical window start	03 [00]	1st line after VS = 0; (2)
08	AFS, VP(1:0), YO(8), YS(9, 8), YD(9, 8)	adaptive and vertical filter select; MSB's of subaddresses 05, 06, 07	00 [FF]	no adaptive select vertical filter bypassed
09	VS(7:0)	LSB's vertical bypass start position	00	not bypassed
0A	VC(7:0)	LSB's vertical bypass lines/field	00	region
0B	VS(8), VC(8), TCC, POE	MSB's of subaddresses 09, 0A; UV input data representation and odd/even polarity switch	00	defined; (3) (4)
0C	VL(7:0)	UV keyer: lower limit V (R-Y)	00	) keying is switched off
0D	VU(7:0)	UV keyer: upper limit V (R-Y)	FF	) by VU < VL
0E	UL(7:0)	UV keyer: lower limit U (B-Y)	00	-
0F	UU(7:0)	UV keyer: upper limit U (B-Y)	00	-
10	MCT, QPP, QPL, TTR, EFE	Y or UV output data representation, output data transfer mode, pixel/ line qualifier polarity.	00	(5)

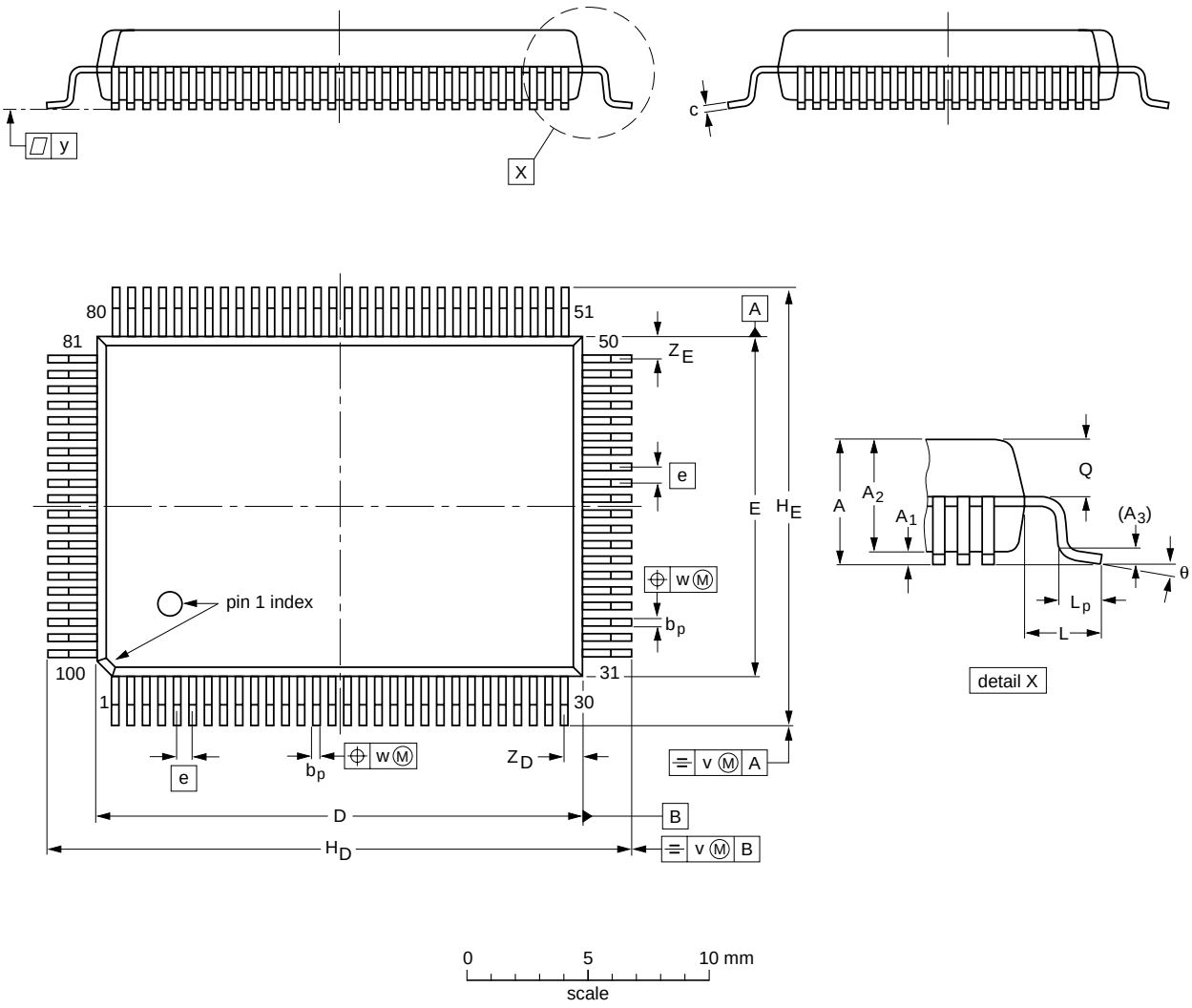
Notes

1. RTB = 0 ROM table is active (only for RGB formats)
   OF = 00 SAA7186 processes the both fields for interlaced display
   VPE = 1 VRAM port is enabled
   LW = 00 longword position of first pixel in each output line = 0
   FS = 01 16-bit 4:2:2 YUV output format is selected
2. for nominal VS length of 6 × H-period (input SAA7191B respectively SAA7151B with active VNL)
3. TTC = 0 straight binary UV input data expected

4. odd/even polarity unchanged - can be used to change the field sequence if phase relations between HREF and VS are not according to SAA7191B respectively SAA7151B specification
5. MCT = 0 when EFE, FS = 001h: UV output data are straight binary
   QPP = 0 the pixel qualifier PXQ is “0”-active (if TTR, EFE = 1)
   QPL = 0 line qualifier LNQ is “0”-active (if TTR, EFE = 1)
   TTR = 0 VRAM port is set to data burst transfer
   EFE = 0 32-bit longword formats selected.

15 PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~92-11-17~~ 95-02-04

16 SOLDERING

16.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

16.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

16.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

18 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

19 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Printed in The Netherlands 657027/00/01/pp44 Date of release: May 1993 Document order number: 9397 750 02436

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