INTEGRATED CIRCUITS

DATA SHEET

SAA7187
Digital video encoder (DENC2-SQ)

Preliminary specification
File under Integrated Circuits, IC22

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Philips Semiconductors

PHILIPS

Digital video encoder (DENC2-SQ) SAA7187

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency selectable for 12.27 MHz (60 Hz fields) or 14.75 MHz (50 Hz fields)
- 24-bit wide YUV input port or
- 16-bit wide YUV input port or
- Input data format Cb, Y, Cr, etc. (CCIR 656)
- I^2C-bus control port
- MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OSD overlay with Look-Up Tables (LUTs) 8×3 bytes
- Line 21 Closed Caption encoder
- Cross-colour reduction
- DACs operating at twice oversampling with 10-bit resolution
- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- CVBS and S-Video output simultaneously
- PLCC68 package.

GENERAL DESCRIPTION

The SAA7187 encodes digital YUV video data to an NTSC, PAL CVBS or S-Video signal.

The circuit accepts differently formatted YUV data with 640 or 768 active pixels per line. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family (Square Pixel).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	50	55	mA
I_{DDD}	digital supply current	–	175	210	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7187	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

BLOCK DIAGRAM

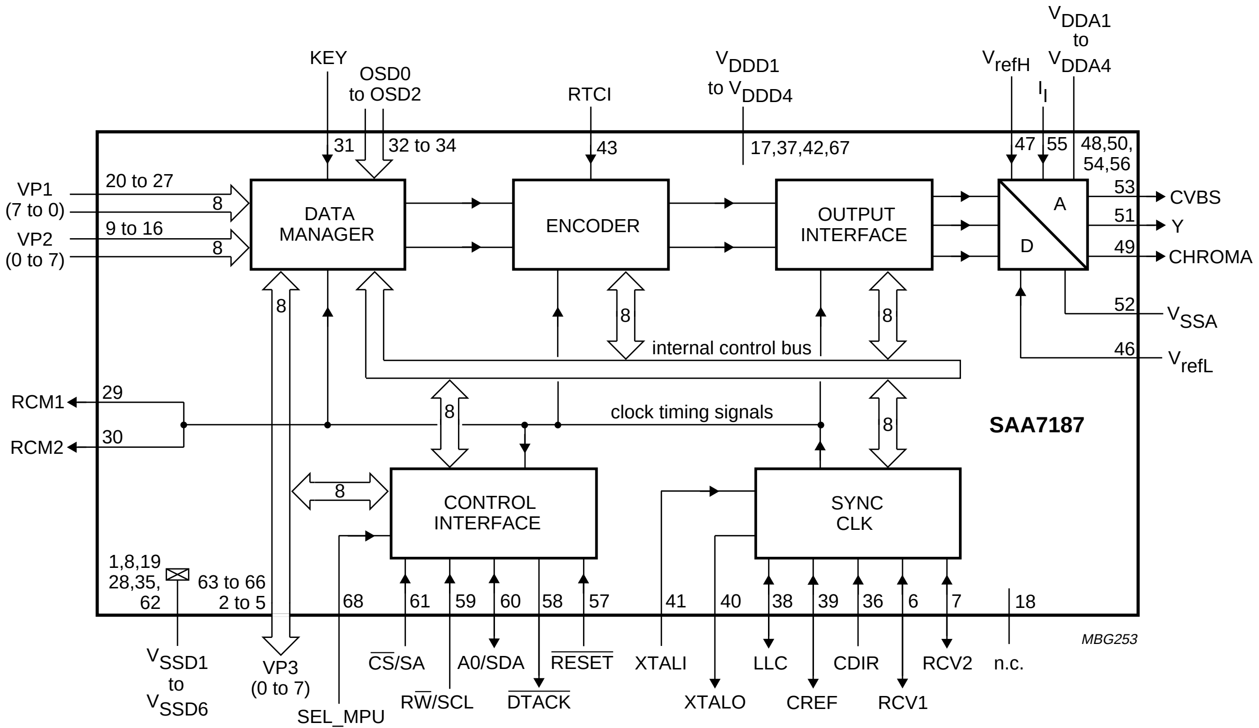


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1
VP3(4)	2	Upper 4 bits of the Video Port VP3. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, there can be multiplexed UV lines (422) or the U signal (444) of the Video input.
VP3(5)	3	
VP3(6)	4	
VP3(7)	5	
RCV1	6	Raster Control 1 for Video port. Depending on the synchronization mode, this pin receives/provides a VS/FS/FSEQ signal.
RCV2	7	Raster Control 2 for Video port. Depending on the synchronization mode, this pin receives/provides an HS/HREF/CBL signal.
V_{SSD2}	8	digital ground 2
VP2(0)	9	Video Port VP2. In 444 input mode, this is input for the V-signal.
VP2(1)	10	
VP2(2)	11	
VP2(3)	12	
VP2(4)	13	
VP2(5)	14	
VP2(6)	15	
VP2(7)	16	
V_{DDD1}	17	digital supply voltage 1
n.c.	18	reserved, do not connect
V_{SSD3}	19	digital ground 3
VP1(7)	20	Video Port VP1. This is an input for CCIR 656 compatible, multiplexed video data, or during other input modes, this is the Y-signal.
VP1(6)	21	
VP1(5)	22	
VP1(4)	23	
VP1(3)	24	
VP1(2)	25	
VP1(1)	26	
VP1(0)	27	
V_{SSD4}	28	digital ground 4
RCM1	29	Raster Control Master 1. This pin provides a VS/FS/FSEQ signal.
RCM2	30	Raster Control Master 2. This pin provides a programmable HS pulse.
KEY	31	Key signal for OSD. It is active HIGH.
OSD0	32	On-Screen Display data. This is the index for the internal OSD look-up table.
OSD1	33	
OSD2	34	
V_{SSD5}	35	digital ground 5
CDIR	36	Clock direction. If the CDIR input is HIGH, the circuit receives a clock signal, otherwise LLC and CREF are generated by the internal crystal oscillator.
V_{DDD2}	37	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
LLC	38	Line-Locked Clock. This is the 24.54 MHz or 29.5 MHz master clock for the encoder. The direction is set by the CDIR pin.
CREF	39	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
XTALO	40	Crystal oscillator output (to crystal).
XTALI	41	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
V_{DDD3}	42	digital supply voltage 3
RTCI	43	Real Time Control Input. If the clock is provided by an SAA7191B, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	Test pin. Connected to digital ground for normal operation.
SP	45	Test pin. Connected to digital ground for normal operation.
V_{refL}	46	Lower reference voltage input for the DACs.
V_{refH}	47	Upper reference voltage input for the DACs.
V_{DDA1}	48	Analog supply voltage 1 for the DACs and output amplifiers.
CHROMA	49	Analog output of the chrominance signal.
V_{DDA2}	50	Analog supply voltage 2 for the DACs and output amplifiers.
Y	51	Analog output of the luminance signal.
V_{SSA}	52	Analog ground for the DACs and output amplifiers.
CVBS	53	Analog output of the CVBS signal.
V_{DDA3}	54	Analog supply voltage 3 for the DACs and output amplifiers.
I_I	55	Current input for the output amplifiers, connect via a 15 kΩ resistor to V_{DDA}.
V_{DDA4}	56	Analog supply voltage 4 for the DACs and output amplifiers.
$\overline{RESET}$	57	Reset input, active LOW. After reset is applied, all outputs are in 3-state input mode. The I^2C-bus receiver waits for the START condition.
$\overline{DTACK}$	58	Data acknowledge output of the parallel MPU interface, active LOW, otherwise high impedance.
$R\overline{W}$/SCL	59	If pin 68 (SEL_MPU) is HIGH, this is the read/write signal of the parallel MPU interface, otherwise it is the I^2C-bus serial clock input.
A0/SDA	60	If pin 68 (SEL_MPU) is HIGH, this is the address signal of the parallel MPU interface, otherwise it is the I^2C-bus serial data input/output.
$\overline{CS}$/SA	61	If pin 68 (SEL_MPU) is HIGH, this is the chip select signal of the parallel MPU interface, otherwise it is the I^2C-bus slave address select pin. LOW: slave address = 88H, HIGH = 8CH.
V_{SSD6}	62	digital ground 6
VP3(0)	63	Lower 4 bits of the Video Port VP3. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, there can be multiplexed UV lines (422) of the U-signal (444) of the Video input.
VP3(1)	64	
VP3(2)	65	
VP3(3)	66	
V_{DDD4}	67	digital supply voltage 4
SEL_MPU	68	Select MPU interface input. If it is HIGH, the parallel MPU interface is active, otherwise the I^2C-bus interface will be used.

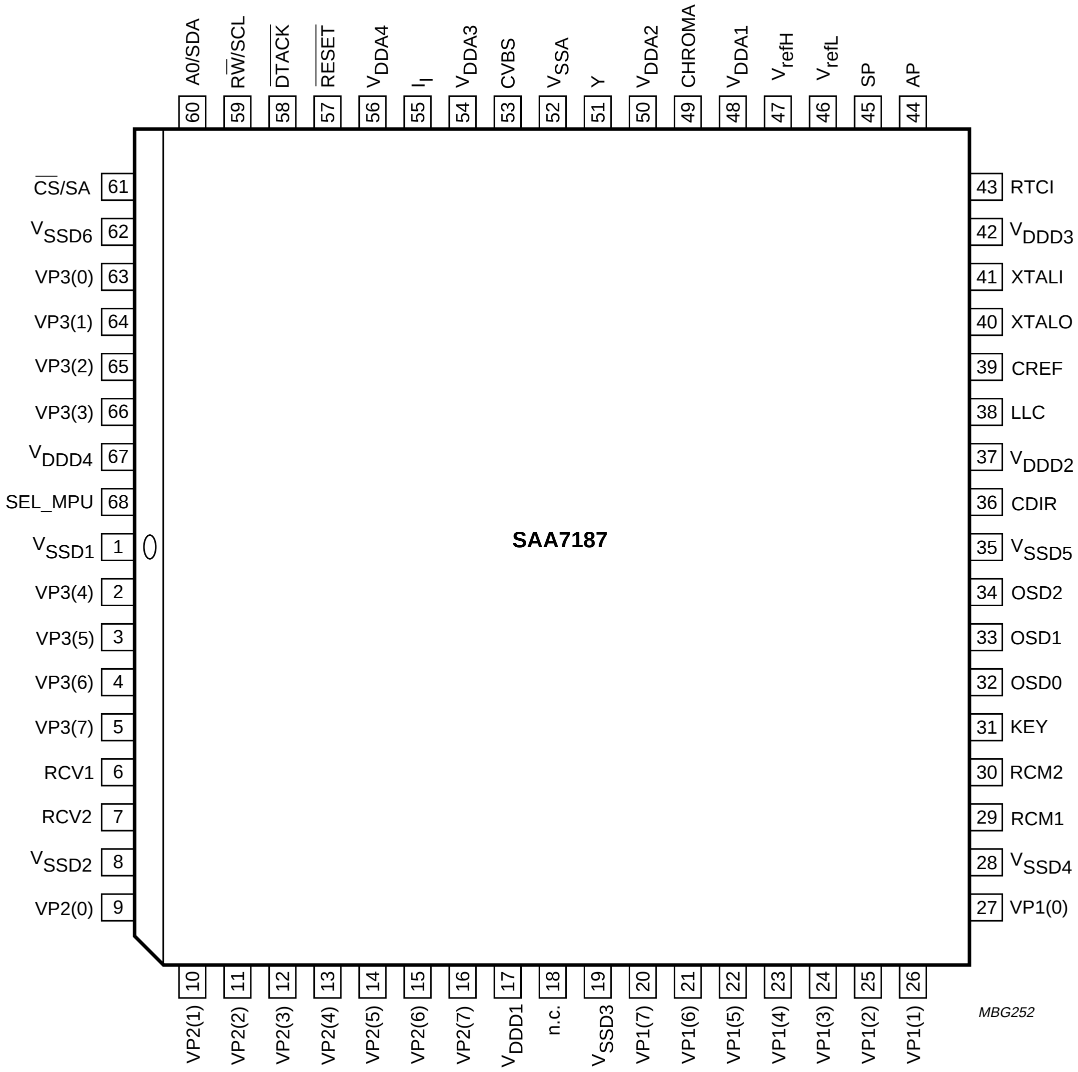


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The digital video encoder (DENC2-SQ) encodes digital luminance and chrominance into analog CVBS and simultaneously S-Video (Y/C) signals. NTSC-M and PAL B/G standards also sub-standards are supported.

The basic encoder function consists of subcarrier generation and colour modulation also insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements RS-170-A and CCIR 624.

For ease of analog post filtering the signals are twice oversampled with respect to pixel clock before digital-to-analog conversion.

For total filter transfer characteristics see Figs 3 to 6 for 60 Hz field rate, and Figs 7 to 10 for 50 Hz field rate. The DACs are realized with full 10-bit resolution. The encoder provides three 8-bit wide data ports, that serve different applications.

The VP1 port accepts 8 lines multiplexed Cb-Y-Cr data (CCIR 656 mode), or Y data only (444 mode).

The VP2 port accepts Cr data in 444 input mode.

The VP3 port accepts Cb data (444 input mode) or multiplexed Cb/Cr data (422 input mode). If not used for video input data, it can alternatively also handle the data of an 8-bit wide microprocessor interface.

Minimum suppression of output chrominance alias components approximately 1 MHz due to high frequency 444 input is better than 12 dB.

The 8-bit multiplexed Cb-Y-Cr formats are CCIR 656 (D1 format) compatible, but the SAV, EAV, etc. codes are not decoded.

A crystal-stable master clock (LLC) of 24.54 or 29.5 MHz, which is twice the line-locked pixel clock, needs to be supplied externally. Optionally, a crystal oscillator input/output pair of pins and an on-chip clock driver is provided. Additionally, a DMSD2 compatible clock interface, using CREF (input or output) and RTC (see *“data sheet SAA7191B”*) is available.

The DENC2-SQ synthesizes all necessary internal signals, colour subcarrier frequency, and synchronization signals, from that clock. DENC2-SQ can be timing master or slave.

The IC also contains Closed Caption and Extended Data Services Encoding (Line 21); it also supports OSD via KEY and three-bit overlay techniques by a 24×8 LUT.

The IC can be programmed via I^{2}C-bus or 8-bit MPU interface, but only one interface configuration can be active at a time; if 422 or 444 input format is being used, only the I^{2}C-bus interface can be selected.

A number of possibilities are provided for setting of different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the control interfaces to abort any running bus transfer and to set register 3AH to contents 00H, register 61H to contents 15H, and register 6CH to contents 00H. All other control registers are not influenced by a reset.

Data manager

In the data manager, the demultiplexing scheme is chosen in accordance with the input format.

Depending on hardware conditions (signals on pins KEY, OSD2 to OSD0), and software programming either data from the VP ports or from the OSD port are selected to be encoded to CVBS and Y/C signals.

Optionally, the OSD colour look-up tables located in this block, can be read out in a pre-defined sequence (8 steps per active video line), achieving e.g. a colour bar test pattern generator without need for an external data source. The colour bar function is only under software control.

Encoder

VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y/C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). After having been inserted a fixed synchronization level, in accordance with standard composite synchronization schemes, a variable blanking level, programmable also in a certain range, is inserted.

Transients of both synchronization pulses and start/stop of blanking are reduced compared to overall luminance bandwidth.

In order to enable easy analog post filtering, luminance is interpolated from square pixel data rate to twice that rate (24.54 or 29.5 MHz respectively), providing luminance in 10-bit resolution. For transfer characteristic of the luminance interpolation filter see Figs 5 and 6 for 60 Hz field rate and Figs 9 and 10 for 50 Hz field rate.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated correctly to 24.54 or 29.5 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y/C output. For transfer characteristics of the chrominance interpolation filter see Figs 3 and 4 for 60 Hz field rate and Figs 7 and 8 for 50 Hz field rate.

The amplitude of inserted burst is programmable in a certain range, suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in 10-bit resolution is provided on subcarrier.

The numeric ratio between Y and C outputs is in accordance with set standards.

CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of Closed Caption or Extended Data Service, delivered by the control interface, can be encoded (Line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

Data clock frequency is in accordance with definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption Data for 50 Hz field frequencies at 32 times horizontal line frequency.

Output interface

In the output interface encoded Y and C signals are converted from digital-to-analog in 10-bit resolution both Y and C signals are combined to a 10-bit CVBS signal, also; in front of the summation point, the luminance signal can optionally be fed through a further filter stage, suppressing components in the range of subcarrier frequency. Thus, a type of cross colour reduction is provided, which is useful in a standard TV set with CVBS input.

Slopes of synchronization pulses are not affected with any cross colour reduction active.

Three different filter characteristics or bypass are available, see Fig.5 for 60 Hz field rate and Fig.9 for 50 Hz field rate.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitudes at the input of the DAC for CVBS is reduced by $^{15}\!/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of all DACs can be set together via software control to minimum output voltage for either purpose.

Synchronization

The synchronization of the DENC2-SQ is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to the video signal on VP ports can be influenced by programming the polarity and on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it can be also used to set the horizontal phase.

If the horizontal phase is not be influenced by RCV1, a horizontal pulse needs to be supplied at the RCV2 pin. Timing and trigger behaviour can also be influenced for RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of DENC2-SQ runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (such with wrong phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the IC can output:

- A Vertical Sync signal (VS) with 3 or 2.5 lines duration, or
- An ODD/EVEN signal which is LOW in odd fields, or
- A field sequence signal (FSEQ) which is HIGH in the first of 4 respectively 8 fields.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up e.g. a composite blanking signal.

The phase of the pulses output on RCV1 or RCV2 are referenced to the VP ports, polarity of both signals is selectable.

On the RCM1 port the same signals as on RCV1 (as output) are available; on RCM2 the IC provides a horizontal pulse with programmable start and stop phase.

The length of a field also start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

Control interface

DENC2-SQ contains two control interfaces: an I^{2}C-bus slave transceiver and 8-bit parallel microprocessor interface. The interfaces cannot be used simultaneously.

The I^{2}C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 100 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

Two I^{2}C-bus slave addresses can be selected (pin SEL_MPU must be LOW):

88H: LOW at pin 61

8CH: HIGH at pin 61.

The parallel interface is defined by:

D7 to D0 data bus

$\overline{\text{CS}}$ active-LOW chip select signal

R$\overline{\text{W}}$ read/not write signal, LOW for a write cycle

$\overline{\text{DTACK}}$ 680xx style data acknowledge (handshake), active-LOW

A0 register select, LOW selects address, HIGH selects data.

The parallel interface uses two registers, one auto-incremental containing the current address of a control register (equals subaddress with I^{2}C-bus control), one containing actual data. The currently addressed register is mapped to the corresponding control register.

The status byte can be read optionally via a read access to the address register, no other read access is provided.

Input levels and formats

DENC2-SQ expects digital YUV data with levels (digital codes) in accordance with CCIR 601.

Deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

When the IC is operating with input data in accordance with CCIR 656, programming can be carried out alternatively via the parallel interface using VP3 port for data transfer.

For other input modes, the I^{2}C-bus interface has to be used for programming.

Table 1 CCIR signal component levels

SIGNAL	IRE	DIGITAL LEVEL	CODE
Y	0	16	straight binary
	50	126	
	100	235	
Cb	bottom peak	16	straight binary
	colourless	128	
	top peak	240	
Cr	bottom peak	16	straight binary
	colourless	128	
	top peak	240	

Table 2 8-bit multiplexed format (similar to CCIR 656)

TIME	FORMAT							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Sample	Cb_0	Y_0	Cr_0	Y_1	Cb_2	Y_2	Cr_2	Y_3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 3 16-bit multiplexed format (DTV2 format)

TIME	FORMAT							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample UV line	Cb_0		Cr_0		Cb_2		Cr_2	
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

Table 4 24-bit direct 444 format

TIME	FORMAT							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Sample Y line	Y_0		Y_1		Y_2		Y_3	
Sample U line	Cb_0		Cb_1		Cb_2		Cb_3	
Sample V line	Cr_0		Cr_1		Cr_2		Cr_3	
Luminance pixel number	0		1		2		3	
Colour pixel number	0		1		2		3	

Bit allocation map

Table 5 Slave receiver (slave address 88H or 8CH)

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Null	00	0	0	0	0	0	0	0	0
	01 to 38					→			
Null	39	0	0	0	0	0	0	0	0
Input port control	3A	CBENB	0	0	0	VY2C	VUV2C	FMT1	FMT0
OSD LUT Y0	42	OSDY07	OSDY06	OSDY05	OSDY04	OSDY03	OSDY02	OSDY01	OSDY00
OSD LUT U0	43	OSDU07	OSDU06	OSDU05	OSDU04	OSDU03	OSDU02	OSDU01	OSDU00
OSD LUT V0	44	OSDV07	OSDV06	OSDV05	OSDV04	OSDV03	OSDV02	OSDV01	OSDV00
	45 to 56					→			
OSD LUT Y7	57	OSDY77	OSDY76	OSDY75	OSDY74	OSDY73	OSDY72	OSDY71	OSDY70
OSD LUT U7	58	OSDU77	OSDU76	OSDU75	OSDU74	OSDU73	OSDU72	OSDU71	OSDU70
OSD LUT V7	59	OSDV77	OSDV76	OSDV75	OSDV74	OSDV73	OSDV72	OSDV71	OSDV70
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	0	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	0	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
Null	5F	0	0	0	0	0	0	0	0
Cross-colour select	60	CCRS1	CCRS0	0	0	0	0	0	0
Standard control	61	0	DOWN	INPI1	YGS	RTCE	SCBW	PAL	FISE
Burst amplitude	62	SQP	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
CC line	6B	0	0	0	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0

REGISTER FUNCTION	SUB ADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
RCV port control	6C	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
RCM, CC mode	6D	0	0	0	0	SRCM11	SRCM10	CCEN1	CCEN0
Horizontal trigger	6E	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Horizontal trigger	6F	0	0	0	0	0	HTRIG10	HTRIG09	HTRIG08
f_{sc} reset mode, Vertical trigger	70	PHRES1	PHRES0	SBLBN	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Begin master request	71	BMRQ7	BMRQ6	BMRQ5	BMRQ4	BMRQ3	BMRQ2	BMRQ1	BMRQ0
End master request	72	EMRQ7	EMRQ6	EMRQ5	EMRQ4	EMRQ3	EMRQ2	EMRQ1	EMRQ0
MSBs master request	73	0	EMRQ10	EMRQ09	EMRQ08	0	BMRQ10	BMRQ09	BMRQ08
Null	74	0	0	0	0	0	0	0	0
Null	75	0	0	0	0	0	0	0	0
Null	76	0	0	0	0	0	0	0	0
Begin RCV2 output	77	BRCV7	BRCV6	BRCV5	BRCV4	BRCV3	BRCV2	BRCV1	BRCV0
End RCV2 output	78	ERCV7	ERCV6	ERCV5	ERCV4	ERCV3	ERCV2	ERCV1	ERCV0
MSBs RCV2 output	79	0	ERCV10	ERCV09	ERCV08	0	BRCV10	BRCV09	BRCV08
Field length	7A	FLEN7	FLEN6	FLEN5	FLEN4	FLEN3	FLEN2	FLEN1	FLEN0
First active line	7B	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7C	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSBs field control	7D	0	0	LAL8	FAL8	0	0	FLEN9	FLEN8

I^2C-bus format

Table 6 I^2C-bus address; see Table 7

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 7 Explanation of Table 6

PART	DESCRIPTION
S	START condition
Slave address	1 0 0 0 1 0 0 X or 1 0 0 0 1 1 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read, no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Slave receiver

Table 8 Subaddress 3A

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FMT	see Table 9	Select input data format.
VUV2C	0	Cb/Cr data input to VP ports is two's complement. Default after reset.
	1	Cb/Cr data input to VP ports is straight binary.
VY2C	0	Y data input to VP1 port is two's complement. Default after reset.
	1	Y data input to VP1 port is straight binary.
CBENB	0	Data from input ports is encoded. Default after reset.
	1	Colour bar with programmable colours (entries of OSD_LUTs) is encoded. The LUTs are read in upward order from index 0 to index 7.

Table 9 Logic levels and function of FMT

DATA BYTE		FUNCTION
FMT1	FMT0	
0	0	Input data YUV 444, 24 lines, Y on VP1, Cr on VP2, Cb on VP3. Default after reset.
0	1	Input data YUV 422, 16 lines, Y on VP1, multiplexed CbCr on VP3.
1	0	Input data YUV 422, 8 lines, multiplexed in accordance with CCIR 656 on VP1.
1	1	Input data YUV 422, 8 lines, multiplexed in accordance with CCIR 656 on VP1.

Table 10 Subaddress 42 to 59

COLOUR	DATA BYTE (note 1)			INDEX (note 2)
	OSDY	OSDU	OSDV	
White	107 (6BH)	0 (00H)	0 (00H)	0
	107 (6BH)	0 (00H)	0 (00H)	
Yellow	82 (52H)	144 (90H)	18 (12H)	1
	34 (22hH	172 (ACH)	14 (0EH)	
Cyan	42 (2AH)	38 (26H)	144 (90H)	2
	03 (03H)	29 (1DH)	172 (ACH)	
Green	17 (11H)	182 (B6H)	162 (A2H)	3
	240 (F0H)	200 (C8H)	185 (B9H)	
Magenta	234 (EAH)	74 (4AH)	94 (5EH)	4
	212 (D4H)	56 (38H)	71 (47H)	
Red	209 (D1H)	218 (DAH)	112 (70H)	5
	193 (C1H)	227 (E3H)	84 (54H)	
Blue	169 (A9H)	112 (70H)	238 (EEH)	6
	163 (A3H)	84 (54H)	242 (F2H)	
Black	144 (90H)	0 (00H)	0 (00H)	7
	144 (90H)	0 (00H)	0 (00H)	

Notes

1. Contents of OSD Look-up tables. All 8 entries are 8-bits. Data representation is in accordance with CCIR 601 (Y, Cb, Cr), but two's complement, e.g. for a $^{100}/_{100}$ (upper number) or $^{100}/_{75}$ (lower number) colour bar.
2. For normal colour bar with CBENB = logic 1.

Table 11 Subaddress 5A

DATA BYTE	DESCRIPTION
CHPS	Phase of encoded colour subcarrier (including burst) relative to horizontal sync. Can be adjusted in steps of 360 or 256 degrees.

Table 12 Subaddress 5B and 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for Cb signal; input representation accordance with CCIR 601	white-to-black = 92.5 IRE(1)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE(2)	
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Notes

1. GAINU = –2.17 × nominal to +2.16 × nominal.
2. GAINU = –2.05 × nominal to +2.04 × nominal.

Table 13 Subaddress 5C and 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for Cr signal; input representation accordance with CCIR 601	white-to-black = 92.5 IRE[(1)]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE[(2)]	
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Notes

1. GAINV = –1.55 × nominal to +1.55 × nominal.
2. GAINV = –1.46 × nominal to +1.46 × nominal.

Table 14 Subaddress 5D

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation accordance with CCIR 601	white-to-sync = 140 IRE[(1)]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 49 IRE
		white-to-sync = 143 IRE[(2)]	
		BLCKL = 0	output black level = 24 IRE
		BLCKL = 63 (3FH)	output black level = 50 IRE

Notes

1. Output black level/IRE = BLCKL × 25/63 + 24; recommended value: BLCKL = 60 (3CH) normal.
2. Output black level/IRE = BLCKL × 26/63 + 24; recommended value: BLCKL = 45 (2DH) normal.

Table 15 Subaddress 5E

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE[(1)]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 42 IRE
		white-to-sync = 143 IRE[(2)]	
		BLNNL = 0	output blanking level = 17 IRE
		BLNNL = 63 (3FH)	output blanking level = 43 IRE

Notes

1. Output black level/IRE = BLNNL × 25/63 + 17; recommended value: BLNNL = 58 (3AH) normal.
2. Output black level/IRE = BLNNL × 26/63 + 17; recommended value: BLNNL = 63 (3FH) normal.

Table 16 Subaddress 60 (CCRS; select cross colour reduction filter in luminance)

DATA BYTE		FUNCTION
CCRS1	CCRS0	
0	0	no cross colour reduction (for transfer characteristic of luminance see Figs 5 and 9)
0	1	cross colour reduction #1 active (for transfer characteristic see Figs 5 and 9)
1	0	cross colour reduction #2 active (for transfer characteristic see Figs 5 and 9)
1	1	cross colour reduction #3 active (for transfer characteristic see Figs 5 and 9)

Table 17 Subaddress 61

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	944 total pixel clocks per line
	1	780 total pixel clocks per line; default after reset
PAL	0	NTSC encoding (non-alternating V component); default after reset
	1	PAL encoding (alternating V component)
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3, 4, 7 and 8)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3, 4, 7 and 8); default after reset
RTCE	0	no real time control of generated subcarrier frequency; default after reset
	1	real time control of generated subcarrier frequency through SAA7191B (timing see Fig.13)
YGS	0	luminance gain for white-to-black 100 IRE
	1	luminance gain for white-to-black 92.5 IRE including 7.5 IRE set-up of black; default after reset
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal
DOWN	0	DACs in normal operational mode; default after reset
	1	DACs forced to lowest output voltage

Table 18 Subaddress 62

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation accordance with CCIR 601	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 1.25 × nominal(1) white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 1.76 × nominal(2) white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.20 × nominal(3) white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 1.67 × nominal(4)	
SQP	subcarrier real time	logic 0	not supported in current version, do not use
		logic 1	control from SAA7191B digital colour decoder

Notes

1. Recommended value: BSTA = 102 (66H).
2. Recommended value: BSTA = 72 (48H).
3. Recommended value: BSTA = 106 (6AH).
4. Recommended value: BSTA = 75 (4BH).

Table 19 Subaddress 63 to 66 (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{sc} = subcarrier frequency (in multiples of line frequency); f_{LLC} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{sc}}{f_{LLC}} \times 2^{32}\right)$ see note 1	FSC3 = most significant byte FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{sc} = 227.5, f_{LLC} = 1560 → FSC = 626349397 (25555555H).
   b) PAL-B/G: f_{sc} = 283.7516, f_{LLC} = 1888 → FSC = 645499916 (26798C0CH).

Table 20 Subaddress 67 to 6A

DATA BYTE[1]	DESCRIPTION
L21O0	first byte of captioning data, odd field
L21O1	second byte of captioning data, odd field
L21E0	first byte of extended data, even field
L21E1	second byte of extended data, even field

Note

1. LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 21 Subaddress 6B

DATA BYTE	DESCRIPTION
SCCLN	selects the actual line, where closed caption or extended data are encoded; see note 1

Note

1. Line = (SCCLN + 4) for M systems; line = (SCCLN + 1) for other systems.

Table 22 Subaddress 6C

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (Horizontal Reference Pulse that is HIGH during active portion of line, also during vertical blanking Interval); default after reset
	1	if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset if ORCV2 = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) also as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input, respectively
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port; default after reset
	1	horizontal synchronization is taken from RCV2 port
SRCV1	–	defines signal type on pin RCV1; see Table 23

Table 23 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	Vertical Sync each field; default after reset
0	1	FS	FS	Frame Sync (odd/even)
1	0	FSEQ	FSEQ	Field Sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	–	–	not applicable

Table 24 Subaddress 6D

DATA BYTE	DESCRIPTION
CCEN	enables individual line 21 encoding; see Table 25
SRCM	defines signal type on pin RCM1; see Table 26

Table 25 Logic levels and function of CCEN

DATA BYTE		FUNCTION
CCEN1	CCEN0	
0	0	line 21 encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 26 Logic levels and function of SRCM

DATA BYTE		AS OUTPUT	FUNCTION
SRCM1	SRCM0		
0	0	VS	Vertical Sync each field
0	1	FS	Frame Sync (odd/even)
1	0	FSEQ	Field Sequence, vertical sync every fourth field (FISE = 1) or eighth field (FISE = 0)
1	1	–	not applicable

Table 27 Subaddress 6E to 6F

DATA BYTE	DESCRIPTION
HTRIG	sets the Horizontal Trigger phase related to signal on RCV1 or RCV2 input values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed increasing HTRIG decreases delays of all internally generated timing signals reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 031H (033H)

Table 28 Subaddress 70

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VTRIG	–	sets the Vertical Trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines variation range of VTRIG = 0 to 31 (1FH)
SBLBN	0	vertical blanking is defined by programming of FAL and LAL
	1	vertical blanking is forced automatically at least during field synchronization and equalization pulses; note 1
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 29

Note

1. If cross-colour reduction is programmed, it is active between FAL and LAL in both events.

Table 29 Logic levels and function of PHRES

DATA BYTE		FUNCTION
PHRES1	PHRES0	
0	0	no reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 30 Subaddress 71 to 73

DATA BYTE	DESCRIPTION
BMRQ	beginning of master request signal (RCM2) values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at BMRQ = 0E1H (130H)
EMRQ	end of master request signal (RCM2) values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCM2) at EMRQ = 5E9H (72AH)

Table 31 Subaddress 77 to 79

DATA BYTE	DESCRIPTION
BRCV	beginning of output signal on RCV2 pin values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at BRCV = 0E1H (130H)
ERCV	end of output signal on RCV2 pin values above 1559 (FISE = 1) or 1887 (FISE = 0) are not allowed last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at ERCV = 5E9H (72AH)

Table 32 Subaddress 7A to 7D

DATA BYTE	DESCRIPTION
FLEN	Length of a Field = FLEN + 1, measured in half lines valid range is limited to 524 to 1022 (FISE = 1) respectively 624 to 1022 (FISE = 0), FLEN should be even
FAL	First Active Line, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	Last Active Line, measured in lines LAL = 0 coincides with the first field synchronization pulse

SUBADDRESSES

In subaddresses 5B, 5C, 5D, 5E and 62 all IRE values are rounded up.

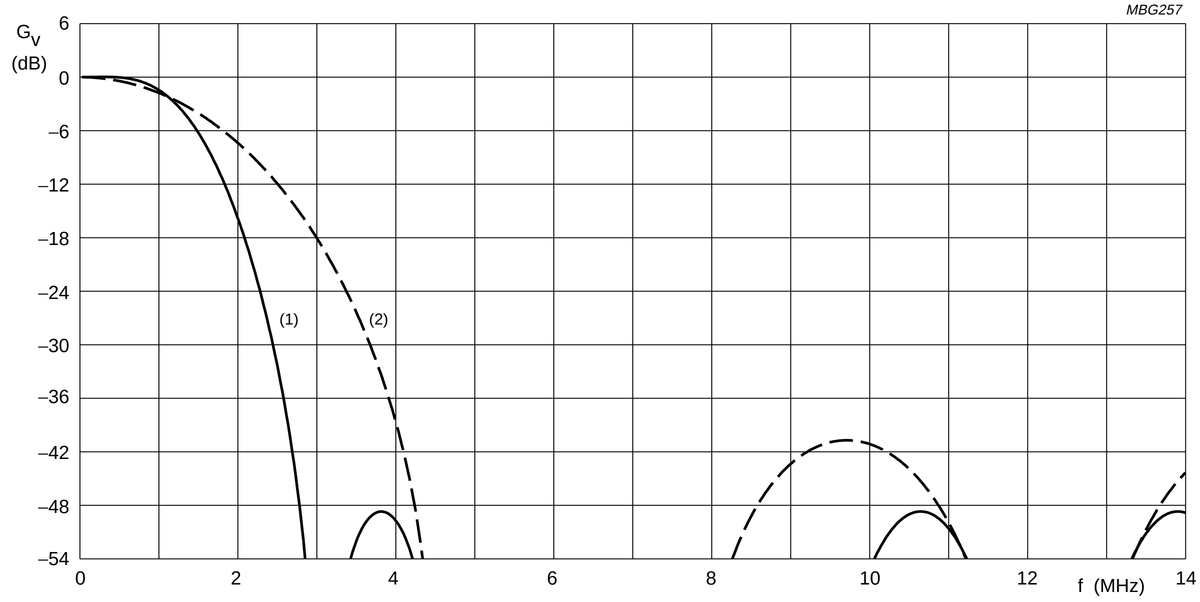
Slave transmitter

Table 33 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	FSQ2	FSQ1	FSQ0

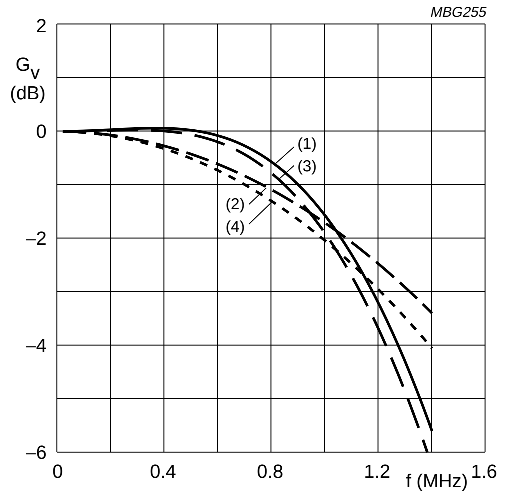
Table 34 No subaddress

DATA BYTE	DESCRIPTION
VER	Version identification of the device. It will be changed with all versions of the IC that have different programming models. Current Version is 000 binary.
CCRDE	Closed caption bytes of the even field have been encoded. The bit is reset after information has been written to the subaddresses 69 and 6A. It is set immediately after the data have been encoded.
CCRDO	Closed caption bytes of the odd field have been encoded. The bit is reset after information has been written to the subaddresses 67 and 68. It is set immediately after the data have been encoded.
FSQ	State of the internal field sequence counter. Bit 0 (FSQ0) gives the odd/even information; odd = LOW, even = HIGH.



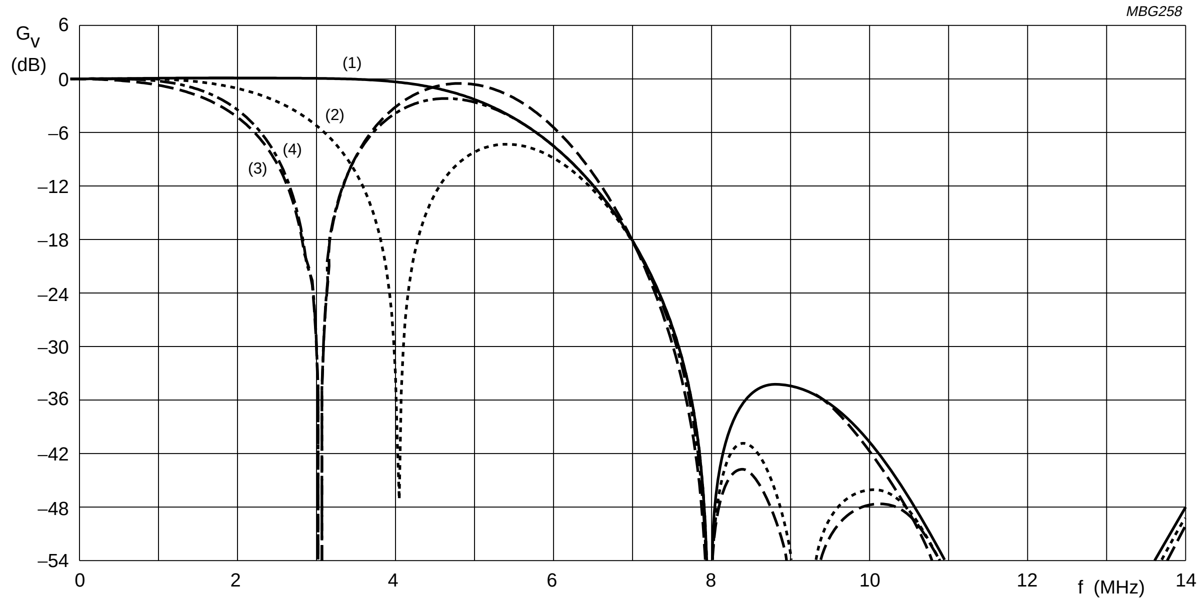
(1) SCBW = 1; 444 input.
(2) SCBW = 0; 444 input.

Fig.3 Chrominance transfer characteristic 1 (60 Hz).



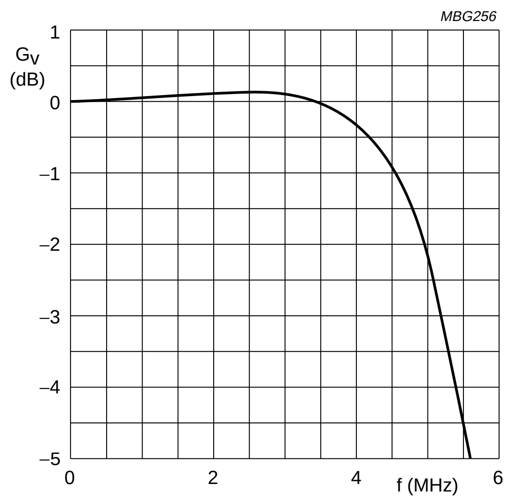
(1) SCBW = 1.
(2) SCBW = 0.
(3) SCBW = 1; 444 input.
(4) SCBW = 0; 444 input.

Fig.4 Chrominance transfer characteristic 2 (60 Hz).



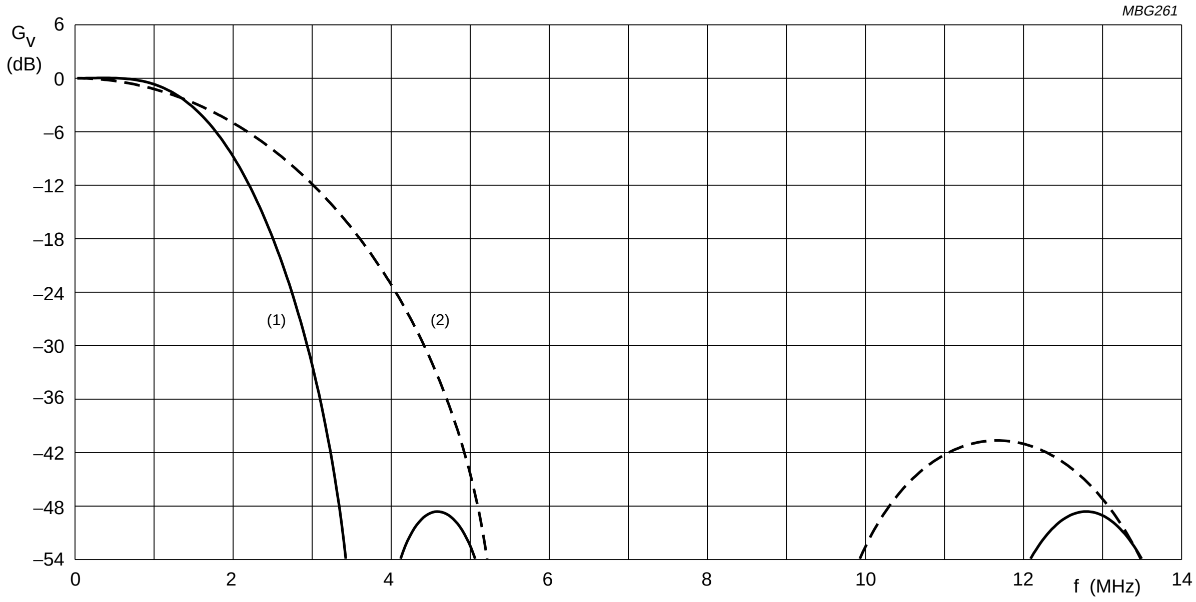
(1) CCRS1 = 0; CCRS0 = 0.
(2) CCRS1 = 0; CCRS0 = 1.
(3) CCRS1 = 1; CCRS0 = 0.
(4) CCRS1 = 1; CCRS0 = 1.

Fig.5 Luminance transfer characteristic 1 (60 Hz).



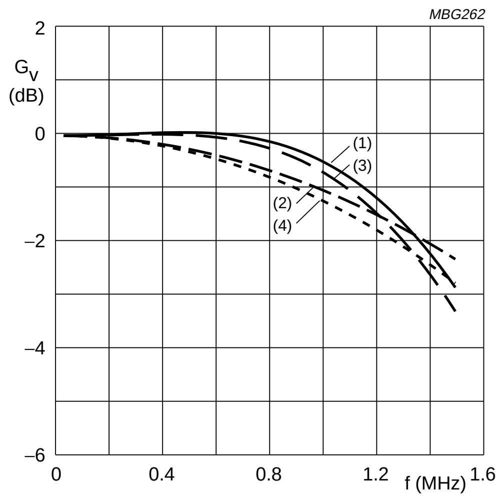
CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2 (60 Hz).



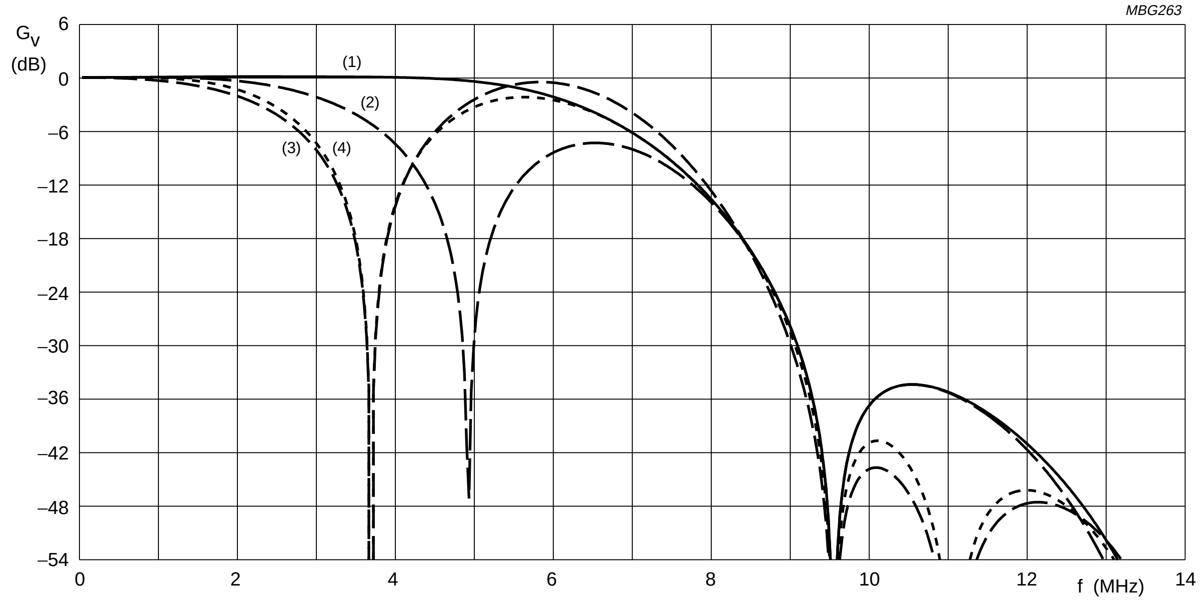
(1) SCBW = 1; 444 input.
(2) SCBW = 0; 444 input.

Fig.7 Chrominance transfer characteristic 1 (50 Hz).



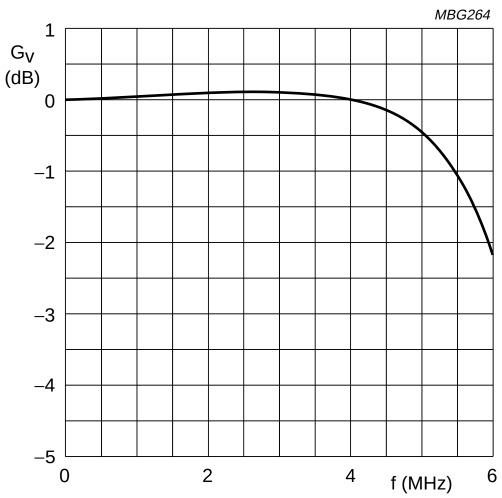
(1) SCBW = 1.
(2) SCBW = 0.
(3) SCBW = 1; 444 input.
(4) SCBW = 0; 444 input.

Fig.8 Chrominance transfer characteristic 2 (50 Hz).



(1) CCRS1 = 0; CCRS0 = 0.
(2) CCRS1 = 0; CCRS0 = 1.
(3) CCRS1 = 1; CCRS0 = 0.
(4) CCRS1 = 1; CCRS0 = 1.

Fig.9 Luminance transfer characteristic 1 (50 Hz).



CCRS1 = 0; CCRS0 = 0.

Fig.10 Luminance transfer characteristic 2 (50 Hz).

CHARACTERISTICS

V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDD}	digital supply voltage		4.5	5.5	V
V_{DDA}	analog supply voltage		4.75	5.25	V
I_{DDD}	digital supply current	note 1	–	210	mA
I_{DDA}	analog supply current	note 1	–	55	mA
Inputs					
V_{IL}	LOW level input voltage (except SDA, SCL, AP, SP and XTALI)		–0.5	+0.8	V
V_{IH}	HIGH level input voltage (except SDA, SCL, AP, SP and XTALI)		2.0	V_{DDD} + 0.5	V
	HIGH level input voltage (LLC)		2.4	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–	1	μA
C_i	input capacitance	clocks operating	–	10	pF
		data available	–	8	pF
		I/Os at high impedance	–	8	pF
Outputs					
V_{OL}	LOW level output voltage (except SDA and XTALO)	note 2	0	0.6	V
V_{OH}	HIGH level output voltage (except SDA, $\overline{DTACK}$ and XTALO)	note 2	2.4	V_{DDD} + 0.5	V
	HIGH level output voltage (LLC)	note 2	2.6	V_{DDD} + 0.5	V
I^2C-bus; SDA and SCL					
V_{IL}	LOW level input voltage		–0.5	+1.5	V
V_{IH}	HIGH level input voltage		3.0	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–	±10	μA
V_{OL}	LOW level output voltage (SDA)	I_{OL} = 3 mA	–	0.4	V
I_O	output current	during acknowledge	3	–	mA
Clock timing (LLC)					
T_{LLC}	cycle time	note 3	31	44	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 4	40	60	%
t_r	rise time	note 3	–	5	ns
t_f	fall time	note 3	–	6	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Input timing					
$t_{SU;CREF}$	input data set-up time (CREF)		6	–	ns
$t_{HD;CREF}$	input data hold time (CREF)		3	–	ns
t_{SU}	input data set-up time (any other except SEL_MPU, CDIR, R$\overline{W}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RESET}$, AP and SP)		6	–	ns
t_{HD}	input data hold time (any other except SEL_MPU, CDIR, R$\overline{W}$/SCL, A0/SDA, $\overline{CS}$/SA, $\overline{RESET}$, AP and SP)		3	–	ns
Crystal oscillator					
f_n	nominal frequency (usually 24.545454 or 29.5 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 5	–50	+50	10^{-6}
CRYSTAL SPECIFICATION					
T_{amb}	operating ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resonance resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 –20%	1.5 +20%	fF
C_0	parallel capacitance (typical)		3.5 –20%	3.5 +20%	pF
MPU interface timing					
t_{AS}	address set-up time	note 6	9	–	ns
t_{AH}	address hold time		0	–	ns
$t_{R\overline{W}S}$	read/write set-up time	note 6	9	–	ns
$t_{R\overline{W}H}$	read/write hold time		0	–	ns
t_{DD}	data valid from $\overline{CS}$ (read)	notes 7, 8 and 9; n = 9	–	440	ns
t_{DF}	data bus floating from $\overline{CS}$ (read)	notes 7 and 8; n = 5	–	275	ns
t_{DS}	data bus set-up time (write)	note 6	9	–	ns
t_{DH}	data bus hold time (write)	note 6	9	–	ns
t_{ACS}	acknowledge delay from $\overline{CS}$	notes 7 and 8; n = 11	–	520	ns
$t_{\overline{CS}D}$	$\overline{CS}$ HIGH from acknowledge		0	–	ns
t_{DAT}	$\overline{DTACK}$ floating from $\overline{CS}$ HIGH	notes 7 and 8; n = 7	–	360	ns
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_{OH}	output hold time		4	–	ns
t_{OD}	output delay time	CREF in output mode	–	25	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CHROMA, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 10	1.9	2.1	V
R_I	internal serial resistance		18	35	Ω
R_L	output load resistance		80	–	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
ILE	LF integral linearity error of DACs		–	±2	LSB
DLE	LF differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The levels have to be measured with load circuits of 1.2 kΩ to 3.0 V (standard TTL load) and C_L = 25 pF.
3. The data is for both input and output direction.
4. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
5. If an internal oscillator is used, crystal deviation of nominal frequency (f_n) is directly proportional to the deviation of subcarrier frequency and line/field frequency.
6. The value is calculated via equation $t = t_{SU} + t_{HD}$
7. The value depends on the clock frequency. The numbers given are calculated with f_{LLC} = 24.54 MHz.
8. The values given are calculated via equation $t_{dmax} = t_{OD} + n \times t_{LLC} + t_{LLC} + t_{SU}$
9. The falling edge of $\overline{DTACK}$ will always occur1 × LLC after data is valid.
10. For full digital range, without load, V_{DDA} = 5.0 V. The typical voltage swing is 2.0 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

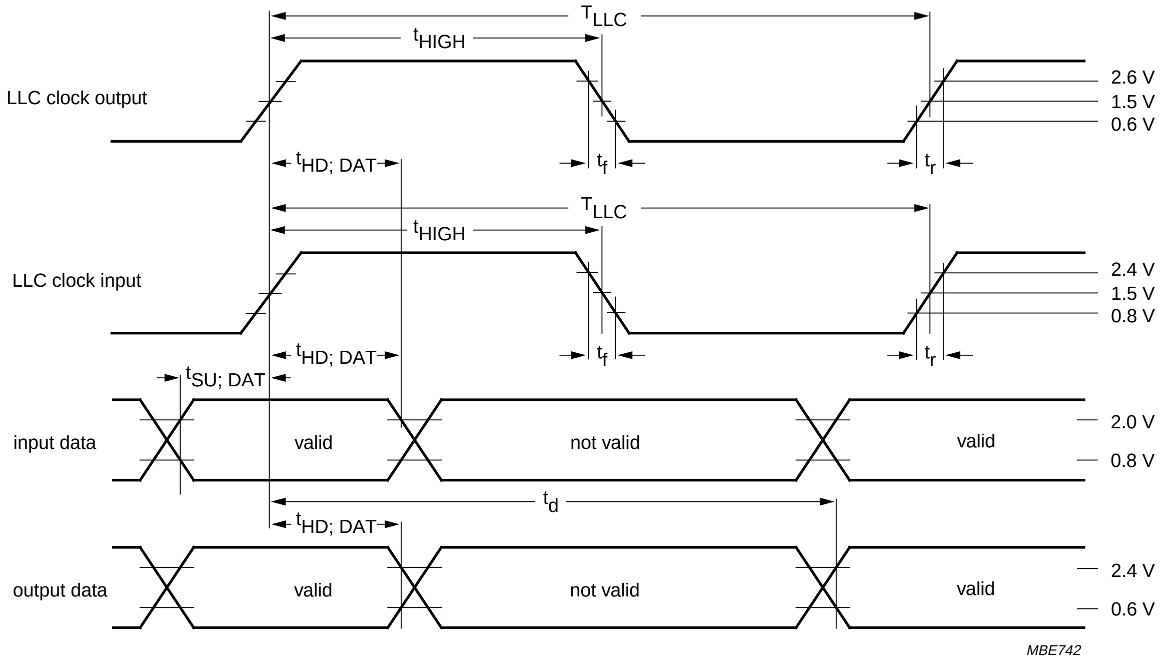
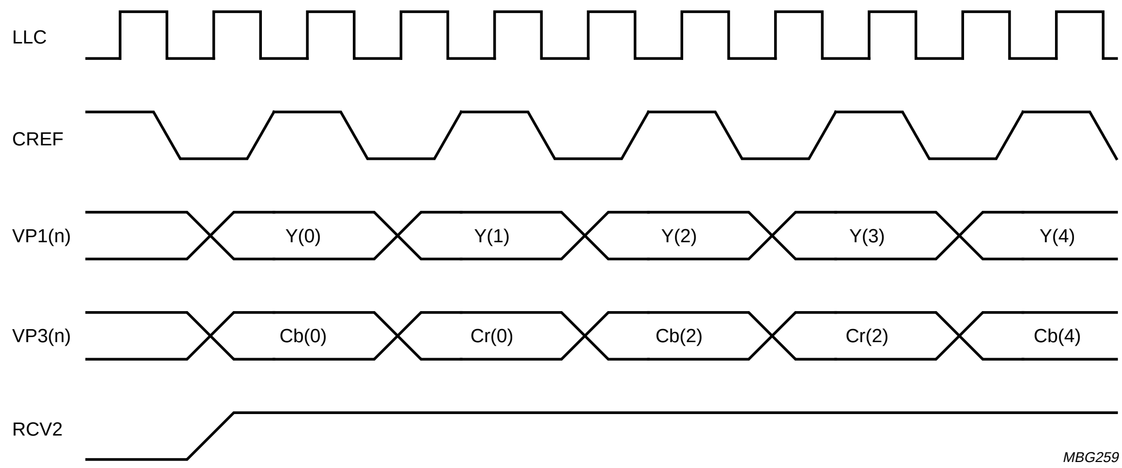
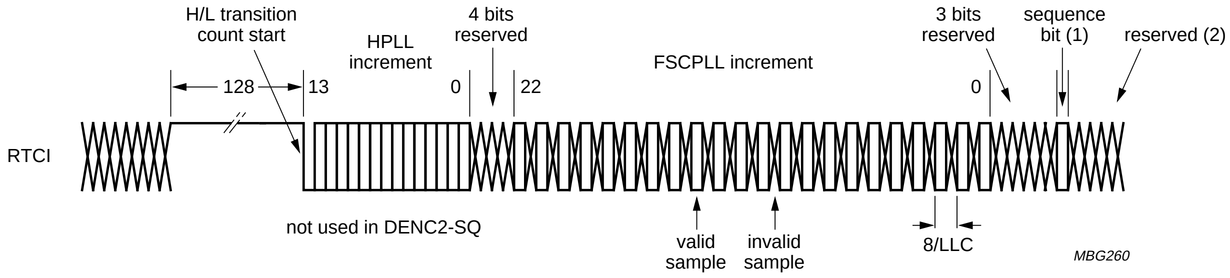


Fig.11 Clock data timing.



The data demultiplexing phase is coupled to the internal horizontal phase.
The CREF signal applies only for the 16 lines digital TV format, because these signals are only valid in 12.27 or 14.75 MHz.
The phase of the RCV2 signal is programmed to 0E1H (130H for 50 Hz) in this example in output mode (BRCV2).

Fig.12 Digital TV timing.



(1) Sequence bit:
PAL = logic 0 then (R – Y) line normal; PAL = logic 1 then (R – Y) line inverted.
NTSC = logic 0 then no change.

(2) Reserved bits: 276 with 50 Hz systems; 188 with 60 Hz systems.

Fig.13 RTCI timing.

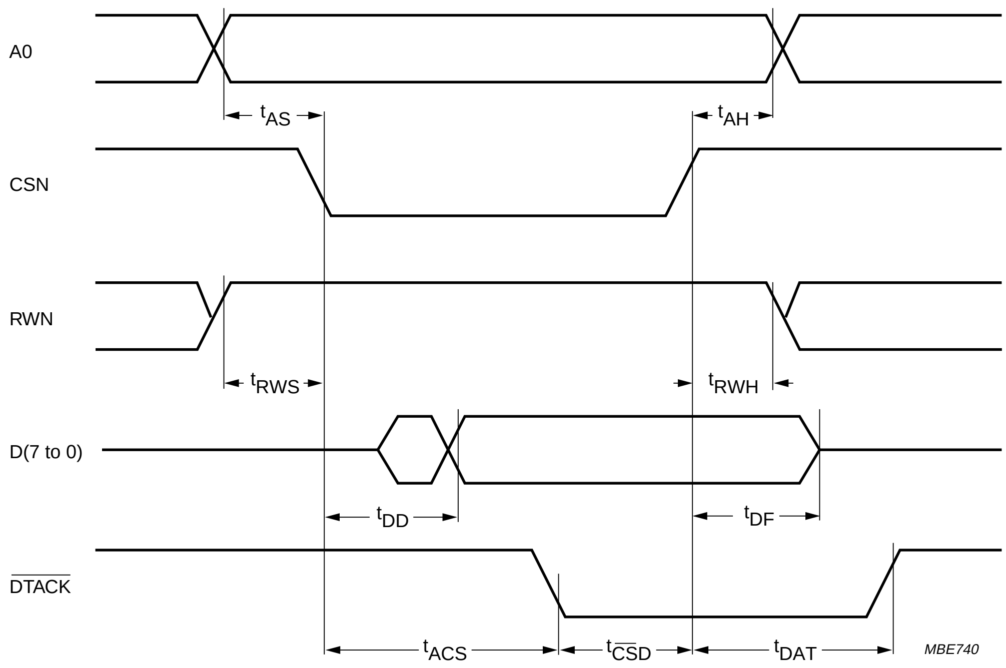


Fig.14 MPU interface timing (read cycle).

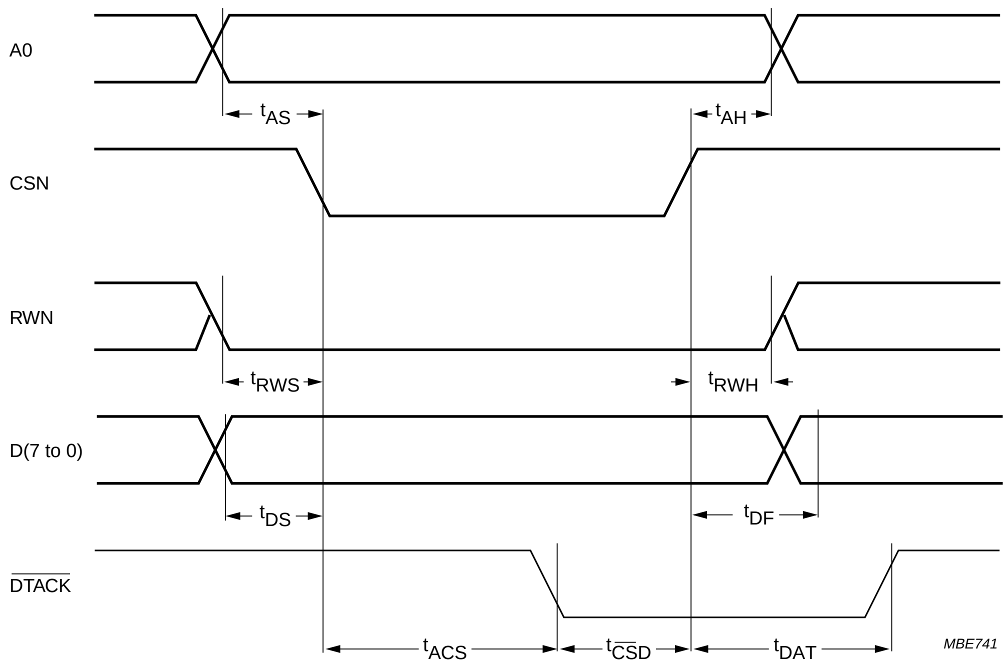


Fig.15 MPU interface timing (write cycle).

APPLICATION INFORMATION

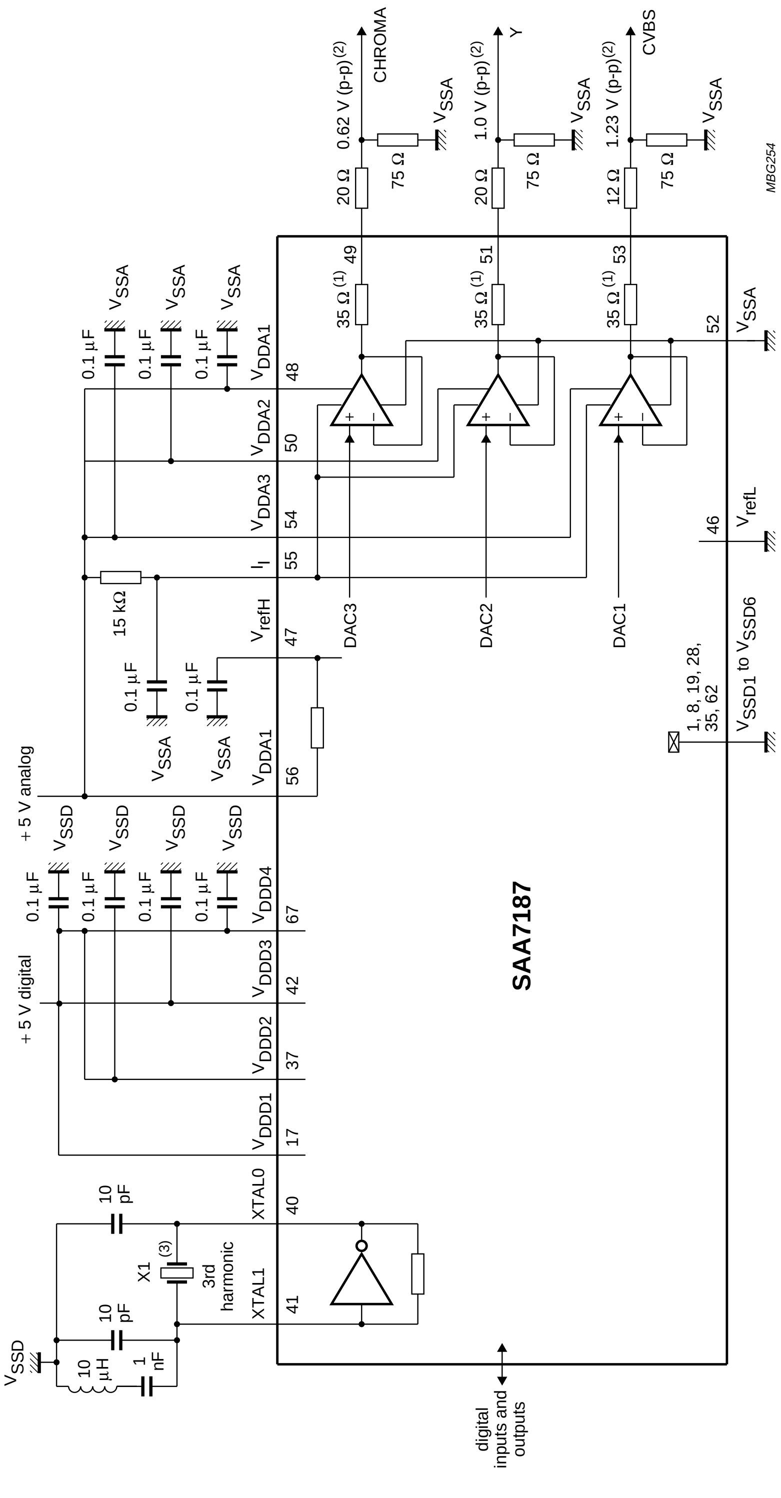
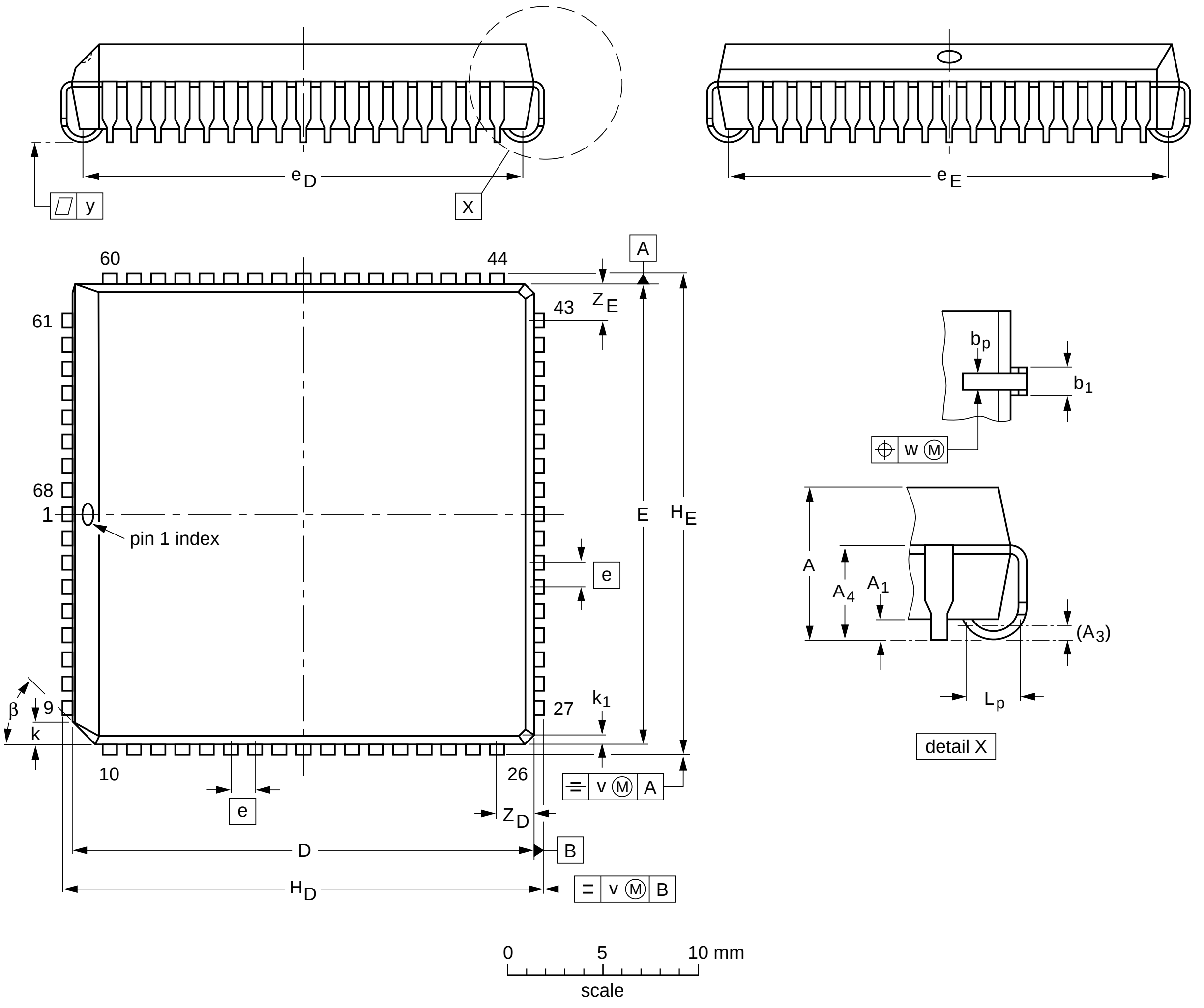


Fig.16 Application environment of the DENC2-SQ.

(1) Typical value.
(2) For 100/100 colour bar.
(3) 24.545454 or 29.5 MHz.

PACKAGE OUTLINE

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**

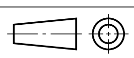


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45^o
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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