INTEGRATED CIRCUITS

DATA SHEET

SAA7199B
Digital Video Encoder (DENC) GENLOCK-capable

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC22

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Philips Semiconductors

PHILIPS

Digital Video Encoder (DENC) GENLOCK-capable

SAA7199B

FEATURES

- Monolithic integrated CMOS video encoder circuit
- Standard MPU (12 lines) and I^2C-bus interfaces for controls
- Three 8-bit signal inputs PD7 to PD0 for RGB respectively YUV or indexed colour signals (Tables 19 to 26)
- Square pixel and CCIR input data rates
- Band limited composite sync pulses
- Three 256 × 8 colour look-up tables (CLUTs) for example for gamma correction
- External subcarrier from a digital decoder (SAA7151B or SAA7191B)
- Multi-purpose key for real time format switching
- Autonomous internal blanking
- Optional GENLOCK operation with adjustable horizontal sync timing and adjustable subcarrier phase
- Stable GENLOCK operation in VCR standard playback mode
- Optional still video capture extension
- Three suitable video 9-bit digital-to-analog converters
- Composite analog output signals CVBS, Y and C for PAL/NTSC
- Line 21 data insertion possible.

GENERAL DESCRIPTION

The SAA7199B encodes digital baseband colour/video data into analog Y, C and CVBS signals (S-video included). Pixel clock and data are line-locked to the horizontal scanning frequency of the video signal.
The circuit can be used in a square pixel or in a consumer TV application. Flexibility is provided by programming facilities via MPU-bus (parallel) or I^2C-bus (serial).

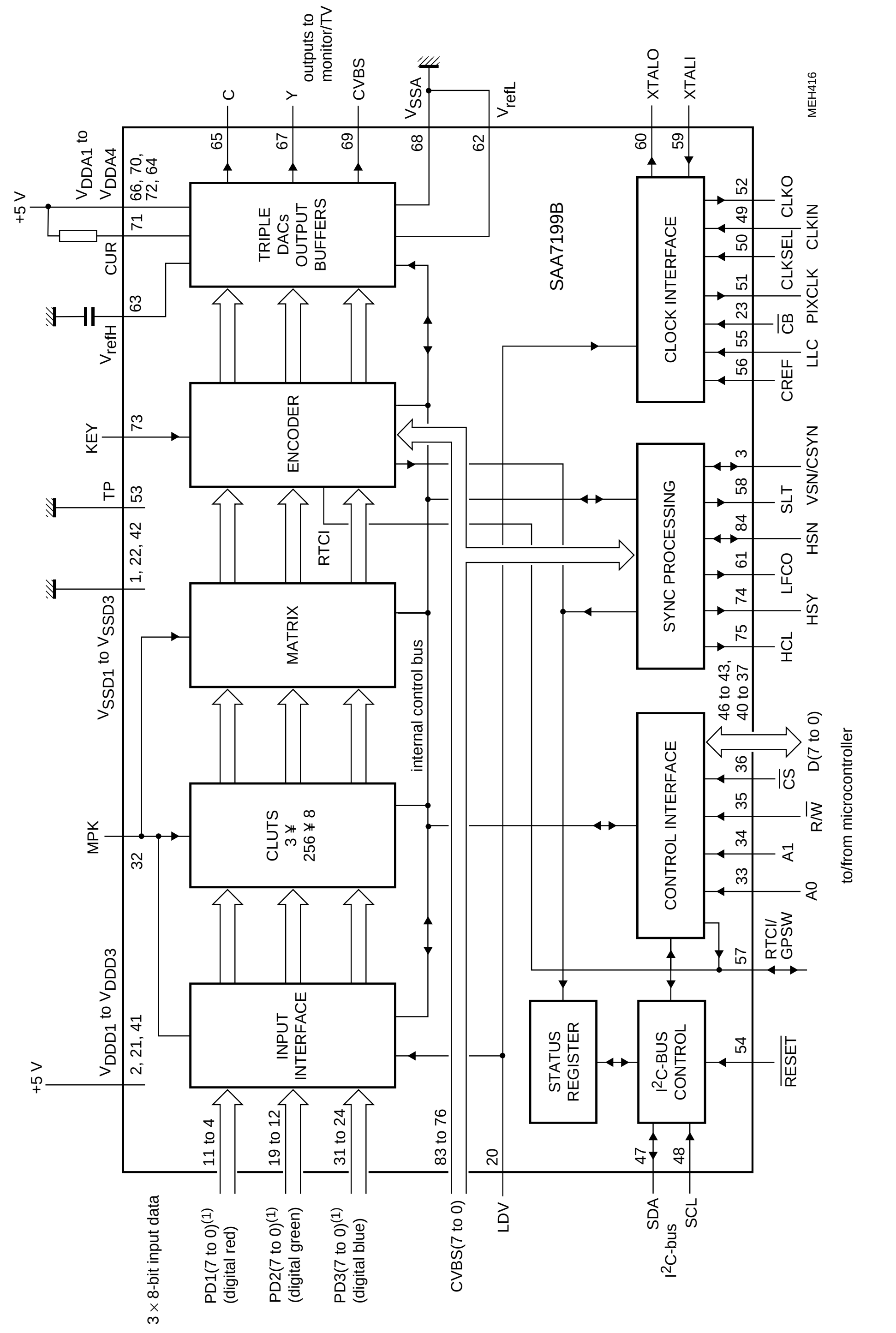
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage (pins 2, 21 and 41)	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage (pins 64, 66, 70 and 72)	4.75	5.0	5.25	V
$I_{P(tot)}$	total supply current	–	–	200	mA
V_I	input signal levels	TTL-compatible			
V_o	analog output voltage Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	output load resistance	90	–	–	Ω
ILE	LF integral linearity error in output signal (9-bit DAC)	–	–	±1	LSB
DLE	LF differential linearity error in output signal (9-bit DAC)	–	–	±0.5	LSB
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7199BWP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2

BLOCK DIAGRAM



(1) RGB respectively input formats YUV and indexed colour (Tables 19 to 26).

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1 (0 V)
V_{DDD1}	2	digital supply 1 (5 V)
VSN/CSYN	3	vertical sync output (3-state), conditionally composite sync output; active LOW or active HIGH
PD1(0)	4	data 1 input: digital signal R (red) respectively V signal; bit 0 (formats in Tables 19 to 25)
PD1(1)	5	data 1 input: digital signal R (red) respectively V signal; bit 1 (formats in Tables 19 to 25)
PD1(2)	6	data 1 input: digital signal R (red) respectively V signal; bit 2 (formats in Tables 19 to 25)
PD1(3)	7	data 1 input: digital signal R (red) respectively V signal; bit 3 (formats in Tables 19 to 25)
PD1(4)	8	data 1 input: digital signal R (red) respectively V signal; bit 4 (formats in Tables 19 to 25)
PD1(5)	9	data 1 input: digital signal R (red) respectively V signal; bit 5 (formats in Tables 19 to 25)
PD1(6)	10	data 1 input: digital signal R (red) respectively V signal; bit 6 (formats in Tables 19 to 25)
PD1(7)	11	data 1 input: digital signal R (red) respectively V signal; bit 7 (formats in Tables 19 to 25)
PD2(0)	12	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 0 (formats in Tables 19 to 25)
PD2(1)	13	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 1 (formats in Tables 19 to 25)
PD2(2)	14	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 2 (formats in Tables 19 to 25)
PD2(3)	15	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 3 (formats in Tables 19 to 25)
PD2(4)	16	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 4 (formats in Tables 19 to 25)
PD2(5)	17	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 5 (formats in Tables 19 to 25)
PD2(6)	18	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 6 (formats in Tables 19 to 25)
PD2(7)	19	data 2 input: digital signal G (green) respectively Y signal or indexed colour data; bit 7 (formats in Tables 19 to 25)
LDV	20	load data clock input signal to input interface (samples PDn(7 to 0), $\overline{CB}$, MPK, KEY and RTCI)
V_{DDD2}	21	digital supply 2 (5 V)
V_{SSD2}	22	digital ground 2 (0 V)
$\overline{CB}$	23	composite blanking input; active LOW
PD3(0)	24	data 3 input: digital signal B (blue) respectively U signal; bit 0 (formats in Tables 19 to 25)
PD3(1)	25	data 3 input: digital signal B (blue) respectively U signal; bit 1 (formats in Tables 19 to 25)
PD3(2)	26	data 3 input: digital signal B (blue) respectively U signal; bit 2 (formats in Tables 19 to 25)
PD3(3)	27	data 3 input: digital signal B (blue) respectively U signal; bit 3 (formats in Tables 19 to 25)
PD3(4)	28	data 3 input: digital signal B (blue) respectively U signal; bit 4 (formats in Tables 19 to 25)
PD3(5)	29	data 3 input: digital signal B (blue) respectively U signal; bit 5 (formats in Tables 19 to 25)
PD3(6)	30	data 3 input: digital signal B (blue) respectively U signal; bit 6 (formats in Tables 19 to 25)
PD3(7)	31	data 3 input: digital signal B (blue) respectively U signal; bit 7 (formats in Tables 19 to 25)
MPK	32	multi-purpose key input; active HIGH
A0	33	subaddress bit A0 input for microcontroller access (Table 3)

SYMBOL	PIN	DESCRIPTION
A1	34	subaddress bit A1 input for microcontroller access (Table 3)
R/$\overline{W}$	35	read/write not input signal from microcontroller
$\overline{CS}$	36	chip select input for parallel interface; active LOW
D0	37	bidirectional port from/to microcontroller; bit D0
D1	38	bidirectional port from/to microcontroller; bit D1
D2	39	bidirectional port from/to microcontroller; bit D2
D3	40	bidirectional port from/to microcontroller; bit D3
V_{DDD3}	41	digital supply 3 (5 V)
V_{SSD3}	42	digital ground 3
D4	43	bidirectional port from/to microcontroller; bit D4
D5	44	bidirectional port from/to microcontroller; bit D5
D6	45	bidirectional port from/to microcontroller; bit D6
D7	46	bidirectional port from/to microcontroller; bit D7
SDA	47	I^2C-bus data input/output
SCL	48	I^2C-bus clock input
CLKIN	49	external clock signal input (maximum frequency 60 MHz)
CLKSEL	50	clock source select input
PIXCLK	51	CLKO/2 or conditionally CLKO output signal
CLKO	52	selected clock output signal (LLC or CLKIN)
TP	53	test pin; connected to ground
$\overline{RESET}$	54	reset input; active LOW
LLC	55	line-locked clock input signal from external clock generation circuit (CGC)
CREF	56	clock qualifier input of external CGC
GPSW/RTCI	57	general purpose switch output (set via I^2C-bus or MPU-bus); real time control input, defined by I^2C or MPU programming
SLT	58	GENLOCK output flag (3-state): HIGH = sync lost in GENLOCK mode; LOW = otherwise
XTALI	59	crystal oscillator input (26.8 or 24.576 MHz)
XTALO	60	crystal oscillator output
LFCO	61	line frequency control output signal for external CGC
V_{refL}	62	reference voltage LOW of DACs (resistor chains)
V_{refH}	63	reference voltage HIGH of DACs (resistor chains)
V_{DDA4}	64	analog supply 4 for resistor chains of the DACs (5 V)
C	65	chrominance analog output signal
V_{DDA1}	66	analog supply 1 for output buffer amplifier of DAC1 (5 V)
Y	67	luminance analog output signal
V_{SSA}	68	analog ground (0 V)
CVBS	69	CVBS analog output signal
V_{DDA2}	70	analog supply 2 for output buffer amplifier of DAC2 (5 V)
CUR	71	current input for analog output buffers
V_{DDA3}	72	analog supply 3 for output buffer amplifier of DAC3 (5 V)
KEY	73	key input signal to insert CVBS input signal into encoded CVBS output signal; active HIGH

SYMBOL	PIN	DESCRIPTION
HSY	74	horizontal sync indicator output signal; active HIGH (3-state output to ADC)
HCL	75	horizontal clamping output; active HIGH (3-state output)
CVBS0	76	digital CVBS input signal; bit 0
CVBS1	77	digital CVBS input signal; bit 1
CVBS2	78	digital CVBS input signal; bit 2
CVBS3	79	digital CVBS input signal; bit 3
CVBS4	80	digital CVBS input signal; bit 4
CVBS5	81	digital CVBS input signal; bit 5
CVBS6	82	digital CVBS input signal; bit 6
CVBS7	83	digital CVBS input signal; bit 7
HSN	84	horizontal sync output; active LOW or active HIGH for 60/66/72 × PIXCLK at 12.27/13.5/14.75 MHz (3-state output)

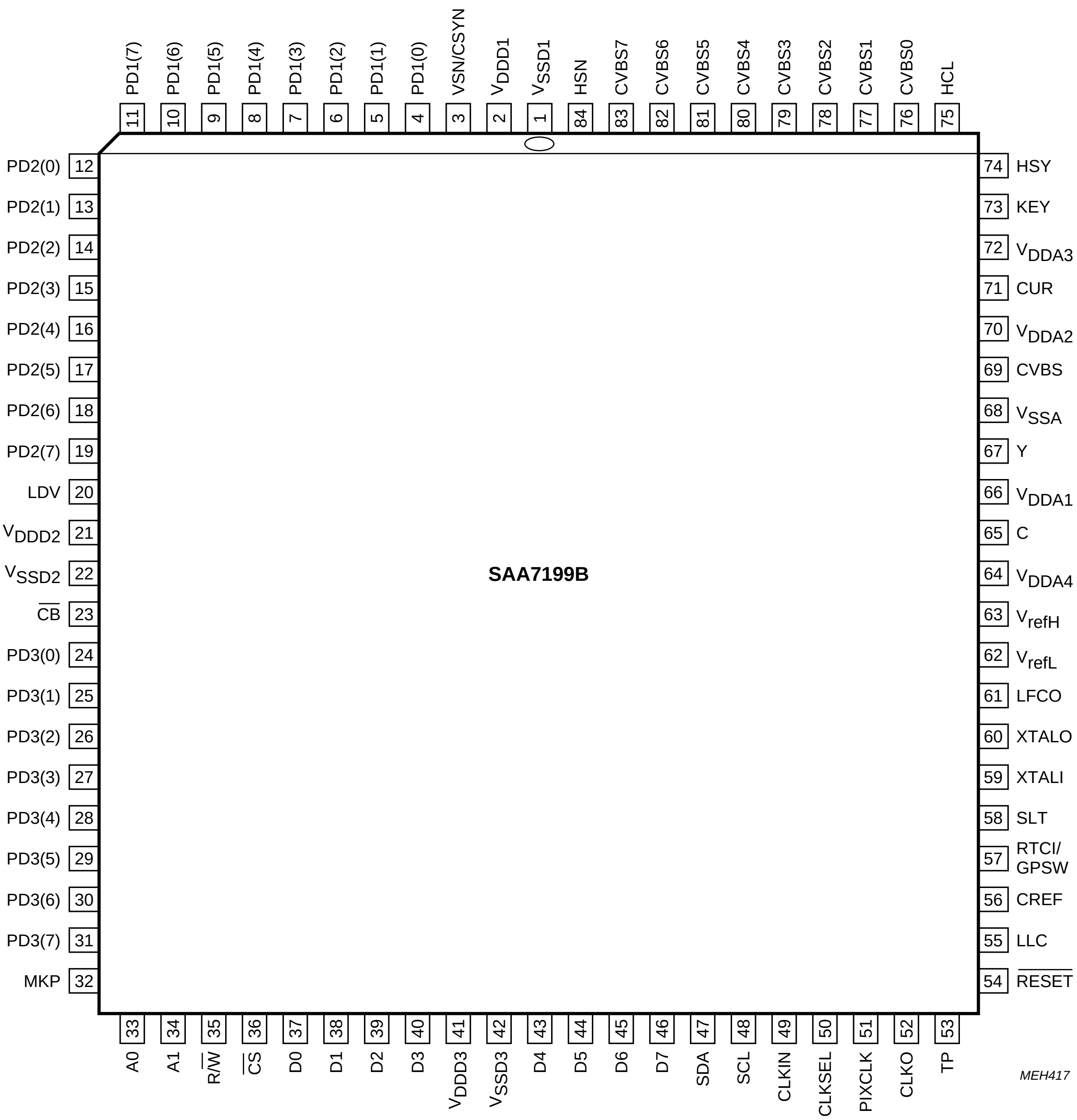


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The SAA7199B is a digital video encoder that translates digital RGB, YUV or 8-bit indexed colour signals into the analog PAL/NTSC output signals Y (luminance), C (4.43/3.58 MHz chrominance) and CVBS (composite signal including sync).

Four different modes are selectable (Table 18):

- Stand-alone mode (horizontal and vertical timings are generated)
- Slave mode (stand-alone unit that accepts external horizontal and vertical timing), and optional real time information for subcarrier/clock from a digital colour decoder
- GENLOCK mode (GENLOCK capabilities are achieved in conjunction with determined ICs)
- Test mode (only clock signal is required).

The input data rate (pixel sequence) has an integer relationship to the number of horizontal clock cycles (Table 1). A sufficient stable external clock signal ensures correct encoding. The generated clock frequency in the GENLOCK mode may deviate by ±7% depending on the reference signal which is corresponding to its input sync signal. The clock will be nominal in the GENLOCK mode when the reference signal is absent (nominal with crystal oscillator accuracy for TV time constants, and nominal ±1.4% for VCR time constants).

The on-chip colour conversion matrix provides "*CCIR 601"* code-compatible transcoding of RGB to YUV data.

RGB data out of bounds, with respect to *"CCIR 601"* specification, can be clipped to prevent over-loading of the colour modulator. RGB data input can be either in linear colour space or in gamma-corrected colour space.

YUV data must be gamma-corrected in accordance with "*CCIR 601"*. This circuit operates primarily in a 24-bit colour space (3 × 8-bit) but can also accommodate different data formats (4 : 1 : 1, 4 : 2 : 2 and 4 : 4 : 4) plus 8-bit indexed pseudo-colour space operations (FMT-bits in Table 8).

RGB CLUTs on-chip provide gamma-correction and/or other CLUT functions. They consist of programmable tables to be loaded independently, and they generate 24-bit gamma-corrected output signals from 24-bit data of one of the input formats or from 8-bit indexed pseudo-colour data.

Required modulation is performed. The digital YUV data is encoded in accordance with standards *"RS-170A*" (composite NTSC) and *"CCIR 624-4*" (composite PAL-B/G). S-video output signal is available (Y/C) also some sub-standard output signals (STD-bits in Table 12).

A 7.5 IRE set-up level is automatically selected in the 60 Hz mode, but not selected in the 50 Hz mode.

The analog signal outputs can drive directly into terminated 75 Ω coaxial lines, a passive external filter is recommended (Figs 3, 13 and 14). Analog post-filtering is required (LP in Fig.3).

GENLOCK to an external reference signal is achieved by addition of a video ADC and a clock generator combination. Thus, the system is enabled to lock on a stable video source or to a stable VCR source (normal playback). The SAA7199B, the ADC and the clock generator combination (Fig.3) form a control loop achieving a highly stable line-locked clock. The clock has to be generated by a crystal oscillator without this availability. The GENLOCK mode is not available in a single device set-up.

Control interface

The SAA7199B supports a standard parallel MPU interface and the serial I^{2}C-bus interface. The MPU has direct access to internal control registers and colour tables. Update is possible at any time, excluding coincident internal reading and external writing of the same cell (the current pixel value could be destroyed).

The two interfaces of Table 2 are selected automatically. However, the I^{2}C-bus control is inactive when the MPU interface is selected by $\overline{CS}$ = LOW. No simultaneous access may occur. I^{2}C-bus and MPU control complement each other and have access to common registers controlled via a common internal bus. The programmer can use virtually identical programs.

The internal memory space is devided into the look-up table and the control table, each with its own 8-bit address register used as a pointer for specific location.
This address register is provided with auto-incrementation and can be written by only one addressing.

The look-up table contains three banks of 256 bytes. Therefore, each read or write cycle must access all three banks in a pre-determined order. The support logic is part of the control interface.

Timing (see Fig.3)

The reference to generate internal clocks from LLC in GENLOCK operation with SAA7197 is CREF

$$CREF = \frac{LLC}{2}.$$

In this event input CLKSEL is HIGH and the SRC-bit = 1.

In non-GENLOCK operation the signal from CLKIN is used and LDV is clock reference (input CLKSEL = 0; SCR-bit = CPR-bit = 0).

Pins LLC and CLKIN are tied together when no switching between LLC and CLKIN is applied. In Fig.3 it is assumed that LLC and CLKIN are double the pixel clock frequency of CREF and LDV respectively.

CREF must be at the same frequency (or constant HIGH or LOW) when LLC is at pixel clock frequency. CPR-bit = 1 if CLKIN is at pixel clock frequency.

The buffered CLKO signal is always delayed. LLC or CLKIN signals are in accordance with CLKSEL.

Mapping

The method of mapping external control signals on to the internal bus is simple. The MPU-bus contains the signals as shown in Table 4 (names in chip-internal nomenclature).

Bit allocation

The Bit Allocation Map (BAM) shows the individual control signals, used to control the different operational modes of the circuit. The I^2C-bus is normally used for control. The SAA7199B also has an MPU-bus interface for direct microcontroller connection. The BAM shown in Table 6 resembles the I^2C-bus type but can be also used for the parallel bus; the control registers are indexed from 00H to 0FH. Auto-incrementation is applied.

Digital-to-analog converters

The converters use a combination of resistor chains with low-impedance output buffers. The bottom output voltage is 200 mV to reduce integral non-linearity errors. The analog signal, without load on output pin, is between 0.2 and 2.2 V. Figure 16 shows the application for 1.23 V/75 Ω outputs, using the serial 25 + 22 Ω resistors.

Each digital-to-analog converter has its own supply pin for the purpose of decoupling. V_{DDA4} is the supply voltage for the resistor chains of the three DACs. The accuracy of this supply voltage directly influences the output amplitudes. The current CUR into pin 71 is 0.3 mA (V_{DDA4} = 5 V; R_{64-71} = 20 kΩ); a larger current improves the bandwidth but increases the integral non-linearity.

Table 1 Pixel relationships

ACTIVE PIXELS PER LINE	FIELD RATE (Hz)	MULTIPLES OF LINE FREQUENCY	PIXCLK OUTPUT SIGNAL (MHz)	CRYSTAL (MHz)
640 (square)	60	780	12.27	26.8
720	60	858	13.5	24.576
768	50	944	14.75	26.8
720	50	864	13.5	24.576

Table 2 Access to the control interface

SYMBOL	DESCRIPTION
SDA	I^2C-bus serial data line (bidirectional)
SCL	I^2C-bus clock line
A1, A0	MPU-bus address inputs
$R/\overline{W}$	read/write control input
$\overline{CS}$	chip select input; I^2C-bus disabled when LOW
GPSW	general purpose switch output (bit of control register)
$\overline{RESET}$	reset input signal; active-LOW

Table 3 Address assignment

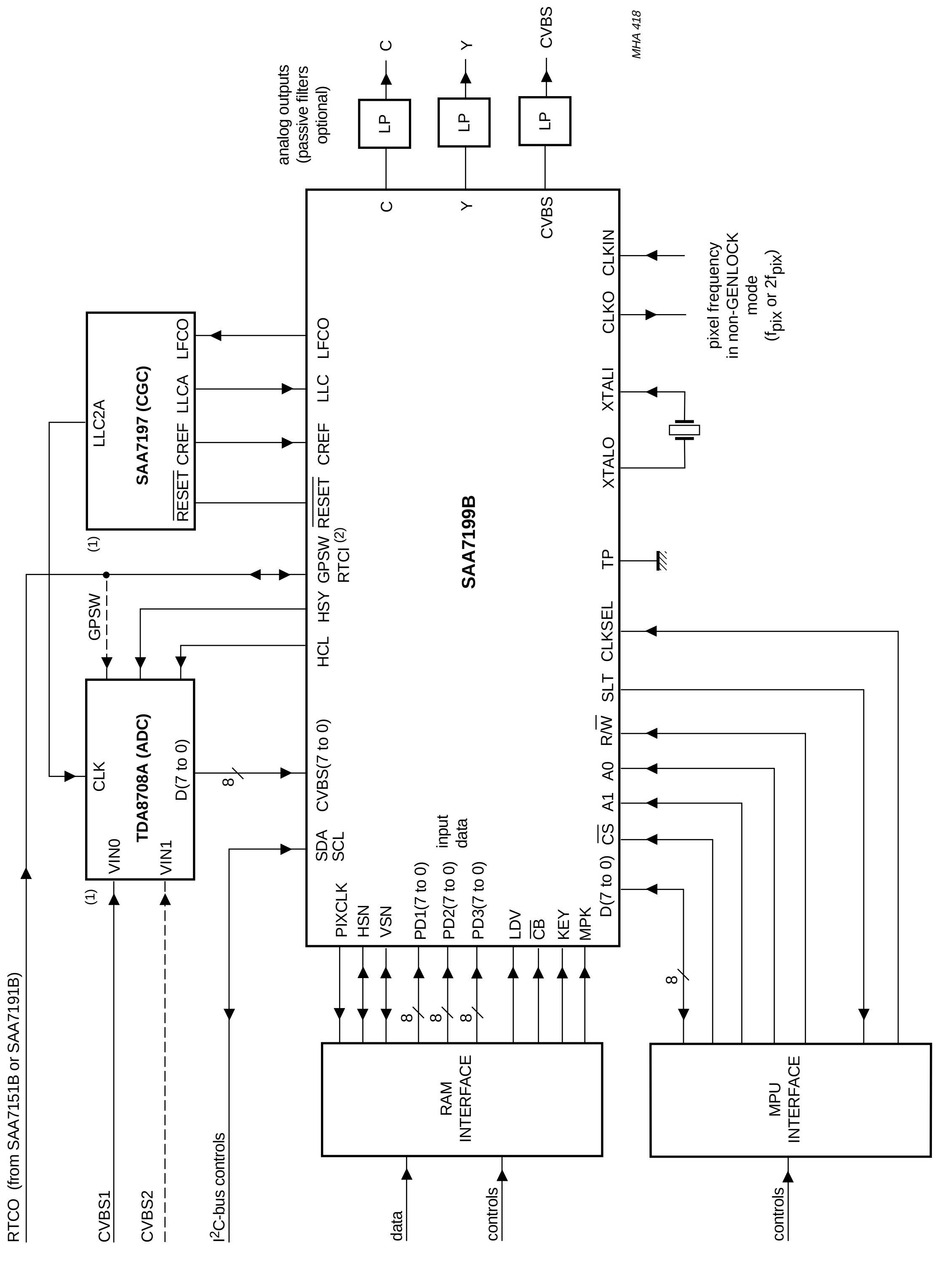
ADDRESS INPUTS		I^2C-BUS SUBADDRESS	SELECTION
A1	**A0**		
0	0	00	ADR-CLUT (address register of look-up tables)
0	1	01	DATA-CLUT
1	0	02	ADR-CTRL (index register of control table)
1	1	03	DATA-CTRL

Table 4 Signals on the internal bus

SYMBOL	DESCRIPTION
$R/\overline{W}$	select read/write (read = 1; write = 0)
$C/\overline{T}$	control table/look-up table (control table = 1; look-up table = 0)
$D/\overline{A}$	select data/address (data = 1; address = 0)
DI/DO (0 to 7)	data bus on port inputs/outputs D7 to D0
EN	enable from control interface to synchronize data transfer

Table 5 Signals on the internal bus

INTERNAL PARALLEL BUS	PARALLEL INTERFACE	I^2C-BUS INTERFACE
$R/\overline{W}$	$R/\overline{W}$ (pin 35)	LSB of slave address byte (read = HIGH; write = LOW)
$C/\overline{T}$	A1 (pin 34)	X 4 subaddresses after decoding
$A/\overline{T}$	A0 (pin 33)	X 4 subaddresses after decoding
DI/DO (0 to 7)	D7 to D0	data bits D7 to D0 for each subaddress
EN	$\overline{CS}$ and $R/\overline{W}$	enable by every 9th clock of sample of SCL (control of serial-to-parallel conversion)



(1) Not necessary in GENLOCK mode.
(2) RTCI optional (GPSW not possible).

Fig.3 System configuration.

Table 6 Bit allocation map (I^2C-bus access in Table 17)

INDEX		DATA BYTE								DF[1]
BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0	
Input processing										
0000 0000	00	VTBY	FMT2	FMT1	FMT0	SCBW	CCIR	MOD1	MOD0	5C
0000 0001	01	TRER7	TRER6	TRER5	TRER4	TRER3	TRER2	TRER1	TRER0	XX
0000 0010	02	TREG7	TREG6	TREG5	TREG4	TREG3	TREG2	TREG1	TREG0	XX
0000 0011	03	TREB7	TREB6	TREB5	TREB4	TREB3	TREB2	TREB1	TREB0	XX
Sync processing										
0000 0100	04	SYSEL1	SYSEL0	SCEN	VTRC	NINT	HPLL	HLCK[2]	OEF[2]	10
0000 0101	05	0	0	GDC5	GDC4	GDC3	GDC2	GDC1	GDC0	21
0000 0110	06	IDEL7	IDEL6	IDEL5	IDEL4	IDEL3	IDEL2	IDEL1	IDEL0	52
0000 0111	07	0	0	PSO5	PSO4	PSO3	PSO2	PSO1	PSO0	32
Control, clock and output formatter										
0000 1000	08	DD	KEYE	SRC	CPR	COKI	IM	GPSW	SRSN	64
0000 1001	09	0	BAME	MPKC1	MPKC0	IEPI	RTSC	RTIN	RTCE	02
0000 1010[3]	0A[3]	0	0	0	0	0	0	0	0	00
0000 1011[3]	0B[3]	0	0	0	0	0	0	0	0	00
Encoder control										
0000 1100	0C	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0	XX[4]
0000 1101	0D	FSCO7	FSCO6	FSCO5	FSCO4	FSCO3	FSCO2	FSCO1	FSCO0	00
0000 1110	0E	0	0	0	CLCK[2]	STD3	STD2	STD1	STD0	0C
0000 1111[3]	0F[3]	0	0	0	0	0	0	0	0	

Notes

1. DF is the default value for a typical programming example: GENLOCK mode for a VCR; non-gamma-corrected RGB data (real time keying is possible). SLT will be set if there is no horizontal lock.NTSC-M standard with normal colour bandwidth and 12.2727 MHz pixel rate. CSYN signal will be provided, arriving 8 pixel clocks earlier, to compensate pipeline delay in the previous RAM interface. The encoded CVBS is 12 clocks earlier than the CVBS reference on the input of the previous ADC. The CLUTs are bypassed at MPK = HIGH in real time.
2. Read only bits.
3. Reserved.
4. Adjust as required.

Table 7 Function of registers bits of Table 6

BIT	FUNCTION
Index 00 VTBY	video look-up table by-pass: 0 = not bypassed; 1 = bypassed (logically OR-ed with MPK)
FMT2 to FMT0	input formats see Table 8
SCBW	chrominance bandwidth: 0 = enhanced; 1 = standard
CCIR	select level: 0 = DMSD2 levels; 1 = CCIR levels
MOD1 to MOD0	select mode see Table 9
Index 01 TRER7 to TRER0	test register red (read/write via MPU-bus; write only via I^2C-bus)
Index 02 TREG7 to TREG0	test register green (read/write via MPU-bus; write only via I^2C-bus)
Index 03 TREB7 to TREB0	test register blue (read/write via MPU-bus; write only via I^2C-bus)
Index 04 SYSEL1 to SYSEL0	sync select see Table 10
SCEN	sync/clamping (HSY/HCL) enable: 0 = disabled (set to HIGH); 1 = enabled
VTRC	select TV/VTR mode: 0 = TV mode (slow); 1 = VTR mode (fast)
NINT	select interlace of encoded signal: 0 = interlaced (262.5/262.5 or 312.5/312.5); 1 = non-interlaced (262/262 or 312/312 in modes 1 and 3 only)
HPLL	select horizontal lock: 0 = lock enabled; 1 = lock disabled (crystal reference)
OEF	status bit field organization (to be read): 0 = even field; 1 = odd field
HLCK	status bit sync indication (to be read): 0 = locked to external sync; 1 = external sync lost
Index 05 GDC5 to GDC0	GENLOCK delay compensation; note 1: data 00 to 3F equals timing of CVBS output signal which is (46 – GDC) pixel clocks = t_{ofs} earlier with respect to reference point t_{REF1}. (t_{REF1} corresponds to the falling edge of the horizontal sync pulse of CVBS input signal; t_{ofs} is designated for propagation delay of external GENLOCK source, Fig.10).
Index 06 IDEL7 to IDEL0	increment delay: update of line-locked clock frequency (Table 6, data ‘43’ hex recommended)
Index 07 PSO7 to PSO0	Phase sync in output signal, note 1: data 00 to 3F equals to active slope of HSN, VSN/CSYN is (58 – PSO) pixel clocks = t_{Rint} earlier with respect to reference point t_{REF2} (t_{REF2} corresponds to PSO = 58; t_{Rint} is designated for pipeline delay of the feeding RAM interface, Fig.10).
Index 08 DD	digital video encoder disable: 0 = enabled; 1 = disabled
KEYE	keying enable: 0 = disabled; 1 = enabled (logically AND-connected with KEY)
SRCC	clock source: 0 = external system clock; 1 = DTV2 system clock
CPR	clock phase reference: 0 = LDV is input (pin 20); 1 = LDV is not
COKI	colour-killer: 0 = colour on; 1 = colour off (subcarrier is switched off)
IM	interrupt mask: 1 = interrupt not masked at sync lost (pin 58) 0 = interrupt masked at sync lost (pin 58)
GPSW	general purpose switch at bit RTIN = 1: 0 = pin 57 LOW; 1 = pin 57 HIGH
SRSN	software reset: 0 = no reset; 1 = reset (see “Reset” procedure)
Index 09 BAME	Burst amplitude indication: 0 = burst amplitude measurement is overridden; colour lock always assumed; 1 = burst amplitude is used to control the CLCK status bit, recommended for reference signal without subcarrier burst (pure black and white) in order to avoid PLL hunting.
MPKC1 to MPKC0	multipurpose key control: with MKP = LOW (pin 32) all functions are as given by software programming; MKP = HIGH sets in real time with respect to PDn (7 to 0); functions see Table 11

BIT	FUNCTION
IEPI	polarity of external PAL-ID signal (H/2 signal) from RTCI input (pin 57): 0 = not inverted; 1 = inverted
RTSC	Real time select control: 0 = real time control HPLL increment is selected, which means, information concerning actual clock frequency from the digital colour decoder is received (SAA7151B or SAA7191B); the corresponding subcarrier frequency is calculated; 1 = real time control FSC increment with PAL-ID is selected, which means, information concerning actual subcarrier frequency and PAL-ID from the digital colour decoder is received (SAA7151B or SAA7191B).
RTIN	select real time control input: 0 = pin 57 is input for RTCI signal; 1 = pin 57 is port output GPSW
RTCE	real time control enabled: 0 = disabled; 1 = enabled (RTIN = 0)
Index 0C CHPS7 to CHPS0	phase adjustment between chrominance output signal and reference: 00 to FF equals 0 to 358.59375 degrees in steps of 1.40625 degrees
Index 0D FSC7 to FSC0	fine adjustment of subcarrier frequency in non-GENLOCK modes: 00 to 7F increasing and FF to 80 decreasing equal approximately to 450×10^{-6} of the subcarrier frequency in 256 steps
Index 0E CLCK	lock to external chrominance (to be read): 0 = possible; 1 = not possible
STD3 to STD0	colour encoding standards; see Table 12
–	status bits to be read via I^2C-bus: see Table 15
–	status bits to be read by microcontroller: all registers from 00 up to 0F can be read via MPU-bus, read only bits are OEF, HCLK (index 04) and CLCK (index 0E)

Note

1. Field blanking (Figs 11 and 12): normally, video to be encoded should not become active after the active edge of VSN or CSYN before line 22.5 at 50 Hz (line 18 at 60 Hz). Total internal field blanking is 11 lines at 50 Hz (13 lines at 60 Hz).

Table 8 Input formats

FMT2	FMT1	FMT0	FORMAT
0	0	0	YUV 4 : 1 : 1 format; DMSD2 compatible
0	0	1	YUV 4 : 1 : 1 format; customized
0	1	0	YUV 4 : 2 : 2 format; DMSD2 compatible
0	1	1	YUV 4 : 2 : 2 format; customized
1	0	0	YUV 4 : 4 : 4 format
1	0	1	RGB 4 : 4 : 4 format
1	1	0	reserved
1	1	1	8-bit indexed colour

Table 9 Select mode

MOD1	MOD0	MODE
0	0	GENLOCK mode
0	1	stand alone mode
1	0	slave mode
1	1	test mode

Table 10 Sync select

SYSEL1	SYSEL0	SYNCHRONIZED FROM
0	0	CSYN (active LOW; pin 3)
0	1	HSN and VSN (active LOW; pins 84 and 3)
1	0	CSYN (active HIGH; pin 3)
1	1	HSN and VSN (active HIGH; pins 84 and 3)

Table 11 Multi-purpose key control

SET BY BITS		IN FUNCTION BLOCKS INPUT FORMATTER	CLUTs	MATRIX	LEVEL MATCHING
MPKC1	MPKC0				
0	0	control via CCIR bit and FMT bits	bypass	control via FMT bits	control via CCIR bit
0	1	format 5 (RGB) CCIR level	active, no indexed colour	active	CCIR level
1	X	format 7 (indexed colour) CCIR level	active, no indexed colour	active	CCIR level

Table 12 Colour encoding standards

STD3	STD2	STD1	STD0	STANDARD
0	0	0	0	NTSC 4.43; 60 Hz; SQP (12.27 MHz)
0	0	0	1	NTSC 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	0	PAL-B/G 4.43; 50 Hz; SQP (14.75 MHz)
0	0	1	1	NTSC 4.43; 60 Hz; CCIR (13.5 MHz)
0	1	0	0	NTSC 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	0	1	PAL-B/G 4.43; 50 Hz; CCIR (13.5 MHz)
0	1	1	0	reserved
0	1	1	1	reserved
1	0	0	0	PAL-M; 60 Hz; SQP (12.27 MHz)
1	0	0	1	PAL-M; 60 Hz; CCIR (13.5 MHz)
1	0	1	0	PAL-N; 50 Hz; CCIR (13.5 MHz)
1	0	1	1	PAL-N; 50 Hz; SQP (14.75 MHz)
1	1	0	0	NTSC-M; 60 Hz; SQP (12.27 MHz)
1	1	0	1	NTSC-M; 60 Hz; CCIR (13.5 MHz)
1	1	1	0	reserved
1	1	1	1	reserved

Colour look-up tables (CLUTs)

The CLUTs consist of RAM tables. The RAM tables can be loaded with X = 0 to 255 in accordance with equation 1 for the signals R, G and B. Gamma-correction (pre-distortion) by the following equation:

$Y = NINT(b + a \times X1^{1/g})$; $Y(X \leq 16) = 16$; $Y(X \geq 235) = 235$ (equation 1) with g = 2.2: $a = \frac{219}{235^{-2.2} - 16^{-2.2}}$; $b = 16 - a \times 16^{-2.2}$

The RAM tables are loaded via MPU-bus or via I^2C-bus (Table 17).

I^2C-bus format

Table 13 I^2C-bus address; see Table 14

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 14 Explanation of Table 13

PART	DESCRIPTION
S	START condition
Slave address	1 0 1 1 0 0 0 X (note 1)
ACK	acknowledge, generated by the slave
Subaddress (note 2)	subaddress byte (Table 17)
DATA	data byte (Table 6)
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = 0 is order to write (the circuit is slave receiver); X = 1 is order to read (the circuit is slave transmitter).
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

Table 15 I^2C-bus status byte (address byte B1)

FUNCTION	STATUS BYTE							
	D7	D6	D5	D4	D3	D2	D1	D0
Read status	0	0	0	0	FFOS	OEF	CLCK	HLCK

Table 16 Function of the bits in Table 15

BIT	FUNCTION
FFOS	first field of sequence: 0 = false; 1 = first of 4 fields for NTSC (first of 8 fields for PAL). FFOS is not valid for non-interlaced signals.
OEF	field organization: 0 = even field; 1 = odd field
CLCK	lock to external chrominance: 0 = possible; 1 = not possible
HLCK	sync indication: 0 = locked to external sync; 1 = external sync lost

Table 17 I^2C-bus write bytes (address byte B0)

ACCESS	DESCRIPTION OF BYTE			
Control registers	address byte B0	subaddress byte 02	index byte (00 to 0F); Table 6	data bytes (auto-increment)
CLUTs registers	address byte B0	subaddress byte 00	CLUT address bytes (00 to FF)	3 data bytes for one RGB sequence (auto-increment)

Modes of the SAA7199B

Table 18 The four different modes of the SAA7199B

MODE	DESCRIPTION
Stand alone	The SAA7199B receives a line-locked clock CLKIN and generates CSYN or HSN/VSN output signals, which trigger the RGB or the YUV source signal to provide data and composite blanking $\overline{CB}$.
Slave	The SAA7199B receives the line-locked clock CLKIN, CSYN or HSN/VSN, $\overline{CB}$ and data from an RGB or YUV source. The sync inputs are edge-sensitive; their minimum active length is 1 PIXCLK. A real time control signal RTCI is received from a digital colour decoder as an option.
GENLOCK	Horizontal and vertical sync plus colour are locked on a received CVBS reference signal. The CVBS reference signal also generates a line-locked clock by the SAA7197 clock generator. Auxiliary signals HCL and HSY plus CSYN or HSN/VSN are generated to trigger the RGB or the YUV source providing data and composite blanking $\overline{CB}$.
Test	Similar to stand alone mode, but the contents of the test registers TRER, TREG and TREB consists of data to be encoded. VSN/CSYN and HSN outputs are in 3-state condition.

RELATIONSHIP BETWEEN HORIZONTAL FREQUENCY AND COLOUR SUBCARRIER FREQUENCY IN NON-GENLOCK MODE

1. Internal subcarrier frequency with n = integer

   PAL: $f_{SC} = f_H$ (n/4 + 1/625) respectively f_H (n/4 + 1/525)

   NTSC: $f_{SC} = f_H$ (n/2)

   Necessary conditions: non-GENLOCK mode; RTCE = 0, FSCO = 00H; phase coupling of the two frequencies is given by a definite phase reset every 8th field at PAL (4th field at NTSC).

   FSCO ≠ 00H adjusts the subcarrier frequency, phase reset is disabled and phase between f_{SC} and f_H is not constant.

2. External subcarrier frequency

   f_{SC} is given by RTCI real time input from a digital colour decoder

   Necessary conditions: Slave mode; RTCE = 1, RTSC = 1. The 8th respectively 4th field reset is enabled at FSCO = 00H (disabled at FSCO ≠ 00H). The subcarrier frequency is not influenced by FSCO bits, but is given by real time increment.

3. External HPLL increment

   f_{SC} is calculated by RTCI real time input signal from a digital colour decoder. The frequency of f_{SC} depends on the absolute crystal frequency value used by the digital colour decoder.

   Necessary conditions: Slave mode; RTCE = 1, RTSC = 0. The 8th respectively 4th field reset is enabled at FSCO = 00H (disabled at FSCO ≠ 00H). The subcarrier frequency is influenced by FSCO bits.

The absolute phase relationship between sync and subcarrier (colour burst output) can be influenced in all three events by CHPS7 to CHPS0 register byte (index 0C).

Data input formats

One clock cycle equals 12.27 MHz, 13.5 MHz or 14.75 MHz; Cb = (B – Y) equals U; Cr = (R – Y) equals V; (n) = number of pixels.

Table 19 Format 0; DMSD2 compatible YUV 4 : 1 : 1 format (FMT-bits in index 00 = 000)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cb5(0)	Cb3(0)	Cb1(0)	Cb7(4)	Cb5(4)	Cb3(4)	Cb1(4)
PD3(6)	Cb6(0)	Cb4(0)	Cb2(0)	Cb0(0)	Cb6(4)	Cb4(4)	Cb2(4)	Cb0(4)
PD3(5)	Cr7(0)	Cr5(0)	Cr3(0)	Cr1(0)	Cr7(4)	Cr5(4)	Cr3(4)	Cr1(4)
PD3(4)	Cr6(0)	Cr4(0)	Cr2(0)	Cr0(0)	Cr6(4)	Cr4(4)	Cr2(4)	Cr0(4)
PD3(3 to 0)	not used							
PD1(7 to 0)	not used							

Table 20 Format 1; customized YUV 4 : 1 : 1 format (FMT-bits in index 00 = 001)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	–	Cr7(0)	–	Cb7(4)	–	Cr7(4)	–
PD3(6)	Cb6(0)	–	Cr6(0)	–	Cb6(4)	–	Cr6(4)	–
PD3(5)	Cb5(0)	–	Cr5(0)	–	Cb5(4)	–	Cr5(4)	–
PD3(4)	Cb4(0)	–	Cr4(0)	–	Cb4(4)	–	Cr4(4)	–
PD3(3)	Cb3(0)	–	Cr3(0)	–	Cb3(4)	–	Cr3(4)	–
PD3(2)	Cb2(0)	–	Cr2(0)	–	Cb2(4)	–	Cr2(4)	–
PD3(1)	Cb1(0)	–	Cr1(0)	–	Cb1(4)	–	Cr1(4)	–
PD3(0)	Cb0(0)	–	Cr0(0)	–	Cb0(4)	–	Cr0(4)	–
PD1(7 to 0)	not used							

Table 21 Format 2; DMSD2 compatible YUV 4 : 2 : 2 format (FMT-bits in index 00 = 010)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7)	Cb7(0)	Cr7(0)	Cb7(2)	Cr7(2)	Cb7(4)	Cr7(4)	Cb7(6)	Cr7(6)
PD3(6)	Cb6(0)	Cr6(0)	Cb6(2)	Cr6(2)	Cb6(4)	Cr6(4)	Cb6(6)	Cr6(6)
PD3(5)	Cb5(0)	Cr5(0)	Cb5(2)	Cr5(2)	Cb5(4)	Cr5(4)	Cb5(6)	Cr5(6)
PD3(4)	Cb4(0)	Cr4(0)	Cb4(2)	Cr4(2)	Cb4(4)	Cr4(4)	Cb4(6)	Cr4(6)
PD3(3)	Cb3(0)	Cr3(0)	Cb3(2)	Cr3(2)	Cb3(4)	Cr3(4)	Cb3(6)	Cr3(6)
PD3(2)	Cb2(0)	Cr2(0)	Cb2(2)	Cr2(2)	Cb2(4)	Cr2(4)	Cb2(6)	Cr2(6)
PD3(1)	Cb1(0)	Cr1(0)	Cb1(2)	Cr1(2)	Cb1(4)	Cr1(4)	Cb1(6)	Cr1(6)
PD3(0)	Cb0(0)	Cr0(0)	Cb0(2)	Cr0(2)	Cb0(4)	Cr0(4)	Cb0(6)	Cr0(6)
PD1(7 to 0)	not used							

Table 22 Format 3; customized YUV 4 : 2 : 2 format (FMT-bits in index 00 = 011)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7 to 0)	Cb(0)	–	Cb(2)	–	Cb(4)	–	Cb(6)	–
PD1(7 to 0)	Cr(0)	–	Cr(2)	–	Cr(4)	–	Cr(6)	–

Table 23 Format 4; YUV 4 : 4 : 4 format (FMT-bits in index 00 = 100)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
PD3(7 to 0)	Cb(0)	Cb(1)	Cb(2)	Cb(3)	Cb(4)	Cb(5)	Cb(6)	Cb(7)
PD1(7 to 0)	Cr(0)	Cr(1)	Cr(2)	Cr(3)	Cr(4)	Cr(5)	Cr(6)	Cr(7)

Table 24 Format 5; RGB 4 : 4 : 4 format (FMT-bits in index 00 = 101)

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)
PD3(7 to 0)	G(0)	G(1)	G(2)	G(3)	G(4)	G(5)	G(6)	G(7)
PD1(7 to 0)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)

Table 25 Format 7; indexed colour format (FMT-bits in index 00 = 111), input codes 0 to 255 are allowed, output code of CLUTs should preferably be the same as given in format 5

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
PD2(7 to 0)	INC(0)	INC(1)	INC(2)	INC(3)	INC(4)	INC(5)	INC(6)	INC(7)

Table 26 Input data levels for formats 0 to 4 and 5; EBU colour bar; 100% white equals 100 IRE intensity, 5% colour saturation for formats 1 to 4, 100% for format 5

INPUT CHANNEL	LEVEL	DIGITAL LEVEL	CODE	CCRIR-BIT	FORMAT
Y	0 IRE	12	offset binary	0	0 to 4
	100 IRE	230			
Cb	bottom peak	–101	two’s complement	0	0 to 4
	colourless	0			
	top peak	100			
Cr	bottom peak	–106	two’s complement	0	0 to 4
	colourless	0			
	top peak	105			
Y	0 IRE	16	offset binary	1	0 to 4
	100 IRE	235			
Cb	bottom peak	44	offset binary	1	0 to 4
	colourless	128			
	top peak	212			
Cr	bottom peak	44	offset binary	1	0 to 4
	colourless	128			
	top peak	212			
R, G and B	0 IRE	16	offset binary	1	5
	100 IRE	235			

GENLOCK INPUT DATA

Table 27 Format 7; CVBS GENLOCK input data format has an 8-bit word length, the input data comes from an analog-to-digital converter (TDA8708) with gain controlled and clamped CVBS or VBS signals

INPUT SIGNAL	CLOCK CYCLE (PIXEL SEQUENCE)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
CVBS(7-0)	CVBS(0)	CVBS(1)	CVBS(2)	CVBS(3)	CVBS(4)	CVBS(5)	CVBS(6)	CVBS(7)

Conditions of CVBS input signal	two’s complement representation
Sync bottom	corresponding to binary code –128
0 IRE (black)	corresponding to binary code –64[(1)]
100 IRE (white)	corresponding to binary code 95
Top peak of 75% colour	corresponding to binary code 95
Bottom peak of 75% colour	corresponding to binary code –100

Note

1. If exactly matched levels are required in the internal multiplexer, the value 0 IRE should correspond to –68 and 100 IRE to 82.

ENCODING DATA LEVELS

Input data levels are transformed in three stages:

In the matrix when RGB or indexed colour is applied (formats 5 and 7)

In the normalizing amplifier depending on 50/60 Hz mode and CCIR-bit (index 00)

In the modulator.

Table 28 Y and C output levels for RGB input levels (100/100 colour bar)

SIGNAL	INPUT DATA			MATRIX OUTPUT DATA			NORMALIZER OUTPUT DATA			MODULATOR OUTPUT DATA	
	R	G	B	(R – Y)	Y	(B – Y)	V(1)	Y	U	Y	C(2)
Y and C output levels in 50 Hz mode (PAL)											
White	235	235	235	128	235	128	0	421	0	421	0
Yellow	235	235	16	146	210	16	29	387	–132	387	±135
Cyan	16	235	235	16	170	166	–184	332	44	332	±189
Green	16	235	16	34	145	54	–155	297	–87	297	±178
Magenta	235	16	235	221	107	202	152	245	86	245	±175
Red	235	16	16	240	82	90	183	211	–45	211	±188
Blue	16	16	235	110	41	240	–30	154	131	154	±134
Black	16	16	16	128	16	128	0	120	0	120	0
Blanking	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	120	0
Burst	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	45	X(3)	–45	X(3)	±63
Top sync	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	0	X(3)
Y and C output levels in 60 Hz mode (NTSC)											
White	235	235	235	128	235	128	0	416	0	416	0
Yellow	235	235	16	146	210	16	29	385	–132	385	±135
Cyan	16	235	235	16	170	166	–184	335	44	335	±189
Green	16	235	16	34	145	54	–155	303	–87	303	±178
Magenta	235	16	235	221	107	202	152	256	86	256	±175
Red	235	16	16	240	82	90	183	225	–45	225	±188
Blue	16	16	235	110	41	240	–30	173	131	173	±134
Black	16	16	16	128	16	128	0	142	0	142	0
Blanking	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	120	0
Burst	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	0	X(3)	–64	X(3)	±64
Top sync	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	X(3)	0	X(3)

Notes

1. The V component is inverted in the PAL line.
2. The ± are peak values of the subcarrier signal.
3. X = not defined.

CHROMINANCE FILTERING IN THE ENCODER

1. Decimation for 4 : 4 : 4 format input data (formats 4, 5 and 7; Fig.4).
2. Interpolation for 4 : 1 : 1 input data into 4 : 2 : 2 data, also suitable to reduce the bandwidth of 4 : 2 : 2 data. This filter is controlled by the SCBW-bit (SCWB = 1 means active).
3. Interpolation at 13.5 MHz for 4 : 2 : 2 input data into 4 : 4 : 4 data before modulating baseband signals onto the colour subcarrier. Figures 5, 6 and 7 show the overall transfer characteristics of chrominance in “standard bandwidth condition” (SCBW = 1). Figures 8 and 9 show the overall transfer characteristics of chrominance in enhanced bandwidth condition (SCBW = 0), which is not possible for 4 : 1 : 1 input data. The transfer curves are slightly different at 12.27 and 14.75 MHz.

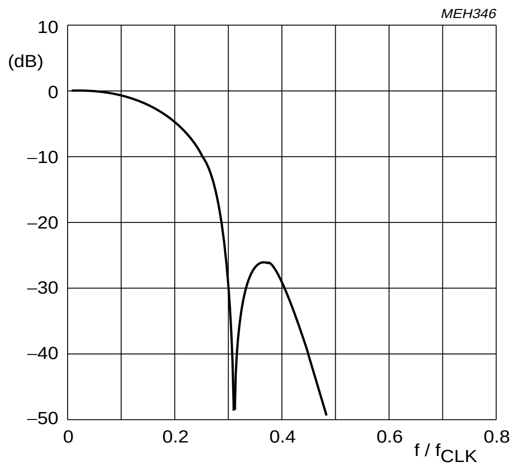


Fig.4 Transfer characteristics of 4 : 4 : 4 to 4 : 2 : 2 decimator.

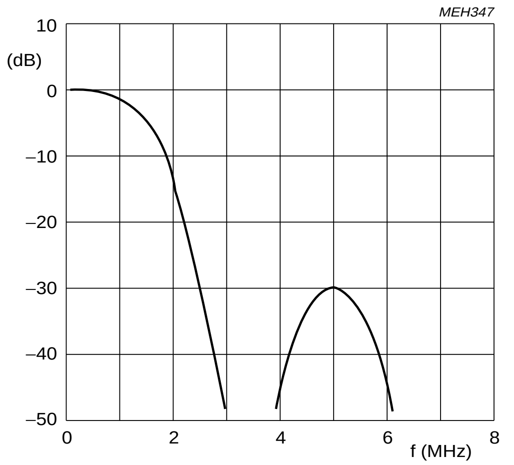


Fig.5 Overall transfer characteristics 4 : 1 : 1 input data.

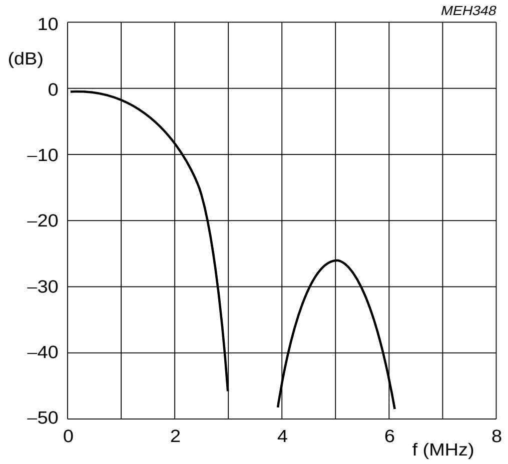


Fig.6 Overall transfer characteristics 4 : 2 : 2 input data (SCBW-bit = 1).

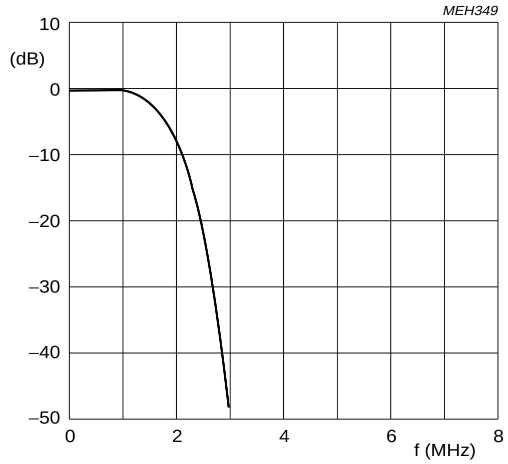


Fig.7 Overall transfer characteristics 4 : 4 : 4 input data (SCBW-bit = 1).

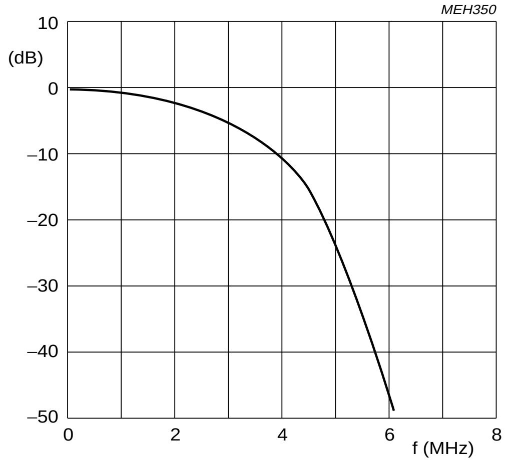


Fig.8 Overall transfer characteristics 4 : 2 : 2 input data (SCBW-bit = 0).

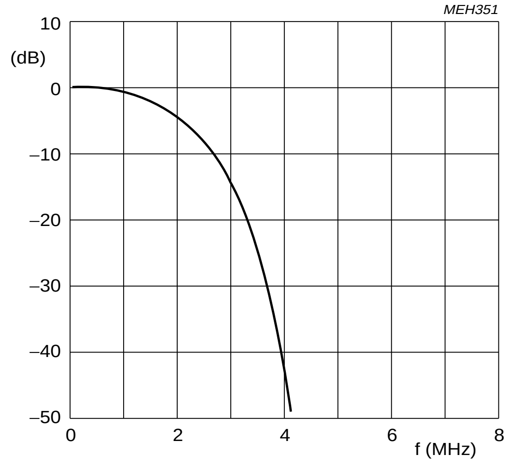


Fig.9 Overall transfer characteristics 4 : 4 : 4 input data (SCBW-bit = 0).

Accuracy of matrix

Evaluation of quantization errors.

The RGB to YUV matrix is achieved in accordance with the following algorithm:

Y = INT [(NINT(R × 2 × 0.299) + NINT(G × 2 × 0.587) + NINT(B × 2 × 0.114) / 2]

U = NINT [(B – Y) × 0.57722]

V = NINT [(R – Y) × 0.72955].

Errors can occur in the calculation of Y, which as a result influence the U and V outputs. The greatest positive error occurs, if in all of the three for Y calculation used ROMs the values are rounded up to 0.5 LSB, and no truncation error of 0.5 LSB is generated after summation:

$$3 \times \frac{0.5\ \text{LSB}}{2} = +0.75\ \text{LSB};$$

with truncation “error”:

$$3 \times \frac{0.5\ \text{LSB}}{2} -0.5\ \text{LSB} = +0.25\ \text{LSB}.$$

The greatest negative error occurs at rounding off in all the three ROMs and by consecutive truncation:

$$3 \times \frac{-0.5\ \text{LSB}}{2} - 0.5\ \text{LSB} = -1.25\ \text{LSB}.$$

As a result, the matrix error can be ±1 digit, which corresponds to approximately ±0.5% differential non-linearity.

Estimation of noise by quantization

The sum of all sqared quantization errors is SS normalized to 220^3 input combinations (3-dimensional colour scale).

SS = 0.187545 LSB^2.

Compared with noise energy for ideal quantization, SSI = $\frac{1}{12}\text{LSB}^2$ results in a deterioration by the conversion matrix of:

D = 10 log (0.187545 × 12) = 3.5 dB (equals 0.5 bit).

If SS is the sum of all squared quantization errors, normalized to 220 input combinations of a grey-scale (R = G = B), then:

SS = 0.12273 LSB^2.

Compared with noise energy for ideal quantization, SSI = $\frac{1}{12}\text{LSB}^2$ results in a deterioration by the conversion matrix of:

D = 10 log (0.12273 × 12) = 1.7 dB (equals 0.25 bit).

Normalizing amplifiers in the luminance channel

The absolute amplification error for 50 Hz non-set-up signals is 0.375%; differential non-linearity is –0.333% (equals –1 LSB).

The absolute amplification error for 60 Hz set-up signals is –1.5%; differential non-linearity is –0.365% (equals –1 LSB).

Normalizing amplifiers in the chrominance channel

The absolute amplification error is approximately ±0.5% with a truncation error of –0.5 LSB.

The subcarrier amplitude for standards with luminance set-up is the same as for the standards without luminance set-up.

Modulator

The absolute amplification error is –0.39%; there is no truncation error.

Functional timing (see Fig.10)

GENLOCK MODE

The encoded signal can be generated earlier with respect to CVBS7 to CVBS0 bits (offset t_{ofs} set by GDC-bits; index 05). The HSN output signal can be generated early by PSO-bits (index 07) with respect to $\overline{\text{CB}}$ to compensate for pipelining delay t_{Rint} of the RAM interface (valid also in stand alone mode).

The horizontal timing is independent of active video at data inputs PDn(7 to 0). The line blanking period on the outputs is set to approximately 12 µs in 50 Hz standards (11 µs in 60 Hz standards).

SLAVE MODE

HSN pin is used as an input. The active edge of the input signal is assumed to fit to the incoming $\overline{\text{CB}}$ signal. Deviations can be compensated in the range of the GCD-bits (index 05).

The t_{enc} time is the total delay from data input to analog CVBS output; it is 55 pixel clock periods long (PIXCLK) plus the propagation delay of the LDV input register regardless of mode and colour standard.

The key input signal is delay compensated with respect to PDn(7 to 0) data input. The generated vertical field and burst blanking sequences are shown in Fig.11 (50 Hz PAL) and Fig.12 (60 Hz NTSC).

Reset

Prior to a reset all outputs are undefined. $\overline{\text{RESET}}$ = LOW sets the circuit into the slave mode.

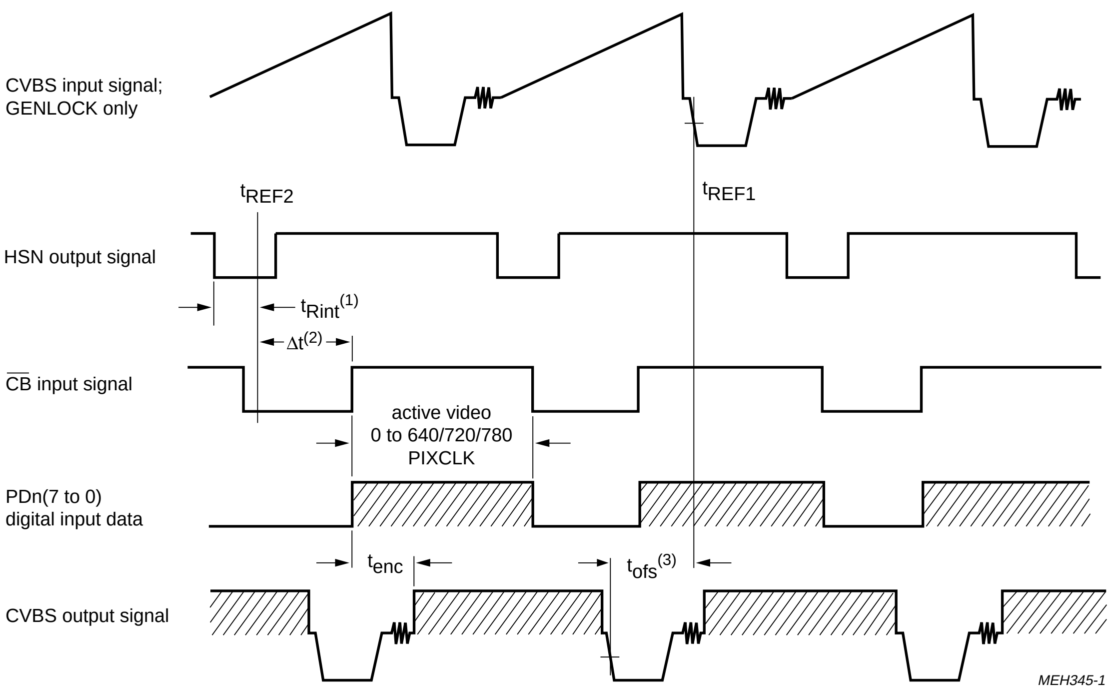
MOD1 bit = 1, MOD0-bit = 0. All other control register bits are set to zero. The outputs CSYN/VSN, HSN, SLT, HSY and HCL are automatically set to a high impedance state.The I^2C-bus interface is set to a slave receiver.

The D7 to D0 pins of the MPU interface are inputs during $\overline{\text{RESET}}$ = LOW. As the circuit requires an external clock signal on pin CLKIN in slave mode, the clock select signal CLKSEL (pin 50) must be LOW during $\overline{\text{RESET}}$ = LOW (pin 54). The LOW time of $\overline{\text{RESET}}$ is at least 50 pixel clock periods long.

Disable chip

All analog outputs are set to zero by DD-bit = 1 (index 08); while the outputs CSYN/VSN, HSN, HCL, HSY and SLT are set to a high impedance state. The internal clock is divided-by-4 at DD-bit = 1. The circuit can be disabled for any reason and it must be disabled when CLKIN exceeds 32 MHz. After setting DD-bit = 1, the CLKIN input signal can be set to a frequency of <60 MHz (modification of control registers and RAM tables is not certain).

To re-enable the circuit, CLKIN must be set to a frequency <32 MHz, a hardware reset is then required to set DD-bit to zero.



(1) t_{Rint} is the pipeline delay of the RAM interface adjustable from –5 to +58 pixel clocks (PIXCLK).

(2) $\Delta t = 125 \times$ PIXCLK at 12.27 MHz
$\Delta t = 163 \times$ PIXCLK at 14.75 MHz
$\Delta t = 134 \times$ PIXCLK at 13.50 MHz in 50 Hz mode
$\Delta t = 122 \times$ PIXCLK at 13.50 MHz in 60 Hz mode.

(3) t_{ofs} is the propagation delay of external GENLOCK line adjustable from –17 to +46 pixel clocks.

Fig.10 Horizontal timing.

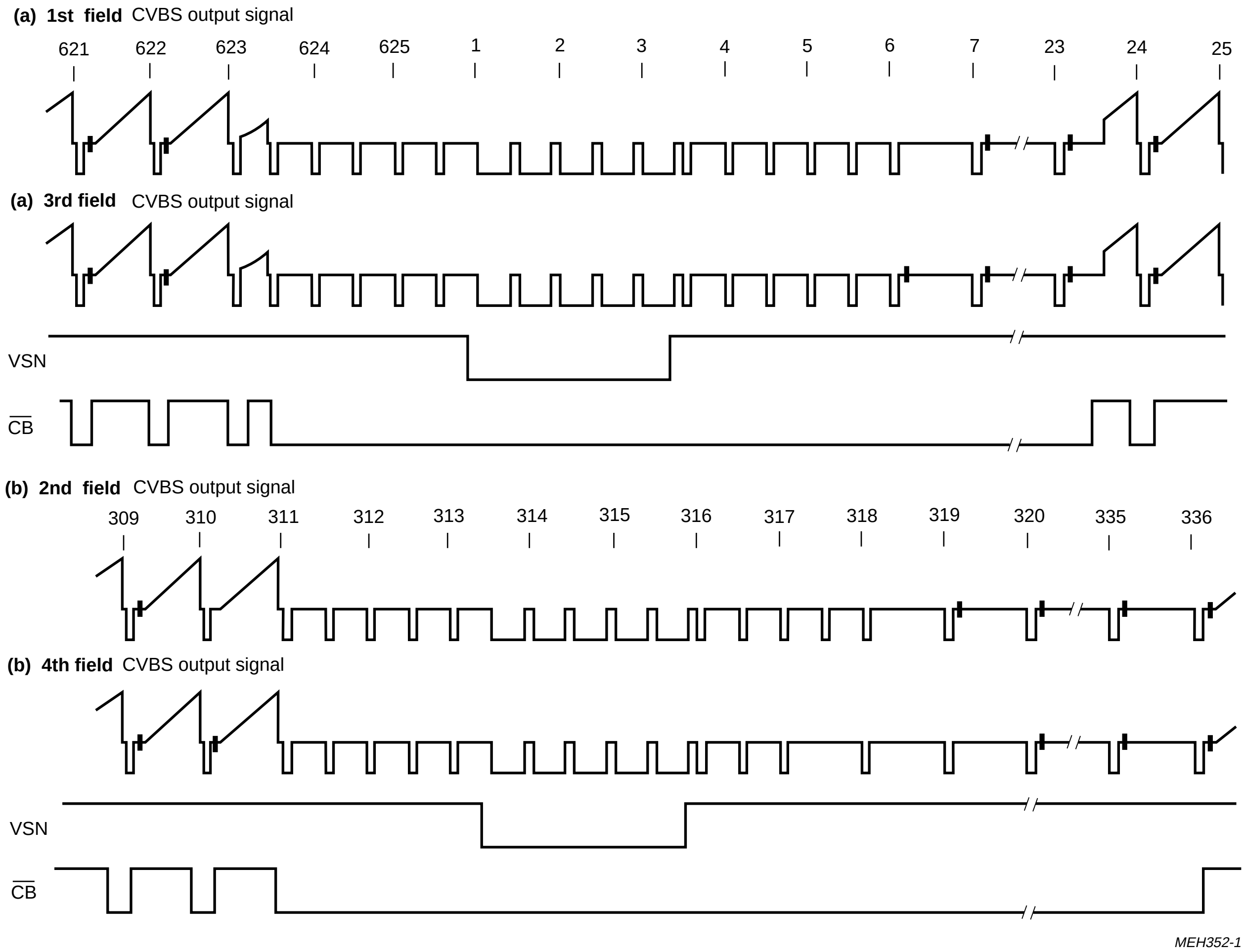


Fig.11 Vertical field and burst blanking sequence for PAL 50 Hz mode.

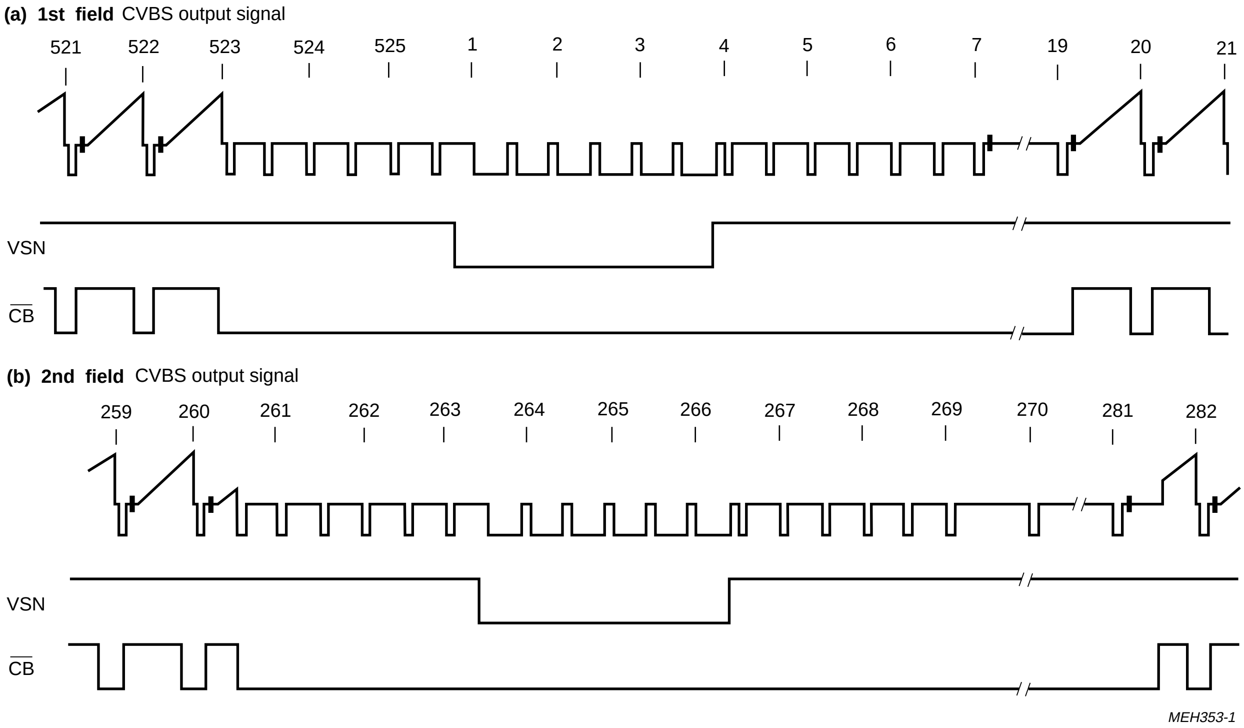


Fig.12 Vertical field and burst blanking sequence for NTSC 60 Hz mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (pin 66)		–0.3	+7	V
V_{DDA2}	analog supply voltage 2 (pin 70)		–0.3	+7	V
V_{DDA3}	analog supply voltage 3 (pin 72)		–0.3	+7	V
V_{DDA4}	analog supply voltage 4 (pin 64)		–0.3	+7	V
V_{DDD1}	digital supply voltage 1 (pin 2)		–0.3	+7	V
V_{DDD2}	digital supply voltage 2 (pin 21)		–0.3	+7	V
V_{DDD3}	digital supply voltage 3 (pin 41)		–0.3	+7	V
$V_{diff(GND)}$	voltage difference between analog and digital ground pins ($V_{SSA} - V_{SSDn}$)		–	±100	mV
V_n	voltage on all pins except grounds		0	V_P	V
P_{tot}	total power dissipation		–	1.1	W
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{esd}	electrostatic handling for all pins	note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDA} = 4.75 to 5.25 V; V_{DDD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pins 64, 66, 70 and 72)		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage (pins 2, 21 and 41)		4.5	5.0	5.5	V
I_{DDA}	analog supply current I_{DDA1} to I_{DDA4}	40 pF output load	–	–	60	mA
I_{DDD}	digital supply current I_{DDD1} to I_{DDD3}	40 pF output load	–	–	140	mA
Data and control inputs (pins 3 to 20, 23 to 40, 43 to 46, 49, 50, 54 to 56, 59, 73 and 76 to 84)						
V_{IL}	LOW level input voltage	note 1	0	–	0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–1	–	+1	µA
C_i	input capacitance					
	data inputs		–	–	8	pF
	CLKIN, LLC and LDV		–	–	10	pF
	3-state I/O		–	–	10	pF
LFCO output (pin 61)						
$V_{o(p-p)}$	output voltage (peak-to-peak value)		1.4	–	2.6	V
V_{61}	output voltage range		0	–	V_{DDD}	V
Data and other control outputs (pins 3, 51, 52, 57, 58, 60, 74 and 75)						
V_{OL}	LOW level output voltage	note 2	0	–	0.6	V
V_{OH}	HIGH level output voltage	note 2	2.4	–	V_{DDD}	V
C, Y and CVBS analog outputs (pins 65, 67 and 69)						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	without load; V_{DDA} = 5 V	–	2	–	V
$V_{o(min)}$	minimum output voltage	without load; V_{DDA} = 5 V	–	0.2	–	V
$V_{o(max)}$	maximum output voltage	without load; V_{DDA} = 5 V	–	2.2	–	V
$R_{o(int)}$	internal serial output resistance	not tested	18	25	35	Ω
R_L	output load resistance	recommendation	90	–	–	Ω
B	output signal bandwidth	–3 dB	10	–	–	MHz
ILE	LF integral linearity error	9-bit data	–	–	±1.0	LSB
DLE	LF differential linearity error	9-bit data	–	–	±0.5	LSB
I_{CUR}	input current (pin 71)	Fig.1; R_{70-71} = 20 kΩ	–	300	–	µA
I^2C-bus SDA and SCL (pins 47 and 48)						
V_{IL}	LOW level input voltage		–0.5	–	+1.5	V
V_{IH}	HIGH level input voltage		3.0	–	V_{DDD} + 0.5	V
I_I	input current	V_I = LOW or HIGH	–10	–	+10	µA
V_{OL}	SDA LOW level output voltage	I_{OL} = 3 mA	–	–	0.4	V
I_O	SDA output current	during acknowledge	3	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator (see Fig.15)						
f_n	nominal frequency	3rd harmonic; Table 1	–	24.576	–	MHz
		3rd harmonic; Table 1	–	26.8	–	MHz
$\Delta f/f_n$	permissible deviation of f_n		–	50	–	10^{-6}
X1 crystal specification						
T_{amb}	ambient temperature range		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_s	series resonance resistance		–	40	80	Ω
C_{mot}	motional capacitance		–20%	1.5	+20%	fF
C_{par}	parallel capacitance		–20%	3.5	+20%	pF
LDV and LLC timing (pins 20 and 55) see Fig.17						
$T_{cy(LLC)}$	LLC cycle time	note 3	31.5	–	44.5	ns
$t_{W(CH)}$	pulse width		40	50	60	%
t_r	rise time		–	–	5	ns
t_f	fall time		–	–	6	ns
$t_{cy(LDV)}$	LDV cycle time		63	–	89	ns
$t_{su(LDV)}$	LDV set-up time		4	–	–	ns
$t_{h(LDV)}$	LDV hold time		10	–	–	ns
PIXCLK and CLKO timing (pins 51 and 52) see Fig.17						
$t_{d(CLK)}$	PIXCLK and CLKO delay time		–	–	25	ns
PD1 to 3(7 to 0), $\overline{CB}$, MPK, KEY and RTCI input timing (pins 4 to 19, 23 to 32, 57 and 73) see Fig.17						
$t_{SU;\,DAT}$	input data set-up time		4	–	–	ns
$t_{HD;\,DAT}$	input data hold time		6	–	–	ns
CVBS(7 to 0), VSN/CSYN and HSN timing (pins 76 to 83, 3 and 84) see Fig.18						
$t_{SU;\,DAT}$	input data set-up time		10	–	–	ns
$t_{HD;\,DAT}$	input data hold time		5	–	–	ns
CREF timing (pin 56) see Fig.18						
$t_{SU(CREF)}$	input set-up time		10	–	–	ns
$t_{h(CREF)}$	input hold time		2	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MPU timing A1, A0, R/$\overline{W}$, $\overline{CS}$, D(7 to 0) (pins 33 to 36, 37 to 40 and 43 to 46) see Fig.19						
$t_{su(ADD)}$	A1 and A0 address set-up time (pins 33 and 34)		4	–	–	ns
$t_{h(ADD)}$	A1 and A0 address hold time		25	–	–	ns
$t_{su(R)}$	R/$\overline{W}$ set-up time (pin 35)		4	–	–	ns
$t_{h(R)}$	R/$\overline{W}$ hold time		25	–	–	ns
$t_{W(CL)}$	$\overline{CS}$ pulse width LOW	note 4	95	–	–	ns
$t_{W(CH)}$	$\overline{CS}$ pulse width HIGH	note 4	95	–	–	ns
$t_{su;DAT}$	data set-up time (D7 to D0)	write mode	80	–	–	ns
$t_{h;DAT}$	data hold time (D7 to D0)	write mode	5	–	–	ns
$t_{d(Q)}$	data output hold time (D7 to D0)	read mode	5	–	–	ns
t_{ZR}	delay to driven ports (D7 to D0)	read mode	5	–	–	ns
$t_{d(ZR)}$	delay to ports valid (D7 to D0)	read mode; note 5	–	–	275	ns
$t_{d(RZ)}$	port outputs disable time (D7 to D0)	read mode	–	–	25	ns
Output timing (pins 3, 74, 75 and 84); see Fig.18						
t_d	output delay time	minimum clock period; note 6	–	20	45	ns

Notes

1. XTALO, XTALI and TP are not characterized with respect to levels; CLKO is characterized up to 32 MHz and PIXCLK up to 16 MHz.
2. Levels are measured with load circuit. LFCO output with 10 kΩ in parallel with 15 pF and other outputs with 1.2 kΩ in parallel with 40 pF at 3 V (TTL load).
3. T_{LLC} must be 63 to 89 ns at CREF = HIGH (pin 56); T_{LLC} = 16.5 ns is only allowed if the multiplexer clock is active.
4. $t_{PIXCLK(min)}$ + 5 ns.
5. 3 × [$t_{PIXCLK(min)}$ + 5 ns].
6. 40 ns at low supply voltage (4 V) and high temperature (70 °C).

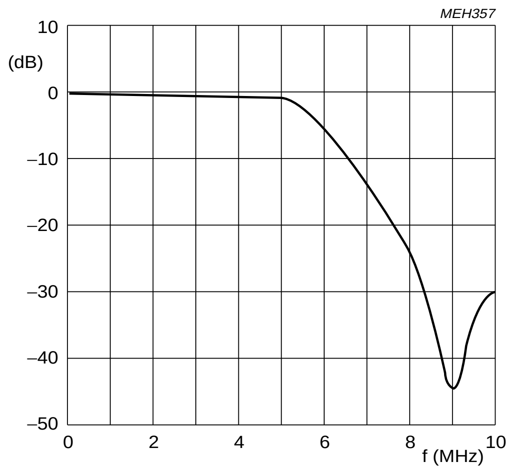


Fig.13 Characteristics of low-pass post-filters; without compensation of DC hold.

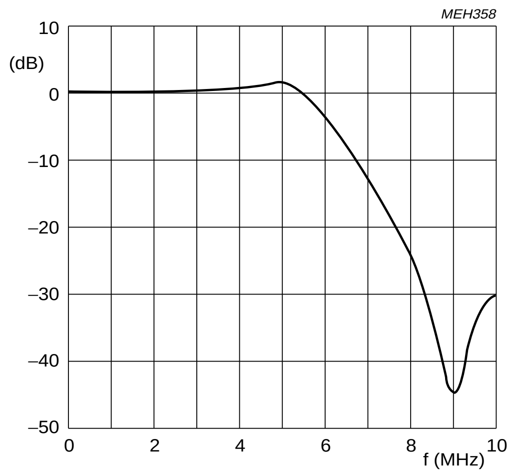
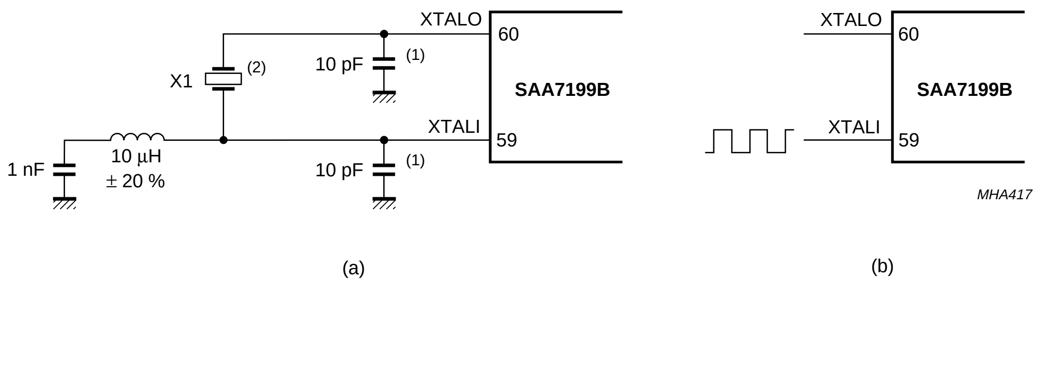


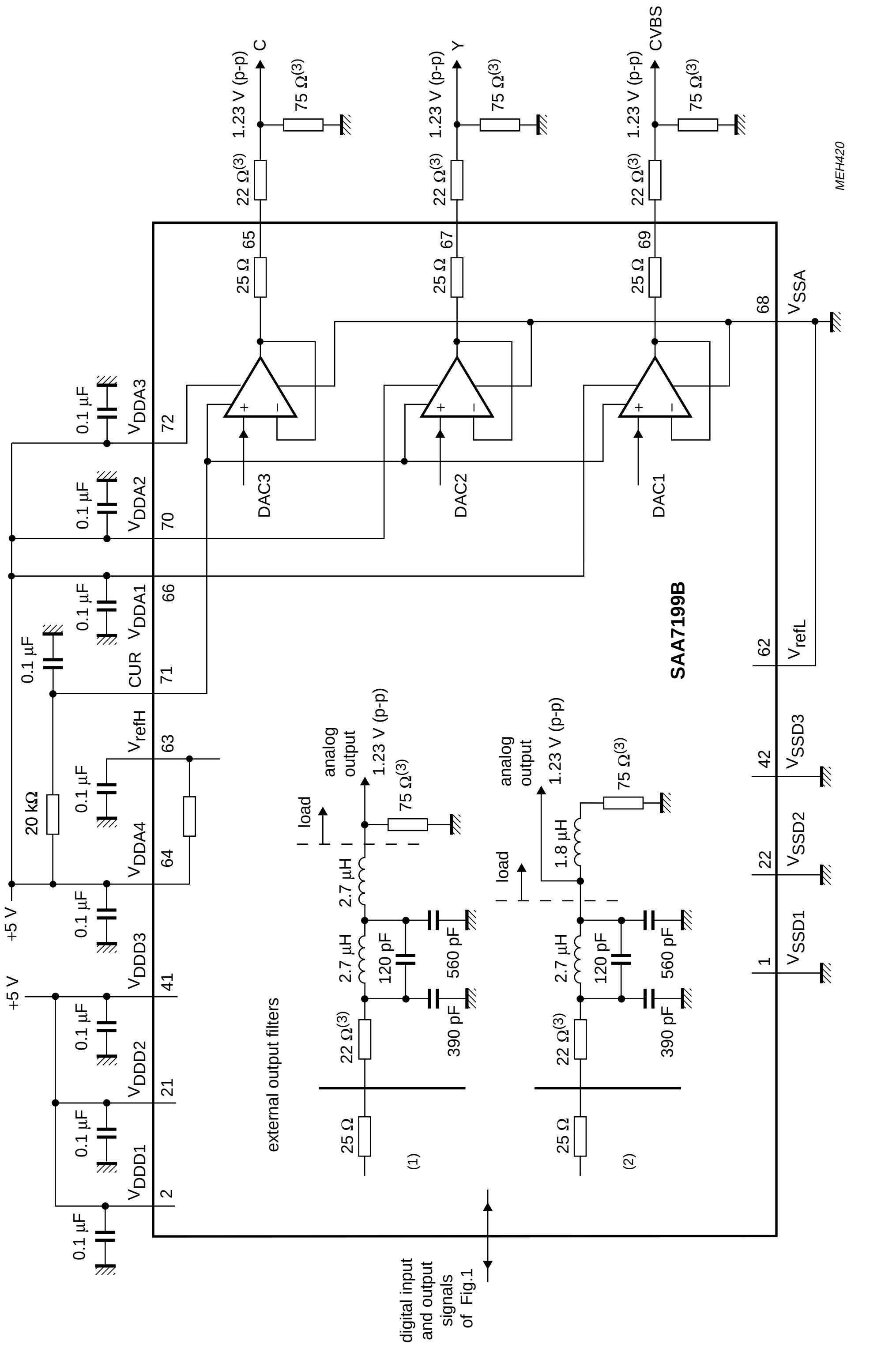
Fig.14 Characteristics of low-pass post-filters.; with compensation of DC hold.



(1) Value depends on crystal parameters.

(2) 24.576 MHz (3rd harmonic), Philips: 4322 143 05291; 26.8 MHz (3rd harmonic), Philips: 9922 520 30004.

Fig.15 Oscillator application (a) and optional external clock sync (b).



(1) Without compensation of the DAC hold characteristic (see Fig.13).

(2) With compensation of the DAC hold characteristic $\frac{\sin(x)}{x}$ correction (see Fig.14).

(3) Output amplitude determined by load resistors $R_L > 90\ \Omega$.

Fig.16 Application details of Fig.1 showing proposals of analog low-pass post-filtering of output signals.

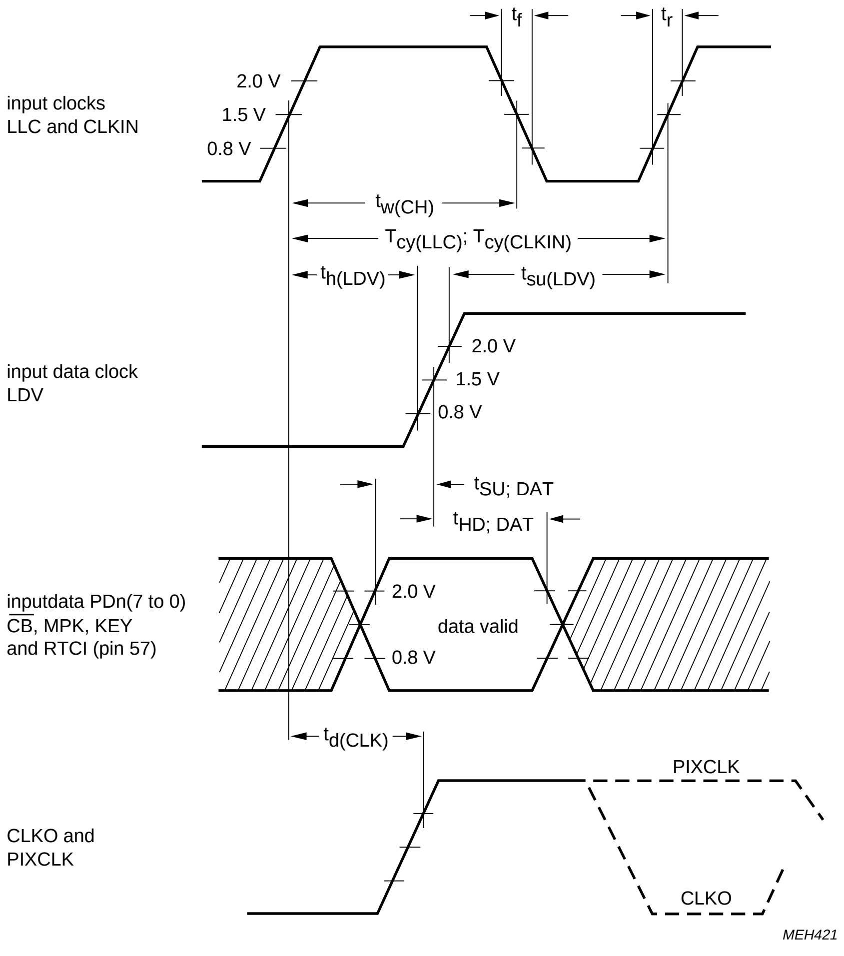


Fig.17 LDV input data timing.

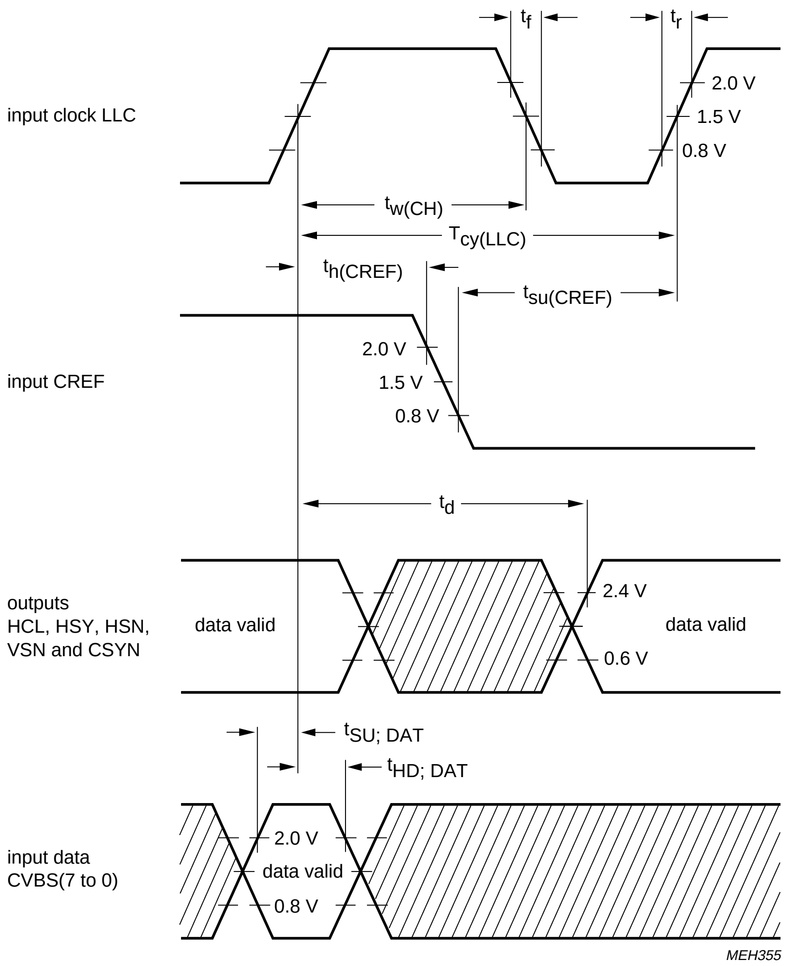


Fig.18 Clock and data timing.

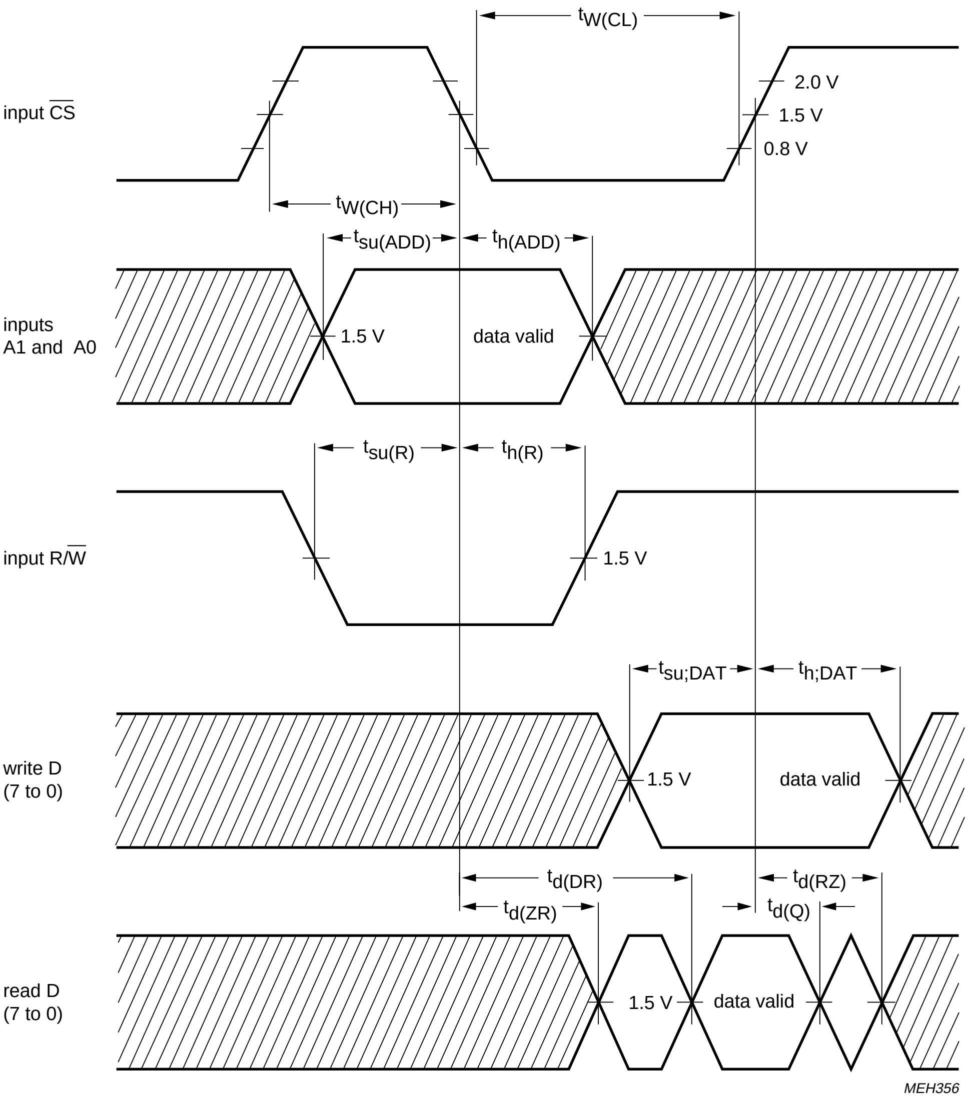
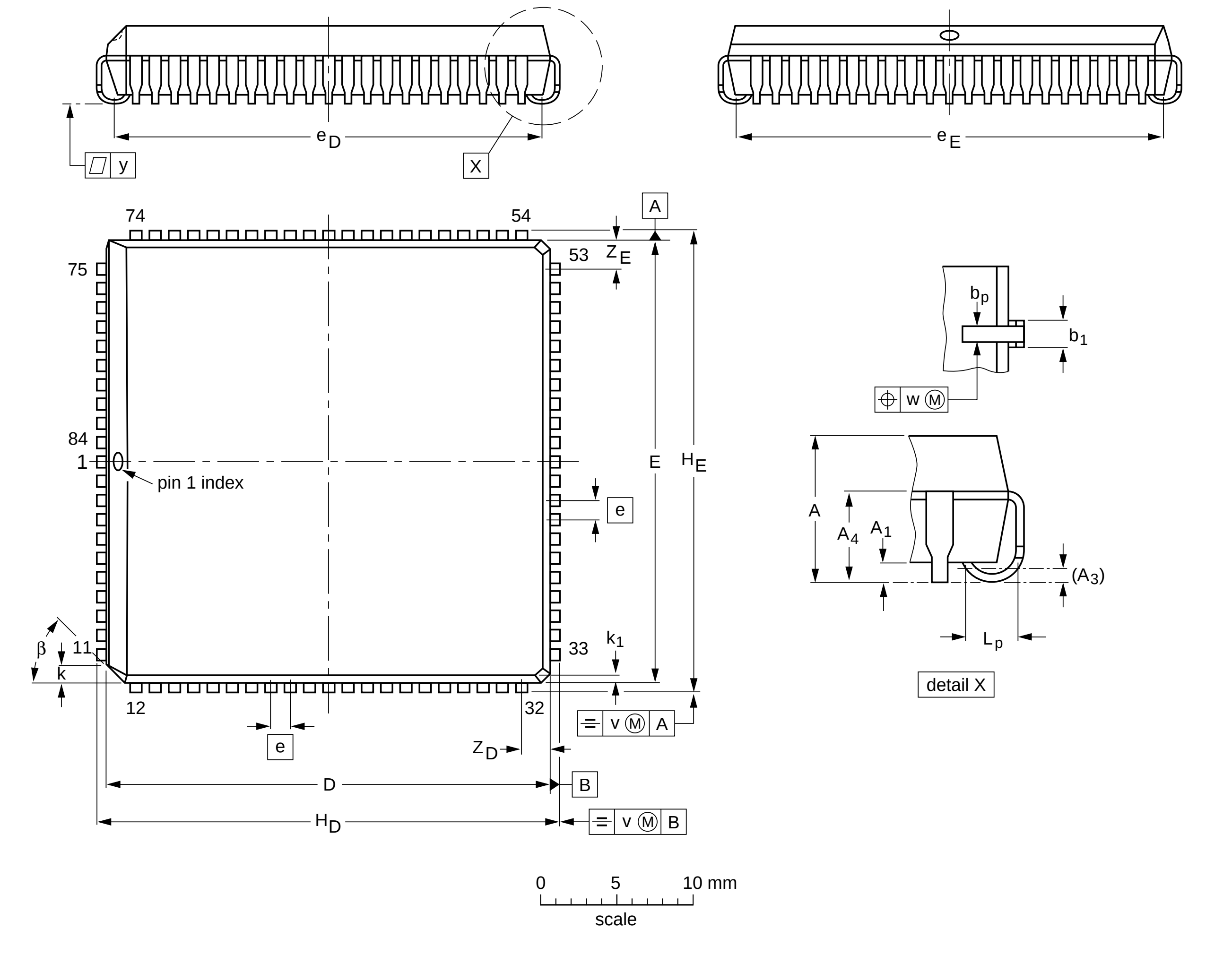


Fig.19 MPU-bus timing.

PACKAGE OUTLINE

PLCC84: plastic leaded chip carrier; 84 leads **SOT189-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45^{o}
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-2						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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