INTEGRATED CIRCUITS

DATA SHEET

SAA7215; SAA7216; SAA7221
Integrated MPEG AVGD decoders

Philips
Semiconductors

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Integrated MPEG AVGD decoders   SAA7215; SAA7216; SAA7221

FEATURES

General features

- Integrated MPEG AVGD decoder: audio, video and graphics decoding and digital video encoding

- 5 planes display chain: background colour, background plane, MPEG display plane, graphics plane and cursor plane

- 16-Mbit or 32-Mbit external Synchronous DRAM (SDRAM) for MPEG audio and video decoding and graphics data storage

- Single or double external SDRAM organized as 1 M $\times$ 16 or 2 $\times$ 1 M $\times$ 16 (two independent 16-bit data bus) interfacing at 81 MHz. Due to efficient memory use in MPEG decoding, more than 1 Mbit is available for graphics in the single SDRAM configuration whereas 17 Mbits are available in the double SDRAM configuration.

- All basic operations of the AVGD decoder are possible in both 16- and 32-Mbit configuration; enhanced performance is achieved by the use of 32-Mbit external SDRAM

- Targeted to BSkyB 3.0 and Canal+ basic box and web box specifications

- Fast 16-bit data + 22-bit address synchronous or asynchronous interface with external controller at up to 40.5 MHz

- Dedicated input for compressed audio and video in Packetized Elementary Stream (PES) or Elementary Stream (ES) in byte wide or bit serial format. Accompanying strobe signals distinguish between audio and video data. Transport stream error correction available.

- Audio and/or video can also be input via the CPU interface in PES or ES in 8 or 16-bit parallel format

- Single 27 or 40.5 MHz external clock for time base reference and internal processing. Internal system time base at 90 kHz can be synchronized via CPU port. All required decoding and presentation clocks are generated internally.

- Flexible memory allocation under control of the external CPU enables optimized partitioning of memory for different tasks

- Optimum compatibility with T-MIPS controller family (SAA7214, SAA7219 and successors)

- Boundary scan testing implemented

- External SDRAM self test

- Supply voltage: 3.3 V; package: SQFP208.

CPU related features

- 16-bit data, 22-bit address, Chip Select, Data Strobe and DaTa ACKnowledge external control protocol

- Fast 16-bit data plus 22-bit address synchronous interface with the SAA7214, SAA7219 family at up to 40.5 MHz

- Asynchronous interface possible with external microcontroller

- Support of fast DMA transfer

- Flexible bidirectional interface to external SDRAM

- High speed/low latency interface with second graphics SDRAM

- Byte access to the full SDRAM in the upper 16-Mbit address range

- Independent memory mapping of SDRAM and control registers

- Two programmable independent interrupt lines available

- Supports Motorola 68xxx interfaces as well as LSI L64108 interface.

MPEG-2 system features

- Parsing of MPEG-2 PES and MPEG-1 packet streams

- Double system time clock counters

- Stand-alone or supervised audio/video synchronization

- Processing of errors flagged by channel decoding section.

MPEG-2 video features

- Decoding of MPEG-2 video up to main level, main profile

- Output picture format: CCIR-601 4 : 2 : 2 interlaced pictures. Picture format 720 $\times$ 576 at 50 Hz or 720 $\times$ 480 at 60 Hz.

- Support of constant and variable bit rates up to 15 Mbits/s for the elementary stream

- Horizontal and vertical pan and scan allows the extraction of a window from the coded picture

- Flexible horizontal scaling from 0.5 up to 4 allows easy aspect ratio conversion including support for 2.21 : 1 aspect ratio movies; in case of shrinking an anti-aliasing pre-filter is applied

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- Vertical scaling with fixed factors 0.5, 0.75, 1 or 2; factor 0.5 realizes picture shrink. Factor 2 can be used for up-conversion of pictures with 288 (240) lines or less; factor 0.75 is used for letterbox presentation.

- Horizontal and vertical scaling can be combined to scale pictures to $\frac{1}{4}$ of their original size, thus freeing up screen space for graphic applications like electronic program guides

- Non full screen MPEG pictures can be displayed in a box of which position and background colour are adjustable by the external microcontroller; structured background is available as part of the graphic features

- Nominal video input buffer size for MP at ML 2.7-Mbit

- Video output may be slaved to internally (master) generated or externally (slave) supplied HV synchronization signals or CCIR-656 contained synchronization signals. The position of active video is programmable. Display phase is not affected by MPEG timebase changes.

- Decoding and presentation can be independently handled under CPU control

- Various trick modes under control of external microcontroller:
  - Freeze field/frame on I- or P-frames; restart on I-picture
  - Freeze field on B-frames; restart at any moment
  - Scanning and decoding of I- or I- and P-frames in a IBP sequence
  - Single step mode
  - Repeat/skip field for time base correction
  - Repeat/skip frame for display parity integrity.

- Synchronization modes: DTS controlled, DTS free running, software controlled, buffer controlled

- DTS register can be set via external controller; programmable processing delay compensation.

MPEG-2 audio features

- Supported audio sampling frequencies: 48, 44.1, 32, 24, 22.05 and 16 kHz

- Independent channel volume control and programmable inter-channel crosstalk through a baseband audio processing unit

- MPEG audio decoder
  - Decoding of 2 channels, layer I and II MPEG-1 audio and low sampling frequency extension of MPEG-2
  - Supports for mono, stereo, intensity stereo and dual channel mode

  - CRC error detection with automatic mute
  - Constant and variable bit rates up to 448 kbit/s
  - Selectable output channel in dual channel mode
  - Storage of last 54 bytes in ancillary data field
  - Dynamic range control at output.

- Muting possibility via external controller; automatic muting in case of errors

- Generation of 'beeps' with programmable tone height, duration and amplitude

- Linear PCM decoding
  - Support for up to 8 channels linear PCM elementary audio streams
  - Supports for 8, 16, 20 and 24 bit/sample
  - Supports for bit rates up to 6.144 Mbit/s
  - 96 kHz LPCM samples will be mapped to a 48 kHz multi-channel format
  - Volume control for linear PCM samples in three steps: −6, −12 and −18 dB.

- Burst-formatting for interconnection with an external multi-channel decoder
  - AC-3 elementary streams (IEC1937)
  - MPEG-2 multi-channel streams in ES or PES format
  - Output via the digital audio output or the IEC 958 output.

- Output stage
  - Global control for volume and balance
  - Serial multi-channel digital audio output with 16, 18, 20 or 22 bits per sample, compatible either to I^{2}S or Japanese formats; output can be set to high impedance mode via the external controller
  - IEC958 (Serial SPDIF) audio output; output can be set to high impedance mode
  - Clock output 256 or 384 × f$_s$ for external DA converter or clock input; output can be set to high impedance mode.

- Audio FIFO in external SDRAM; programmable buffer size, at least 64 kbit is available

- Synchronization modes: PTS controlled, PTS free running, software controlled, buffer controlled

- PTS register can be set via external controller; programmable processing delay compensation.

Background colour

- 24 bit YC$_b$C$_r$ colour.

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Graphics features

2 nearly identical graphics planes: the first graphics plane commonly called the background plane and the second graphics plane commonly called foreground plane.
The following features apply for both planes.

- Graphics is presented in boxes independent of video format

- Boxes can be up to full screen allowing double buffer display mechanism

- Two independent data paths with RGB 4 : 4 : 4 and YC_bC_r 4 : 2 : 2 formats available with independent mixing

- RGB path transparent to YC_bC_r format

- Conversion matrices available to allow any format on any different data path (RGB or YC_bC_r)

- Screen arrangement of boxes is determined by display list mechanism which allows for multiple boxes, background loading, fast switching, scrolling, overlapping and fading of regions

- Real-time anti-flickering performed in hardware; programmable hardware available for off-line anti-flickering

- Hard edged or soft edged wiping of regions available

- Support of 2, 4, 8, 16 bit/pixel in fixed bit maps format or coded in accordance to the DVB variable/run length standard for region based graphics

- Chrominance down-sampling filter switched per region

- Display colours are obtained via colour look up tables or directly from bitmap; CLUT output can be YC_bC_rT at 8-bit for each signal component thus enabling 16 M different colours and 6-bit for T which gives 64 mixing levels with video; CLUT output can also be RGBT with same resolutions; non linear processing available by means of LUTs

- Map table mechanism to specify a sub set of entries if the CLUT is larger than required by the coded bit pattern; supported map tables are 16 to 256, 4 to 256 and 4 to 16

- Up to 4 graphics boxes may overlap vertically even inside one graphics layer thanks to the use of flexible chained descriptors

- Graphics mechanism can be used for signal generation in the vertical blanking interval; useful for teletext, wide screen signalling, closed caption etc.

In addition to the previous listed features, the second graphics plane sustains:

- Teletext insertion with automatic teletext data retrieving from the external SDRAM.

Data manipulation unit

- Powerful 3D block move with different patterns for source and destination area

- Dedicated events for video synchronization

- Scaling, format conversion and bit manipulation from a chained list of instructions.

Cursor

- Size of 1024 pixels

- Programmable shape (8×128, 16×64, 32×32, 64×16 and 128×8)

- 16 colours available with a 4 level transparency mixing with video and graphics

- Cursor colours obtained via two 16 entry CLUTs with YC_bC_rT at 6, 4, 4 respectively 2 bits and RGBT at 4, 4, 4 respectively 4 bits (or 4, 5, 3, respectively 4 bits)

- Cursor can be moved freely across the screen without overlapping restrictions.

Digital output

- Programmable selection for the mixed graphics planes with video for the CVBS and RGB outputs

- Digital video input/output interface on 8 bit, 27 MHz (C_bYC_rY multiplexed bus), at a CCIR-656 format.

Analog output

- Analog video output interface on both the RGB and Y/C/CVBS formats available simultaneously

- PAL/NTSC/SECAM encoding (SAA7221HS only)

- Two DACs for CVBS, Y and C, CVBS running at 27 MHz 10-bit resolution

- Three DACs for R (Y), G (Cb) and B (Cr) running at 27 MHz; 9-bit resolution connected to a 10-bit input DAC

- Closed captioning and teletext encoding on CVBS

- Macrovision 7.01 and 6.1 encoding capability on Y or CVBS and C or CVBS (SAA7216HS only).

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APPLICATIONS

The SAA7215 integrated MPEG AVGD decoder is aimed at being used in MPEG digital TV applications. This decoder is primarily designed to be connected to a SAA7214 transport stream descrambler/demultiplexer/microcontroller by means of glueless interfaces even though connections to other market demultiplexers and/or microcontrollers are possible. Compatibility is also targeted with the SAA7219 and with the successor of the T-MIPS family.

The SAA7215 can be used in any system where high-end graphics are needed (associated SDRAM can be extended to 32-Mbit) as well as in low cost systems (all functions can be enabled with only 16-Mbit of associated SDRAM).

GENERAL DESCRIPTION

The SAA7215HS, SAA7216HS, SAA7221H is a MPEG-2 source decoder which combines audio decoding and video decoding. Additionally to these basic MPEG functions it also provides means for enhanced graphics, background display and/or on-screen display as well as encoding of output video. Due to an optimized architecture for audio and video decoding, maximum capacity in external memory and processing power from the external CPU is available for graphics support.

Possible options are indicated in Table 1.

Table 1   Possible options

TYPE NUMBER	MACROVISION	SECAM
SAA7215HS/C2	no	no
SAA7216HS/C1	yes	no
SAA7221HS/C1	no	yes

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	functional supply voltage range	3.0	3.3	3.6	V
I_{DD}	total supply current; V_{DD} = 3.3 V	–	tbf	–	mA
CLK	device clock input frequency (2 solutions are possible)	–30 ppm	+27	+30 ppm	MHz
		–30 ppm	+40.5	+30 ppm	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7215HS/C2	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm	SOT316-1
SAA7216HS/C1			
SAA7221HS/C1			

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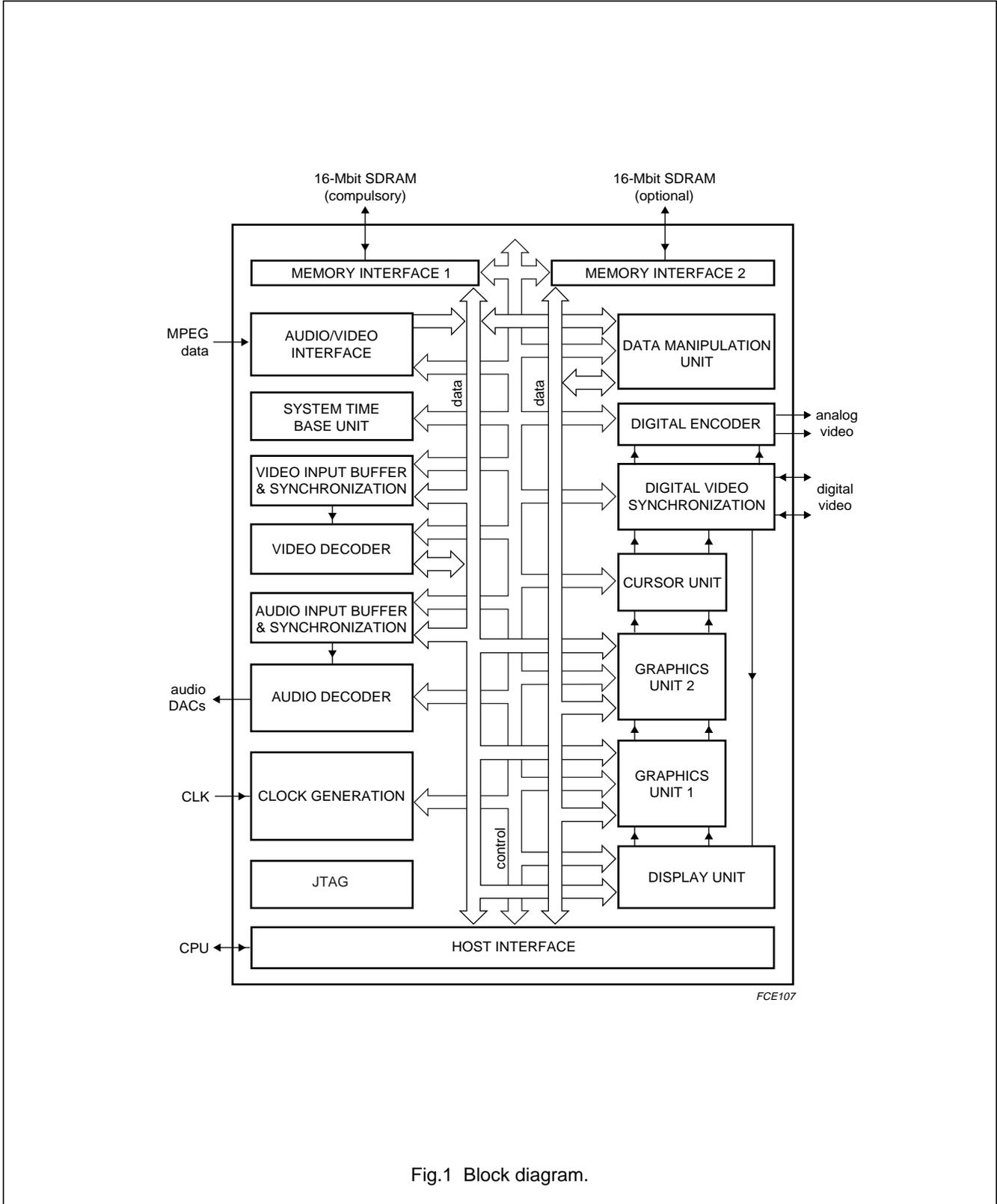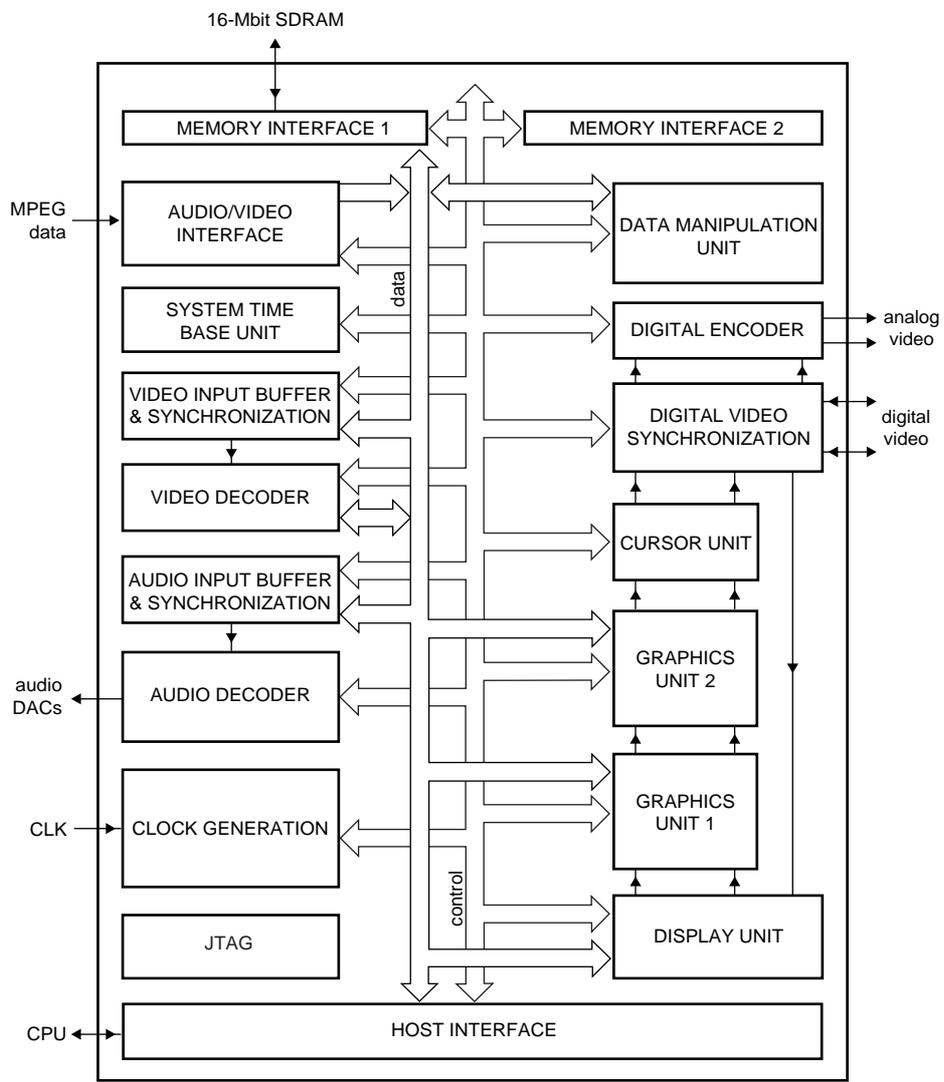
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BLOCK DIAGRAMS

Fig.1 Block diagram.

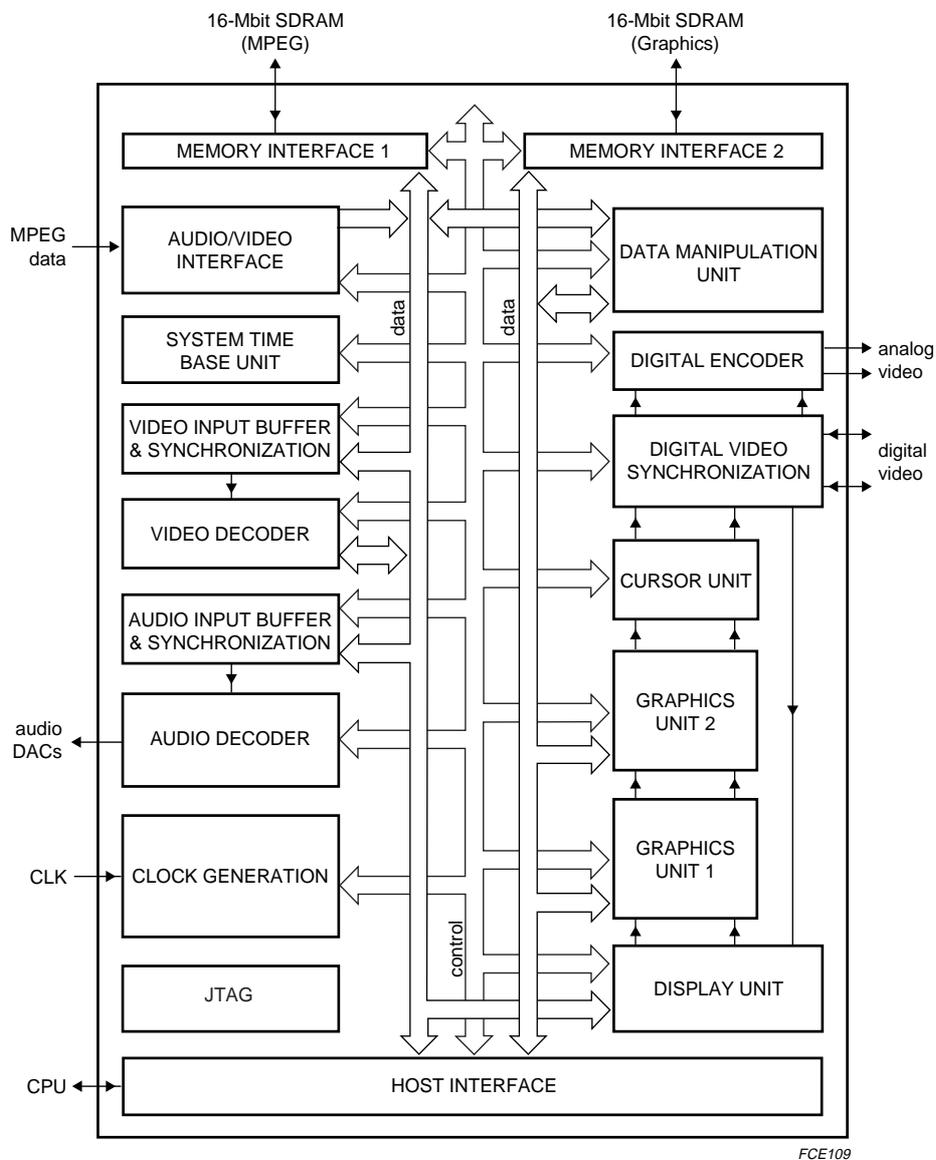## Integrated MPEG AVGD decoders   SAA7215; SAA7216; SAA7221

Fig.2 Block diagram with preferred use in 16-Mbit configuration.

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Fig.3 Block diagram with preferred use in 32-Mbit configuration.

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PINNING

Pinning table (listed numerically)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
V_{SS}	1	S	ground for pad ring
DATA(4)	2	I/O	CPU data input or output (bit 4); note 2
DATA(5)	3	I/O	CPU data input or output (bit 5); note 2
DATA(6	4	I/O	CPU data input or output (bit 6); note 2
DATA(7)	5	I/O	CPU data input or output (bit 7); note 2
DATA(8)	6	I/O	CPU data input or output (bit 8); note 2
DATA(9)	7	I/O	CPU data input or output (bit 9); note 2
V_{DD}	8	S	supply voltage for pad ring
DATA(10)	9	I/O	CPU data input or output (bit 10); note 2
DATA(11)	10	I/O	CPU data input or output (bit 11); note 2
DATA(12)	11	I/O	CPU data input or output (bit 12); note 2
DATA(13)	12	I/O	CPU data input or output (bit 13); note 2
DATA(14)	13	I/O	CPU data input or output (bit 14); note 2
DATA(15)	14	I/O	CPU data input or output (bit 15); note 2
V_{SS}	15	S	ground for pad ring
SDRAM_ADDR1(3)	16	O	SDRAM address 1 output (bit 3)
SDRAM_ADDR1(2)	17	O	SDRAM address 1 output (bit 2)
SDRAM_ADDR1(4)	18	O	SDRAM address 1 output (bit 4)
SDRAM_ADDR1(1)	19	O	SDRAM address 1 output (bit 1)
SDRAM_ADDR1(5)	20	O	SDRAM address 1 output (bit 5)
SDRAM_ADDR1(0)	21	O	SDRAM address 1 output (bit 0)
V_{DD}	22	S	supply voltage for pad ring
SDRAM_ADDR1(6)	23	O	SDRAM address 1 output (bit 6)
SDRAM_ADDR1(10)	24	O	SDRAM address 1 output (bit 10)
SDRAM_ADDR1(7)	25	O	SDRAM address 1 output (bit 7)
$V_{SS(CO)}$	26	S	ground for core logic
$V_{DD(CO)}$	27	S	supply voltage for digital core logic
SDRAM_ADDR1(11)	28	O	SDRAM address 1 output (bit 11)
SDRAM_ADDR1(9)	29	O	SDRAM address 1 output (bit 9)
SDRAM_ADDR1(8)	30	O	SDRAM address 1 output (bit 8)
V_{SS}	31	S	ground for pad ring
SDRAM_UDQ1	32	O	SDRAM write mask 1 output
SDRAM_RAS1	33	O	SDRAM row address strobe 1 output
SDRAM_CAS1	34	O	SDRAM column address 1 output
SDRAM_WE1	35	O	SDRAM write enable 1 output
V_{DD}	36	S	supply voltage for pad ring
SDRAM_DATA1(8)	37	I/O	SDRAM data 1 input or output (bit 8)
SDRAM_DATA1(7)	38	I/O	SDRAM data 1 input or output (bit 7)

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SYMBOL	PIN	TYPE[1]	DESCRIPTION
SDRAM_DATA1(9)	39	I/O	SDRAM data 1 input or output (bit 9)
SDRAM_DATA1(6)	40	I/O	SDRAM data 1 input or output (bit 6)
SDRAM_DATA1(10)	41	I/O	SDRAM data 1 input or output (bit 10)
SDRAM_DATA11(5)	42	I/O	SDRAM data 1 input or output (bit 5)
V_{SS}	43	S	ground for pad ring
SDRAM_DATA1(11)	44	I/O	SDRAM data 1 input or output (bit 11)
SDRAM_DATA1(4)	45	I/O	SDRAM data 1 input or output (bit 4)
SDRAM_DATA1(12)	46	I/O	SDRAM data 1 input or output (bit 12)
SDRAM_DATA1(3)	47	I/O	SDRAM data 1 input or output (bit 3)
SDRAM_DATA1(13)	48	I/O	SDRAM data 1 input or output (bit 13)
SDRAM_DATA1(2)	49	I/O	SDRAM data 1 input or output (bit 2)
V_{DD}	50	S	supply voltage for pad ring
SDRAM_DATA1(14)	51	I/O	SDRAM data 1 input or output (bit 14)
SDRAM_DATA1(1)	52	I/O	SDRAM data 1 input or output (bit 1)
SDRAM_DATA1(15)	53	I/O	SDRAM data 1 input or output (bit 15)
SDRAM_DATA1(0)	54	I/O	SDRAM data 1 input or output (bit 0)
READ_OUT1	55	O	read command 1 output
READ_IN1	56	I	read command 1 input
V_{SS}	57	S	ground for pad ring
CP81MEXT	58	I	81 MHz SDRAM clock memory input
CP81M	59	O	81 MHz SDRAM clock return path output
V_{DD}	60	S	supply voltage for pad ring
READ_IN2	61	I	read command 2 input
READ_OUT2	62	O	read command 2 output
SDRAM_DATA2(0)	63	I/O	SDRAM data 2 input or output (bit 0)
SDRAM_DATA2(15)	64	I/O	SDRAM data 2 input or output (bit 15)
SDRAM_DATA2(1)	65	I/O	SDRAM data 2 input or output (bit 1)
SDRAM_DATA2(14)	66	I/O	SDRAM data 2 input or output (bit 14)
V_{SS}	67	S	ground for pad ring
SDRAM_DATA2(2)	68	I/O	SDRAM data 2 input or output (bit 2)
SDRAM_DATA2(13)	69	I/O	SDRAM data 2 input or output (bit 13)
SDRAM_DATA2(3)	70	I/O	SDRAM data 2 input or output (bit 3)
SDRAM_DATA2(12)	71	I/O	SDRAM data 2 input or output (bit 12)
SDRAM_DATA2(4)	72	I/O	SDRAM data 2 input or output (bit 4)
SDRAM_DATA2(11)	73	I/O	SDRAM data 2 input or output (bit 11)
V_{DD}	74	S	supply voltage for pad ring
SDRAM_DATA2(5)	75	I/O	SDRAM data 2 input or output (bit 5)
SDRAM_DATA2(10)	76	I/O	SDRAM data 2 input or output (bit 10)
SDRAM_DATA2(6)	77	I/O	SDRAM data 2 input or output (bit 6)
$V_{SS(CO)}$	78	S	ground for core logic
$V_{DD(CO)}$	79	S	supply voltage for digital core logic

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SYMBOL	PIN	TYPE[1]	DESCRIPTION
SDRAM_DATA2(9)	80	I/O	SDRAM data 2 input or output (bit 9)
SDRAM_DATA2(7)	81	I/O	SDRAM data 2 input or output (bit 7)
SDRAM_DATA2(8)	82	I/O	SDRAM data 2 input or output (bit 8)
V_{SS}	83	S	ground for pad ring
SDRAM_WE2	84	O	SDRAM write enable 2 output
SDRAM_CAS2	85	O	SDRAM column address 2 output
SDRAM_RAS2	86	O	SDRAM row address strobe 2 output
SDRAM_UDQ2(0)	87	O	SDRAM write mask 2 (0) output
SDRAM_UDQ2(1)	88	O	SDRAM write mask 2 (1) output
V_{DD}	89	S	supply voltage for pad ring
SDRAM_ADDR2(8)	90	O	SDRAM address 2 output (bit 8)
SDRAM_ADDR2(9)	91	O	SDRAM address 2 output (bit 9)
SDRAM_ADDR2(11)	92	O	SDRAM address 2 output (bit 11)
SDRAM_ADDR2(7)	93	O	SDRAM address 2 output (bit 7)
SDRAM_ADDR2(10)	94	O	SDRAM address 2 output (bit 10)
SDRAM_ADDR2(6)	95	O	SDRAM address 2 output (bit 6)
V_{SS}	96	S	ground for pad ring
SDRAM_ADDR2(0)	97	O	SDRAM address 2 output (bit 0)
SDRAM_ADDR2(5)	98	O	SDRAM address 2 output (bit 5)
SDRAM_ADDR2(1)	99	O	SDRAM address 2 output (bit 1)
SDRAM_ADDR2(4)	100	O	SDRAM address 2 output (bit 4)
SDRAM_ADDR2(2)	101	O	SDRAM address 2 output (bit 2)
SDRAM_ADDR2(3)	102	O	SDRAM address 2 output (bit 3)
V_{DD}	103	S	supply voltage for pad ring
TDI	104	I	boundary scan test data input; note 2
TDO	105	O/Z	boundary scan test data output; note 2
TMS	106	I	boundary scan test mode select input; note 2
TRST	107	I	boundary scan test data input; note 2
TCK	108	I	boundary scan test clock input
$V_{DD(AN)}$	109	S	3.3 V supply for analog blocks(PLL)
IDUMP2	110	–	analog sink 2
B	111	–	analog video (blue)
G	112	–	analog video (green)
AV_{DD3}	113	S	analog supply 3
R	114	–	analog video (red)
AV_{DD2}	115	S	analog supply 2
Y/CVBS	116	–	analog luminance/analog composite video
C/CVBS	117	–	analog chrominance/analog composite video
IDUMP1	118	–	analog sink 1
AV_{SS}	119	S	analog supply ground
RSET	120	–	analog reference

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SYMBOL	PIN	TYPE[1]	DESCRIPTION
AV_{DD1}	121	S	analog supply 1
V_{SS}	122	S	ground for pad ring
GRPH	123	O/Z	indicator for graphics information output; note 2
VS	124	I/O	vertical synchronization input or output; note 2
HS	125	I/O	horizontal synchronization input or output; note 2
CP27	126	O	27 MHz video presentation clock output; note 2
V_{DD}	127	S	supply voltage for pad ring
YUV(0)	128	I/O	YUV video input or output (bit 0);at 27 MHz; note 2
$V_{SS(CO)}$	129	S	ground for core logic
$V_{DD(CO)}$	130	S	supply voltage for digital core logic
YUV(1)	131	I/O	YUV video input or output (bit 1); at 27 MHz; note 2
YUV(2)	132	I/O	YUV video input or output (bit 2); at 27 MHz; note 2
YUV(3)	133	I/O	YUV video input or output (bit 3); at 27 MHz; note 2
YUV(4)	134	I/O	YUV video input or output (bit 4); at 27 MHz; note 2
YUV(5)	135	I/O	YUV video input or output (bit 5); at 27 MHz; note 2
YUV(6)	136	I/O	YUV video input or output (bit 6); at 27 MHz; note 2
YUV(7)	137	I/O	YUV video input or output (bit 7); at 27 MHz; note 2
V_{SS}	138	S	ground for pad ring
SPDIF	139	O/Z	digital audio output; note 2
WS	140	O/Z	word select output; note 2
WB	141	O/Z	word begin output; note 2
SD	142	O/Z	serial audio data output; note 2
SCK	143	O/Z	serial audio clock output; note 2
FSCLK	144	I/O	256 or 384 x f_s clock input or output;
RESET	145	I	hard reset input; note 2
TTX	146	I	teletext data input; note 2
TTXRQ/CPU_SEL(1)	147	I/O	teletext data request or CPU data interface selection (1); note 2; note 3
V_{DD}	148	S	supply voltage for pad ring
IRQ(1)	149	O/Z	individually maskable interrupt (1) output; note 2
IRQ(0)	150	O/Z	individually maskable interrupt (0) output; note 2
V_REQ	151	O/Z	video data request output; note 2
A_REQ	152	O/Z	audio data request output; note 2
AUDDEN	153	I	byte synchronisation of serial audio input A_DATA; note 2
A_DATA	154	I	MPEG audio stream serial port input; note 2
AV_DATA(0)	155	I	MPEG stream port input (bit 0); note 2
AV_DATA(1)	156	I	MPEG stream port input (bit 1); note 2
AV_DATA(2)	157	I	MPEG stream port input (bit 2); note 2
AV_DATA(3)	158	I	MPEG stream port input (bit 3); note 2
AV_DATA(4)	159	I	MPEG stream port input (bit 4); note 2
AV_DATA(5)	160	I	MPEG stream port input (bit 5); note 2
AV_DATA(6)	161	I	MPEG stream port input (bit 6); note 2

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SYMBOL	PIN	TYPE[1]	DESCRIPTION
AV_DATA(7)	162	I	MPEG stream port input (bit 7); note 2
ERROR	163	I	flag for bitstream error; note 2
A_STROBE	164	I	audio data strobe for AV_DATA and A_DATA inputs; note 2
V_STROBE	165	I	video data strobe for AV_DATA and A_DATA inputs; note 2
V_{SS} (gate input)	166	S	ground for pad ring
CPU_SEL(0)	167	I	CPU data interface selection (0) input; note 2; note 3
CLK	168	I	27 or 40.5 MHz clock input; note 2
V_{SS}	169	S	ground for pad ring
SIZ(1)	170	I	size of data on bus DATA (1) input; note 2
SIZ(0)	171	I	size of data on bus DATA (0) input; note 2
ADDRESS(20)	172	I	CPU address input (bit 20); note 2
ADDRESS(19)	173	I	CPU address input (bit 19); note 2
ADDRESS(18)	174	I	CPU address input (bit 18); note 2
ADDRESS(17)	175	I	CPU address input (bit 17); note 2
ADDRESS(16)	176	I	CPU address input (bit 16); note 2
ADDRESS(15)	177	I	CPU address input (bit 15); note 2
ADDRESS(14)	178	I	CPU address input (bit 14); note 2
ADDRESS(13)	179	I	CPU address input (bit 13); note 2
ADDRESS(12)	180	I	CPU address input (bit 12); note 2
ADDRESS(11)	181	I	CPU address input (bit 11); note 2
$V_{SS(CO)}$	182	S	ground for core logic
$V_{DD(CO)}$	183	S	supply voltage for digital core logic
V_{DD}	184	S	supply voltage for pad ring
ADDRESS(10)	185	I	CPU address input (bit 10); note 2
ADDRESS(9)	186	I	CPU address input (bit 9); note 2
ADDRESS(8)	187	I	CPU address input (bit 8); note 2
ADDRESS(7)	188	I	CPU address input (bit 7); note 2
ADDRESS(6)	189	I	CPU address input (bit 6); note 2
ADDRESS(5)	190	I	CPU address input (bit 5); note 2
ADDRESS(4)	191	I	CPU address input (bit 4); note 2
ADDRESS(3)	192	I	CPU address input (bit 3); note 2
ADDRESS(2)	193	I	CPU address input (bit 2); note 2
ADDRESS(1)	194	I	CPU address input (bit 1); note 2
ADDRESS(0)	195	I	CPU address input (bit 0); note 2
R/$\overline{W}$	196	I	read or write input; note 2
DMA_RDY	197	O/Z	DMA ready output; note 2
DMA_DONE	198	I	DMA end input; note 2
DMA_REQ	199	I/O	DMA request input or output; note 2
DMA_ACK	200	I	DMA acknowledge input; note 2
$\overline{CS}_{RG}$	201	I	chip select for control register access input; note 2
$\overline{CS}_{SD}$/ADDRESS(21)	202	I	chip select for SDRAM access or CPU address (bit 21) input; note 2

Integrated MPEG AVGD decoders

SAA7215; SAA7216; SAA7221

SYMBOL	PIN	TYPE(1)	DESCRIPTION
$\overline{\text{DATACK}}$	203	O/Z	data acknowledge output; note 2
$\overline{\text{DS}}/\overline{\text{TS}}$	204	I	data strobe or transfer start input; note 2
DATA(0)	205	I/O	CPU data input or output (bit 0); note 2
DATA(1)	206	I/O	CPU data input or output (bit 1); note 2
DATA(2)	207	I/O	CPU data input or output (bit 2); note 2
DATA(3)	208	I/O	CPU data input or output (bit 3); note 2

Notes

1. Pin type abbreviations: I = Input, O = Output, I/O = Input or Output, O/Z = high impedance Output and S = Supply voltage.

2. 5 V tolerant outputs swing between V_{SS} and V_{DD}. 5 V tolerant inputs can receive signals swinging between V_{SS} and 3.3 V or V_{SS} and 5 V.

3. Signal CPU_SEL(1) is used only after a global hardware reset is applied on external input line RESET for determining the type of the microcontroller connected to SAA7215; SAA7216; SAA7221 and therefore apply the proper communication protocol. This microcontroller type must be given by means of weak pull-up or pull-down externally connected to CPU_SEL(1). During normal operation, the pin TTXRQ/CPU_SEL(1) is used for implementing the Teletext Data Request protocol and must not be disturbed by the microcontroller type setting.

Integrated MPEG AVGD decoders

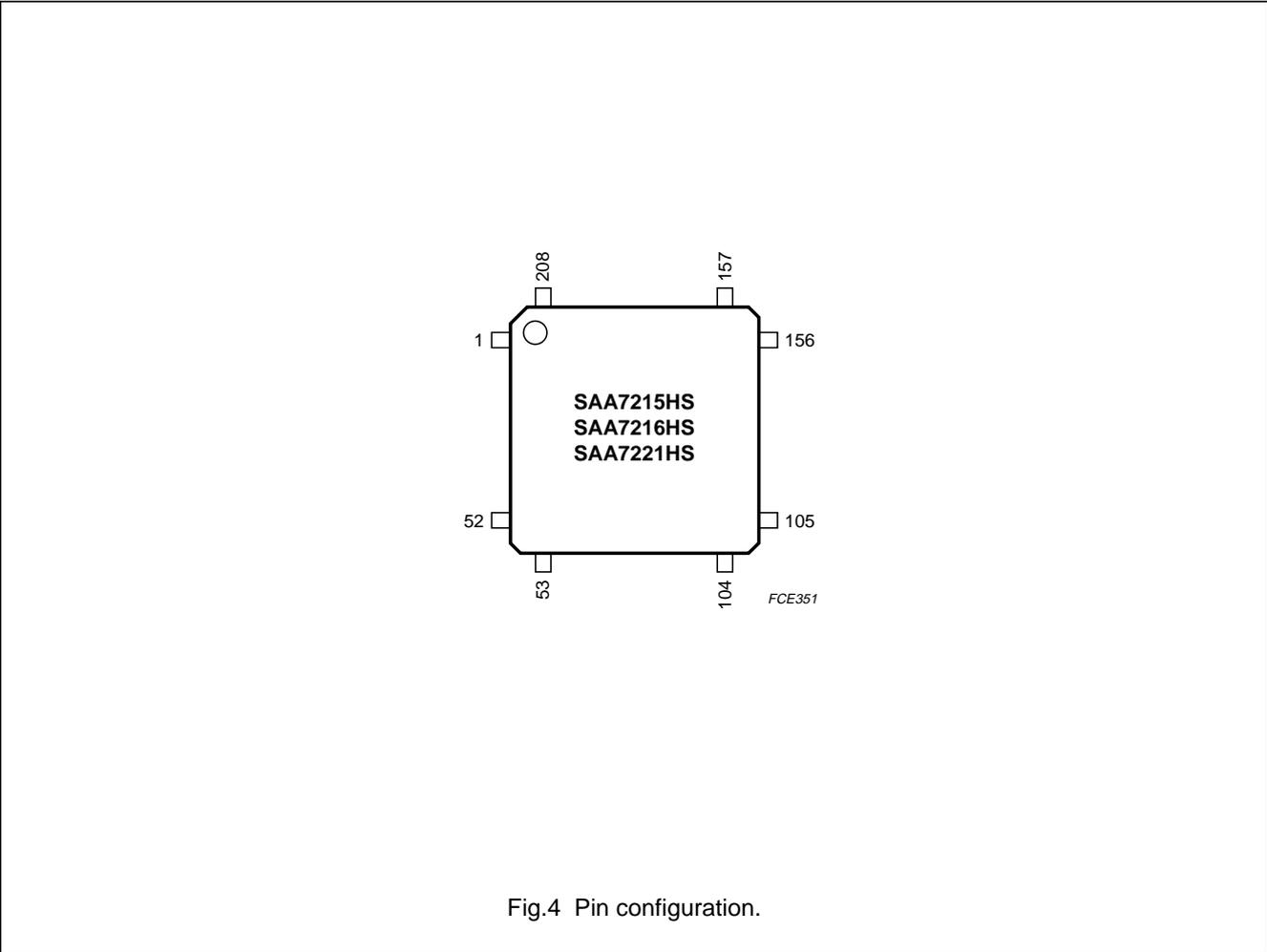SAA7215; SAA7216; SAA7221

Pin configuration

Fig.4 Pin configuration.

Pinning table (listed by function)

PIN	SYMBOL	TYPE[1]	DRIVE	VOLTAGE	ACTIVITY
166	V_{SS} (gate input)	S	–	0 V	–
168	CLK	I	–	5.0 V tolerant	rising edge
145	RESET	I	–	5.0 V tolerant	low level
162	AV_DATA(7)	I	–	5.0 V tolerant	direct level
161	AV_DATA(6)	I	–	5.0 V tolerant	direct level
160	AV_DATA(5)	I	–	5.0 V tolerant	direct level
159	AV_DATA(4)	I	–	5.0 V tolerant	direct level
158	AV_DATA(3)	I	–	5.0 V tolerant	direct level
157	AV_DATA(2)	I	–	5.0 V tolerant	direct level
156	AV_DATA(1)	I	–	5.0 V tolerant	direct level
155	AV_DATA(0)	I	–	5.0 V tolerant	direct level
154	A_DATA	I	–	5.0 V tolerant	low level
153	AUDDEN	I	–	5.0 V tolerant	high level
164	A_STROBE	I	–	5.0 V tolerant	program level
165	V_STROBE	I	–	5.0 V tolerant	program level
152	A_REQ	O/Z	3 mA	5.0 V tolerant	program level
151	V_REQ	O/Z	3 mA	5.0 V tolerant	program level
163	ERROR	I	–	5.0 V tolerant	program level
142	SD	O/Z	3 mA	5.0 V tolerant	direct level
143	SCK	O/Z	3 mA	5.0 V tolerant	edge
140	WS	O/Z	3 mA	5.0 V tolerant	direct level
141	WB	O/Z	3 mA	5.0 V tolerant	direct level
139	SPDIF	O/Z	3 mA	5.0 V tolerant	direct level
144	FSCLK	I/O	3 mA	5.0 V tolerant	edge
126	CP27	O	3 mA	5.0 V tolerant	rising edge
137	YUV(7)	I/O	3 mA	5.0 V tolerant	direct level
136	YUV(6)	I/O	3 mA	5.0 V tolerant	direct level
135	YUV(5)	I/O	3 mA	5.0 V tolerant	direct level
134	YUV(4)	I/O	3 mA	5.0 V tolerant	direct level
133	YUV(3)	I/O	3 mA	5.0 V tolerant	direct level
132	YUV(2)	I/O	3 mA	5.0 V tolerant	direct level
131	YUV(1)	I/O	3 mA	5.0 V tolerant	direct level
128	YUV(0)	I/O	3 mA	5.0 V tolerant	direct level
125	HS	I/O	3 mA	5.0 V tolerant	program level
124	VS	I/O	3 mA	5.0 V tolerant	program level
123	GRPH	O/Z	3 mA	5.0 V tolerant	high level
114	R/CVBS	–	–	–	analog
112	G	–	–	–	analog
111	B	–	–	–	analog
116	Y/CVBS	–	–	–	analog

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PIN	SYMBOL	TYPE[1]	DRIVE	VOLTAGE	ACTIVITY
117	C/CVBS	–	–	–	analog
53	SDRAM_DATA1(15)	I/O	2 mA	3.3 V	direct level
51	SDRAM_DATA1(14)	I/O	2 mA	3.3 V	direct level
48	SDRAM_DATA1(13)	I/O	2 mA	3.3 V	direct level
46	SDRAM_DATA1(12)	I/O	2 mA	3.3 V	direct level
44	SDRAM_DATA1(11)	I/O	2 mA	3.3 V	direct level
41	SDRAM_DATA1(10)	I/O	2 mA	3.3 V	direct level
39	SDRAM_DATA1(9)	I/O	2 mA	3.3 V	direct level
37	SDRAM_DATA1(8)	I/O	2 mA	3.3 V	direct level
38	SDRAM_DATA1(7)	I/O	2 mA	3.3 V	direct level
40	SDRAM_DATA1(6)	I/O	2 mA	3.3 V	direct level
42	SDRAM_DATA1(5)	I/O	2 mA	3.3 V	direct level
45	SDRAM_DATA1(4)	I/O	2 mA	3.3 V	direct level
47	SDRAM_DATA1(3)	I/O	2 mA	3.3 V	direct level
49	SDRAM_DATA1(2)	I/O	2 mA	3.3 V	direct level
52	SDRAM_DATA1(1)	I/O	2 mA	3.3 V	direct level
54	SDRAM_DATA1(0)	I/O	2 mA	3.3 V	direct level
28	SDRAM_ADDR1(11)	O	2 mA	3.3 V	direct level
24	SDRAM_ADDR1(10)	O	2 mA	3.3 V	direct level
29	SDRAM_ADDR1(9)	O	2 mA	3.3 V	direct level
30	SDRAM_ADDR1(8)	O	2 mA	3.3 V	direct level
25	SDRAM_ADDR1(7)	O	2 mA	3.3 V	direct level
23	SDRAM_ADDR1(6)	O	2 mA	3.3 V	direct level
20	SDRAM_ADDR1(5)	O	2 mA	3.3 V	direct level
18	SDRAM_ADDR1(4)	O	2 mA	3.3 V	direct level
16	SDRAM_ADDR1(3)	O	2 mA	3.3 V	direct level
17	SDRAM_ADDR1(2)	O	2 mA	3.3 V	direct level
19	SDRAM_ADDR1(1)	O	2 mA	3.3 V	direct level
21	SDRAM_ADDR1(0)	O	2 mA	3.3 V	direct level
33	SDRAM_RAS1	O	2 mA	3.3 V	low level
34	SDRAM_CAS1	O	2 mA	3.3 V	low level
35	SDRAM_WE1	O	2 mA	3.3 V	low level
32	SDRAM_UDQ1	O	2 mA	3.3 V	direct level
59	CP81M	O	8 mA	3.3 V	edge
58	CP81MEXT	I	–	3.3 V	edge
55	READ_OUT1	O	2 mA	3.3 V	low level
56	READ_IN1	I	–	3.3 V	low level
64	SDRAM_DATA2(15)	I/O	2 mA	3.3 V	direct level
66	SDRAM_DATA2(14)	I/O	2 mA	3.3 V	direct level
69	SDRAM_DATA2(13)	I/O	2 mA	3.3 V	direct level
71	SDRAM_DATA2(12)	I/O	2 mA	3.3 V	direct level

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PIN	SYMBOL	TYPE[1]	DRIVE	VOLTAGE	ACTIVITY
73	SDRAM_DATA2(11)	I/O	2 mA	3.3 V	direct level
76	SDRAM_DATA2(10)	I/O	2 mA	3.3 V	direct level
80	SDRAM_DATA2(9)	I/O	2 mA	3.3 V	direct level
82	SDRAM_DATA2(8)	I/O	2 mA	3.3 V	direct level
81	SDRAM_DATA2(7)	I/O	2 mA	3.3 V	direct level
77	SDRAM_DATA2(6)	I/O	2 mA	3.3 V	direct level
75	SDRAM_DATA2(5)	I/O	2 mA	3.3 V	direct level
72	SDRAM_DATA2(4)	I/O	2 mA	3.3 V	direct level
70	SDRAM_DATA2(3)	I/O	2 mA	3.3 V	direct level
68	SDRAM_DATA2(2)	I/O	2 mA	3.3 V	direct level
65	SDRAM_DATA2(1)	I/O	2 mA	3.3 V	direct level
63	SDRAM_DATA2(0)	I/O	2 mA	3.3 V	direct level
92	SDRAM_ADDR2(11)	O	2 mA	3.3 V	direct level
94	SDRAM_ADDR2(10)	O	2 mA	3.3 V	direct level
91	SDRAM_ADDR2(9)	O	2 mA	3.3 V	direct level
90	SDRAM_ADDR2(8)	O	2 mA	3.3 V	direct level
93	SDRAM_ADDR2(7)	O	2 mA	3.3 V	direct level
95	SDRAM_ADDR2(6)	O	2 mA	3.3 V	direct level
98	SDRAM_ADDR2(5)	O	2 mA	3.3 V	direct level
100	SDRAM_ADDR2(4)	O	2 mA	3.3 V	direct level
102	SDRAM_ADDR2(3)	O	2 mA	3.3 V	direct level
101	SDRAM_ADDR2(2)	O	2 mA	3.3 V	direct level
99	SDRAM_ADDR2(1)	O	2 mA	3.3 V	direct level
97	SDRAM_ADDR2(0)	O	2 mA	3.3 V	direct level
86	SDRAM_RAS2	O	2 mA	3.3 V	low level
85	SDRAM_CAS2	O	2 mA	3.3 V	low level
84	SDRAM_WE2	O	2 mA	3.3 V	low level
88	SDRAM_UDQ2(1)	O	2 mA	3.3 V	direct level
87	SDRAM_UDQ2(0)	O	2 mA	3.3 V	direct level
62	READ_OUT2	O	2 mA	3.3 V	low level
61	READ_IN2	I	–	3.3 V	low level
147	TTXRQ/CPU_SEL(1)	I/O	3 mA	5.0 V tolerant	direct level
167	CPU_SEL(0)	I	–	5.0 V tolerant	level
146	TTX	I	–	5.0 V tolerant	direct level
14	DATA(15)	I/O	6 mA	5.0 V tolerant	direct level
13	DATA(14)	I/O	6 mA	5.0 V tolerant	direct level
12	DATA(13)	I/O	6 mA	5.0 V tolerant	direct level
11	DATA(12)	I/O	6 mA	5.0 V tolerant	direct level
10	DATA(11)	I/O	6 mA	5.0 V tolerant	direct level
9	DATA(10)	I/O	6 mA	5.0 V tolerant	direct level
7	DATA(9)	I/O	6 mA	5.0 V tolerant	direct level

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PIN	SYMBOL	TYPE[1]	DRIVE	VOLTAGE	ACTIVITY
6	DATA(8)	I/O	6 mA	5.0 V tolerant	direct level
5	DATA(7)	I/O	6 mA	5.0 V tolerant	direct level
4	DATA(6)	I/O	6 mA	5.0 V tolerant	direct level
3	DATA(5)	I/O	6 mA	5.0 V tolerant	direct level
2	DATA(4)	I/O	6 mA	5.0 V tolerant	direct level
208	DATA(3)	I/O	6 mA	5.0 V tolerant	direct level
207	DATA(2)	I/O	6 mA	5.0 V tolerant	direct level
206	DATA(1)	I/O	6 mA	5.0 V tolerant	direct level
205	DATA(0)	I/O	6 mA	5.0 V tolerant	direct level
172	ADDRESS(20)	I	–	5.0 V tolerant	direct level
173	ADDRESS(19)	I	–	5.0 V tolerant	direct level
174	ADDRESS(18)	I	–	5.0 V tolerant	direct level
175	ADDRESS(17)	I	–	5.0 V tolerant	direct level
176	ADDRESS(16)	I	–	5.0 V tolerant	direct level
177	ADDRESS(15)	I	–	5.0 V tolerant	direct level
178	ADDRESS(14)	I	–	5.0 V tolerant	direct level
179	ADDRESS(13)	I	–	5.0 V tolerant	direct level
180	ADDRESS(12)	I	–	5.0 V tolerant	direct level
181	ADDRESS(11)	I	–	5.0 V tolerant	direct level
185	ADDRESS(10)	I	–	5.0 V tolerant	direct level
186	ADDRESS(9)	I	–	5.0 V tolerant	direct level
187	ADDRESS(8)	I	–	5.0 V tolerant	direct level
188	ADDRESS(7)	I	–	5.0 V tolerant	direct level
189	ADDRESS(6)	I	–	5.0 V tolerant	direct level
190	ADDRESS(5)	I	–	5.0 V tolerant	direct level
191	ADDRESS(4)	I	–	5.0 V tolerant	direct level
192	ADDRESS(3)	I	–	5.0 V tolerant	direct level
193	ADDRESS(2)	I	–	5.0 V tolerant	direct level
194	ADDRESS(1)	I	–	5.0 V tolerant	direct level
195	ADDRESS(0)	I	–	5.0 V tolerant	direct level
170	SIZ(1)	I	–	5.0 V tolerant	direct level
171	SIZ(0)	I	–	5.0 V tolerant	direct level
201	$\overline{CS}_{RG}$	I	–	5.0 V tolerant	low level
202	$\overline{CS}_{SD}$/ADDRESS(21)	I	–	5.0 V tolerant	low level
204	$\overline{DS}$	I	–	5.0 V tolerant	low level
196	R/$\overline{W}$	I	–	5.0 V tolerant	direct level
203	$\overline{DTACK}$	O/Z	6 mA	5.0 V tolerant	low level
199	DMA_REQ	I/O	3 mA	5.0 V tolerant	program level
200	DMA_ACK	I	–	5.0 V tolerant	program level
197	DMA_RDY	O/Z	3 mA	5.0 V tolerant	program level
198	DMA_DONE	I	–	5.0 V tolerant	program level

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PIN	SYMBOL	TYPE[1]	DRIVE	VOLTAGE	ACTIVITY
149	IRQ(1)	O/Z	3 mA	5.0 V tolerant	program level
150	IRQ(0)	O/Z	3 mA	5.0 V tolerant	program level
104	TDI	I	–	5.0 V tolerant	direct level
105	TDO	O/Z	3 mA	5.0 V tolerant	direct level
106	TMS	I	–	5.0 V tolerant	direct level
108	TCK	I	–	5.0 V tolerant	edge
107	TRST	I	–	5.0 V tolerant	low level
121	AV_{DD1}	S	–	–	–
115	AV_{DD2}	S	–	–	–
113	AV_{DD3}	S	–	–	–
118	IDUMP1	–	–	–	–
110	IDUMP2	–	–	–	–
120	RSET	–	–	–	–
119	AV_{SS}	S	–	–	–
27	$V_{DD(CO)}$	S	–	3.3 V	–
79	$V_{DD(CO})$	S	–	3.3 V	–
130	$V_{DD(CO})$	S	–	3.3 V	–
183	$V_{DD(CO)}$	S	–	3.3 V	–
8	V_{DD}	S	–	3.3 V	–
22	V_{DD}	S	–	3.3 V	–
36	V_{DD}	S	–	3.3 V	–
50	V_{DD}	S	–	3.3 V	–
60	V_{DD}	S	–	3.3 V	–
74	V_{DD}	S	–	3.3 V	–
89	V_{DD}	S	–	3.3 V	–
103	V_{DD}	S	–	3.3 V	–
127	V_{DD}	S	–	3.3 V	–
148	V_{DD}	S	–	3.3 V	–
184	V_{DD}	S	–	3.3 V	–
109	$V_{DD(AN)}$	S	–	3.3 V	–
26	$V_{SS(CO)}$	S	–	0 V	–
78	$V_{SS(CO)}$	S	–	0 V	–
129	$V_{SS(CO})$	S	–	0 V	–
182	$V_{SS(CO)}$	S	–	0 V	–
1	V_{SS}	S	–	0 V	–
15	V_{SS}	S	–	0 V	–
31	V_{SS}	S	–	0 V	–
43	V_{SS}	S	–	0 V	–
57	V_{SS}	S	–	0 V	–
67	V_{SS}	S	–	0 V	–
83	V_{SS}	S	–	0 V	–

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PIN	SYMBOL	TYPE[1]	DRIVE	VOLTAGE	ACTIVITY
96	V_{SS}	S	–	0 V	–
122	V_{SS}	S	–	0 V	–
138	V_{SS}	S	–	0 V	–
169	V_{SS}	S	–	0 V	–

Notes

1. Pin type abbreviations: I = Input, O = Output, I/O = Input or Output, O/Z = high impedance Output and S = Supply voltage.

Integrated MPEG AVGD decoders

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APPLICATION INFORMATION
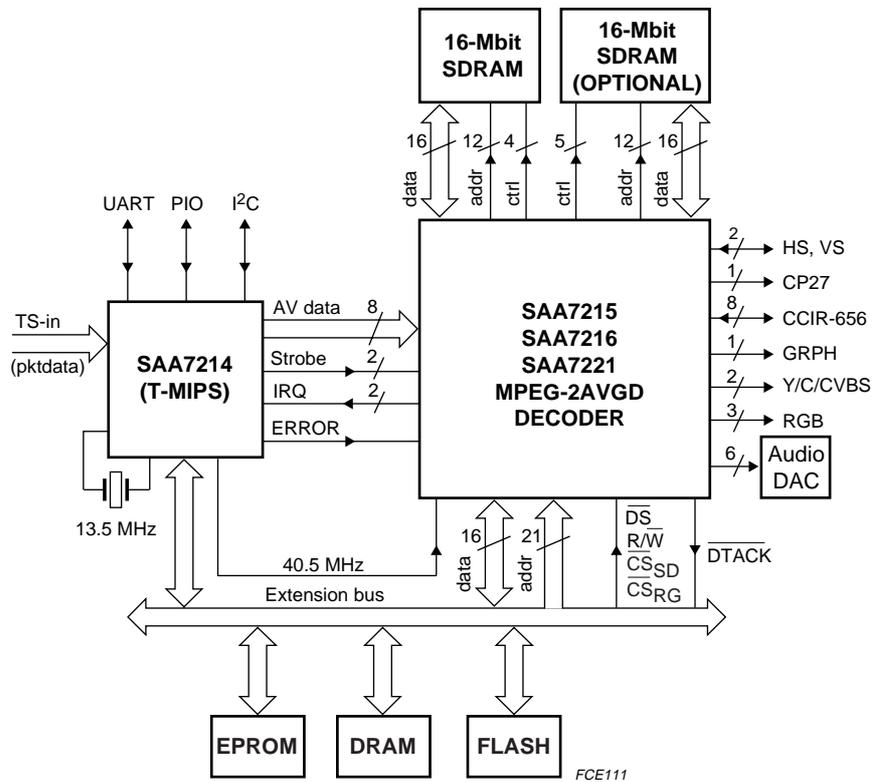
Fig.5 Set-top box example.

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PACKAGE OUTLINE

SQFP208: plastic shrink quad flat package;
208 leads (lead length 1.3 mm); body 28 x 28 x 3.4 mm; high stand-off height

SOT316-1

0   5   10 mm
scale
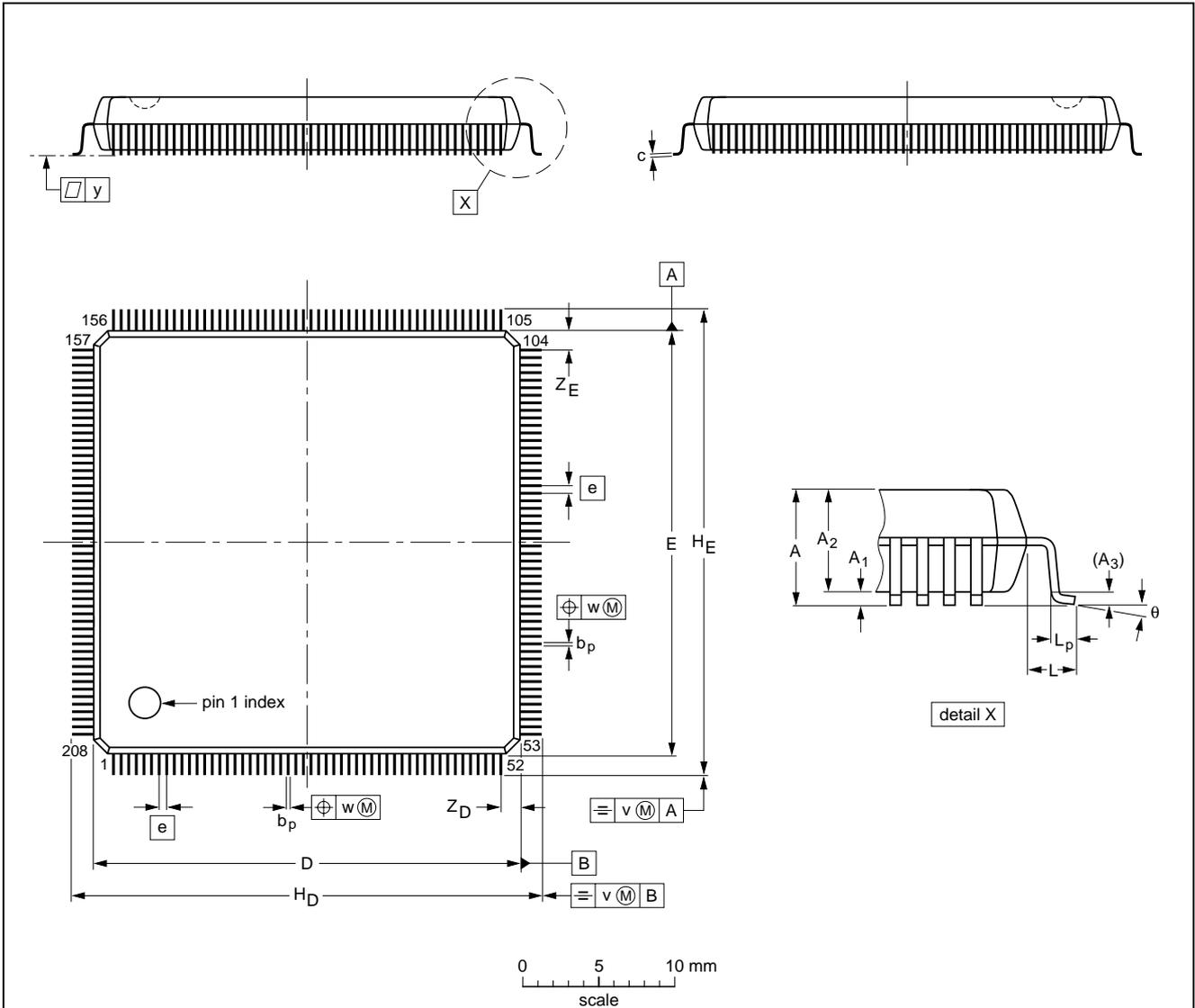
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D⁽¹⁾	E⁽¹⁾	e	H_D	H_E	L	Lₚ	v	w	y	Z_D⁽¹⁾	Z_E⁽¹⁾	θ
mm	4.10	0.50 0.25	3.6 3.2	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.9 30.3	30.9 30.3	1.3	0.75 0.45	0.2	0.08	0.08	1.39 1.11	1.39 1.11	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT316-1		MS-029				~~99-12-27~~ 00-01-25

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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