

INTEGRATED CIRCUITS

DATA SHEET



SAA8115HL Digital camera USB interface

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Digital camera USB interface**SAA8115HL**

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1 FEATURES

- VGA (progressive mode), CIF and medium resolution (PAL non-interlaced mode) CCD sensors compliant
- D1 digital video input (8 bits YUV 4 : 2 : 2 time multiplexed)
- Internal Pulse Pattern Generator (PPG) dedicated for VGA Panasonic, CIF and medium resolution Sharp sensors or compatibles, and frame rate selection
- Frame rate converter
- SDRAM interface for high quality VGA snapshot (uncompressed 4 : 2 : 2 or 4 : 2 : 0)
- Downsampler and scaler (programmable formatter for CIF, QCIF, sub-QCIF, SIF and QSIF) controlled via SNERT (UART) interface
- Flexible compression engine controlled via SNERT (UART) interface
- Selectable output frame rate (up to 15 fps in VGA, up to 30 fps in CIF and QCIF)
- Video packetizer FIFO
- I²C-bus interface for communication between the USB protocol hardware and the external microcontroller
- Microphone/audio input to USB (microphone supply, controllable gain and ADC)
- Integrated analog bus driver (ATX)
- Integrated main oscillator
- Integrated 5 V power supply and reset circuit including functionalities for bus-powered USB device
- Programmable (frequency and duty cycle) switch mode power signal for CCD supply
- Miscellaneous functions (e.g. power management, PLL for audio frequencies).



2 APPLICATIONS

Low-cost desktop video applications with USB interface.

3 GENERAL DESCRIPTION

The SAA8115HL is the second generation of integrated circuit applicable in PC video cameras to convert D1 video signals and analog audio signals to properly formatted USB packets.

This powerful successor of the SAA8117HL can handle up to 15 fps in VGA format or 30 fps in CIF format. High snapshot quality is achievable using the SDRAM interface to an external memory.

It is designed as a back-end of the SAA8112HL (general camera digital processing IC) and is optimized for use with the TDA8784 to TDA8787 (camera pre-processing ICs).

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4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|----------|
| | NAME | DESCRIPTION | VERSION |
| SAA8115HL | LQFP144 | plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm | SOT486-1 |

5 QUICK REFERENCE DATA

Measured over full voltage and temperature range

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------|--------------------------------|----------------------------------|----------------------------|------|------|------|
| V _{DDD} | digital supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V _{DDA} | analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V _{DDA_USB} | analog supply voltage from USB | note 1 | 4.0 | 5.0 | 5.5 | V |
| I _{DD(tot)} | total supply current | V _{DDD} = 3.3 V | – | – | tbf | mA |
| V _I | input signal levels | 3.0 V < V _{DDD} < 3.6 V | low voltage TTL compatible | | | V |
| V _O | output signal levels | 3.0 V < V _{DDD} < 3.6 V | low voltage TTL compatible | | | V |
| f _{clk} | clock frequency | | – | 48 | – | MHz |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | – | – | tbf | mW |
| T _{stg} | storage temperature | | –55 | – | – | °C |
| T _{amb} | ambient temperature | | 0 | 25 | 70 | °C |
| T _j | junction temperature | T _{amb} = 70 °C | –40 | – | +125 | °C |

Note

1. This concerns pins VBUS1 and VBUS2.

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6 BLOCK DIAGRAM

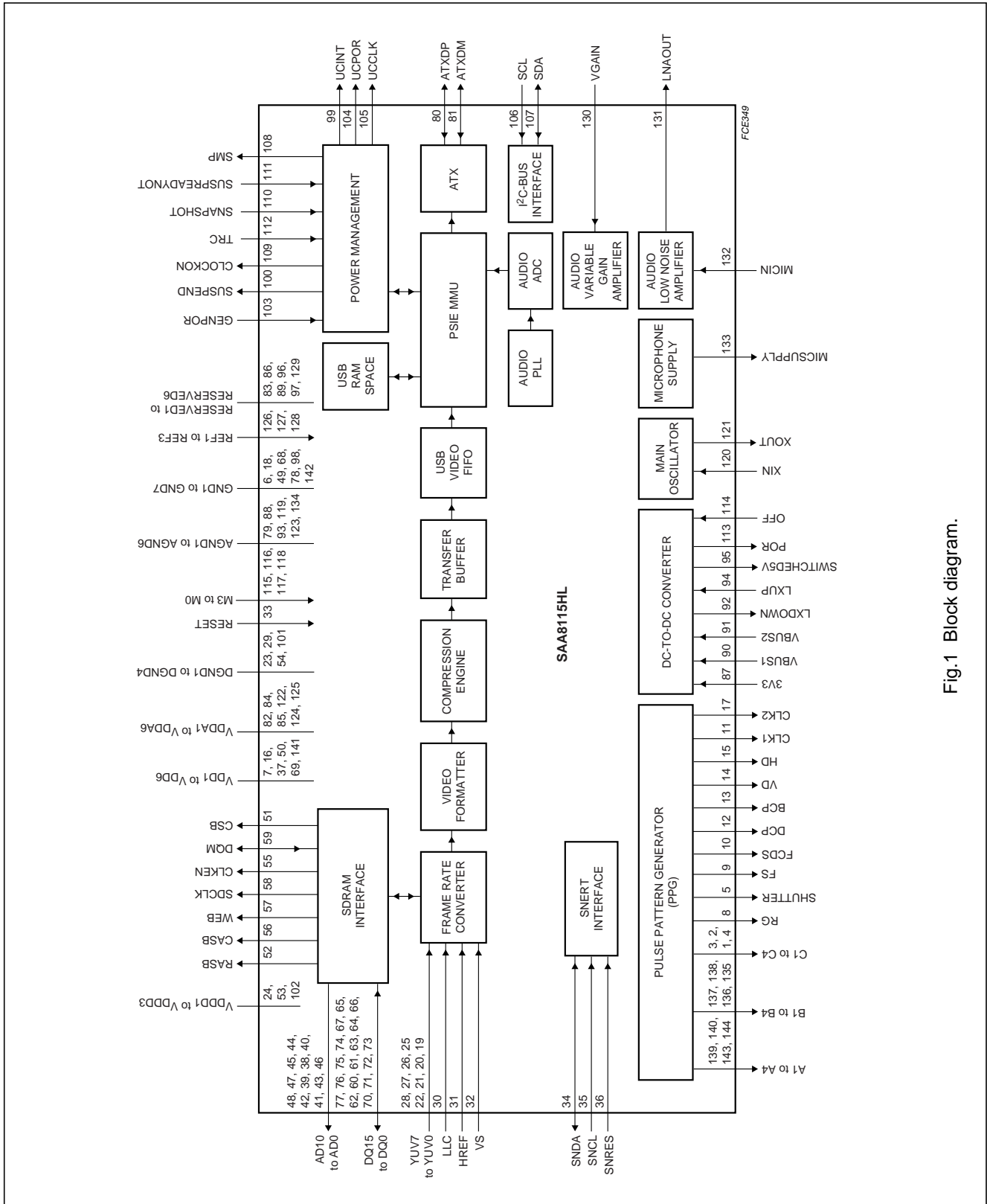


Fig.1 Block diagram.

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7 PINNING

| SYMBOL | PIN | TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|-----|---------------------|---|
| C3 | 1 | O | horizontal CCD transfer pulse output |
| C2 | 2 | O | horizontal CCD transfer pulse output (FH1) |
| C1 | 3 | O | horizontal CCD transfer pulse output (FH2) |
| C4 | 4 | O | horizontal CCD transfer pulse output |
| SHUTTER | 5 | O | shutter control output for CCD charge reset |
| GND1 | 6 | P | ground 1 for output buffers |
| V _{DD1} | 7 | P | supply voltage 1 for output buffers |
| RG | 8 | O | reset output for CCD output amplifier gate |
| FS | 9 | O | data sample-and-hold pulse output to TDA8784/87 (SHD) |
| FCDS | 10 | O | preset sample-and-hold pulse output to TDA8784/87 (SHP) |
| CLK1 | 11 | O | pixel clock to TDA8784/87 and SAA8112HL |
| DCP | 12 | O | dummy clamp pulse output to TDA8784/87 |
| BCP | 13 | O | optical black clamp pulse output to TDA8784/87 |
| VD | 14 | O | vertical definition pulse to SAA8112HL |
| HD | 15 | O | horizontal definition pulse to SAA8112HL |
| V _{DD2} | 16 | P | supply voltage 2 for output buffers |
| CLK2 | 17 | O | double pixel clock to SAA8112HL |
| GND2 | 18 | P | ground 2 for output buffers |
| YUV0 | 19 | I | multiplexed YUV bit 0 |
| YUV1 | 20 | I | multiplexed YUV bit 1 |
| YUV2 | 21 | I | multiplexed YUV bit 2 |
| YUV3 | 22 | I | multiplexed YUV bit 3 |
| DGND1 | 23 | P | digital ground 1 for input buffers, predrivers and for the digital core |
| V _{DD1} | 24 | P | digital supply voltage 1 for input buffers, predrivers and one part of the digital core |
| YUV4 | 25 | I | multiplexed YUV bit 4 |
| YUV5 | 26 | I | multiplexed YUV bit 5 |
| YUV6 | 27 | I | multiplexed YUV bit 6 |
| YUV7 | 28 | I | multiplexed YUV bit 7 |
| DGND2 | 29 | P | digital ground 2 for input buffers, predrivers and for the digital core |
| LLC | 30 | I | line-locked clock input (delayed CLK2) for YUV-port from SAA8112HL |
| HREF | 31 | I | horizontal reference input for YUV-port from SAA8112HL |
| VS | 32 | I | vertical synchronization input for YUV-port from SAA8112HL |
| RESET | 33 | I | Power-on reset input (for video processing and PPG) |
| SNDA | 34 | I/O | data input/output for SNERT-interface (communication between SAA8115HL and SAA8112HL) |
| SNCL | 35 | I | clock input for SNERT-interface (communication between SAA8115HL and SAA8112HL) |
| SNRES | 36 | I | reset input for SNERT-interface (communication between SAA8115HL and SAA8112HL) |

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| SYMBOL | PIN | TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|-----|---------------------|---|
| V _{DD3} | 37 | P | supply voltage 3 for output buffers |
| AD4 | 38 | O | SDRAM output address bit 4 |
| AD5 | 39 | O | SDRAM output address bit 5 |
| AD3 | 40 | O | SDRAM output address bit 3 |
| AD2 | 41 | O | SDRAM output address bit 2 |
| AD6 | 42 | O | SDRAM output address bit 6 |
| AD1 | 43 | O | SDRAM output address bit 1 |
| AD7 | 44 | O | SDRAM output address bit 7 |
| AD8 | 45 | O | SDRAM output address bit 8 |
| AD0 | 46 | O | SDRAM output address bit 0 |
| AD9 | 47 | O | SDRAM output address bit 9 |
| AD10 | 48 | O | SDRAM output address bit 10 |
| GND3 | 49 | P | ground 3 for output buffers |
| V _{DD4} | 50 | P | supply voltage 4 for output buffers |
| CSB | 51 | O | SDRAM chip select output |
| RASB | 52 | O | SDRAM row address strobe output |
| V _{DD2} | 53 | P | digital supply voltage 2 for the switchable digital core |
| DGND3 | 54 | P | digital ground 3 for input buffers, predrivers and for the digital core |
| CLKEN | 55 | O | SDRAM clock enable output |
| CASB | 56 | O | SDRAM column address strobe output |
| WEB | 57 | O | SDRAM write enable output |
| SDCLK | 58 | O | SDRAM clock output |
| DQM | 59 | I/O | SDRAM data mask enable |
| DQ8 | 60 | I/O | SDRAM data I/O bit 8 |
| DQ7 | 61 | I/O | SDRAM data I/O bit 7 |
| DQ9 | 62 | I/O | SDRAM data I/O bit 9 |
| DQ6 | 63 | I/O | SDRAM data I/O bit 6 |
| DQ5 | 64 | I/O | SDRAM data I/O bit 5 |
| DQ10 | 65 | I/O | SDRAM data I/O bit 10 |
| DQ4 | 66 | I/O | SDRAM data I/O bit 4 |
| DQ11 | 67 | I/O | SDRAM data I/O bit 11 |
| GND4 | 68 | P | ground 4 for output buffers |
| V _{DD5} | 69 | P | supply voltage 5 for output buffers |
| DQ3 | 70 | I/O | SDRAM data I/O bit 3 |
| DQ2 | 71 | I/O | SDRAM data I/O bit 2 |
| DQ1 | 72 | I/O | SDRAM data I/O bit 1 |
| DQ0 | 73 | I/O | SDRAM data I/O bit 0 |
| DQ12 | 74 | I/O | SDRAM data I/O bit 12 |
| DQ13 | 75 | I/O | SDRAM data I/O bit 13 |
| DQ14 | 76 | I/O | SDRAM data I/O bit 14 |
| DQ15 | 77 | I/O | SDRAM data I/O bit 15 |

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| SYMBOL | PIN | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------------|-----|---------------------|---|
| GND5 | 78 | P | ground 5 for output buffers |
| AGND1 | 79 | P | analog ground 1 for ATX (transceiver) |
| ATXDP | 80 | I/O | positive driver of the differential data pair input/output (ATX) |
| ATXDM | 81 | I/O | negative driver of the differential data pair input/output (ATX) |
| V _{DDA1} | 82 | P | analog supply voltage 1 for ATX |
| RESERVED1 | 83 | – | test pin 1 (should not be used) |
| V _{DDA2} | 84 | P | analog supply voltage 2 for bandgap (reference) |
| V _{DDA3} | 85 | P | analog supply voltage 3 for bandgap, comparator and ring oscillator |
| RESERVED2 | 86 | – | test pin 2 (should not be used) |
| 3V3 | 87 | I | 3V3 detector input signal |
| AGND2 | 88 | P | analog ground 2 for N-switch |
| RESERVED3 | 89 | – | test pin 3 (should not be used) |
| VBUS1 | 90 | I | supply voltage input 1 from the USB |
| VBUS2 | 91 | I | supply voltage input 2 from the USB |
| LXDOWN | 92 | O | LX coil node output (5 V downconverter) |
| AGND3 | 93 | P | analog ground 3 for N-switch |
| LXUP | 94 | I | LX coil node input (5 V upconverter) |
| SWITCHED5V | 95 | O | 5 V switched power supply |
| RESERVED4 | 96 | – | test pin 4 (should not be used) |
| RESERVED5 | 97 | – | test pin 5 (should not be used) |
| GND6 | 98 | P | ground 6 for output buffers |
| UCINT | 99 | O | interrupt output from USB to microcontroller |
| SUSPEND | 100 | O | control output from USB protocol hardware to microcontroller |
| DGND4 | 101 | P | digital ground 4 for input buffers, predrivers and for the digital core |
| V _{DDD3} | 102 | P | digital supply voltage 3 for input buffers, predrivers and one part of the digital core |
| GENPOR | 103 | I | Power-on reset input (for USB protocol hardware) |
| UCPOR | 104 | O | control output from USB protocol hardware to microcontroller |
| UCCLK | 105 | O | clock output from USB protocol hardware to microcontroller |
| SCL | 106 | I | slave I ² C-bus clock input |
| SDA | 107 | I/O | slave I ² C-bus data input/output |
| SMP | 108 | O | switch mode power pulse output for CCD supplies |
| CLOCKON | 109 | O | control output for main oscillator switched on |
| SNAPSHOT | 110 | I | input for remote wake-up (snapshot) |
| SUSPREADYNOT | 111 | I | input from microcontroller for SUSPEND mode |
| TRC | 112 | I | threshold control input for enabling clock |
| POR | 113 | O | 3.3 V supply domain ready indicator output |
| OFF | 114 | I | disable 5 V switchable supply domain input |
| M3 | 115 | I | test mode control input signal bit 3 |
| M2 | 116 | I | test mode control input signal bit 2 |
| M1 | 117 | I | test mode control input signal bit 1 |

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| SYMBOL | PIN | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------------|-----|---------------------|---|
| M0 | 118 | I | test mode control input signal bit 0 |
| AGND4 | 119 | P | analog ground 4 for crystal oscillator (48 MHz, 3rd overtone) |
| XIN | 120 | I | oscillator input |
| XOUT | 121 | O | oscillator output |
| V _{DDA4} | 122 | P | analog supply voltage 4 for crystal oscillator (48 MHz, 3rd overtone) |
| AGND5 | 123 | P | analog ground 5 for PLL |
| V _{DDA5} | 124 | P | analog supply voltage 5 for PLL |
| V _{DDA6} | 125 | P | analog supply voltage 6 for amplifier and ADC |
| REF1 | 126 | I | reference voltage 1 (used in the ADC) |
| REF2 | 127 | I | reference voltage 2 (used in the ADC) |
| REF3 | 128 | I | reference voltage 3 (used in the amplifier and the ADC) |
| RESERVED6 | 129 | O | test pin 6 (should not be used) |
| VGAIN | 130 | I | variable gain amplifier input |
| LNAOUT | 131 | O | low noise amplifier output |
| MICIN | 132 | I | microphone input |
| MICSUPPLY | 133 | O | microphone supply output |
| AGND6 | 134 | P | analog ground 6 for amplifier and ADC |
| B4 | 135 | O | vertical CCD load pulse output (VH1X) |
| B3 | 136 | O | vertical CCD load pulse output (VH3X) |
| B1 | 137 | O | vertical CCD load pulse output |
| B2 | 138 | O | vertical CCD load pulse output |
| A1 | 139 | O | vertical CCD transfer pulse output (V1X) |
| A2 | 140 | O | vertical CCD transfer pulse output (V2X) |
| V _{DD6} | 141 | P | supply voltage 6 for output buffers |
| GND7 | 142 | P | ground 7 for output buffers |
| A3 | 143 | O | vertical CCD transfer pulse output (V3X) |
| A4 | 144 | O | vertical CCD transfer pulse output (V4X) |

Note

1. I = input, O = output and P = power supply.

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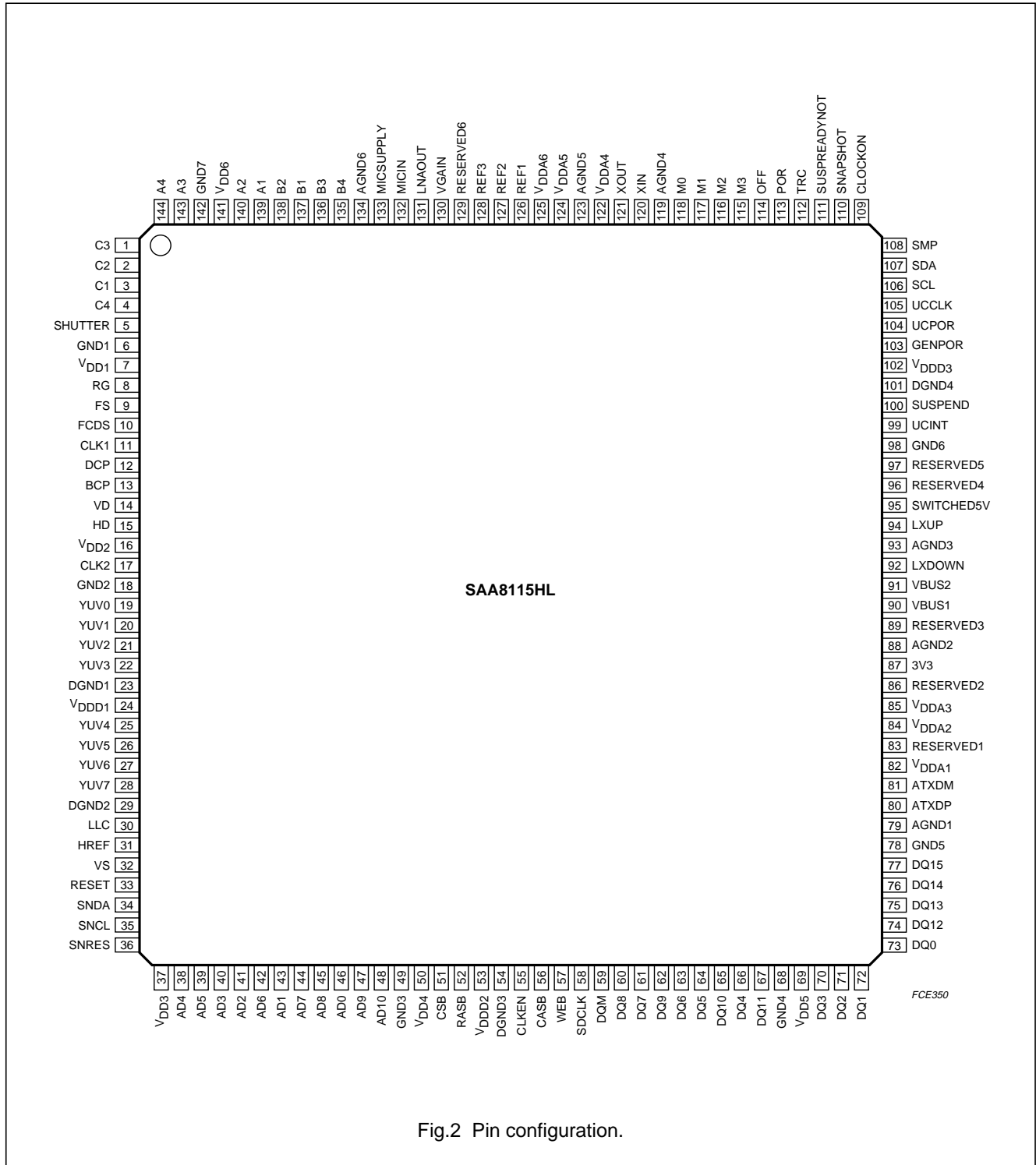


Fig.2 Pin configuration.

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8 FUNCTIONAL DESCRIPTION

8.1 Video synchronization

The video synchronization module is capable of locking to the video signal implementing a horizontal gate signal HREF (HREF = HIGH when data is valid) and a VS signal indicating the start of a new video frame.

8.2 Frame rate converter and SDRAM interface

An optional SDRAM (external) can be accessed using the SDRAM interface which is integrated in the SAA8115HL. Pinning and functionality is based on the NEC μ PD4516161 (16 Mbits) and the NEC μ PD4564163 (64 Mbits).

When used, the memory is placed at the video input of the SAA8115HL before prefilter, scaler and compression engine. At this point only YUV 4 : 2 : 2 formatted data is available.

The use of the SDRAM is twofold:

- Lowering the frame rate. The memory enables to store one frame of video accumulated at a specific rate and to read it out at a lower frame rate. For interline VGA sensors, the input frame rate is either 30 fps or 15 fps. It can be lowered with a factor of 2, 3, 6, 16 or 32. For CIF or medium resolution PAL, the input frame rate is only 30 fps
- Enhanced snapshot mode. Storage of full size VGA pictures in 4 : 2 : 2 format which can be retrieved upon dedicated software command.

8.3 Video formatter: downsampler and cutter

This block is used to achieve the required output format from the specified sensor formats (see Fig.3). It works for YUV 4 : 2 : 2 only. In RAW mode this block is by-passed to create a full resolution snapshot.

Horizontally a downsampling from 512 or 640 to either 384, 320, 192 or 160 or from 352 to 176 is necessary. The horizontal downsampling is performed with the use of a Variable Phase Delay filter (VPD-4). This filter can realize the needed downsample factors. To avoid aliasing, this module also contains a prefilter which has four modes:

- No filter for medium resolution PAL (512 \times 288) to CIF (352 \times 288) or SIF (320 \times 240)
- Prefilter A (3 taps) for VGA (640 \times 480) to CIF or SIF, CIF to QCIF (176 \times 144) or QSIF (160 \times 120)
- Prefilter B (7 taps) for medium resolution PAL to QCIF or QSIF
- Prefilter A combined with prefilter B-comb (13 taps) for VGA to QCIF or QSIF.

Prefilter B-comb is similar to prefilter B but inserts extra taps with amplification 0.

The vertical downsampling in PAL mode is from CIF to QCIF only. This is done via a vertical filter A (3 taps). In VGA mode a 4 taps polyphase filter is applied to scale from 640 \times 480 to CIF and QCIF.

From a full size QCIF picture a sub-QCIF (128 \times 96) cut can be made. For the zoomed sub-QCIF format, the origin (upper left corner) is programmable via SNERT in 13 steps (both horizontally and vertically), so that an electronic pan and tilt is possible.

The incoming 4 : 2 : 2 data is vertically filtered to 4 : 2 : 0, in order to be sent over USB, by throwing away colour samples. In the even lines the V-samples are discarded, in the odd lines the U-samples.

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8.4 Compression engine

The compression engine module (see Fig.3) can process VGA, CIF, SIF, QCIF and QSIF but has optimal performance with CIF resolution (30 fps) and VGA resolution (5 fps). The algorithm is Philips proprietary. The compression ratio is continuously programmable by setting the maximum number of bits which can be used for 4 compressed lines, a so-called band (see Table 1). It is possible to reduce the YUV input data by scaling down (divide by 2 or divide by 4 operations) to 7 or 6 bits per sample. For compression with an output rate below 2 bpp (bits per pixel) it leads to performance improvement.

For a number of compression ratios, performance is also improved thanks to different quantization tables which are defined and stored in a ROM. The required table must be selected via software.

Real time decoding can be done in software on any Pentium™ platform.

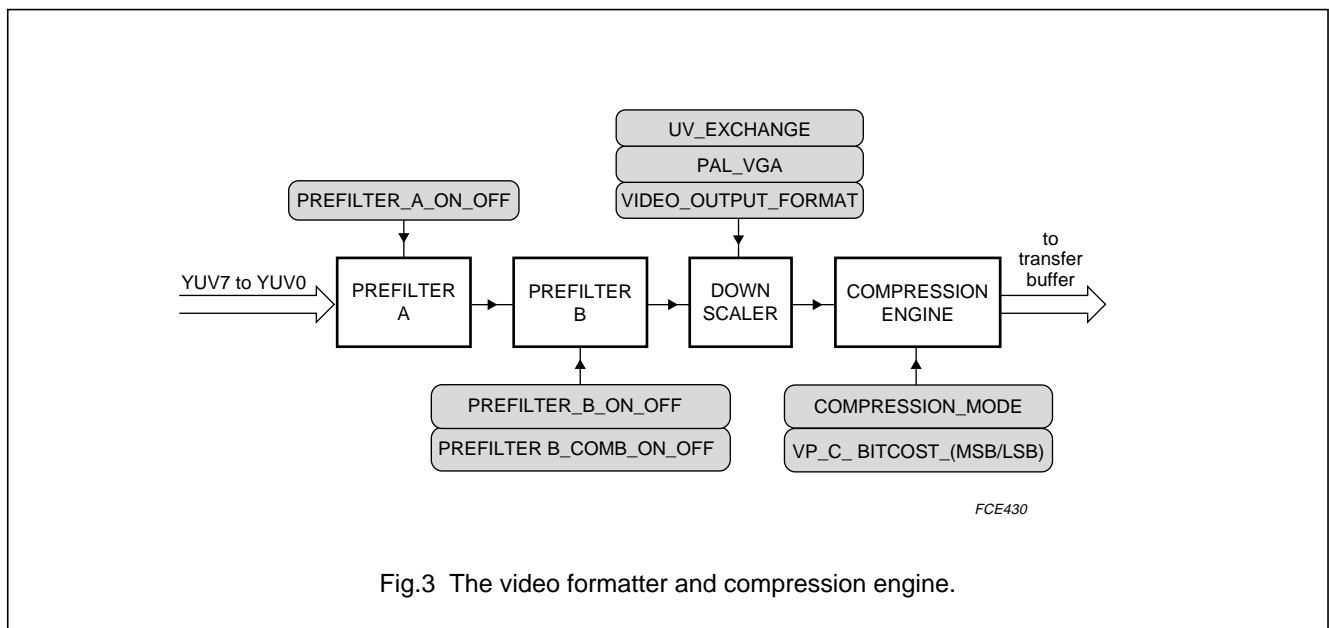


Fig.3 The video formatter and compression engine.

Table 1 Data rate performed by compression engine

| FORMAT | ADVISED DATA RATE | MAXIMUM DATA RATE |
|----------------------|-------------------|-----------------------|
| CIF/SIF | 2 bpp | 12 bpp (uncompressed) |
| QCIF/QSIF | 6 bpp | uncompressed |
| VGA high quality | 3 bpp | 4 bpp |
| VGA | 1.5 bpp | 3 bpp |
| RAW VGA high quality | 4 bpp | 4 bpp |

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8.5 Transfer buffer

The transfer buffer module (see Fig.4) takes care of a smooth transfer of the data to the FIFO of the USB. Moreover the transfer buffer can insert inband synchronization words in the video data stream. This function can be switched on and off with INBAND_CONTROL in register VP_TR_CONTROL (0x36). The synchronization words can only be used with non-compressed data stream and are formatted like 0x00 0xFF 0x<framecounter>₇<linecounter>₉. (Subscript denotes the number of bits and the frame counter is circular incrementing).

The non-compressed data is formatted like:

```
4 : 2 : 0: <optional sync word><Y0><Y1><Y2><Y3>
<C0><C2><Y4><Y5><Y6><Y7><C4><C6>....,
4 : 2 : 2: <optional sync word><Y0><Y1><Y2><Y3>
<U0><V0><U2><V2><Y4>....,
```

where C denotes U-data in the even lines (0, 2, 4 etc.) and V-data in the odd lines (1, 3, 5 etc.).

8.6 USB video FIFO

The USB video FIFO is programmed via the I²C-bus (see Fig.5). The FIFO is designed to achieve three different packets containing video on the isochronous USB channel. Video data is contained in a chain of equally sized USB packets, except for the last packet of a video frame which is always smaller. The video frames can be separated from each other by one or more 0-length packets. For low frame rates (below 10 frames per second) there are always 0-length packets in the stream.

The host can synchronize on the smaller packets for the high frame rates and on the 0-length packets for the low frame rates.

For every mode the FIFO must be adjusted. There are three parameters to program the video FIFO:

- PACKET_SIZE (0x06): this value indicates the length of all packets with video data except for the last packet of a video frame
- FIFO_OFFSET (0x04): this value indicates the number of data in the FIFO before a new packet will be transmitted over USB
- READ_SPACING (0x07): this value indicates the number of 12 MHz clock cycles between read actions from the FIFO.

Moreover the FIFO is enabled and disabled with FIFO_ACTIVE (0x05).

The write process to the FIFO is controlled by the transfer buffer and not programmable.

The read process is executed in the PSIE-MMU and is driven by the USB frame interval (1 ms). Every frame interval the PSIE-MMU tries to read PACKET_SIZE bytes from the FIFO. This read process will not be started when a new video frame is stored in the FIFO and there are less than FIFO_OFFSET bytes written. The read process stops if the next bytes are of another video frame, or if the read-pointer would overtake the write-pointer.

READ_SPACING determines the read rate. Its value can easily be determined with the formula:

$$READ_SPACING < \frac{12000}{PACKET_SIZE}$$

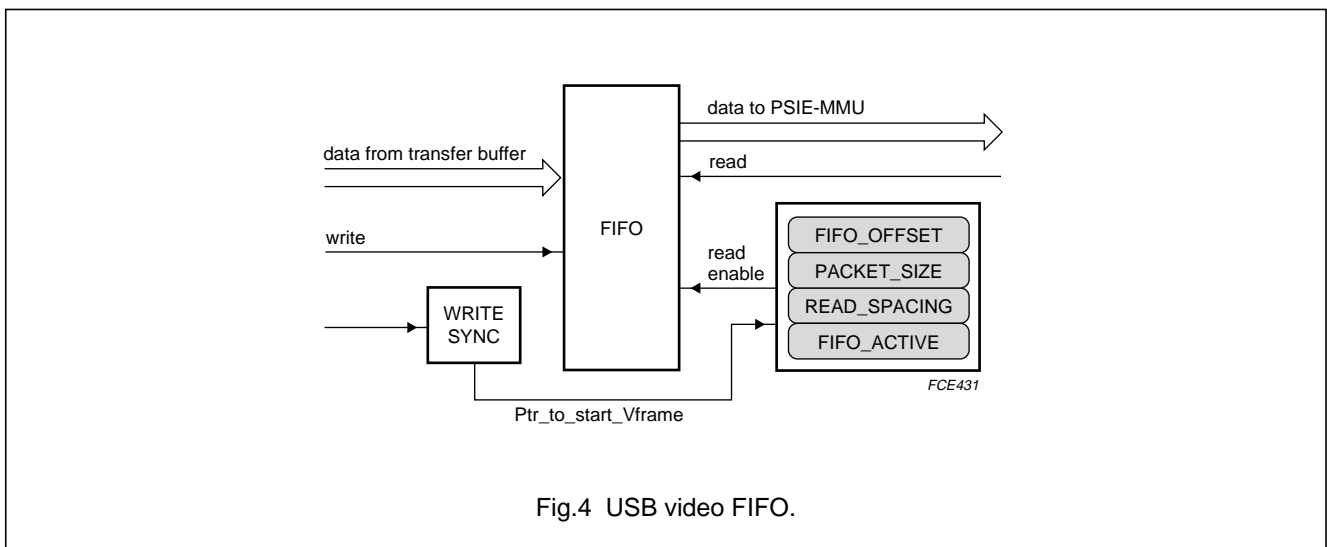


Fig.4 USB video FIFO.

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8.7 PSIE-MMU, I²C-bus interface and USB RAM space

The Programmable Serial Interface Engine (PSIE) and Memory Management Unit (MMU) is the heart of the USB protocol hardware (see Fig.5). It formats the actual packets that are transferred to the USB and passes the incoming packets to the right end-point buffers. These buffers are allocated as part of the USB RAM space.

The microcontroller communicates via the I²C-bus with the PSIE-MMU. The I²C-bus protocol distinguishes three register spaces. These spaces are addressed via different commands. The command is sent to the command address.

Depending on the command it is sent to the PSIE-MMU and/or to the command interpreter which configures the (de-)mux to open the path to the right register space. Subsequent write/reads to/from the data address store or retrieve data from the register space selected by the command.

8.8 ATX interface

The SAA8115HL contains an analog bus driver, called the ATX. It incorporates a differential and two single-ended receivers and a differential transmitter.

The interface to the bus consists of a differential data pair (ATXDM and ATXDP).

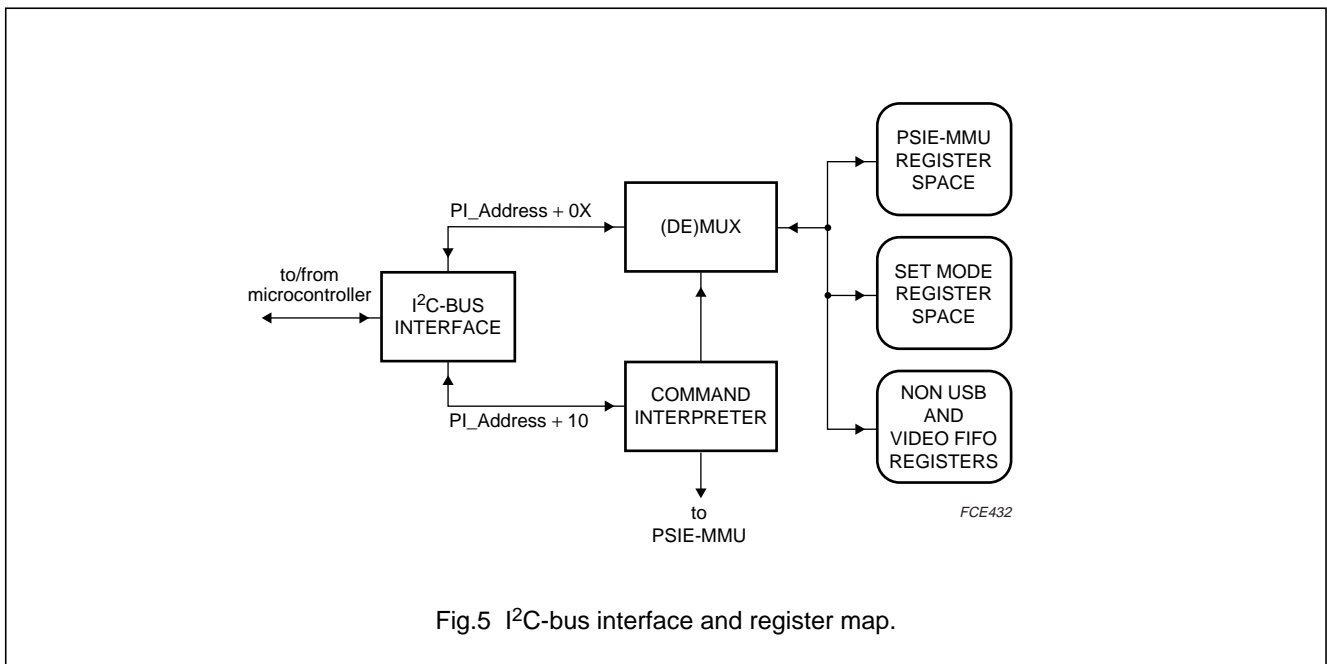


Fig.5 I²C-bus interface and register map.

8.9 Audio

The SAA8115HL contains a microphone supply and an amplifier circuit composed of two stages: a Low Noise Amplifier (LNA) and a variable gain amplifier. The LNA has a fixed gain of 26 dB while the variable gain amplifier can be programmed between 0 and 30 dB by steps of 2 dB. The gain control can be done via either the SNERT interface or the I²C-bus interface (see Table 57).

The serial interface must be first selected using bit SIS (see Table 57). The frequency transfer characteristic of the audio path must be controlled via external high-pass or low-pass filters.

The PLL converts the 48 MHz to $256f_s$ (f_s = audio sample frequency). There are three modes for the PLL to achieve the sample frequencies of 48, 44.1 or 32 kHz (see Table 2).

The bitstream ADC samples the audio signal. It runs at an oversample rate of 256 times the base sample rate. In the application, the bitstream can be converted to parallel 16-bit samples. This conversion is programmable with respect to the effective sample frequency (dropping sample results in a lower effective sample frequency) and sample resolution. As a result the effective sample rate can be determined.

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Table 2 ADC clock frequencies and sample frequencies

| CLOCK (MHz) | DIVIDING NUMBER | SAMPLE FREQUENCY (kHz) | ADCCLOCK (MHz) |
|-------------|-----------------|------------------------|----------------|
| 8.1920 | 1 | 32 | 4.096 |
| | 2 | 16 | 2.048 |
| | 4 | 8 | 1.042 |
| | 8 | note 1 | note 1 |
| 11.2996 | 1 | 44.1 | 5.6448 |
| | 2 | 22.05 | 2.8224 |
| | 4 | 11.025 | 1.4112 |
| | 8 | 5.5125 | 0.7056 |
| 12.2880 | 1 | 48 | 6.144 |
| | 2 | 24 | 3.072 |
| | 4 | 12 | 1.536 |
| | 8 | 6 | 0.768 |

Note

1. Not supported.

Table 3 Typical SAA8115HL compatible sensors

| SENSOR TYPE | BRAND | PART NUMBER |
|-----------------------|---|---------------------------|
| VGA | Sony | ICX098AK |
| | Panasonic | MN3777PP and MN37771PT |
| | Sharp | LZ24BP |
| Medium resolution PAL | Sony | ICX054, ICX086 and ICX206 |
| | Panasonic | MN37210FP |
| | Sharp | LZ2423B and LZ2423H |
| | Toshiba | TCD5391AP |
| CIF | Sharp | LZ244D and LZ2547 |
| Other sensors | all the sensors fully compatible with the above mentioned sensors | |

8.10 Sensor pulse pattern generator

The SAA8115HL incorporates a Pulse Pattern Generator (PPG) function. The PPG can be used for medium resolution PAL, CIF and VGA CCD-sensors (see Table 3).

Depending on the sensor type, an external inverter driver should be required to convert the 3.3 V pulses into a voltage suitable for the used CCD-sensor.

The active video size is 512 × 288 for medium resolution PAL, 352 × 288 for CIF and 640 × 480 for VGA. The total H × V size are 685 × 292 for medium resolution PAL/CIF and 823 × 486 for VGA. It should be noted that additional HD pulses are added during the vertical blanking interval to reach a total of 312 lines in PAL and CIF modes and 525 lines in VGA mode as required by the SAA8112HL.

A high level of flexibility is available for the PPG thanks to 19 internal registers (see Section 9.1.3).

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8.11 Power management

USB requires the device to switch power states. The SAA8115HL contains a power management module since the complete camera may not consume more than 500 μ A during the power state called SUSPEND. This requires that even the crystal oscillator must be switched off. The SAA8115HL is not functional except for some logic that enables the IC to wake-up the camera. After wake-up of the SAA8115HL first the clock to the microcontroller is generated and thereafter an interrupt is generated to wake-up the microcontroller. Therefore the clock of the microcontroller is generated by the SAA8115HL.

The power management module also sets a flag in register SET_MODE_AND_READ (PSIE_MMU_STATUS). After a reset the microcontroller should check this register via the I²C-bus and find the cause of the wake-up. Different causes may require different start-up routines.

The internal video processing core uses another supply domain which can be switched off during SUSPEND mode.

The PPG is switched off by setting PPG_RESUME_MODE (0x08) and resetting PAL_VGA (0x09).

In non CIF modes the power consumption is reduced by resetting COMPRESSION_MODE (0x2F) and COMPRESSION_CLOCK (0x09).

The SAA8115HL has the feature to autonomously wake-up from SUSPEND mode, but requires microcontroller interference before going in SUSPEND mode (via the signal on pin SUSPREADYNOT).

Since the main oscillator of the SAA8115HL is switched off during SUSPEND mode, precautions are needed to avoid undefined states when the clock is switched on. This is ensured via the pins CLOCKON and TRC. Pin CLOCKON goes HIGH as soon as the main oscillator is switched on. The oscillator will need some time to make a stable 48 MHz signal. However, the clock is only passed through to other parts of the SAA8115HL when the level on pin TRC reaches a certain threshold. The time needed to reach the threshold can be trimmed with an external RC circuit.

8.12 Power supply

A power supply regulator is integrated in the device. This DC-to-DC converter transforms the USB supply voltage (range from 4.0 to 5.5 V) into a stable 5 V supply voltage. This power domain is switchable. The power circuit also generates a reset signal when the external 3.3 V supply voltage is stable and in range.

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9 CONTROL REGISTER DESCRIPTION

This specification gives an overview of all registers.

9.1 SNERT (UART)

The SAA8115HL is partly controlled via SNERT. The frame rate converter, the SDRAM interface, the video formatter, the compression engine, the PPG, the SMP and the audio functions are controlled via SNERT. This SNERT interface works independently from the frame rate and can always be operated in the full frequency range.

Via SNERT the following registers are accessible (see Table 4).

Table 4 SNERT write registers SAA8115HL

| ADDRESS | FUNCTION |
|-----------|--|
| 00 | write register soft reset (see Table 5) |
| 01 to 05 | write registers Frame Rate Converter (FRC) including the SDRAM interface |
| 06 and 07 | reserved |
| 08 to 1A | write registers Pulse Pattern Generator (PPG) |
| 1B to 1F | reserved |
| 20 to 38 | write registers video formatter and compression engine |
| 39 to 3C | reserved |
| 3D and 3E | write registers Switch Mode Power (SMP) |
| 3F | write register audio variable gain amplifier |

9.1.1 GENERAL REGISTER

Table 5 Detailed description of SNERT general register 0x00

| BIT | | | | | | | | SNERT REGISTER 00: SOFT_RESET |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | | | | reserved |
| | | | | | 1 | | | RESET_VP_C compression engine in reset state |
| | | | | | 0 | | | compression engine operating |
| | | | | | | 1 | | RESET_VP_VF formatter engine in reset state |
| | | | | | | 0 | | formatter engine operating |
| | | | | | | | 1 | RESET_FRC frame rate converter engine in reset state (by default) |
| | | | | | | | 0 | frame rate converter engine operating |

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9.1.2 FRAME RATE CONVERTER AND SDRAM INTERFACE REGISTERS

Table 6 Detailed description of SNERT FRC and SDRAM register 0x01

| BIT | | | | | | | | SNERT REGISTER 01: FRC_CONTROL_0 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | | | | | number of active lines after rising edge of VS signal; range: 0 to 6 (by default 0) |
| | | | | | | | | FRAMERATE_DIVIDER_SELECT_BIT |
| | | | | 1 | 1 | 1 | | undefined |
| | | | | 1 | 1 | 0 | | 32 (30 fps in; 0.9375 fps out) |
| | | | | 1 | 0 | 1 | | 16 (15 fps in; 0.9375 fps out) |
| | | | | 1 | 0 | 0 | | 6 (30 fps in; 5 fps out) |
| | | | | 0 | 1 | 1 | | 3 (30 fps in; 10 fps out) or (15 fps in; 5 fps out) |
| | | | | 0 | 1 | 0 | | 2 (30 fps in; 15 fps out) or (15 fps in; 7.5 fps out) |
| | | | | 0 | 0 | 1 | | 1 (1 fps in; 1 fps out) (by default) |
| | | | | 0 | 0 | 0 | | undefined |
| | | | | | | | 1 | LLC_CLKFREQ 24 MHz (by default) |
| | | | | | | | 0 | 12 MHz |

Table 7 Detailed description of SNERT FRC and SDRAM register 0x02

| BIT | | | | | | | | SNERT REGISTER 02: FRC_CONTROL_1 |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | | | | | | reserved |
| | | | | | | | | REFRESH_MODE |
| | | | 1 | | | | | automatic SRAM refresh |
| | | | 0 | | | | | precharge command as implicit refresh (by default) |
| | | | | X | X | | | REFRESH_CLOCK (MSBs) see Table 9 |
| | | | | | | | | INPUT_FORMAT |
| | | | | | | 1 | 1 | undefined |
| | | | | | | 1 | 0 | medium resolution |
| | | | | | | 0 | 1 | CIF |
| | | | | | | 0 | 0 | VGA (by default) |

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Table 8 Detailed description of SNERT FRC and SDRAM register 0x03

| BIT | | | | | | | | SNERT REGISTER 03: FRC_ROWWIDTH |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | specifies the width of the row of the SDRAM 95 for PAL sensors 159 for VGA sensors (by default) 63 for CIF sensors |

Table 9 Detailed description of SNERT FRC and SDRAM register 0x04

| BIT | | | | | | | | SNERT REGISTER 04: FRC_REFRESH_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | specifies the number of clock cycles between two refresh cycles 246 for PAL sensors 395 for VGA sensors (by default) 239 for CIF sensors |

Table 10 Detailed description of SNERT FRC and SDRAM register 0x05

| BIT | | | | | | | | SNERT REGISTER 05: FRC_STOPWRITE |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | number of lines in a frame 243 for VGA sensors (by default) 146 for PAL or CIF sensors |

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9.1.3 PULSE PATTERN GENERATOR REGISTERS

Table 11 Detailed description of SNERT PPG register 0x08

| BIT | | | | | | | | SNERT REGISTER 08: PPG_CONTROL_0 |
|-----|---|---|--------|--------|---------------------------------|---------------------------------|---------------------------------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | | | | | | reserved |
| | | | 1 0 | | | | | SHUTTER_UPDATE_BUFFER during the vertical blanking (shutter speed is buffered) immediately (by default) |
| | | | | 1 0 | | | | PPG_RESUME_MODE switched off (except vertical transfer pulses in case of VGA sensors) operating (by default) |
| | | | | | 1 1 1 0 0 0 0 | 1 0 0 1 1 0 1 | X 1 0 1 1 0 1 | PPG_FRAMERATE undefined 5 fps 10 fps 15 fps 20 fps 24 fps 30 fps (by default) |

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Table 12 Detailed description of SNERT PPG register 0x09

| BIT | | | | | | | | SNERT REGISTER 09: PPG_CONTROL_1 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | | | | | | | | COMPRESSION_CLOCK |
| | 1 | 1 | X | X | | | | reserved |
| | 1 | 0 | 1 | 1 | | | | 24 MHz |
| | 1 | 0 | 1 | 0 | | | | 19.2 MHz |
| | 1 | 0 | 0 | 1 | | | | 16 MHz |
| | 1 | 0 | 0 | 0 | | | | 12 MHz (by default) |
| | 0 | 1 | 1 | 1 | | | | 9.6 MHz |
| | 0 | 1 | 1 | 0 | | | | 8.0 MHz |
| | 0 | 1 | 0 | 1 | | | | 6.0 MHz |
| | 0 | 1 | 0 | 0 | | | | 4.8 MHz |
| | 0 | 0 | 1 | 1 | | | | 4.0 MHz |
| | 0 | 0 | 1 | 0 | | | | 2.4 MHz |
| | 0 | 0 | 0 | 1 | | | | 2.0 MHz |
| | 0 | 0 | 0 | 0 | | | | off |
| | | | | | | 1 | 1 | VGA_SENSOR_TYPE (valid if MSB set to logic 0) |
| | | | | | | 1 | 0 | VGA (Sony and Panasonic) |
| | | | | | | 0 | X | VGA (Sharp) |
| | | | | | | | | reserved |
| | | | | | | | | PAL_VGA |
| | | | | | | 1 | | PAL or CIF timing |
| | | | | | | 0 | | VGA timing (by default) |

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Table 13 Detailed description of SNERT PPG register 0x0A

| BIT | | | | | | | | SNERT REGISTER 0A: PPG_H_CTRL |
|-----|--------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | 1 0 | | | | | | | RG_SHORT RG pulse width is set to half of nominal value RG pulse width is set to nominal value |
| | | 1 1 0 0 0 0 | X X 1 1 0 0 | 1 0 1 0 1 0 | | | | FH2_CTRL (non FT mode); note 1 no horizontal blanking no horizontal blanking, pulse inverted blanked to HIGH, starts HIGH blanked to LOW, starts LOW blanked to LOW, starts HIGH blanked to HIGH, starts LOW |
| | | | | | 1 1 0 0 0 0 | X X 1 1 0 0 | 1 0 1 0 1 0 | FH1_CTRL (non FT mode); note 1 no horizontal blanking, pulse inverted no horizontal blanking blanked to HIGH, starts LOW blanked to HIGH, starts HIGH blanked to HIGH, starts LOW blanked to LOW, starts HIGH |

Note

1. If bits [5 to 3] equal bits [2 to 0] then FH2 is the inverse of FH1.

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Table 14 Detailed description of SNERT PPG register 0x0B

| BIT | | | | | | | | SNERT REGISTER 0B: PPG_V_INV |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | A4_INV positive pulses negative pulses |
| | 1 | | | | | | | A3_INV positive pulses negative pulses |
| | | 1 | | | | | | A2_INV negative pulses positive pulses |
| | | | 1 | | | | | A1_INV negative pulses positive pulses |
| | | | | 1 | | | | B4_INV positive pulses negative pulses |
| | | | | | 1 | | | B3_INV positive pulses negative pulses |
| | | | | | | 1 | | B2_INV negative pulses positive pulses |
| | | | | | | | 1 | B1_INV negative pulses |
| | | | | | | | 0 | positive pulses |

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Table 15 Detailed description of SNERT PPG register 0x0C

| BIT | | | | | | | | SNERT REGISTER 0C: PPG_H_INV |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | CLK2_INV inverted pulses nominal pulses |
| 0 | | | | | | | | |
| | 1 | | | | | | | CLK1_INV inverted pulses nominal pulses |
| | 0 | | | | | | | |
| | | 1 | | | | | | FS_INV positive pulses negative pulses |
| | | 0 | | | | | | |
| | | | 1 | | | | | FCDS_INV positive pulses negative pulses |
| | | | 0 | | | | | |
| | | | | 1 | | | | FR_INV positive pulses negative pulses |
| | | | | 0 | | | | |
| | | | | | 1 | | | C3_INV negative pulses positive pulses |
| | | | | | 0 | | | |
| | | | | | | 1 | | C2_INV negative pulses positive pulses |
| | | | | | | 0 | | |
| | | | | | | | 1 | C1_INV negative pulses positive pulses |
| | | | | | | | 0 | |

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Table 16 Detailed description of SNERT PPG register 0x0D

| BIT | | | | | | | | SNERT REGISTER 0D: PPG_MISC_INV |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | SELECT_A2 A2 is HIGH during read-out gate in line 2 A2 is LOW during read-out gate in line 2 |
| 0 | | | | | | | | |
| | 1 | | | | | | | SELECT_A3 A3 equals A4 (in case of VGA type 1 sensors) A3 equals A2 |
| | 0 | | | | | | | |
| | | 1 | | | | | | C4_INV negative pulses positive pulses |
| | | 0 | | | | | | |
| | | | 1 | | | | | CR_INV positive pulses negative pulses |
| | | | 0 | | | | | |
| | | | | 1 | | | | BCP_INV negative pulses positive pulses |
| | | | | 0 | | | | |
| | | | | | 1 | | | DCP_INV negative pulses positive pulses |
| | | | | | 0 | | | |
| | | | | | | 1 | | HD_INV negative pulses positive pulses |
| | | | | | | 0 | | |
| | | | | | | | 1 | VD_INV negative pulses |
| | | | | | | | 0 | positive pulses |

Table 17 Detailed description of SNERT PPG register 0x0E

| BIT | | | | | | | | SNERT REGISTER 0E: PPG_SHUTTERSPEED_V_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of line number (9 bits) |

Table 18 Detailed description of SNERT PPG register 0x0F

| BIT | | | | | | | | SNERT REGISTER 0F: PPG_SHUTTERSPEED_H_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) |

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Table 19 Detailed description of SNERT PPG register 0x10

| BIT | | | | | | | | SNERT REGISTER 10: PPG_SHUTTERSPEED_MSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | | | | | reserved |
| | | | | 1 | | | | SENSOR_TYPE Sony |
| | | | | 0 | | | | Sharp |
| | | | | | X | X | | MSBs of pixel number (10 bits) |
| | | | | | | | X | MSBs of line number (9 bits) |

Table 20 Detailed description of SNERT PPG register 0x11

| BIT | | | | | | | | SNERT REGISTER 11: PPG_BCP_START_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where BCP starts |

Table 21 Detailed description of SNERT PPG register 0x12

| BIT | | | | | | | | SNERT REGISTER 12: PPG_BCP_STOP_LSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where BCP stops |

Table 22 Detailed description of SNERT PPG register 0x13

| BIT | | | | | | | | SNERT REGISTER 13: PPG_DCP_START_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where DCP starts |

Table 23 Detailed description of SNERT PPG register 0x14

| BIT | | | | | | | | SNERT REGISTER 14: PPG_DCP_STOP_LSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where DCP stops |

Table 24 Detailed description of SNERT PPG register 0x15

| BIT | | | | | | | | SNERT REGISTER 15: PPG_BCP_DCP_MSB |
|-----|---|---|---|---|---|---|---|------------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | | | | | | | MSBs of PPG_DCP_STOP |
| | | X | X | | | | | MSBs of PPG_DCP_START |
| | | | | X | X | | | MSBs of PPG_BCP_STOP |
| | | | | | | X | X | MSBs of PPG_BCP_START |

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Table 25 Detailed description of SNERT PPG register 0x16

| BIT | | | | | | | | SNERT REGISTER 16: PPG_B3_START_LSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where B3 starts |

Table 26 Detailed description of SNERT PPG register 0x17

| BIT | | | | | | | | SNERT REGISTER 14: PPG_B3_STOP_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where B3 stops |

Table 27 Detailed description of SNERT PPG register 0x18

| BIT | | | | | | | | SNERT REGISTER 18: PPG_B4_START_LSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where B4 starts |

Table 28 Detailed description of SNERT PPG register 0x19

| BIT | | | | | | | | SNERT REGISTER 19: PPG_B4_STOP_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | 8 LSBs of pixel number (10 bits) where B4 stops |

Table 29 Detailed description of SNERT PPG register 0x1A

| BIT | | | | | | | | SNERT REGISTER 1A: PPG_B3_B4_MSB |
|-----|---|---|---|---|---|---|---|----------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | | | | | | | MSBs of PPG_B4_STOP |
| | | X | X | | | | | MSBs of PPG_B4_START |
| | | | | X | X | | | MSBs of PPG_B3_STOP |
| | | | | | | X | X | MSBs of PPG_B3_START |

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9.1.4 VIDEO FORMATTER AND COMPRESSION ENGINE REGISTERS

Table 30 Detailed description of SNERT video formatter register 0x20

| BIT | | | | | | | | SNERT REGISTER 20: VP_VF_CONTRL_0 |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | | | | | | | reserved |
| | | X | | | | | | UV_EXCHANGE exchange chrominance irregularities if needed |
| | | | 1 | 1 | | | | SCALE_DATA: limits the number of bits of the video signal undefined |
| | | | 1 | 0 | | | | 6 bits |
| | | | 0 | 1 | | | | 7 bits |
| | | | 0 | 0 | | | | 8 bits |
| | | | | | 1 | | | PREFILTER_B_COMB_ON_OFF (if filter B is on) prefilter B_COMB with 13 taps |
| | | | | | 0 | | | prefilter B_COMB with 7 taps |
| | | | | | | 1 | | PREFILTER_B_ON_OFF on with 7 taps |
| | | | | | | 0 | | bypassed |
| | | | | | | | 1 | PREFILTER_A_ON_OFF on with 3 taps |
| | | | | | | | 0 | bypassed |

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Table 31 Detailed description of SNERT video formatter register 0x21

| BIT | | | | | | | | SNERT REGISTER 21: VP_VF_CONTRL_1 |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | 420_FIL_BYPASS: 4 : 2 : 0 formatter mode throw away samples average UV samples |
| 0 | | | | | | | | |
| | 1 | | | | | | | VGA_RAW: data mode raw data, no scaling or 4 : 2 : 0 formatting YUV data |
| | 0 | | | | | | | |
| | | 1 | 1 | 1 | | | | VIDEO_OUTPUT_FORMAT undefined |
| | | 1 | 1 | 0 | | | | SIF |
| | | 1 | 0 | 1 | | | | QSIF |
| | | 1 | 0 | 0 | | | | undefined |
| | | 0 | 1 | 1 | | | | VGA |
| | | 0 | 1 | 0 | | | | CIF |
| | | 0 | 0 | 1 | | | | QCIF |
| | | 0 | 0 | 0 | | | | sub-QCIF |
| | | | | | 1 | 1 | 1 | VIDEO_INPUT_FORMAT undefined |
| | | | | | 1 | 1 | 0 | square SIF (sensors with square pixels) |
| | | | | | 1 | 0 | 1 | CIF (sensors with 12/11 pixel ratio format) |
| | | | | | 1 | 0 | 0 | medium resolution PAL |
| | | | | | 0 | 1 | 1 | undefined |
| | | | | | 0 | 1 | 0 | undefined |
| | | | | | 0 | 0 | 1 | undefined |
| | | | | | 0 | 0 | 0 | VGA |

Table 32 Detailed description of SNERT video formatter register 0x22

| BIT | | | | | | | | SNERT REGISTER 22: VP_VF_VCOEF_C0_0 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 0 phase 0 |

Table 33 Detailed description of SNERT video formatter register 0x23

| BIT | | | | | | | | SNERT REGISTER 23: VP_VF_VCOEF_C0_1 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 0 phase 1 |

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Table 34 Detailed description of SNERT video formatter register 0x24

| BIT | | | | | | | | SNERT REGISTER 24: VP_VF_VCOEF_C0_2 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 0 phase 2 |

Table 35 Detailed description of SNERT video formatter register 0x25

| BIT | | | | | | | | SNERT REGISTER 25: VP_VF_VCOEF_C1_0 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 1 phase 0 |

Table 36 Detailed description of SNERT video formatter register 0x26

| BIT | | | | | | | | SNERT REGISTER 26: VP_VF_VCOEF_C1_1 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 1 phase 1 |

Table 37 Detailed description of SNERT video formatter register 0x27

| BIT | | | | | | | | SNERT REGISTER 27: VP_VF_VCOEF_C1_2 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 1 phase 2 |

Table 38 Detailed description of SNERT video formatter register 0x28

| BIT | | | | | | | | SNERT REGISTER 28: VP_VF_VCOEF_C2_0 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 2 phase 0 |

Table 39 Detailed description of SNERT video formatter register 0x29

| BIT | | | | | | | | SNERT REGISTER 29: VP_VF_VCOEF_C2_1 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 2 phase 1 |

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Table 40 Detailed description of SNERT video formatter register 0x2A

| BIT | | | | | | | | SNERT REGISTER 2A: VP_VF_VCOEF_C2_2 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 2 phase 2 |

Table 41 Detailed description of SNERT video formatter register 0x2B

| BIT | | | | | | | | SNERT REGISTER 2B: VP_VF_VCOEF_C3_0 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 3 phase 0 |

Table 42 Detailed description of SNERT video formatter register 0x2C

| BIT | | | | | | | | SNERT REGISTER 2C: VP_VF_VCOEF_C3_1 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 3 phase 1 |

Table 43 Detailed description of SNERT video formatter register 0x2D

| BIT | | | | | | | | SNERT REGISTER 2D: VP_VF_VCOEF_C3_2 |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | X | X | X | vertical filter coefficient tap 3 phase 2 |

Table 44 Detailed description of SNERT video formatter register 0x2E

| BIT | | | | | | | | SNERT REGISTER 2E: VP_VF_LIMITER |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | output of the video formatter is clipped to this maximum value |

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Table 45 Detailed description of SNERT compression engine register 0x2F

| BIT | | | | | | | | SNERT REGISTER 2F: VP_VF_CONTROL |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | X | X | X | X | | | | QTABLE_SELECT: quantization table select range [0 : 15] |
| | | | | | 1 | 1 | | DC_COEFF_LENGTH undefined |
| | | | | | 1 | 0 | | 8 bits |
| | | | | | 0 | 1 | | 7 bits |
| | | | | | 0 | 0 | | 6 bits |
| | | | | | | | 1 | COMPRESSION_MODE on |
| | | | | | | | 0 | off (by default) |

Table 46 Detailed description of SNERT compression engine register 0x30

| BIT | | | | | | | | SNERT REGISTER 30: VP_C_YMASK |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | operates an AND between this value and the compression engine input; can be used to set bit positions in the Y signal to 0 (by default 0x00) |

Table 47 Detailed description of SNERT compression engine register 0x31

| BIT | | | | | | | | SNERT REGISTER 31: VP_C_UVMASK |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | operates an AND between this value and the compression engine input; can be used to set bit positions in the UV signal to 0 (by default 0x00) |

Table 48 Detailed description of SNERT compression engine register 0x32

| BIT | | | | | | | | SNERT REGISTER 32: VP_C_BITCOST_MSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | set the compression ratio; the bitcost determines the maximum number of bits generated by the compression algorithm for 4 subsequent lines |

Table 49 Detailed description of SNERT compression engine register 0x33

| BIT | | | | | | | | SNERT REGISTER 33: VP_C_BITCOST_LSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | set the compression ratio; the bitcost determines the maximum number of bits generated by the compression algorithm for 4 subsequent lines |

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Table 50 Detailed description of SNERT compression engine register 0x34

| BIT | | | | | | | | SNERT REGISTER 34: VP_C_THRESHOLD_MSB |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | output of the video formatter is clipped to this maximum value |

Table 51 Detailed description of SNERT compression engine register 0x35

| BIT | | | | | | | | SNERT REGISTER 35: VP_C_THRESHOLD_LSB |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | threshold must be set to: (number of UV blocks per band) × (DC_COEFF_LENGTH + 2) |

Table 52 Detailed description of SNERT compression engine register 0x36

| BIT | | | | | | | | SNERT REGISTER 36: VP_TR_CONTROL |
|-----|--------|--------|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | 1 0 | | | | | | | VGA_FORMAT 4 : 2 : 2 (uncompressed only) 4 : 2 : 0 |
| | | 1 0 | | | | | | INBAND_CONTROL on off |
| | | | X | X | X | X | X | LLC_OUT_DIV: select the rate at which the video data is transmitted to the USB core range [1 to 31] |

Table 53 Detailed description of SNERT compression engine register 0x37

| BIT | | | | | | | | SNERT REGISTER 37: VP_TR_SQCIF_OFFSET |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | | | | | VERTICAL_OFFSET range 3 × [0 to 15] |
| | | | | X | X | X | X | HORIZONTAL_OFFSET range 4 × [0 to 12] |

Table 54 Detailed description of SNERT compression engine register 0x38

| BIT | | | | | | | | SNERT REGISTER 38: VP_VS_V_SHIFT |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | shift internal line counter with respect to VS pulse |

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9.1.5 SWITCH MODE POWER REGISTERS

Table 55 Detailed description of SNERT SMP register 0x3D

| BIT | | | | | | | | SNERT REGISTER 3D: SMP_PERIOD |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | period of SMP signal in units of $4 \times XOSC_PERIOD$ (0 by default) |

Table 56 Detailed description of SNERT SMP register 0x3E

| BIT | | | | | | | | SNERT REGISTER 3E: SMP_LOWTIME |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | low edge of SMP signal in units of $4 \times XOSC_PERIOD$ (0 by default) |

9.1.6 AUDIO VARIABLE GAIN AMPLIFIER

Table 57 Detailed description of SNERT audio gain amplifier register 0x3F

| BIT | | | | | | | | SNERT REGISTER 3F: AUDIO_VGAIN |
|-----|---|---|---|---|---|---|---|---------------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | | | | | | | reserved |
| | | 1 | | | | | | SIS: serial interface select SNERT |
| | | 0 | | | | | | I ² C-bus |
| | | | X | | | | | reserved |
| | | | | X | X | X | X | variable gain settings (0 to 30 dB) |

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9.2 I²C-bus interface

The USB function has its own I²C-bus interface for communication with the microcontroller. The I²C-bus uses two addresses:

- Command address for writing commands to the Memory Manager (MM)
- Data address for writing/reading data to/from the Memory Manager (MM).

An address is a byte. The 7 MSBs are the actual address, the LSB is the R \bar{W} bit. When it is logic 0, data is transferred from the master to the slave, when it is logic 1, data is written from the slave to the master.

The 6 MSBs of the two addresses are equal and are defined by the PI_Address = 010111 (see Table 58). The LSB of the address differentiates between the command address and the data address. When bit 1 is logic 1 the address is the command address (0x5E) and when bit 1 is logic 0 the address is one of the data addresses (0x5C or 0x5D).

Table 58 I²C-bus addresses

| BIT | | | | | | | | ADDRESS |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0x5C: for writing data to the memory manager |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0x5D: for reading data from the memory manager |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0x5E: for writing commands |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0x5F: not in use |

9.2.1 COMMANDS

The commands listed in Table 59 must be sent to the I²C-bus address 0x5E.

Table 59 I²C-bus USB command codes

| BIT | | | | | | | | FUNCTION |
|-----|---|------------------|---|---------|---|---|---|------------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | end-point number | | | | | | select end-point |
| 0 | 1 | end-point number | | | | | | read/write status |
| 1 | 0 | end-point number | | | | | | initialize/read status information |
| 1 | 1 | 0 | 1 | address | | | | read/write register bank |
| 1 | 1 | 1 | 0 | 0 | X | X | X | not used |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | set non-USB register |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | read/write data |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | acknowledge setup |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | set buffer empty |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | set buffer full |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | read interrupt register |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | read current frame number |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | send resume |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | set status change bits |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | set mode |

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Table 60 Detailed description of set mode and write register overview

| BYTE | SET_MODE_AND_WRITE |
|------|---|
| 3 | N1 timer: programmable timer for power management; counts 12 MHz cycles; must be bigger than number of cycles needed for the microcontroller to go in power-down state after pin SUSPREADYNOT is made LOW |
| 2 | N2 timer: programmable timer for power management; counts 12 MHz cycles; determines the time between the microcontroller clock is switched off and the main clock is switched off |
| 1 | PSIE-MMU control byte (see Table 61) |

Table 61 Detailed description of set mode and write byte 3

| BIT | | | | | | | | PSIE-MMU CONTROL BYTE |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | | | | | | reserved |
| | | | 1 | | | | | interrupt after isochronous audio transfer for each isochronous audio transfer an interrupt to the microcontroller will be generated; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8115HL |
| | | | 0 | | | | | no interrupts are given to the microcontroller |
| | | | | 1 | | | | interrupt after isochronous video transfer for each isochronous video transfer an interrupt to the microcontroller will be generated; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8115HL |
| | | | | 0 | | | | no interrupts are given to the microcontroller |
| | | | | | 1 | | | audio end-point audio end-point enabled; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8115HL |
| | | | | | 0 | | | audio end-point disabled; the PSIE-MMU will not react on in-tokens on the audio end-point |
| | | | | | | 1 | | video end-point video end-point enabled; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8115HL |
| | | | | | | 0 | | video end-point disabled; the PSIE-MMU will not react on in-tokens on the video end-point |
| | | | | | | | 1 | error debug mode interrupts are generated only in the event the transfer is not successfully completed; the microcontroller can read data from the interrupt and status registers to see the cause of this error |
| | | | | | | | 0 | all successful USB transactions are reported to the microcontroller via an interrupt; default set to logic 0 upon general power-on reset by the SAA8115HL |

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Table 62 Detailed description of set mode and read status byte

| BIT | | | | | | | | PSIE-MMU STATUS BYTE |
|-----|---|---|---|--------|--------|--------|--------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | | | | | reserved |
| | | | | 1 0 | | | | remote wake-up status flag remote wake-up when device is in SUSPEND mode no remote wake-up |
| | | | | | 1 0 | | | resume status flag bus resume by the host when device is in SUSPEND mode no bus resume |
| | | | | | | 1 0 | | bus reset status flag bus reset no bus reset |
| | | | | | | | 1 0 | power-up status flag general power-up reset no power-up reset |

9.2.2 END-POINTS

The SAA8115HL has 6 logical end-points which are listed in Table 63.

Table 63 Mapping of logical to physical end-point numbers for used end-points

| END-POINT NAME | LOGICAL END-POINT | BUFFER SIZE | PHYSICAL END-POINT | |
|---------------------|-------------------|-------------|--------------------|----|
| | | | OUT | IN |
| Control end-point | 0 | 8 | 0 | 1 |
| Control end-point | 1 | 8 | 2 | 3 |
| Interrupt end-point | 2 | 8 | – | 4 |
| Interrupt end-point | 3 | 8 | – | 5 |
| Iso video end-point | 4 | 96.0 | – | 6 |
| Iso video end-point | 5 | 35.1 | – | 7 |

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9.2.3 CONTROL TOP REGISTERS

The following registers can be written on I²C-bus address 1 after the command 0xE8 on I²C-bus address 0.

Table 64 I²C-bus control top registers

| ADDRESS | CONTROL TOP REGISTERS (BASE ADDRESS: 0x08) |
|---------|--|
| 0x08 | clock control |
| 0x09 | reset control |
| 0x0A | mux block control |
| 0x0B | power-on analog modules control |

Table 65 Detailed description of I²C-bus control top registers 0x08

| BIT | | | | | | | | TOP REGISTER 0x08: CLKSHOP_CONTROL |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | select ADC clock source sel_ad: clock generated from ADC sel_pll: clock generated from PLL |
| | 0 | 0 | | | | | | set clock dividers for ADC set_divide00: divided by 1 set_divide01: divided by 2 set_divide10: divided by 4 set_divide11: divided by 8 |
| | 0 | 1 | | | | | | |
| | 1 | 0 | | | | | | |
| | 1 | 1 | | | | | | |
| | | | X | | | | | reserved |
| | | | | 1 | | | | disable 48 MHz clock dis_clk_48: disable 48 MHz clock enable clock |
| | | | | 0 | | | | |
| | | | | | 1 | | | disable receiver clock dis_clk_rec: disable receiver clock enable clock |
| | | | | | 0 | | | |
| | | | | | | 1 | | disable ADC clock dis_clk_ad: disable ADC clock enable clock |
| | | | | | | 0 | | |
| | | | | | | | X | reserved |

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Table 66 Detailed description of I²C-bus control top registers 0x09

| BIT | | | | | | | | TOP REGISTER 0x09: RST_GEN AND PLL_CONTROL |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 0 | 0 | | | | | | | set PLL frequency fcode00: 256 × 44.1 kHz |
| 0 | 1 | | | | | | | fcode01: 256 × 32 kHz |
| 1 | 0 | | | | | | | fcode10: 256 × 48 kHz |
| 1 | 1 | | | | | | | fcode11: 256 × 44.1 kHz |
| | | X | X | | | | | reserved |
| | | | | 1 | | | | reset PSIE-MMU top module upc_rst_mmu: resetting the USB protocol block (called PSIE-MMU) during tests or in case of errors |
| | | | | 0 | | | | no reset |
| | | | | | X | | | reserved |
| | | | | | | 1 | | reset ADIF top module upc_rst_adif: resetting the digital audio part during tests or in case of errors |
| | | | | | | 0 | | no reset |
| | | | | | | | 1 | reset AGC module upc_rst_AGC: resetting the AGC control during tests or in case of errors |
| | | | | | | | 0 | no reset |

Table 67 Detailed description of I²C-bus control top registers 0x0A

| BIT | | | | | | | | TOP REGISTER 0x0A: IO_MUX_CONTROL |
|-----|---|---|---|---|---|---|---|-----------------------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | reserved |

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Table 68 Detailed description of I²C-bus control top registers 0x0B

| BIT | | | | | | | | TOP REGISTER 0x0B: POWER_CONTROL_OF_ANALOG_MODULES |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | power control oscillator module upc_osc_off: power management 48 MHz enabled power management 48 MHz disabled |
| | 1 | | | | | | | power control audio module upc_osc_ad_off: power management audio enabled power management audio disabled |
| | | 1 | | | | | | power control PLL module upc_pll_off: PLL power-off power-on |
| | | | X | | | | | reserved |
| | | | | 1 | | | | power control ADC module left channel upc_adl_off: power-off power-on |
| | | | | | 1 | | | power control ADC module right channel upc_adr_off: power-off power-on |
| | | | | | | 1 | | power control AGC module left channel upc_AGCl_off: power-off power-on |
| | | | | | | | 1 | power control AGC module right channel upc_AGCr_off: power-off power-on |

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9.2.4 VIDEO FIFO REGISTERS

Table 69 I²C-bus video FIFO registers overview

| ADDRESS | VIDEO FIFO REGISTERS (BASE ADDRESS: 0x04) |
|---------|---|
| 0x04 | FIFO offset (8 LSBs) |
| 0x05 | FIFO active and FIFO offset (3 MSBs) |
| 0x06 | packet size (8 LSBs) |
| 0x07 | read spacing and packet size (2 MSBs) |

Table 70 Detailed description of I²C-bus video FIFO registers 0x04

| BIT | | | | | | | | FIFO REGISTER 0x04: FIFO_OFFSET |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | FIFO_OFFSET mode_fifo_offset: sets the minimum contents of the FIFO that has to be reached, before a new video frame will be put on the USB. This value can be set between 0 and 2047. Total 11 bits with 8 LSBs in this register and 3 MSBs in register 0x05. |

Table 71 Detailed description of I²C-bus video FIFO registers 0x05

| BIT | | | | | | | | FIFO REGISTER 0x05: FIFO_ACTIVE AND FIFO_OFFSET |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| 1 | | | | | | | | FIFO_ACTIVE mode_active: FIFO is active and the contents of the other mode registers should not be updated by the microcontroller (maledictive) |
| 0 | | | | | | | | FIFO not active |
| | X | X | X | X | | | | reserved |
| | | | | | X | X | X | FIFO_OFFSET (MSBs) 3 MSBs of the offset value; see also register 0x04 |

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Table 72 Detailed description of I²C-bus video FIFO registers 0x06

| BIT | | | | | | | | FIFO REGISTER 0x06: PACKET_SIZE |
|-----|---|---|---|---|---|---|---|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | X | X | PACKET_SIZE mode_packet_size: sets the packet size of the USB video channel. Packets can vary in size between 0 and 1023. Total 10 bits with 8 LSBs in this register and 2 MSBs in register 0x07. |

Table 73 Detailed description of I²C-bus video FIFO registers 0x07

| BIT | | | | | | | | FIFO REGISTER 0x07: READ_SPACING AND PACKET_SIZE |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | X | X | X | X | X | | | READ_SPACING mode_read_spacing: sets the periodicity of the read pulses; the periodicity can be set from 1 to 63 (from '000001' to '111111') |
| | | | | | | X | X | PACKET_SIZE mode_packet_size: 2 MSBs of the value (8 LSBs in register 0x06) |

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9.2.5 ADIF TOP REGISTERS

Table 74 I²C-bus ADIF top registers overview

| ADDRESS | ADIF TOP REGISTERS (BASE ADDRESS: 0x0C) |
|---------|---|
| 0x0C | reserved |
| 0x0D | reserved |
| 0x0E | VGA control gain |
| 0x0F | ADIF control (ADIF2MMU) |

Table 75 Detailed description of I²C-bus ADIF top registers 0x0E

| BIT | | | | | | | | ADIF REGISTER 0x0E: GAIN_CONTROL |
|-----|--------|---|---|-----------------------|-----------------------|-----------------------|-----------------------|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | 0 1 | | | | | | | GAIN_SOURCE_SELECT reserved gain is controlled directly by bits 3 to 0 |
| | | X | X | | | | | reserved |
| | | | | 0 0 : 0 1 | 0 0 : 1 1 | 0 0 : 1 1 | 0 1 : 1 1 | GAIN_CONTROL; 0 to 30 dB in steps of 2 dB 0 dB 2 dB : 28 dB 30 dB |

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Table 76 Detailed description of I²C-bus ADIF top registers 0x0F

| BIT | | | | | | | | ADIF REGISTER 0x0F: ADIF_CONTROL |
|-----|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PARAMETER |
| X | | | | | | | | reserved |
| | 0 | 0 | | | | | | number of bytes per sample 0 (reserved) |
| | 0 | 1 | | | | | | 1 (8 bits audio samples) |
| | 1 | 0 | | | | | | 2 (16 bits audio samples) |
| | 1 | 1 | | | | | | 3 (24 bits audio samples) |
| | | | 0 | | | | | selection mono/stereo operation mono |
| | | | 1 | | | | | stereo |
| | | | | 0 | | | | selection input for ADC path (ADIF mux) digital input (from I ² S-bus) |
| | | | | 1 | | | | analog input (from Vin_left and Vin_right) |
| | | | | | 0 | | | selection high-pass filter (DC filter) for ADC down sample filter high-pass filter off |
| | | | | | 1 | | | high-pass filter on |
| | | | | | | 0 | 0 | selection audio serial input format I ² S-bus |
| | | | | | | 0 | 1 | LSB-justified, 16 bits |
| | | | | | | 1 | 0 | LSB-justified, 18 bits |
| | | | | | | 1 | 1 | LSB-justified, 20 bits |

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10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------------|--|------------|--------------|-------------------------------|--------|
| V _{DDA} | analog supply voltage | | -0.5 | +4.0 | V |
| V _{DDA_USB} | analog supply voltage from USB | note 1 | -0.5 | +5.5 | V |
| V _{DDD} | digital supply voltage | | -0.5 | +4.0 | V |
| V _n | voltage on pins AGND and DGND all other pins | | -0.5 -0.5 | +4.0 V _{DD} + 0.5 | V V |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _{amb} | ambient temperature | | 0 | 70 | °C |
| T _j | junction temperature | | -40 | +125 | °C |

Note

1. This concerns pins VBUS1 and VBUS2.

11 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|----------------------|---|-------------|-------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | 45 | K/W |

12 CHARACTERISTICS

V_{DDD} = V_{DDA} = 3.3 V ±10%; T_{amb} = 0 to 70 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------------------|--------------------------------|--------------------------|---------------------|------|---------------------|------|
| Supplies | | | | | | |
| V _{DDDn} | digital supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V _{DDAn} | analog supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V _{DDA_USB} | analog supply voltage from USB | note 1 | 4.0 | 5.0 | 5.5 | V |
| V _{DGND} | digital ground supply | | -0.3 | 0.0 | +0.3 | V |
| V _{AGND} | analog ground supply | | -0.3 | 0.0 | +0.3 | V |
| I _{DDn} | digital supply current | T _{amb} = 25 °C | - | - | tbf | mA |
| I _{DDAn} | analog supply current | T _{amb} = 25 °C | - | - | tbf | mA |
| Data and control inputs | | | | | | |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| V _{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| Data and control outputs | | | | | | |
| V _{OL} | LOW-level output voltage | | 0 | - | 0.1V _{DDD} | V |
| V _{OH} | HIGH-level output voltage | | 0.9V _{DDD} | - | V _{DDD} | V |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------------|-------------------------|------|---------|------|------------|
| Microphone supply | | | | | | |
| I_{DD0} | supply current | | – | 0.85 | 1.2 | mA |
| V_{ref} | input reference voltage | at $\frac{1}{2}V_{DDA}$ | – | 1.65 | – | V |
| V_O | output voltage | $V_{DDA} = 3.3$ V | – | 3.0 | – | V |
| I_o | output current | | – | – | 2.0 | mA |
| Low noise amplifier | | | | | | |
| TRANSFER FUNCTION | | | | | | |
| R_i | input impedance | | 3.5 | 5.0 | – | k Ω |
| I_{DD1} | supply current | | – | 0.85 | 1.2 | mA |
| A | amplification | | 27 | 28 | 29 | dB |
| $V_{o(rms)}$ | output voltage (RMS value) | | – | – | 800 | mV |
| THD | total harmonic distortion | note 2 | – | –69 | –63 | dB |
| V_{OO1} | output offset voltage | | – | 0.0 | 1.0 | mV |
| BIASING | | | | | | |
| I_{ref1} | reference current | | – | 10 | – | μ A |
| Variable gain amplifier | | | | | | |
| TRANSFER FUNCTION | | | | | | |
| R_i | input impedance | | 7.0 | 10.5 | 13 | k Ω |
| I_{DD2} | supply current | | – | 0.45 | 0.6 | mA |
| A | amplification | | 0.0 | – | 32 | dB |
| THD | total harmonic distortion | note 3 | – | –88 | –82 | dB |
| | | note 4 | – | –65 | –57 | dB |
| V_{OO2} | output offset voltage | A = 0 dB | – | 1.0 | 2.0 | mV |
| | | A = 30 dB | – | 14 | 30 | mV |
| BIASING | | | | | | |
| I_{ref2} | reference current | | – | 10 | – | μ A |
| Audio PLL | | | | | | |
| $f_{i(clk)}$ | clock input frequency | | – | 48 | – | MHz |
| $f_{o(clk)}$ | clock output frequency | note 5 | – | 11.2996 | – | MHz |
| B | bandwidth | | – | 2.3 | – | kHz |
| ζ | damping | | – | 0.98 | – | |
| Audio ADC ($\Sigma\Delta$ converter) | | | | | | |
| INPUTS | | | | | | |
| f_i | input signal frequency | | 1 | – | 20 | kHz |
| $V_{i(rms)}$ | input voltage (RMS value) | | – | 800 | – | mV |
| TRANSFER FUNCTION | | | | | | |
| N | order of the $\Sigma\Delta$ | | – | 3 | – | |
| N_{bit} | number of output bits | | – | 1 | – | |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|-----------------------|------|-------|--------|----------|
| $N_{\text{bit(eq)}}$ | equivalent output resolution (bit) | | – | 16 | – | |
| DR_i | dynamic range at input | note 6 | – | 96.6 | – | dB |
| f_{clk} | clock frequency | | – | – | 5.6448 | MHz |
| δ | clock frequency duty factor | | – | 50 | – | % |
| THD | total harmonic distortion | | – | –70 | –55 | dB |
| ATX transceiver | | | | | | |
| DRIVER CHARACTERISTICS IN FULL SPEED MODE: PINS ATXDP AND ATXDM | | | | | | |
| $f_{\text{o(sample)}}$ | sample output frequency | | 4 | – | 48 | kHz |
| t_r | rise transition time | $C_L = 50 \text{ pF}$ | 4 | – | 20 | ns |
| t_f | fall transition time | $C_L = 50 \text{ pF}$ | 4 | – | 20 | ns |
| t_{match} | transition time matching | note 7 | 90 | – | 110 | % |
| V_{cr} | output signal crossover voltage | | 1.3 | – | 2.0 | V |
| Z_o | driver output impedance | steady state drive | 30 | – | 42 | Ω |
| RECEIVER CHARACTERISTICS IN FULL SPEED MODE: PINS ATXDP AND ATXDM | | | | | | |
| $f_{\text{i(sample)}}$ | sample input frequency | | 5 | – | 55 | kHz |
| $f_{\text{i(D)}}$ | data input frequency rate | | – | 12.00 | – | Mbits/s |
| t_{frame} | frame interval | | – | 1.000 | – | ms |
| DC-to-DC converter | | | | | | |
| 5 V UP AND DOWN CONVERTER (SWITCHABLE SUPPLY DOMAIN) | | | | | | |
| V_O | output voltage | | 4.9 | 5.0 | 5.1 | V |
| V_{ripple} | ripple on output voltage | | – | 20 | – | mV |
| I_L | load current | | – | – | 150 | mA |
| $R_{\text{DSON_P1}}$ | PMOS switch-on resistance; down converter | note 8 | – | 1.0 | – | Ω |
| $R_{\text{DSON_N1}}$ | NMOS switch-on resistance; down converter | note 8 | – | 4.5 | – | Ω |
| $R_{\text{DSON_P2}}$ | PMOS switch-on resistance; up converter | note 8 | – | 1.1 | – | Ω |
| $R_{\text{DSON_N2}}$ | NMOS switch-on resistance; up converter | note 8 | – | 4.6 | – | Ω |

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Notes

1. This concerns pins VBUS1 and VBUS2.
2. The distortion is measured at 1 kHz, $V_{o(rms)} = 600$ mV.
3. The distortion is measured at 1 kHz, $V_{o(rms)} = 600$ mV and $A = 0$ dB.
4. The distortion is measured at 1 kHz, $V_{o(rms)} = 600$ mV and $A = 30$ dB.
5. Frequencies depend on PLL settings (see Table 2).
6. Defined here as: $20 \times \log \frac{\text{input voltage}}{\text{equivalent input noise voltage}}$
7. Transition time matching: $t_{\text{match}} = \frac{t_r}{t_f} \times 100\%$
8. Including metal and contact resistance on chip and bonding wire resistance.

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13 TIMING

$V_{DD} = V_{DDA} = 3.3 \text{ V} \pm 10\%$; $T_{amb} = 0 \text{ to } 70 \text{ }^\circ\text{C}$.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|------------|------|------|------|------|
| Data input related to LLC (see Fig.6) | | | | | | |
| PINS YUV0 TO YUV7, HREF, VS | | | | | | |
| $t_{su(i)(D)}$ | data input set-up time | | 5 | – | – | ns |
| $t_{h(i)(D)}$ | data input hold time | | 3 | – | – | ns |
| PPG high-speed pulses for Sony ICX098AK VGA CCD-sensor (see Fig.7) | | | | | | |
| t_{d1} | delay between falling edge C2 and rising edge C1 | | –3.5 | –2.5 | –1.5 | ns |
| t_{d2} | delay between rising edge C2 and falling edge C1 | | 0 | 1.5 | 3 | ns |
| t_{d3} | delay between falling edge C1 and rising edge FCDS | | 20.5 | 21.5 | 22.5 | ns |
| t_{d4} | delay between rising edge C1 and rising edge FS | | 21.5 | 22.5 | 23.5 | ns |
| t_{d5} | delay between rising edge C1 and falling edge RG | | 0 | 1.5 | 3 | ns |
| t_{d6} | delay between falling edge CLK1 and rising edge C1 | | 0 | 0.5 | 2 | ns |
| t_{d7} | delay between rising edge CLK1 and falling edge C1 | | 2.5 | 3.0 | 3.5 | ns |
| t_{d8} | delay between rising edge CLK2 and rising edge C1 | | 1 | 1.5 | 2 | ns |
| $t_{WH(C1)}$ | C1 pulse width HIGH | | 80 | 81 | – | ns |
| $t_{WL(C2)}$ | C2 pulse width LOW | | 84 | 85 | – | ns |
| $t_{WL(FCDS)}$ | FCDS pulse width LOW | | 17 | 18.5 | – | ns |
| $t_{WL(FS)}$ | FS pulse width LOW | | 41 | 42 | – | ns |
| $t_{WL(RG)}$ | RG pulse width LOW | | 42 | 43 | – | ns |
| $t_{WL(CLK1)}$ | CLK1 pulse width LOW | | 84 | 84.5 | – | ns |
| $t_{WH(CLK2)}$ | CLK2 pulse width HIGH | | 39 | 40 | – | ns |
| t_r | rise time | note 1 | | | | |
| | pulse C1 | | – | 4 | – | ns |
| | pulse C2 | | – | 4 | – | ns |
| | pulse RG | | – | 4 | – | ns |
| | pulse FCDS | | – | 4 | – | ns |
| | pulse FS | | – | 4 | – | ns |
| t_f | fall time | note 1 | | | | |
| | pulse C1 | | – | 4 | – | ns |
| | pulse C2 | | – | 4 | – | ns |
| | pulse RG | | – | 4 | – | ns |
| | pulse FCDS | | – | 4 | – | ns |
| | pulse FS | | – | 4 | – | ns |

Note

1. $C_L = 11 \text{ pF}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

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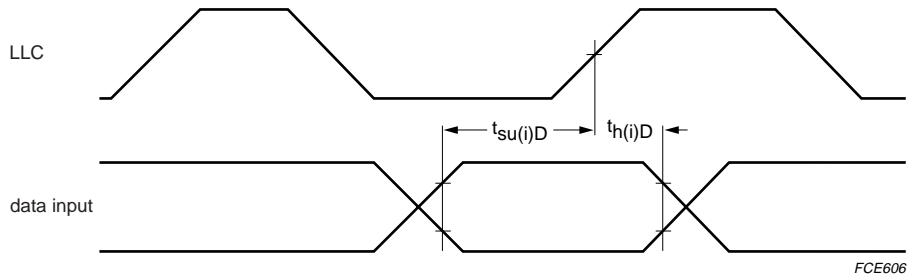


Fig.6 Data input timing.

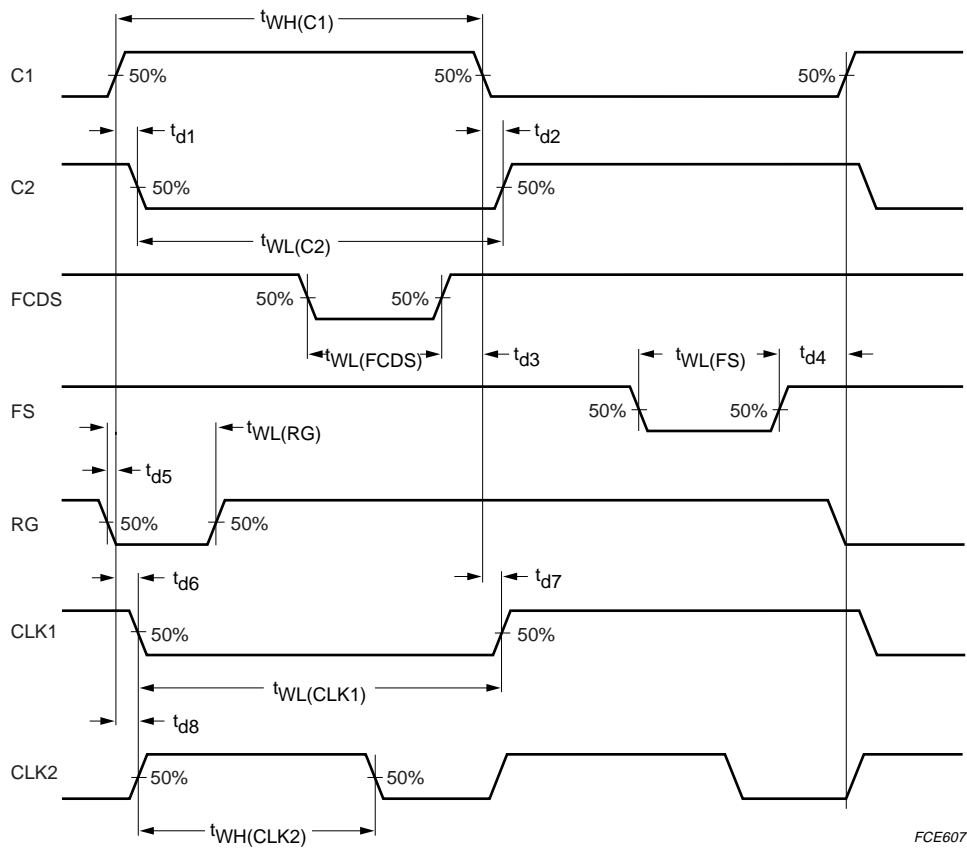


Fig.7 PPG high-speed pulses for Sony ICX098AK VGA CCD-sensor.

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14 APPLICATION INFORMATION

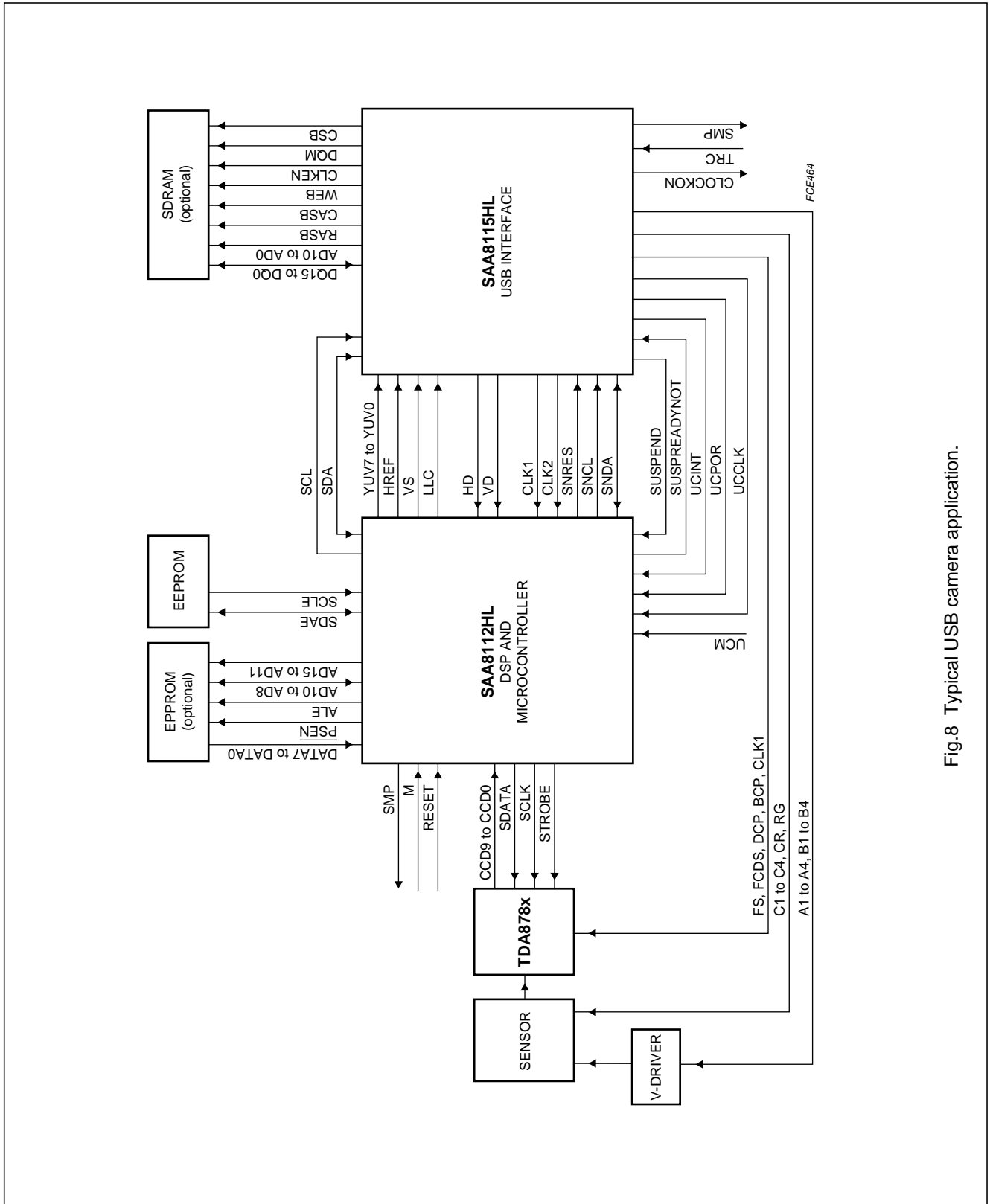


Fig.8 Typical USB camera application.

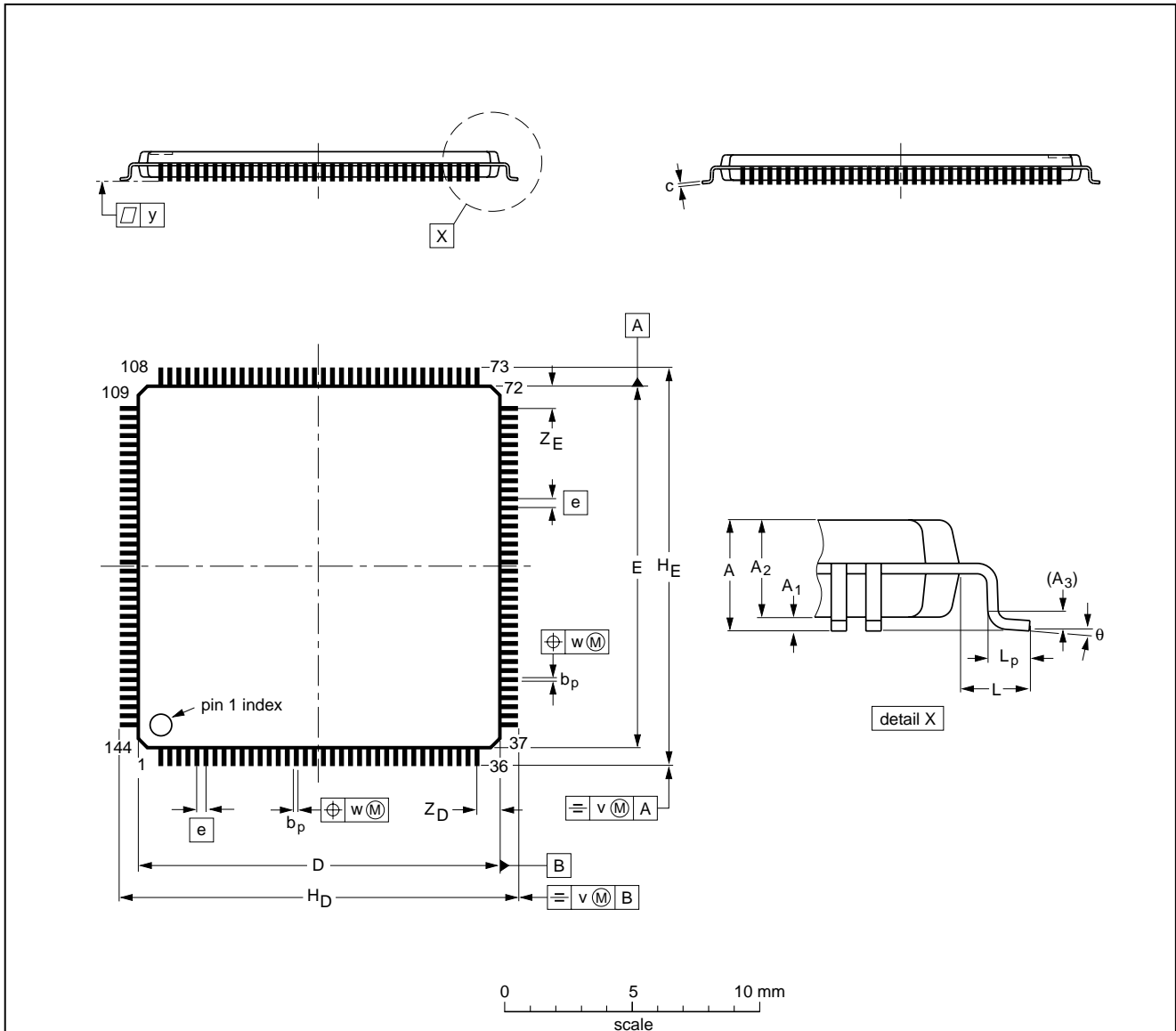
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15 PACKAGE OUTLINE

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm

SOT486-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|----------------|-----|----------------|-----|------|------|-------------------------------|-------------------------------|----------|
| mm | 1.6 | 0.15 0.05 | 1.45 1.35 | 0.25 | 0.27 0.17 | 0.20 0.09 | 20.1 19.9 | 20.1 19.9 | 0.50 | 22.15 21.85 | 22.15 21.85 | 1.0 | 0.75 0.45 | 0.2 | 0.08 | 0.08 | 1.40 1.10 | 1.40 1.10 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT486-1 | 136E23 | MS-026 | | | 99-12-03 00-01-19 |

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16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE | SOLDERING METHOD | |
|---------------------------------|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽¹⁾ |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable ⁽²⁾ | suitable |
| PLCC ⁽³⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽³⁾⁽⁴⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁵⁾ | suitable |

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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17 DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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