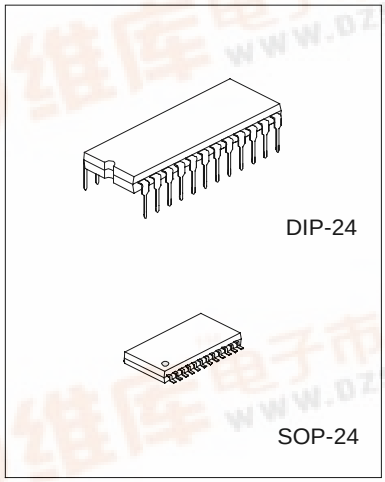
Silan
Semiconductors

SC88E43

EXTENDED VOLTAGE CALLING NUMBER IDENTIFICATION CIRCUIT 2



DESCRIPTION

The SC88E43 Calling Number Identification Circuit 2(ECNIC2) is a low power CMOS integrated circuit intended for receiving physical layer signals transmitted according to BT (British Telecom) SIN227 & SIN242, the U.K.'s CCA (Cable Communications Association) TW/P&E/312 and Bellcore GR-30-CORE & SR-TSV-002476 specifications. The SC88E43 is suitable for applications using a fixed voltage power source between 3 and 5V ±10%.

FEATURES

* Compatible with:
  -- British Telecom (BT) SIN227 & SIN242
  -- U.K.'s Cable Communications Association (CCA) specification TW/P&E/312
  -- Bellcore GR-30-CORE (formerly known as TR-NWT-000030) & SR-TSV-002476
* Bellcore "CPE" Alerting Signal" (CAS) and BT "Idle State Tone Alert Signal" detection
* Ring and line reversal detection
* 1200 baud Bell 202 and CCITT V.23 Frequency Shift Keying (FSK) demodulation
* 3 or 5V ±10% supply voltage
* High input sensitivity (-40dBv Tone and FSK Detection)
* Selectable 3-wire FSK data interface (microcontroller or SC88E43 controlled)
* Low power CMOS with powerdown mode
* Input gain adjustable amplifier
* Carrier detect status output
* Uses 3.58 MHz crystal

APPLICATIONS

* BT Calling Line Identity Presentation (CLIP), CCA CLIP, and Bellcore Calling Identity Delivery (CID) systems
* Feature phones, including Analog Display Services Interface (ADSI) phones
* Phone set adjunct boxes
* FAX and answering machines
* Database query and Computer Telephony Integration (CTI) systems

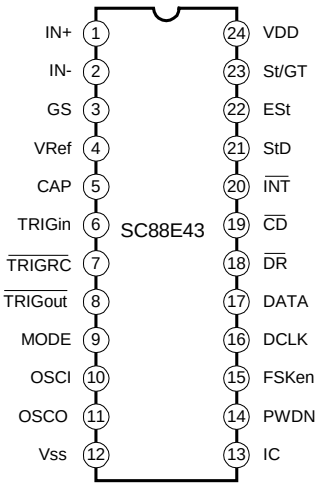
ORDERING INFORMATION

SC88E43	24 Pin DIP
SC88E43S	24 Pin SOIC

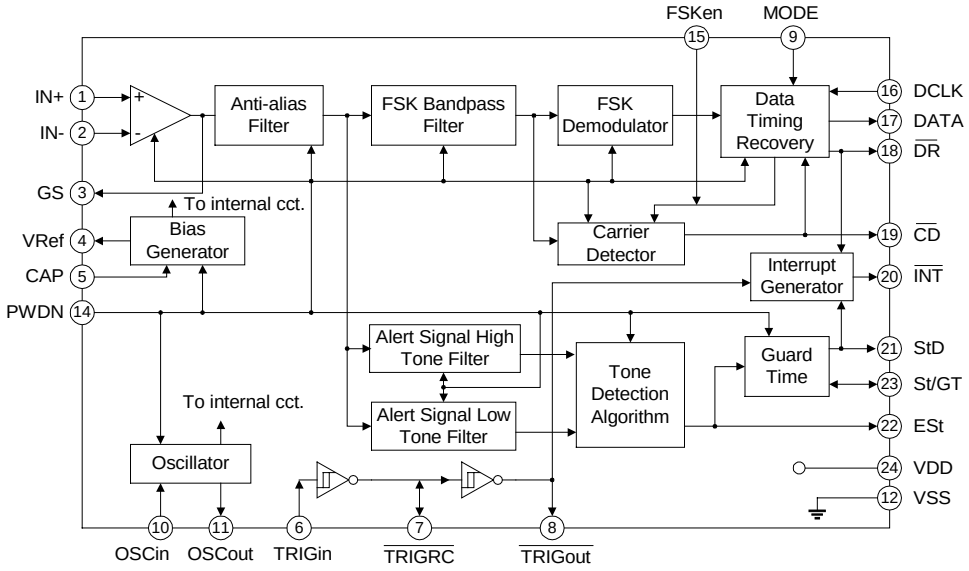
RECOMMENDED OPERATING CONDITIONS (Ta=25°C ; Voltages are with respect to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	V_{DD}	2.7	--	5.5	V
Clock Frequency	f_{OSC}	--	3.579545	--	MHz
Tolerance on Clock Frequency	Δf_C	-0.1	--	+0.1	%
Operating Temperature	T_{OP}	-40	--	85	°C

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages are with respect to VSS, unless otherwise stated).

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 ~ 6.0	V
Voltage on any pin other than supplies*	V_{PIN}	V_{SS}-0.3V ~ V_{DD}+0.3V	V
Current at any pin other than supplies	I_{PIN}	10	mA
Storage Temperature	Tstg	-65 ~ +150	°C

* Under normal operating conditions voltage on any pin except supplies can be minimum V_{SS} -1V to maximum V_{DD} +1V for an input current limited to less than 200mA.

DC ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
Stand-by Supply Current		I_{DDQ}	All input are V_{DD}/V_{SS} except for oscillator pins. No analog input. Outputs unloaded. PWDN = V_{DD}.	--	0.5	15	μA
Operating Supply Current	V_{DD}=5V±10%	I_{DD}	All input are V_{DD}/V_{SS} except for oscillator pins. No analog input. Outputs unloaded. PWDN = V_{SS}; FSKen = V_{DD}.	--	4.7	8	mA
	V_{DD}=3V±10%			--	2.5	4.5	mA
Power Consumption		P_O	--	--	--	44	mW
Schmitt Input High Threshold		V_{T+}	TRIGin, $\overline{TRIGRC}$,PWDN Pins	0.48V_{DD}	--	0.68V_{DD}	V
Schmitt Input Low Threshold		V_{T-}	TRIGin, $\overline{TRIGRC}$,PWDN Pins	0.28V_{DD}	--	0.48V_{DD}	V
Schmitt Hysteresis		V_{HYS}	TRIGin, $\overline{TRIGRC}$,PWDN Pins	0.2	--	--	V
CMOS Input High Voltage		V_{IH}	DCLK,MODE,FSKen Pins	0.7V_{DD}	--	V_{DD}	V
CMOS Input Low Voltage		V_{IL}	DCLK,MODE,FSKen Pins	V_{SS}	--	0.3V_{DD}	V
Output High Sourcing Current		I_{OH}	V_{OH} = 0.9V_{DD} $\overline{TRIGout}$,DCLK,DADA, $\overline{DR}$, $\overline{CD}$,StD,Est,St/GT Pins	0.8	--	--	mA
Output Low Sinking Current		I_{OL}	V_{OL} = 0.1V_{DD} $\overline{TRIGout}$,DCLK,DATA, $\overline{DR}$, $\overline{CD}$, StD, Est,St/GT, $\overline{TRIGRC}$ $\overline{INT}$ Pins	2	--	--	mA
Input Current		I_{IN1}	V_{IN} = V_{DD} to V_{SS} IN+,IN-,TRIGin Pins	--	--	1	μA
		I_{IN2}	V_{IN} = V_{DD} to V_{SS} PWDN,DCLK,MODE,FSKen	--	--	10	μA

(To be continued)

(continued)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Output High-Impedance Current	I_{OZ1}	V_{OUT} = V_{DD} to V_{SS}, $\overline{TRIGRC}$ Pin.	--	--	1	μA
	I_{OZ2}	V_{OUT} = V_{DD} to V_{SS}, $\overline{INT}$ Pin.	--	--	10	μA
	I_{OZ3}	V_{OUT} = V_{DD} to V_{SS}, St/GT Pin.	--	--	5	μA
Output Voltage	V_{REF}	No load. Vref Pin	0.5V_{DD} -0.05	--	0.5V_{DD} +0.05	V
Output Resistance	R_{REF}	Vref Pin		--	2	kΩ
Comparator Threshold Voltage	V_{TGt}	St/GT Pin	0.5V_{DD} - 0.05	--	0.5V_{DD} +0.05	V

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Dual Tone Alert Signal Detection							
Low Tone Frequency	f_L		--	2130	--	Hz	
High Tone Frequency	f_H		--	2750	--	Hz	
Frequency Deviation accept			1.1%	--	--	--	4
Frequency Deviation Reject			3.5%	--	--	--	5
Accept Signal Level Per Tone			-40	--	-2	dBV [a]	3
			-37.78	--	0.22	dBm [b]	
Rejet Signal Level Per Tone			--	--	-46	dBV	3
			--	--	-43.78	dBm	
Positive And Negtive Twist Accept			7	--	--	dB [c]	
Signal to Noise Ratio	SNR_{TONE}		20	--	--	dB	1,2
Timming Parameter Measurement Voltage Levels							
CMOS Threshold Voltage	V_{CT}		--	0.5V_{DD}	--	V	
Rise/Fall Threshold Voltage High	V_{HM}		--	0.7V_{DD}	--	V	
Rise/Fall Threshold Voltage Low	V_{LM}		--	0.3V_{DD}	--	V	
Gain Setting Amplifier							
Input Leakage Current	I_{IN}	$V_{SS} \le V_{IN} \le V_{DD}$	--	--	1	μA	
Input Resistance	R_{IN}	--	10	--	--	MΩ	
Input Offset Voltage	V_{OS}	--	--	--	25	mV	
Power Supply Rejection Ratio	PSRR	1kHz ripple on V_{DD}	40	--	--	dB	

(To be continued)

(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Common Mode Rejection	CMRR	$V_{CMmin} \le V_{IN} \le V_{CMmax}$	40	--	--	dB	
DC Open Loop Voltage Gain	A_{VOL}	--	30	--	--	dB	
Unity Gain Bandwidth	f_C	--	0.3	--	--	MHz	
Output Voltage Swing	V_O	Load ≥ 50kΩ	0.5	--	V_{DD}-0.5	V_{PP}	
Maximum Capacitive Load (GS)	C_L	--	--	--	100	pF	
Maximum Resistive Load (GS)	R_L	--	50	--	--	kΩ	
Common Mode Range Voltage	V_{CM}	--	1.0	--	V_{DD}-0.1	V	
FSK Detection							
Input Detection Level		--	-40	--	-8	dBV [a]	6,8
		--	-37.78	--	-5.78	dBm [b]	
		--	10	--	398.1	mVrms	
Transmission Rate		--	1188	1200	1212	baud	
Input Frequency Detection		Bell 202 1 (Mark)	1188	1200	1212	Hz	
		Bell 202 0 (Space)	2178	2200	2222	Hz	
		CCITT V.23 1 (Mark)	1280.5	1300	1319.5	Hz	
		CCITT V.23 0 (Space)	2068.5	2100	2131.5	Hz	
Signal to Noise Ratio	SNR_{FSK}	--	20	--	--	dB	6,7
Dual Tone Alert Signal Timing							
Alert Signal Present Detect Time	t_{DP}	--	0.5	--	10	ms	9
Alert Signal Absent Detect Time	t_{DA}	--	0.1	--	8	ms	9
3-Wire Interface Timming							
Power-up Time	t_{PU}	PWDN, OSC1 Pins	--	--	50	ms	
Power-down Time	t_{PD}		--	--	1	ms	
Input FSK to $\overline{CD}$ Low Delay	t_{CP}	$\overline{CD}$ Pin	--	--	25	ms	
Input FSK to $\overline{CD}$ High Delay	t_{CA}		8	--	--	ms	
Hysteresis			8	--	--	ms	
3-Wire Interface Timming (Mode 0)							
RiseTime	t_{RR}	$\overline{DR}$ Pin	--	--	200	ns	10
Fall Time	t_{RF}	$\overline{DR}$ Pin	--	--	200	ns	10
Low Time	t_{RL}	$\overline{DR}$ Pin	415	416	417	μs	12
Rate	--	DATA Pin	1188	1200	1212	baud	11
Input FSK to DATA delay	t_{IDD}	DATA Pin	--	1	5	ms	

(To be continued)

(continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Rise time	t_R	DATA, DCLK Pins	--	--	200	ns	10
Fall Time	t_F		--	--	200	ns	10
DATA to DCLK delay	t_{DCD}		6	416	--	µs	11,12, 13
DCLK to DATA delay	t_{CDD}		6	416	--	µs	11,12, 13
Frequency	f_{DCLK0}	DCLK Pin	1201.6	1202.8	1204	Hz	12
High Time	t_{CH}		415	416	417	µs	12
Low Time	t_{CL}		415	416	417	µs	12
DCLK to $\overline{DR}$ delay	t_{CRD}	DCLK , $\overline{DR}$ Pin	415	416	417	µs	12
3-Wire Interface Timming (Mode 1)							
Frequency	f_{DCLK1}	DCLK Pin	--	--	1	MHz	
Duty Cycle			30	--	70	%	
RiseTime	t_{R1}		--	--	20	ns	
Rate	t_{DDS}	DCLK , $\overline{DR}$ Pin	500	--	--	ns	
Input FSK to DATA delay	t_{DDH}		500	--	--	ns	

a. dBV= decibels above or below a reference voltage of 1Vrms. Signal level is per tone.

b. dBm = decibels above or below a reference power of 1mW into 600 ohms. 0dBm = 0.7746Vrms. Signal level is per tone.

c. Twist = 20 log (f_H amplitude / f_L amplitude).

Notes:

1. Both tones have the same amplitude.
2. Band limited random noise 300-3400Hz. Measurement valid only when tone is present.
3. With gain setting as shown in Figure 10. Production tested at V_{DD} =3V±10%, 5V±10%.
4. Range within which tones are accepted.
5. Ranges outside of which tones are rejected.
6. Both mark and space have the same amplitude.
7. Band limited random noise (200-3400Hz). Present when FSK signal is present. Note that the BT band is 300-3400Hz, the Bellcore band is 0-4kHz.
8. Production tested at V_{DD} =5V±10%, 3V±10%.
9. Refer to Figure 16 and 19.
10. into 50pF load.
11. FSK input data at 1200±12 baud.
12. OSCI at 3.579545 MHz±0.1%.
13. Function of signal condition.

PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
1	IN+	Input	Non-inverting Input of the internal opamp.
2	IN-	Input	Inverting Input of the internal opamp.
3	GS	Output	Gain Select of internal opamp. The opamp's gain should be set according to the nominal Vdd of the application using the information in Figure 10.
4	VRef	Output	Reference Voltage. Nominally VDD/2. It is used to bias the input opamp.
5	CAP	--	Capacitor. A 0.1mF decoupling capacitor should be connected across this pin and VSS.
6	TRIGin	Trigger Input	Trigger Input. Schmitt trigger buffer input. Used for line reversal and ring detection.
7	$\overline{\text{TRIGRC}}$	Open Drain Output / Schmitt Input	Trigger RC. Used to set the (RC) time interval from TRIGin going low to $\overline{\text{TRIGout}}$ going high. An external resistor connected to VDD and capacitor connected to VSS determine the duration of the (RC) time interval.
8	$\overline{\text{TRIGout}}$	CMOS Output	Trigger Out. Schmitt trigger buffer output. Used to indicate detection of line reversal and/or ringing.
9	MODE	CMOS Input	3-wire interface: Mode Select. When low, selects FSK data interface mode 0. When high, selects FSK data interface mode 1. See pin 16 (DCLK) description to understand how MODE affects the DCLK pin.
10	OSCI	Input	Oscillator Input. A 3.579545MHz crystal should be connected between this pin and OSCO. It may also be driven directly from an external clock source.
11	OSCO	Output	Oscillator Output. A 3.579545MHz crystal should be connected between this pin and OSCI. When OSCI is driven by an external clock, this pin should be left open.
12	Vss	--	Power Supply Ground.
13	IC	--	Internal Connection. Must be connected to VSS for normal operation.
14	PWDN	Schmitt Input	Power Down. Active high. When high, the device consumes minimal power by disabling all functionality except TRIGin, $\overline{\text{TRIGRC}}$ and. $\overline{\text{TRIGout}}$ Must be pulled low for device operation.

(To be continued)

(continued)

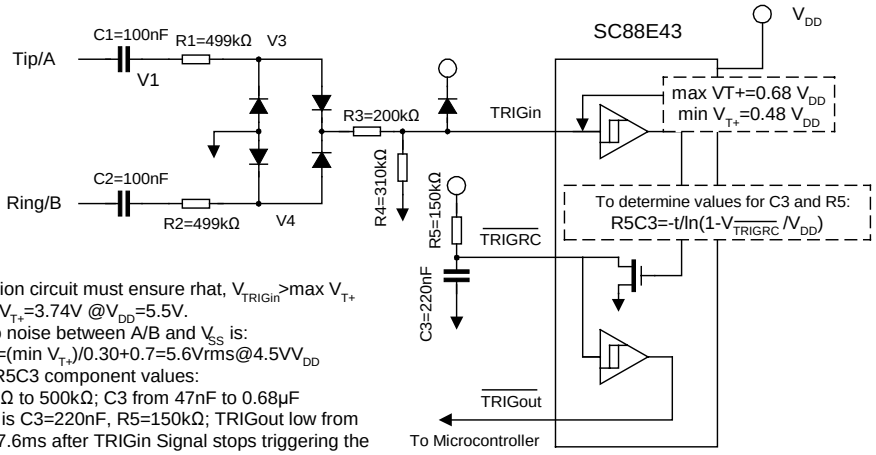
Pin No.	Symbol	I/O	Function
15	FSKen	CMOS Input	FSK Enable. Must be high for FSK demodulation. This pin should be set low to prevent the FSK demodulator from reacting to extraneous signals (such as speech, alert signal and DTMF which are all in the same frequency band as FSK).
16	DCLK	CMOS Input/Output	3-wire Interface: Data Clock. In mode 0 (MODE pin low), this pin is an output. In mode 1 (MODE pin high), this pin is an input.
17	DATA	CMOS Output	3-wire Interface: Data. In mode 0 the FSK data appears at the pin once demodulated. In mode 1 the FSK data is shifted out on the rising edge of the microcontroller supplied DCLK.
18	$\overline{DR}$	CMOS Output	3-wire Interface: Data Ready. Active low. In mode 0 this output goes low after the last DCLK pulse of each data word. This identifies the 8-bit word boundary on the serial output stream. Typically, $\overline{DR}$ is used to latch 8-bit words from a serial-to-parallel converter into a microcontroller. In mode 1 this pin will signal the availability of data.
19	$\overline{CD}$	CMOS Output	Carrier Detect. Active low. A logic low indicates the presence of in-band signal at the output of the FSK bandpass filter.
20	$\overline{INT}$	Open Drain Output	Interrupt. Active low. It is active when $\overline{TRIGout}$ or $\overline{DR}$ is low, or StD is high. This output stays low until all three signals have become inactive.
21	StD	CMOS Output	Dual Tone Alert Signal Delayed Steering Output. When high, it indicates that a guard time qualified alert signal has been detected.
22	ESt	CMOS Output	Dual Tone Alert Signal Early Steering Output. Alert signal detection output. Used in conjunction with St/GT and external circuitry to implement the detect and non-detect guard times.
23	St/GT	Analog Input / CMOS Output	Dual Tone Alert Signal Steering Input/Guard Time. A voltage greater than V_{TGt} (see figure 4) at the St/GT pin causes the device to indicate that a dual tone has been detected by asserting StD high. A voltage less than V_{TGt} frees the device to accept a new dual tone.
24	V_{DD}	--	Positive Power Supply.

FUNCTIONAL DESCRIPTION

Detection of CLIP/CID Call Arrival Indicators

The cricuit in Figure 3 illustrates the relationship between the $\overline{\text{TRIGRC}}$ and $\overline{\text{TRIGout}}$ sig nals.Tpically,the three pin combination is used to detect an event indicated by an increase of the TRIGin voltage from V_{SS} to above the Schmitt trigger high going threshold V_{T+} (see DC electrical characteristics).

Figure 3 shows a circuit to detect any one of three CLIP/CID call arrival indicators:line reversal,ring burst and ringing.



Notes:
The application circuit must ensure rhat, V_{TRIGin}>max V_{T+}
Where max V_{T+}=3.74V @V_{DD}=5.5V.
Tolerance to noise between A/B and V_{SS} is:
max Vnoise=(min V_{T+})/0.30+0.7=5.6Vrms@4.5VV_{DD}
Suggested R5C3 component values:
R5 from 10kΩ to 500kΩ; C3 from 47nF to 0.68μF
An example is C3=220nF, R5=150kΩ; TRIGout low from 21.6ms to 37.6ms after TRIGin Signal stops triggering the circuit.

Figure 3 Circuit to Detect Line Reversal, Ring Burst and Ringing

1.Line Reversal Detection

Line reversal,or polarity reversal on the A and B wires indicates the arrival of an inconming CDScall,as soecified in SIN227.When the event (line reversal) occurs,TRIGin rises past the high going Schmitt threshold V_{T+} and $\overline{\text{TRIGout}}$,which is normally high,is pulled low going Schmitt threshold V_{T-} and $\overline{\text{TRIGout}}$ returns high.The components R5 and C3 (see Figure 3) at $\overline{\text{TRIGout}}$ low interval.

In a TE designed for CLIP,the $\overline{\text{TRIGout}}$ high to low transition may be used to interrupt or wake-up the micro-controller.The controller can thus be put into power-down mode to conserve power in a battery operater TE.

2.Ring Buost Detection

CCA doesnot support the dual tone alert signal (refer to Dual Tone Alert single burst og ringing (duration 200-450ms) that precedes CLIPFSK data.The ring burst may vary fron 30 to 75Vrms and is approximately 25Hz.

Again in aTEdesigned for CCA CLIP ,the $\overline{\text{TRIGout}}$ high to low reansition may be used to interrupt or wake-up the microcontroller.The controller can thus be put into power-down mode to conserve powerin a battery operated TE.

3.Ring Detection

In Bellcore's CND/CNAM scheme, the CID FSK data is transmitted between the first and second ringing cycles. The circuit in Figure 3 will generate a ring envelope signal (active low) at $\overline{\text{TRIGout}}$ for a ring voltage of at least 40Vrms. R5 and C3 filter the ring signal to provide an envelope output.

The diode bridge shown in Figure 3 works for both single ended and balanced ringing. A fraction of the ring voltage is applied to the TRIGin input. When the voltage at TRIGin is above the Schmitt trigger high going threshold V_{T+}, $\overline{\text{TRIGRC}}$ is pulled low as C3 discharges. $\overline{\text{TRIGout}}$ stays low as long as the C3 voltage stays below the minimum V_{T+}.

In a CPE designed for CND/CNAM, the $\overline{\text{TRIGout}}$ high to low transition may be used to interrupt or wake up the microcontroller. The controller can thus be put into power down mode to conserve power.

If precise ring duration determination is critical, capacitor C3 in Figure 3 may be removed. The microcontroller will now be able to time the ring duration directly. The result will be that $\overline{\text{TRIGout}}$ will be low only as long as the ringing signal is present.Previously the RC time constant would cause only one interrupt.

Dual Tone Alert Signal Detection

The BT on hook (idle state) caller ID scheme uses a dual tone alert signal whose characteristics are shown in Table 1.

Bellcore specifications for a similar dual tone signal called CPE Alerting Signal (CAS) for use in off-hook data transmission. For the CIDCW service, the CAS must be detected in the presence of near end speech. The CAS detector must also be immune to imitation from near and farend speech.

Item	BT	Bellcore
Low tone frequency	2130Hz ± 1.1%	2130Hz ± 0.5%
High tone frequency	2750Hz ± 1.1%	2750Hz ± 0.5%
Received signal level	-2dBV to –40dBV per tone on-hook [a] (0.22dBm [b] to –37.78dBm)	-14dBm [b] to –32dBm per tone on-hook
Signal reject level	-46dBV (-43.78dBm)	-45dBm
Signal level differntial (twist)	Up to 7dB	Up to 6dB
Unwanted signals	≤-20dB(300-3400Hz)	≤–7dBm ASL [c] near end speech
Duration	88ms to 110ms [d]	75ms to 85ms
Speech present	No	Yes

Table 1 Dual Tone Alert Signal Characteristics

a. In the future BT may specify the off-hook signal level as –15dBm to –34dBm per tone for BT CIDcw.
b. The signal power is expressed in dBm referenced to 600 ohm at the CPE A/B (tip/ring) interface.
c. ASL = active speech level expressed in dBm referenced to 600 ohm at the CPE tip/ring interface. The level is measured according to method B of Recommendation P.56 "Objective Measurement of Active Speech Level" published in the CCITT Blue Book, volume V "Telephone Transmission Quality" 1989. EPL (Equivalent Peak Level) = ASL+11.7dB.
d. SIN227 suggests that the recognition time should be not less than 20ms if both tones are detected.

In the SC88E43 the dual tone signal is separated into a high and a low tone by two bandpass filters. A detection algorithm examines the two filter outputs to determine the presence of a dual tone alert signal. The ESt pin goes high when both tones are present. Note that ESt is only a preliminary indication. The indication must be sustained over the tone present guard time to be considered valid. Tone present and tone absent guard times can be implemented with external RC components. The tone present guard time rejects signals of insufficient duration. The tone absent guard time masks momentary detection dropout once the tone present guard time has been satisfied. StD is the guard time qualified detector output.

Dual Tone Detection Guard Time

When the dual tone signal is detected by the SC88E43, ESt goes high. When the signal ceases to be detected, ESt goes low.

The ESt pin indicates raw detection of the dual tone signal. Since the BT application requires a minimum signal duration and the Bellcore application requires protection from imitation by speech, Est detection must be guard time qualified. The StD pin provides guard time qualified signal detection. When the SC88E43 is used in a caller identity system, StD indicates correct CAS/Tone Alert Signal detection.

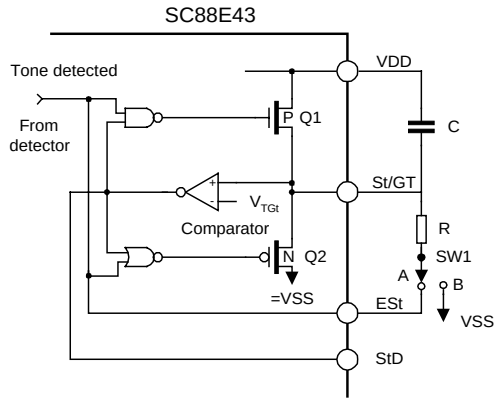


Figure 4 : Guard Time Circuit Operation

Figure 4 shows the relationship between the St/GT, ESt and StD pins. It also shows the operation of the guard time circuit.

The total recognition time is $t_{REC} = t_{GP} + t_{DP}$, where t_{GP} is the tone present guard time and t_{DP} is the tone present detect time (refer to timing between ESt, St/GT and StD in Figures 17 and 20).

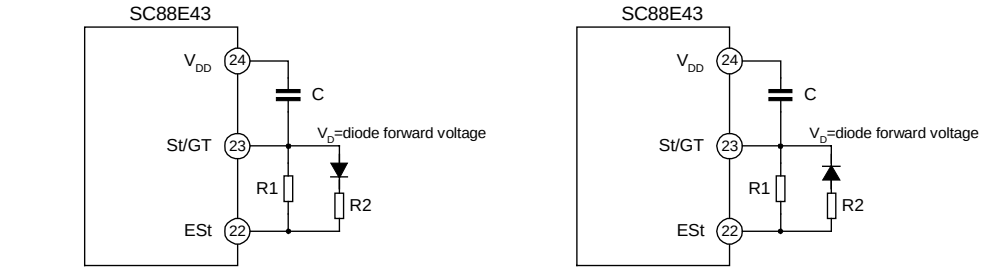
The total tone absent time is $t_{ABS} = t_{GA} + t_{DA}$, where t_{GA} is the tone absent guard time and t_{DA} is the tone absent detect time (refer to timing between ESt, St/GT and StD in Figures 17 and 20).

Bellcore states that it is desirable to be able to turn off CAS detection for an off-hook capable CPE. The disable switch allows the subscriber who disconnects a service that relies on CAS detection (e.g., CIDCW) but retains the CPE, to turn off the detector and not be bothered by false detection.

When SW1 in Figure 4 is in the B position the guard time circuit is disabled. The detector will still process CAS/Alerting tones but the SC88E43 will not signal their presence by ensuring that StD is low.

BT specifies that the idle state tone alert signal recognition time should not be less than 20ms when both tones are used for detection. That is, both tones must be detected together for at least 20ms before the signal can be declared valid. This requirement can be met by setting the t_{GP} (refer to Figure 5) to at least 20ms.

BT also specifies that the TE is required to apply a DC wetting pulse and an AC load 15-25ms after the end of the alerting signal. If tABS =tDA +tGA is 15 to 25ms, the DC current wetting pulse and the AC load can both be applied at the falling edge of StD. The maximum tDA is 8ms so tGA should be 15-17ms. Therefore, tGP must be greater than tGA . Figure 5(a) shows a possible implementation. The values in Figures 9 and 11 (R2=R3=422K, C=0.1mF) will meet the BT timing requirements.



(a) $t_{GP} > t_{GA}$
$t_{GP}=R1Cln[V_{DD}/(V_{DD}-V_{TG})]$
$t_{GA}=RpCln[(V_{DD}-V_D(Rp/R2))/(V_{TGt}-V_D(Rp/R2))]$
$Rp=R1R2/(R1+R2)$

(b) $t_{GP} < t_{GA}$
$t_{GP}=RpCln[(V_{DD}-V_D(Rp/R2))/(V_{DD}-V_{TGt}-V_D(Rp/R2))]$
$t_{GA}=R1Cln[V_{DD}/V_{TG})]$
$Rp=R1R2/(R1+R2)$

Figure 5 Guard Time Circuits With Unequal Times

Input Configuration

The SC88E43 provides an input arrangement comprised of an operational amplifier, and a bias source (Vref) which is used to bias the opamp inputs at VDD/2. The feedback resistor at the opamp output (GS) can be used to adjust the gain. In a single-ended configuration, the opamp is connected as shown in Figure 6. For a differential input configuration, Figure 7 shows the necessary connections.

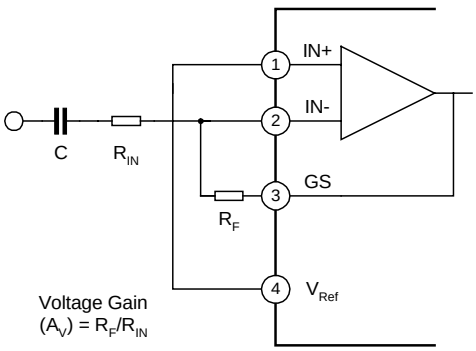
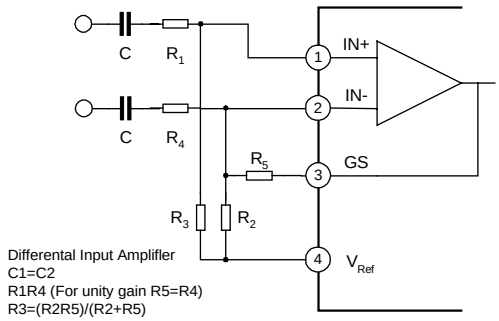


Figure 6 Single Ended Input Configuration



Differental Input Amplifler
C1=C2
R1R4 (For unity gain R5=R4)
R3=(R2R5)/(R2+R5)
Voltage Gain
(AVdiff)=R5/R1 (see Figure 9,10,11)
Input Impedance
$(ZINdiff)=2R1^2+(1/C)^2$

Figure 7 Differential Input Configuration

FSK Demodulation

The SC88E43 first bandpass filters and then demodulates the FSK signal. The carrier detector provides an indication of the presence of signal at the bandpass filter output. The SC88E43's dual mode 3-wire interface allows convenient extraction of the 8-bit data words in the demodulated FSK bit stream.

Note that signals such as CAS/Tone Alert Signal, speech and DTMF tones lie in the same frequency band as FSK. They will, therefore, be demodulated and as a result, false data will be generated. To avoid demodulation of false data, an FSKen pin is provided so that the FSK demodulator may be disabled when FSK signal is not expected. There are two events that if either is true, should be used to disable FSKen. The events are $\overline{CD}$ returning high or receiving all the data indicated by the message length word.

Item	BT	Bellcore
Mark frequency (logic 1)	1300Hz ± 1.5%	1200Hz ± 1%
Space frequency (logic 0)	2100Hz ± 1.5%	2200Hz ± 1%
Received signal level-mark	-8dBV to –40dBV (-5.78dBm to –37.78dBm)	-12dBm [a] to –32dBm
Received signal level-space	-8dBV to –40dBV	-12dBm to –36dBm
Signal level differntial (twist)	Up to 6dB	Up to 10dB [b]
Unwanted signals	≤-20dB (300-3400Hz)	≤–25dBm (0-4kHz) [c]
Transmission rate	1200baud ± 1%	1200baud ± 1%
Word formate	1 start bit (logic 0), 8 bit word (LNB first), 1 to 10 stop bits (logic 1)	1 start bit (logic 0), 8 bit word (LNB first), 1 stop bits (logic 1)

Table 2 FSK Charateristics

a.The signal power is expressed in aBm referenced to 600Ω at the CPE tip/ring (A/B) interface.

b.SR-3004, Issue 2, January 1995.

c.The frequency range is specified in GR-30-CORE.

d.Up to 20 marks may be inserted in specific places in a single or multiple data message.

The FSK characteristics described in Table 2 shows the BT and Bellcore specifications. The BT frequencies correspond to CCITT v.23. The Bellcore frequencies correspond to Bell 202. The U.K.'s CCA requires that the TE be able to receive both CCITT v.23 and Bell 202 formats. The SC88E43 is compatible with both formats without any adjustment.

3-wire FSK Data Interface

The SC88E43 provides a powerful dual mode 3-wire interface so that the 8-bit data words in the demodulated FSK bit stream can be extracted without the need either for an external UART or for the TE/CPE's microcontroller to perform the UART function in software. The interface is specifically designed for the 1200 baud rate and is comprised of the DATA, DCLK (data clock) and $\overline{DR}$ (data ready) pins. Two modes (modes 0 and 1) are selectable via control of the device's MODE pin: in mode 0, data transfer is initiated by the SC88E43; in mode 1, data transfer is initiated by the external microcontroller.

Mode 0

This mode is selected when the MODE pin is low.

In this mode, The SC88E43 receives the FSK signal, demodulates it, and outputs the data directly to the DATA pin (refer to Figure 14). For each received stop and start bit sequence, the SC88E43 outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each clock rising edge occurs in the centre of each DATA bit cell. DCLK is not generated for the stop and start bits. Consequently, DCLK will clock only valid data into a peripheral device such as a serial to parallel shift register or a micro-controller. The SC88E43 also outputs an end of word pulse (data ready) on the $\overline{DR}$ pin. The data ready signal indicates the reception of every 10-bit word (including start and stop bits) sent from the network to the TE/CPE. This $\overline{DR}$ signal can be used to interrupt a micro-controller. $\overline{DR}$ can also cause a serial to parallel converter to parallel load its data into a microcontroller. The mode 0 data pin can also be connected to a personal computer's serial communication port after converting from CMOS to RS-232 voltage levels.

Mode 1

This mode is selected when the MODE pin is high. In this mode, the microcontroller supplies read pulses (DCLK) to shift the 8-bit data words out of the SC88E43, onto the DATA pin. The SC88E43 asserts $\overline{DR}$ to denote the word boundary and indicate to the microprocessor that a new word has become available (refer to Figure 16).

Internal to the SC88E43, the demodulated data bits are sampled and stored. After the 8th bit, the word is parallel loaded into an 8 bit shift register and $\overline{DR}$ goes low. The shift register's contents are shifted out to the DATA pin on the supplied DCLK's rising edge in the order they were received.

If DCLK begins while $\overline{DR}$ is low, $\overline{DR}$ will return to high upon the first DCLK. This feature allows the associated interrupt (see section on "Interrupt") to be cleared by the first read pulse. Otherwise DR is low for half a nominal bit time (1/2400 sec).

After the last bit has been read, additional DCLKs are ignored.

Carrier Detector

The carrier detector provides an indication of the presence of a signal in the FSK frequency band. It detects the presence of a signal of sufficient amplitude at the output of the FSK bandpass filter. The signal is qualified by a digital algorithm before the $\overline{CD}$ output is set low to indicate carrier detection. An 8ms hysteresis is provided to allow for momentary signal drop out once $\overline{CD}$ has been activated. $\overline{CD}$ is released when there is no activity at the FSK bandpass filter output for 8 ms.

When $\overline{CD}$ is inactive (high), the raw output of the demodulator is ignored by the data timing recovery circuit (refer to Figure 1). In mode 0, the DATA pin is forced high. No DCLK or $\overline{DR}$ signal is generated. In mode 1, the internal shift register is not updated. No $\overline{DR}$ is generated. If the mode 1 DCLK is clocked, DATA is undefined.

Note that signals such as CAS/Tone Alert Signal, speech and DTMF tones also lie in the FSK frequency band and the carrier detector may be activated by these signals. The signals will be demodulated and presented as data. To avoid false data detection, the FSKen pin should be used to disable the FSK demodulator when no FSK signal is expected.

Ringing, on the other hand, does not pose a problem as it is ignored by the carrier detector.

Interrupt

To facilitate interfacing with microcontrollers running interrupt driven firmware, an open drain interrupt output $\overline{INT}$ is provided. $\overline{INT}$ is asserted when $\overline{TRIGout}$ is low, StD is high, or $\overline{DR}$ is low. When $\overline{INT}$ is asserted, these signals should be read (into an input port of the microcontroller) to determine the cause of the interrupt ($\overline{TRIGout}$, StD or $\overline{DR}$) so that the appropriate response can be made.

When system power is first applied, $\overline{TRIGout}$ will be low because capacitor C3 at $\overline{TRIGRC}$ (see Figure 3) has no initial charge. This will result in an interrupt upon power up. Also when system power is first applied and the PWDN pin is low, an interrupt will occur due to StD. Since there is no charge across the capacitor at the St/GT pin in Figure 4, StD will be high triggering an interrupt. The interrupts will not clear until both capacitors are charged. The microcontroller should ignore interrupt from these msources on initial power up until there is sufficient time to charge the capacitors.

It is possible to clear StD and its interrupt by asserting PWDN immediately after system power up. When PWDN is high, StD is low. PWDN will also force both ESt and the comparator output low, Q2 will turn on so that the capacitor at the St/GT pin charges up quickly (refer to Figure 4).

Power Down Mode

For applications requiring reduced power consumption, the SC88E43 can be powered up only when it is required, that is, upon detection of one of three CLIP/CID call arrival indicators: line reversal, ring burst and ringing.

The SC88E43 is powered down by setting the PWDN pin to logic high. In power down mode, the oscillator, input opamp and all internal circuitry are disabled except for TRIGin, $\overline{TRIGRC}$ and $\overline{TRIGout}$ pins. These three pins are not affected by power down, such that, the SC88E43 can still react to call arrival indicators. The SC88E43 can be powered up by setting the PWDN pin to logic low.

Crystal Oscillator

The SC88E43 requires a 3.579545MHz crystal oscillator as the master timing source.

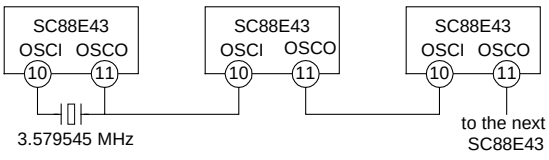


Figure 8 Common Crystal Connection

The crystal specification is as follows :

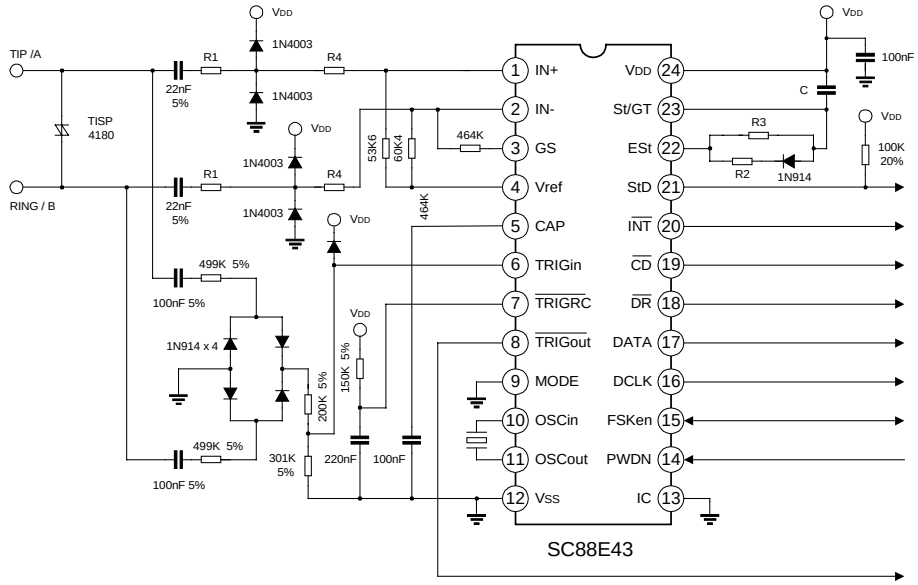
Frequency:	3.579545 MHz
Frequency tolerance:	±0.1%(-40 o C+85 o C)
Resonance mode:	Parallel
Load capacitance:	18 pF
Maximum series resistance:	150 ohms
Maximum drive level (mW):	2 mW

Any number of SC88E43 devices can be connected as shown in Figure 8 such that only one crystal is required. The connection between OSC2 and OSC1 can be DC coupled as shown, or the OSC1 input on all devices can be driven from a CMOS buffer (dc coupled) with the OSC2 outputs left unconnected.

To meet BT and Bellcore requirements for proper tone detection the crystal must have a frequency tolerance of 0.1%.

VRef and CAP Inputs

VRef is the output of a low impedance voltage source equal to VDD/2 and is used to bias the input opamp. A 0.1mF capacitor is required between CAP and VSS to eliminate noise on VRef.



Note:Resistors must have 1% tolerance and capacitors have 20% tolerance unless otherwise specified.

Crystal is 3.579545MHz, 0.1% frequency tolerance.

For BT Application C=0.1μF±5%, R3=422kΩ±1%, R2=422kΩ±1%.

For Applications where CAS speech immunity is required(e.g.CIDCW), C=0.1μF±5%, R3=825kΩ±1%, R2=226kΩ±1%.

R1=430k, R4=34k for VDD=5V±10% (See Figure 10)

R1=620k, R4=63k4 for VDD=3V±10% (See Figure 10)

Figure 9- Application Circuit

Application Circuits

The circuits shown in Figures 9 and 11 are application circuits for the SC88E43. As supply voltage (VDD) is decreased, the threshold of the device's tone and FSK detectors will be reduced. Therefore, to meet the BT or Bellcore tone reject level requirements the gain of the input opamp should be reduced according to the graph in

Figure 10. For example when VDD =5V (+/- 10%), R 1 should equal 430kW and R4 should equal 34kW; and if VDD =3V (+/- 10%) R1 should equal 620kW and R 4 should equal 63.4kW. Resistors R1 and R4 are shown in Figures 9 and 11.

The circuit shown in Figure 9 illustrates the use of the SC88E43 in a proprietary system that doesn't need to meet FCC, DOC, and UL approvals. It should be noted that if glitches on the Tip/Ring interface are of sufficient amplitude, the circuit will falsely detect these signals as ringing or line reversal.

The circuit shown in Figure 11 will provide common mode rejection of signals received by the ringing circuit. This circuit should pass safety related tests specified by FCC Part 68, DOC CS-03, UL 1459, and CSA C22.2. These safety tests will simulate high voltage faults that may occur on the line. The circuit provides isolation from these high voltage faults via R1 and the 12.1kW resistors as well as the 22nF & 330nF capacitors. IRC manufactures a resistor (part number GS3) that should be used for R1. This resistor is a 3W, 5%, 1kV power resistor. The 12k1 resistor is manufactured by IRC (part number FA8425F). This resistor is a 1.5W, 5%, fuseable type resistor. The 22nF and 330nF capacitors have a 400V rating.

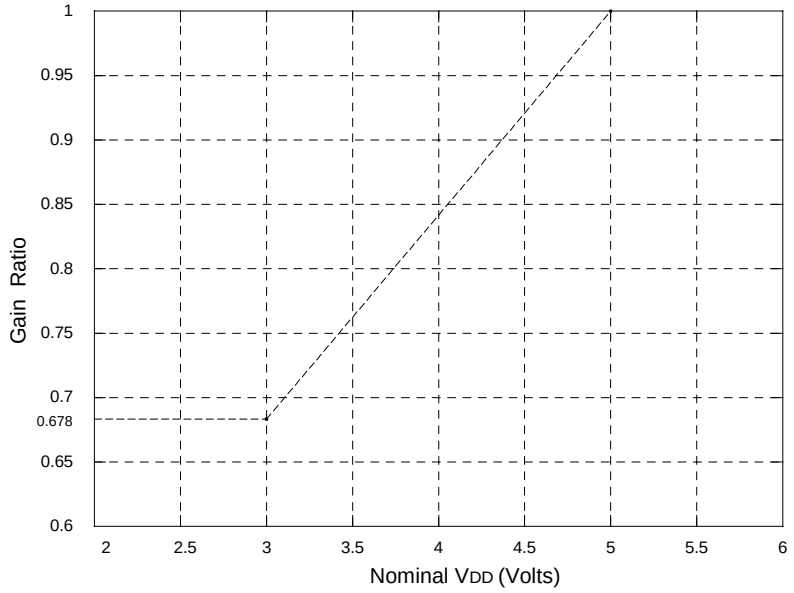
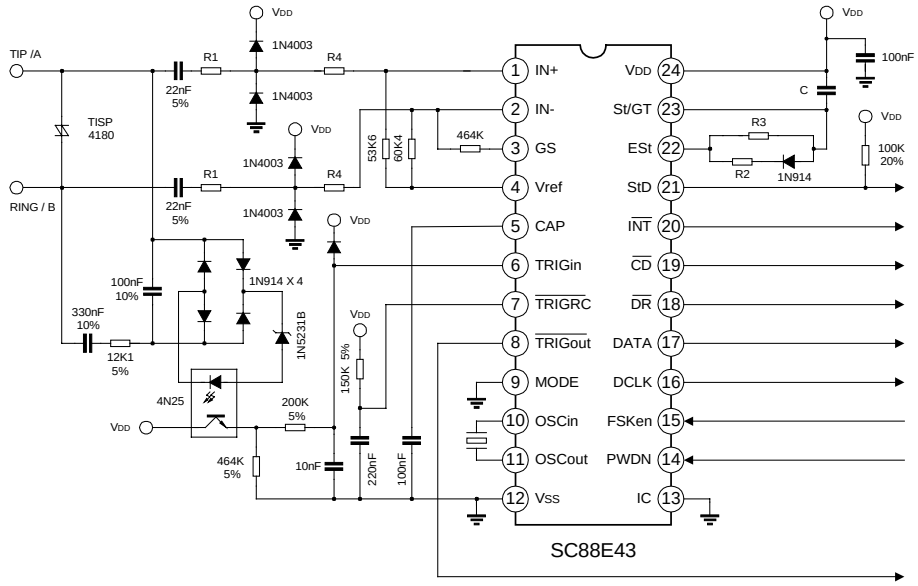


Figure 10: Gain Ratio as a function of Nominal VDD

Note: In the application circuits shown in Figure9 and 11, the Gain ratio of SC88E43 opamp is:

Gain Ratio=464kΩ/(R1+R4)



Note: Please use 0.068μF, 1500pF Mylar Capacitors.

Note:Resistors must have 1% tolerance and capacitors have 20% tolerance unless otherwise specified.

Crystal is 3.579545MHz, 0.1% frequency tolerance.

For BT Application C=0.1μF±5%, R3=422kΩ±1%, R2=422kΩ±1%.

For Applications where CAS speech immunity is required(e.g.CIDCW), C=0.1μF±5%, R3=825kΩ±1%, R2=226kΩ±1%.

R1=430k, R4=34k for VDD=5V±10% (See Figure 10)

R1=620k, R4=63k4 for VDD=3V±10% (See Figure 10)

Figure 11:Application Circuit with Improved Common Mode Noise Immunity and Isolation in Line Interface

Approvals

Fcc Part 68,DOC CS-03,UL1459,and CAN/CSA-22.2 No.225-M90 are all system(i.e. connectors,power supply,cabinet,ect.) requirements. Since the SC88E43 is a component and not a system, the application circuit (Figure 11) has been designed to meet the CO Trunk interface requirments of FCC,DOC,UL, and CSA; thus enabling the complete system to be approved by these standards bodies.

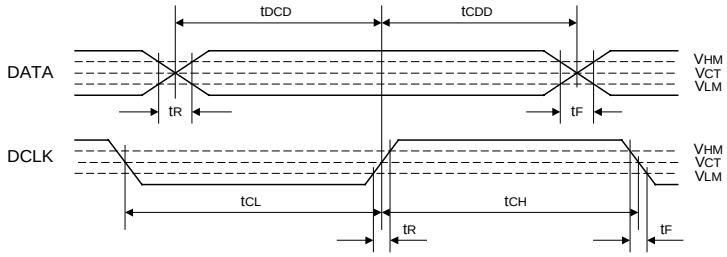


Figure 12: DATA and DCLK Mode 0 Output Timing

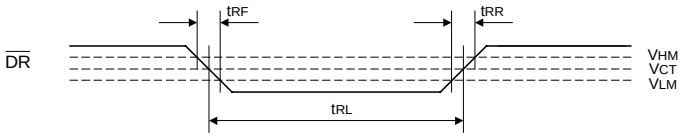


Figure 13: DR Output Timing

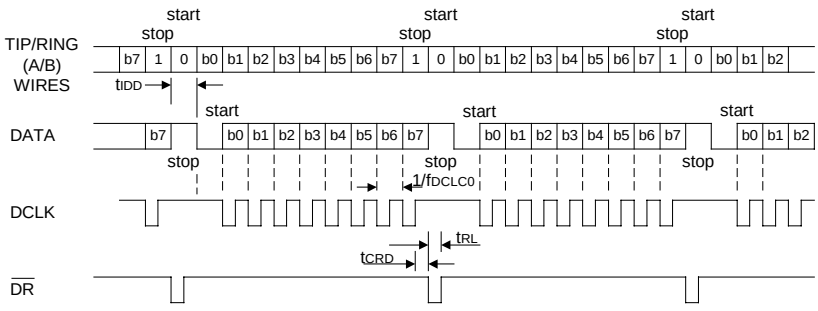


Figure 14: Serial Data Interface Timing (MODE 0)

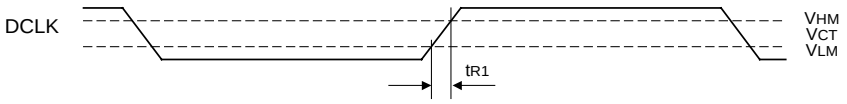
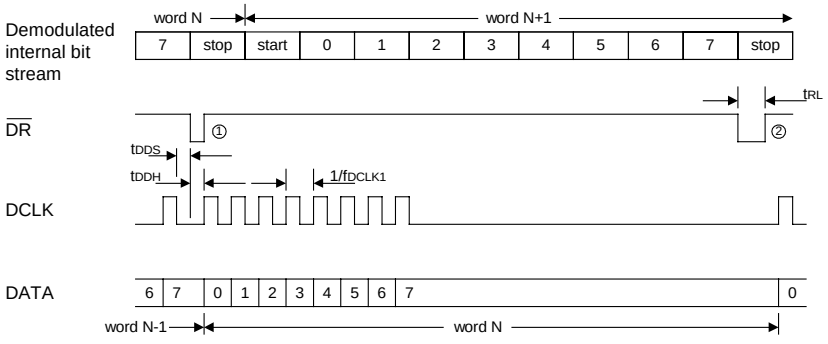


Figure 15: DCLK Mode 1 Input Timing



① DCLK clears $\overline{DR}$

② DCLK does not clear $\overline{DR}$, so $\overline{DR}$ is low for maximum time (1/2 bit width)

Figure 16: Serial Data Interface Timing (MODE 1)

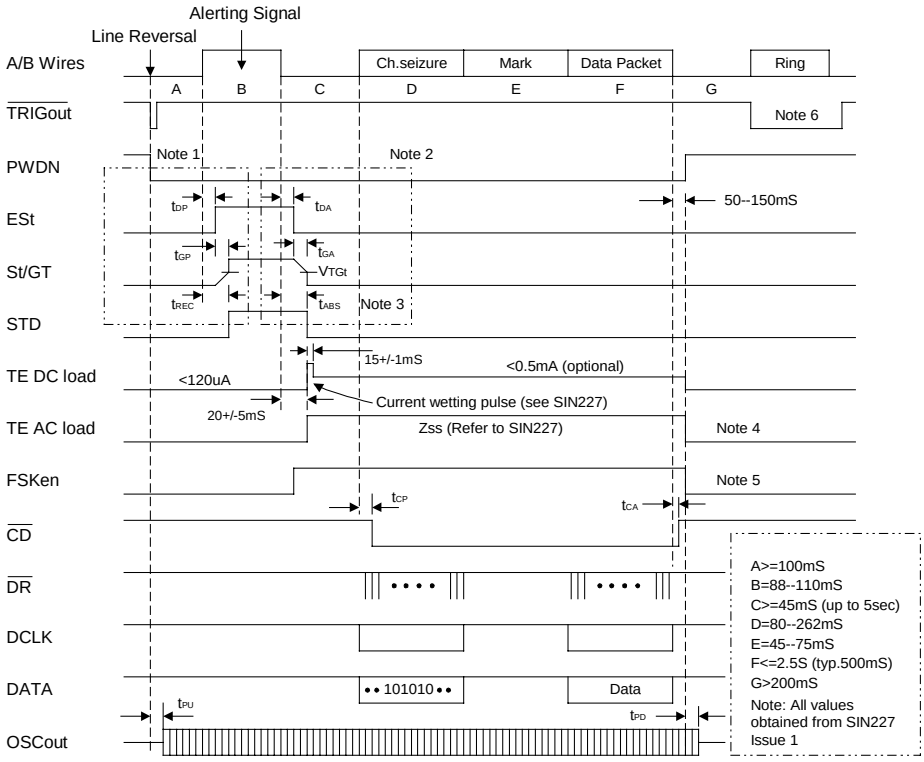


Figure 17: Input and Output Timing for BT Caller Display Service(CDS), e.g.,CLIP

Note:

1) The total recognition time is $t_{REC}=t_{GP}+t_{DR}$,where T_{GP} is the tone present guard time and t_{DP} is the tone present detect time (refer to section “Dual Tone Detection Time” on page 11 for details). V_{TGt} is the comparator threshold (refer to Figure 4).
2) The total tone absent time is $t_{ABS}=t_{GA}+t_{DA}$, where tGA is the tone absent guard time and t_{DA} is the tone absent detect time (refer to section ” Dual Tone Detection Time” on page 11 for details). V_{TGt} is the comparator threshold (refer to Figure 4).
3) By choosing t_{GA}=15mS, t_{ABS} will be 15—25 mS so that the current wetting pulse and AC load can be applied right after the StD falling edge.
4) SIN227 spedifies that the AC and DC loads should be removed between 50—150 mS after the end of the FSK signal, indicated by $\overline{CD}$ returning to high. The SC88E43 may also be powered down at this time.
5) FSKen should be set low when FSK is not expected to prevent the FSK demodulator from reacting to other in-band signals such as speech, tone alert signal and DTMF tones.
6) $\overline{TRIGout}$ is the ring envelope during ringing.

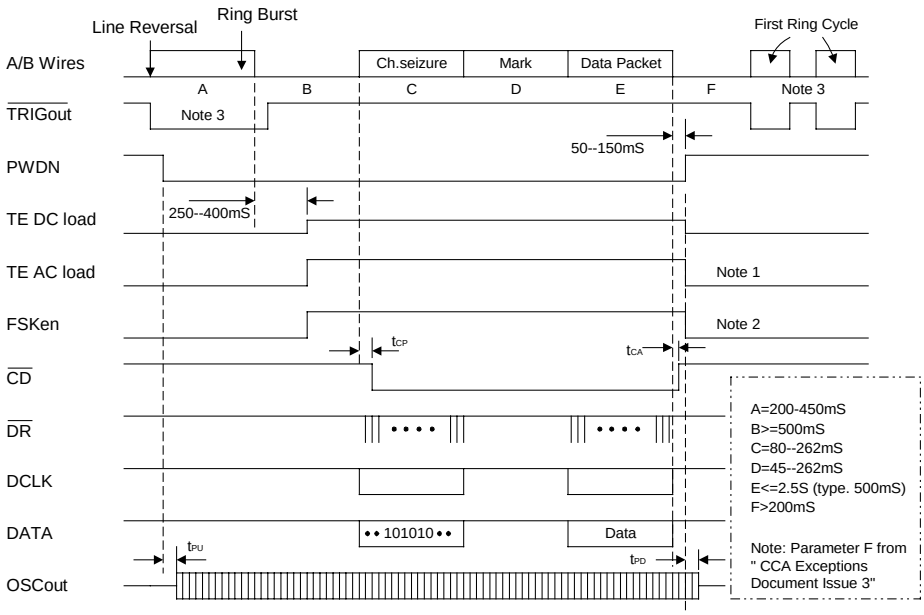


Figure 18: Input and Output Timing for CCA Caller Display Service(CDS), e.g.,CLIP

Note:

1. TW/P&E/312 specifies that the AC and DC loads should be removed between 50 to 150 mS after the end of the FSK signal, indicated by The $\overline{CD}$ returning to high. The SC88E43 may also be powered down at this time.
2. FSKen should be set low when FSK is not expected to prevent the FSK demodulator from reacting to other in-band signals such as speech,and DTMF tones.
3. $\overline{TRIGout}$ represents the ring envelop during ringing.

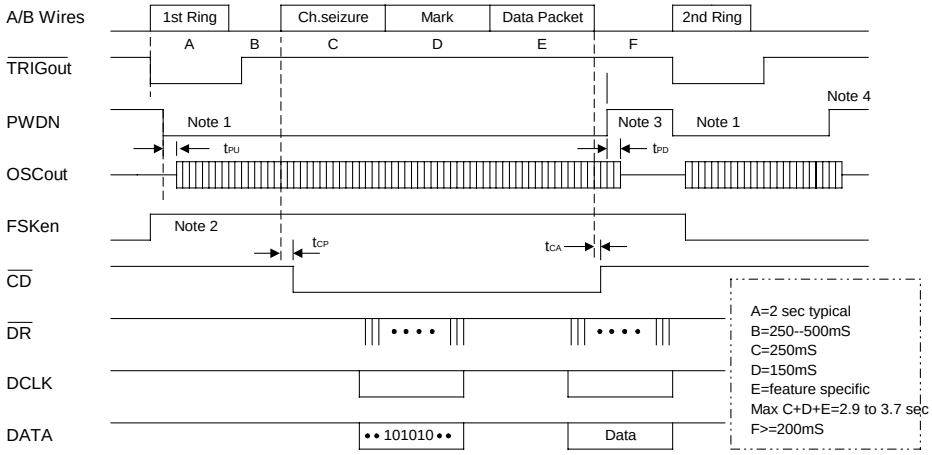


Figure 19: Input and Output Timing for Bellcore On-hook Data Transmission Associated with Ringing,e.g.,CID

Note:

This on-hook case application is included because a CIDCW (off-hook) CPE should also be capable of receiving on-hook data transmission (with ringring) from the end office. TR-NWT-000575 specifies that CIDCW will be offered only to lines which subscribe to CID

1. The CPE designer may choose to enable the SC88E43 only after the end of ringing to conserve power in a battery operated CPE. $\overline{CD}$ is not activated by ringing.
2. The CPE designer may choose to set FSKen always high while the CPE is on-hook. Setting FSKen low prevents the FSK demodulator from reacting to other in-band signals such as speech,CAS or DTMF tones.
3. The microcontroller in the CPE powers down the SC88E43 after $\overline{CD}$ has become inactive.
4. The microcontroller times out if $\overline{CD}$ is not activated.

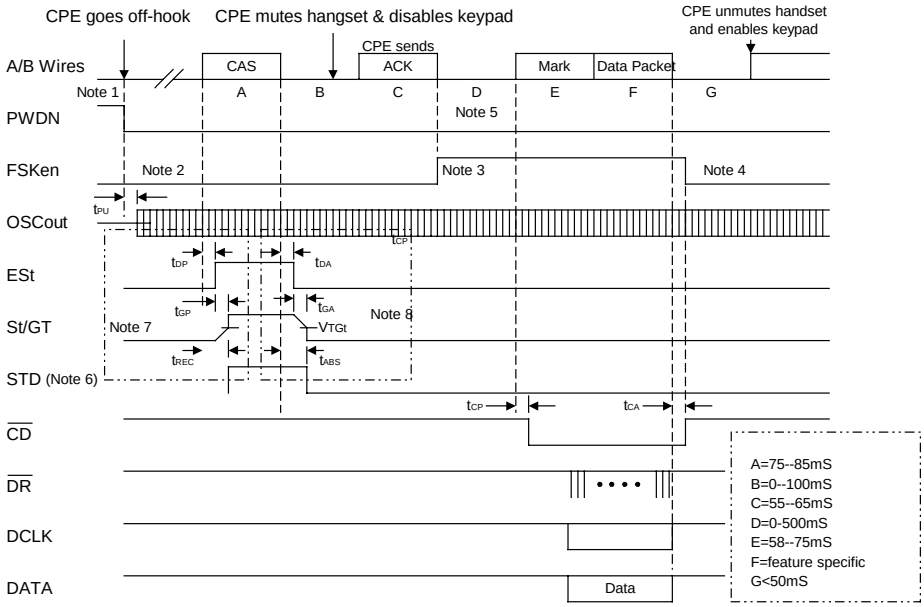


Figure 20: Input and Output Timing for Bellcore off-hook Data Transmission,e.g., CIDCW

Note:

1. In a CPE where AC power is not available, the designer may choose to switch over to line power when the CPE goes off-hook and use battery power while on-hook. The CPE should also be CID (on-hook) capable because TR-NWT-000575 specifies that CIDCW will be offered only to lines which subscribe to CID.
2. Non-FSK signals such as CAS, speech and DTMF tones are in the same frequency band as FSK. They will be demodulated and give false data. The FSKen pin should be set low to disable the FSK demodulator when FSK is not expected.
3. FSKen may be set high as soon as the CPE has finished sending the acknowledgment signal ACK. TR-NWT-000575 specifies that ACK=DTMF D for non-ADSI CPE, A for ADSI CPE.
4. FSKen should be set low when $\overline{CD}$ has become inactive.
5. In an unsuccessful attempt where the end office does not send the FSK signal, the CPE should unmute the handset and enable the keypad after this interval.
6. SR-TSV-002476 states that it is desirable that the CPE have an on/off switch for the CAS detector. See SW1 in Figure 4.
7. The total recognition time is $t_{REC}=t_{GP}+t_{DR}$,where T_{GP} is the tone present guard time and t_{DP} is the tone present detect time (refer to section “Dual Tone Detection Time” on page 11 for details). V_{TGt} is the comparator threshold (refer to Figure 4).
8. The total tone absent time is $t_{ABS}=t_{GA}+t_{DA}$, where tGA is the tone absent guard time and t_{DA} is the tone absent detect time (refer to section ” Dual Tone Detection Time” on page 11 for details). V_{TGt} is the comparator threshold (refer to Figure 4).

PACKAGE OUTLINE

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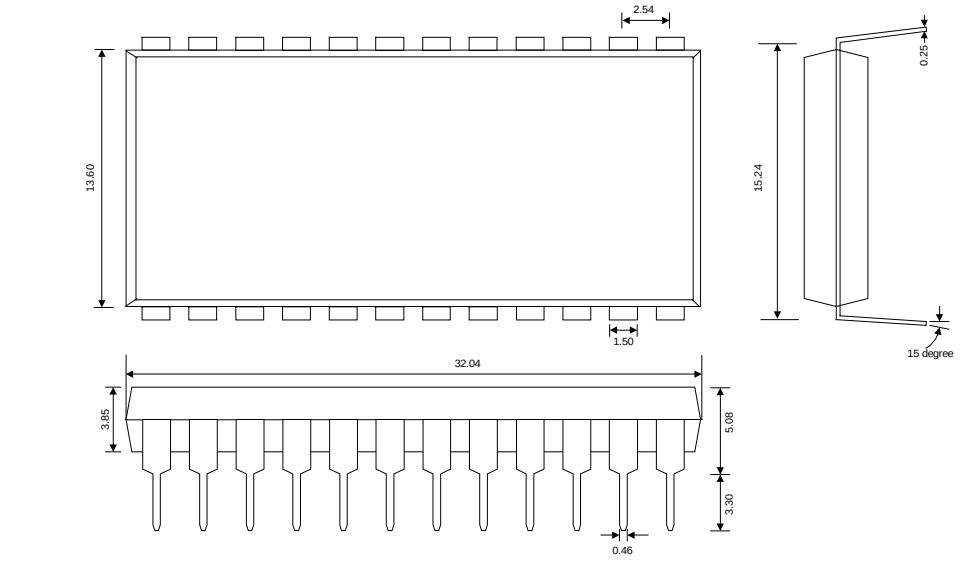

SOP-24-375-1.27 UNIT:mm