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西日本 MOTOROLA SEMICONDUCTOR TECHNICAL DATA

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# Advance Information 128K x 24 Bit Static Random Access Memory

The MCM6341 is a 3,145,728–bit static random access memory organized as 131,072 words of 24 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6341 is equipped with chip enable ( $\overline{E1}$ , E2,  $\overline{E3}$ ) and output enable ( $\overline{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6341 is available in a 119–bump PBGA package.

- Single 3.3 V ± 10% Power Supply
- Fast Access Time: 10/11/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs

REV 2 2/18/98

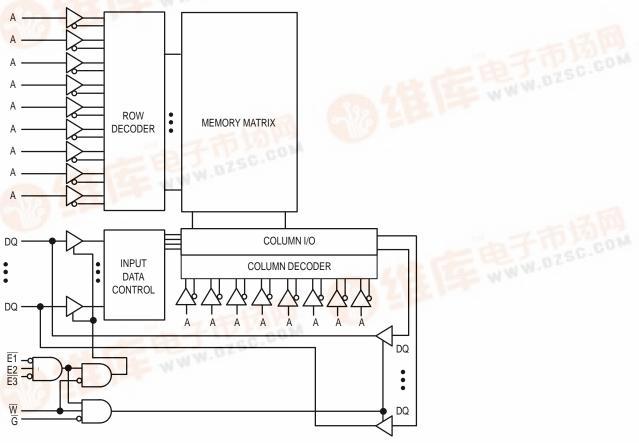
com

- Power Operation: 280/275/270/260 mA Maximum, Active AC
- Commercial Temperature (0°C to 70°C) and Industrial Temperature (– 40°C to + 85°C) Options



PIN	NAMES	

AAddress Inputs WWrite Enable GOutput Enable E1, E2, E3Chip Enable DQData Input/Output NCNo Connection VDD+3.3 V Power Supply VocGround
V <sub>DD</sub> + 3.3 V Power Supply V <sub>SS</sub> Ground



This document contains information on a new product. Specifications and information herein are subject to change without notice.



### **BLOCK DIAGRAM**

**PIN ASSIGNMENT** 

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		1	2	3	4	5	6	7
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	А	O NC	А	А	O A	O A		O NC
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	В	O NC	O A	O A	$\frac{O}{E1}$	O A	O A	O NC
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	С	O DQ	O NC	O E2	O NC	<u>O</u> E3	O NC	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		O DQ	o Vdd	o V <sub>SS</sub>	o V <sub>SS</sub>	o V <sub>SS</sub>	o V <sub>DD</sub>	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Е	O DQ	0 Vss	0 Von	0 Vss	0 VDD	0 Vss	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		O DQ	° V <sub>DD</sub>	o V <sub>SS</sub>	O VSS	Ö VSS	O V <sub>DD</sub>	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	G	O DQ	o Vss	0 VDD	0 VSS	0 VDD	Ö VSS	O DQ
J VDD VSS VDD VSS VDD VSS VDD   K O O O O O O O   DQ VDD VSS VSS VDD VSS VDD DQ   L O O O O O O O O   DQ VSS VDD VSS VSS VDD VSS DQ   M O O O O O O O O   N DQ VSS VDD VSS VSS VSS VDD DQ   N DQ VSS VDD VSS VSS VDD O O   N DQ VSS VDD VSS VSS VDD O O   N DQ VSS VDD VSS VSS VDD O O   P DQ VDD VSS VSS VSS VDD DQ   R DQ NC NC NC NC	Н	O DQ	õ Vnn	õ Vss	õ Vss	õ V <sub>SS</sub>	õ Vnn	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	J		O VSS		O VSS		O VSS	0 V <sub>DD</sub>
L O O O O O O   DQ VSS VDD VSS VDD VSS DQ   M O O O O O O O   DQ VDD VSS VSS VSS VDD DQ   N O O O O O O O   P DQ VSS VDD VSS VDD VSS DQ   R O O O O O O O   T O O O O O O O   NC A A W A A NC	К	O DQ	o VDD	o Vss	o Vss	o Vss	o Vod	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	L	O DQ	Ö Vss	0 Von	0 Vss	0 Vnn	0 Vss	O DQ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	М	O DQ	о О Илл	0 Vee	0 Vss	0 Vee	о О Vпп	O DQ
P   O	Ν	O DQ	o Vss		0 Vss	° VDD	Ö Vss	O DQ
R   O	Ρ	O DQ	о О	õ V <sub>SS</sub>	õ VSS	õ V <sub>SS</sub>	о О	O DQ
T 0 0 0 0 0 0 0 NC A A W A A NC	R	O DQ	O NC	O NC	O NC	O NC	O NC	O DQ
	Т	O NC	O A	O A	o ₩	O A	O A	O NC
NC A A G A A NC	U	O NC	O A	O A	⊖ G	O A	0	O NC

119–BUMP PBGA TOP VIEW

#### TRUTH TABLE (X = Don't Care)

E1	E2	E3	G	W	Mode	I/O Pin	Cycle	Current
Н	Х	Х	Х	Х	Not Selected	High–Z	_	I <sub>SB1</sub> , I <sub>SB2</sub>
Х	L	Х	Х	Х	Not Selected High-Z —		I <sub>SB1</sub> , I <sub>SB2</sub>	
Х	Х	Н	Х	Х	Not Selected	High–Z —		I <sub>SB1</sub> , I <sub>SB2</sub>
L	Н	L	Н	Τ	Output Disabled High-Z —		I <sub>DDA</sub>	
L	Н	L	L	Τ	Read D <sub>out</sub> Re		Read	IDDA
L	Н	L	Х	L	Write	High–Z	Write	IDDA

#### ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to $V_{SS}$	V <sub>DD</sub>	– 0.5 to + 5.0	V
Voltage Relative to $V_{\mbox{SS}}$ for Any Pin Except $V_{\mbox{DD}}$	V <sub>in</sub> , V <sub>out</sub>	– 0.5 to V <sub>DD</sub> + 0.5	V
Output Current (per I/O)	l <sub>out</sub>	± 20	mA
Power Dissipation	PD	1.0	W
Temperature Under Bias Commercial Industrial	T <sub>bias</sub>	– 10 to + 85 – 45 to + 90	°C
Storage Temperature — Plastic	T <sub>stg</sub>	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPER-ATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

#### DC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>DD</sub> = 3.3 V  $\pm$  10%, T<sub>A</sub> = 0 to + 70°C, Unless Otherwise Noted)  $(T_A = -40 \text{ to } + 85^{\circ}\text{C} \text{ for Industrial Temperature Offering})$ 

#### **RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>DD</sub>	3.0	3.3	3.6	V
Input High Voltage	VIH	2.2	_	V <sub>DD</sub> + 0.3**	V
Input Low Voltage	VIL	- 0.5*	—	0.8	V

\* V<sub>IL</sub> (min) = -0.5 V dc; V<sub>IL</sub> (min) = -2.0 V ac (pulse width  $\le 2.0$  ns). \*\* V<sub>IH</sub> (max) = V<sub>DD</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>DD</sub> + 2.0 V ac (pulse width  $\le 2.0$  ns).

#### DC CHARACTERISTICS (See Note)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>DD</sub> )	I <sub>lkg(I)</sub>	-	± 1.0	μΑ
Output Leakage Current ( $\overline{E} = V_{IH}$ , $V_{Out} = 0$ to $V_{DD}$ )	I <sub>lkg(O)</sub>		± 1.0	μΑ
Output Low Voltage (I <sub>OL</sub> = + 8.0 mA)	VOL	_	0.4	V
Output High Voltage (I <sub>OH</sub> = - 4.0 mA)	VOH	2.4	_	V

NOTE: E1, E2, and  $\overline{E3}$  are represented by  $\overline{E}$  in this data sheet. E2 is of opposite polarity to  $\overline{E1}$  and  $\overline{E3}$ .

#### POWER SUPPLY CURRENTS (See Note)

Parameter		Symbol	0 to 70°C	– 40 to + 85°C	Unit
AC Active Supply Current (I <sub>out</sub> = 0 mA, V <sub>DD</sub> = max)	MCM6341-10 MCM6341-11 MCM6341-12 MCM6341-15	IDD	280 275 270 260	290 285 280 270	mA
AC Standby Current ( $V_{DD}$ = max, $\overline{E}$ = $V_{IH}$ , No other restrictions on other inputs)	MCM6341-10 MCM6341-11 MCM6341-12 MCM6341-15	I <sub>SB1</sub>	50 50 50 45	55 55 55 50	mA
CMOS Standby Current ( $\overline{E} \ge V_{DD} - 0.2 \text{ V}$ , $V_{in} \le V_{SS} + 0.2 \text{ V}$ ( $V_{DD} = max$ , f = 0 MHz)	I <sub>SB2</sub>	20	20	mA	

NOTE:  $\overline{E1}$ , E2, and  $\overline{E3}$  are represented by  $\overline{E}$  in this data sheet. E2 is of opposite polarity to  $\overline{E1}$  and  $\overline{E3}$ .

#### **CAPACITANCE** (f = 1.0 MHz, dV = 3.0 V, $T_A = 25^{\circ}C$ , Periodically Sampled Rather Than 100% Tested)

	Parameter	Symbol	Тур	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}, \overline{G}, \overline{W}$	C <sub>in</sub> C <sub>ck</sub>	4 5	6 8	pF
Input/Output Capacitance	DQ	C <sub>I/O</sub>	5	8	pF

#### AC OPERATING CONDITIONS AND CHARACTERISTICS

 $(V_{DD} = 3.3 V \pm 10\%, T_A = 0 \text{ to } + 70^{\circ}\text{C}, \text{ Unless Otherwise Noted})$  $(T_A = -40 \text{ to } + 85^{\circ}\text{C} \text{ for Industrial Temperature Offering})$ 

Input Pulse Levels	0 to 3.0 V
Input Rise/Fall Time	2 ns
Input Timing Measurement Reference Level	1.5 V

Output Timing Measurement Reference Level	1.5 V
Output Load See Fig	jure 1

#### READ CYCLE TIMING (See Notes 1, 2, and 3)

		MCM6341-10		341–10 MCM6341–11		MCM6341-12		MCM6341-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Time	t <sub>AVAV</sub>	10	—	11	_	12	—	15	—	ns	4
Address Access Time	<sup>t</sup> AVQV	-	10	—	11	—	12	_	15	ns	
Enable Access Time	<sup>t</sup> ELQV	-	10	—	11	—	12	_	15	ns	5
Output Enable Access Time	<sup>t</sup> GLQV	-	5	—	6	_	6	_	7	ns	
Output Hold from Address Change	<sup>t</sup> AXQX	3	—	3	_	3	—	3	—	ns	
Enable Low to Output Active	<sup>t</sup> ELQX	3	—	3	_	3	—	3	—	ns	6, 7, 8
Output Enable Low to Output Active	<sup>t</sup> GLQX	0	—	0	_	0	_	0	—	ns	6, 7, 8
Enable High to Output High-Z	<sup>t</sup> EHQZ	0	5	0	6	0	6	0	7	ns	6, 7, 8
Output Enable High to Output High-Z	<sup>t</sup> GHQZ	0	5	0	6	0	6	0	7	ns	6, 7, 8

NOTES:

1.  $\overline{W}$  is high for read cycle.

2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.

3.  $\overline{E1}$ , E2, and  $\overline{E3}$  are represented by  $\overline{E}$  in this data sheet. E2 is of opposite polarity to  $\overline{E1}$  and  $\overline{E3}$ .

4. All read cycle timings are referenced from the last valid address to the first transitioning address.

5. Addresses valid prior to or coincident with  $\overline{E}$  going low.

6. At any given voltage and temperature, t<sub>EHQZ</sub> max < t<sub>ELQX</sub> min, and t<sub>GHQZ</sub> max < t<sub>GLQX</sub> min, both for a given device and from device to device.

7. Transition is measured  $\pm$  200 mV from steady–state voltage.

8. This parameter is sampled and not 100% tested.

9. Device is continuously selected ( $\overline{E} \le V_{IL}$ ,  $\overline{G} \le V_{IL}$ ).

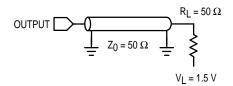


Figure 1. AC Test Load

READ CYCLE 1 (See Note 9) - t<sub>AVAV</sub> -A (ADDRESS) -taxqx -Q (DATA OUT) PREVIOUS DATA VALID DATA VALID t<sub>AVQV</sub> READ CYCLE 2 (See Notes 3 and 5) - t<sub>avav</sub> -A (ADDRESS) tELQV -**E** (CHIP ENABLE) - <sup>t</sup>ehqz -telqx--► G (OUTPUT ENABLE) tGLQV -- <sup>t</sup>GHQZ -tGLQX-4 HIGH-Z Q (DATA OUT) DATA VALID tavqv -IDD SUPPLY CURRENT ISB

Parameter		MCM6341-10		MCM6341-11		MCM6341-12		MCM6341-15			
	Symbol	Min	Мах	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	<sup>t</sup> AVAV	10	-	11	—	12	—	15	—	ns	5
Address Setup Time	<sup>t</sup> AVWL	0	_	0		0	—	0	-	ns	
Address Valid to End of Write	<sup>t</sup> AVWH	9	-	10		10	—	12	-	ns	
Address Valid to End of Write ( $\overline{G}$ High)	<sup>t</sup> AVWH	8	—	9	_	9	_	10	-	ns	
Write Pulse Width	<sup>t</sup> WLWH <sup>t</sup> WLEH	9	—	10	_	10	_	12	-	ns	
Write Pulse Width ( $\overline{G}$ High)	<sup>t</sup> WLWH <sup>t</sup> WLEH	8	—	9	_	9	_	10	-	ns	
Data Valid to End of Write	<sup>t</sup> DVWH	4	—	5		5	—	6	—	ns	
Data Hold Time	<sup>t</sup> WHDX	0	—	0		0	—	0	—	ns	
Write Low to Data High–Z	<sup>t</sup> WLQZ	0	5	0	6	0	6	0	7	ns	6, 7, 8
Write High to Output Active	<sup>t</sup> WHQX	3	-	3	—	3	—	3	—	ns	6, 7, 8
Write Recovery Time	<sup>t</sup> WHAX	0	-	0	_	0	—	0	—	ns	

#### WRITE CYCLE 1 (W Controlled; See Notes 1, 2, 3, and 4)

NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.

2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.

3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.

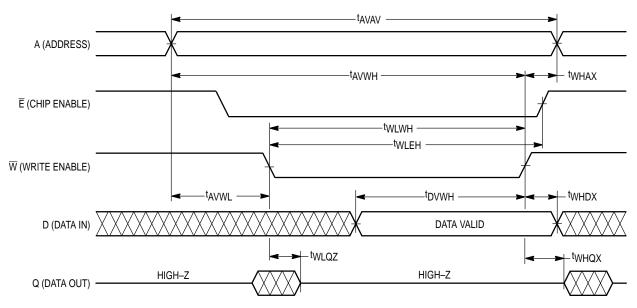
4.  $\overline{E1}$ ,  $\overline{E2}$ , and  $\overline{E3}$  are represented by  $\overline{E}$  in this data sheet.  $\overline{E2}$  is of opposite polarity to  $\overline{E1}$  and  $\overline{E3}$ .

5. All write cycle timings are referenced from the last valid address to the first transitioning address.

6. Transition is measured  $\pm$  200 mV from steady-state voltage.

7. This parameter is sampled and not 100% tested.

8. At any given voltage and temperature, tWLQZ max < tWHQX min both for a given device and from device to device.



WRITE CYCLE 1 ( $\overline{W}$  Controlled; See Notes 1, 2, 3, and 4)

Parameter		MCM6341-10		MCM6341-11		MCM6341-12		MCM6341-15			
	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	tAVAV	10	—	11	—	12	—	15	—	ns	5
Address Setup Time	<sup>t</sup> AVEL	0	—	0	_	0		0	—	ns	
Address Valid to End of Write	<sup>t</sup> AVEH	9	-	10	—	10	_	12	—	ns	
Address Valid to End of Write ( $\overline{G}$ High)	<sup>t</sup> AVEH	8	—	9	_	9	_	10	_	ns	
Enable Pulse Width	<sup>t</sup> ELEH, <sup>t</sup> ELWH	9	—	10	_	10	_	12	_	ns	6, 7
Enable Pulse Width ( $\overline{G}$ High)	<sup>t</sup> ELEH, <sup>t</sup> ELWH	8	—	9	_	9	_	10	_	ns	6, 7
Data Valid to End of Write	<sup>t</sup> DVEH	4	—	5	—	5		6	—	ns	
Data Hold Time	<sup>t</sup> EHDX	0	—	0	_	0		0	—	ns	
Write Recovery Time	<sup>t</sup> EHAX	0	-	0	—	0		0	—	ns	

#### WRITE CYCLE 2 (E Controlled; See Notes 1, 2, 3, and 4)

NOTES:

1. A write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low.

2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.

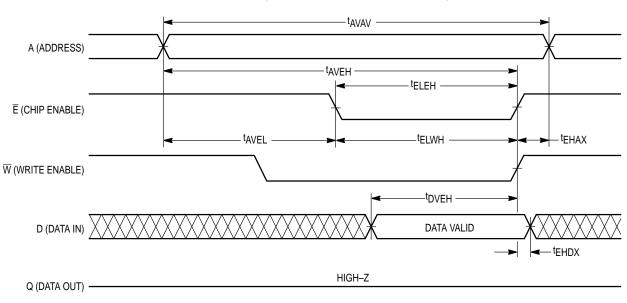
3. If  $\overline{G}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high-impedance state.

4.  $\overline{E1}$ ,  $\overline{E2}$ , and  $\overline{E3}$  are represented by  $\overline{E}$  in this data sheet.  $\overline{E2}$  is of opposite polarity to  $\overline{E1}$  and  $\overline{E3}$ .

5. All write cycle timing is referenced from the last valid address to the first transitioning address.

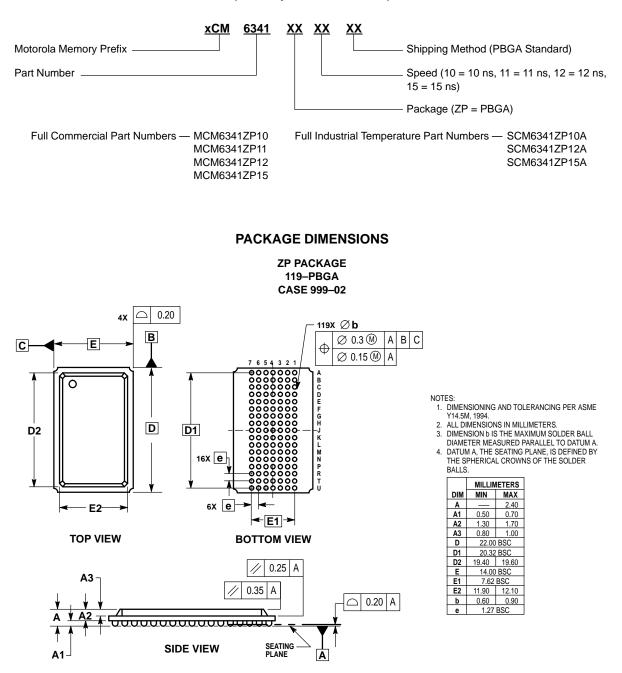
6. If  $\overline{E}$  goes low coincident with or after  $\overline{W}$  goes low, the output will remain in a high–impedance condition.

7. If  $\overline{E}$  goes high coincident with or before  $\overline{W}$  goes high, the output will remain in a high–impedance condition.



#### WRITE CYCLE 2 (E Controlled; See Notes 1, 2, 3, and 4)

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