TOPAZ SEMICONDUCTOR

SD204, SD205

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD204CHP	SD205CHP
TO-205AF (TO-39) Package	SD204HD	SD205HD
Description	6.0 ohm, 25V	6.0 ohm, 25V

FEATURES

- Low Capacitance—c_{iss} 11pF typ.
- Inherently Temperature Stable by Design
- TTL Logic Compatible Input—$V_{GS(th)}$ 2.0V (max)

APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switches and Drivers
- Pulse Amplifiers and Logic Buffers
- CMOS and TTL to High Current Interface

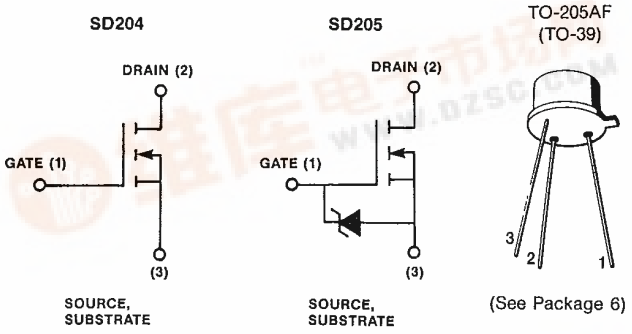
ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

V_{DS} Drain-Source Voltage ..... +25V
V_{DG} Drain-Gate Voltage ..... +25V
V_{GS} Gate-Source (Forward) Voltage ..... +20V
Gate-Source (Reverse) Voltage ..... -0.3V
I_D Continuous Drain Current (Note 1) 0.3A
Continuous Drain Current (Note 2) 0.7A
Peak Pulsed Drain Current 1.0A
P_D Continuous Power Dissipation
T_A = +25°C (Note 1, Note 3) 1.0W
T_C = +25°C (Note 1, Note 4) 6.25W
Power Derating Factors (Note 1)
Free Air ..... 10mW/°C
Infinite Heat Sink ..... 62.5mW/°C

Thermal Resistance (Note 1)
O_{ja} Junction to Ambient ..... 100°C/W
O_{jc} Junction to Case ..... 16°C/W
T_{op} Operating Junction Temperature Range ..... -55 to +125°C
T_{stg} Storage Temperature Range ..... -55 to +150°C

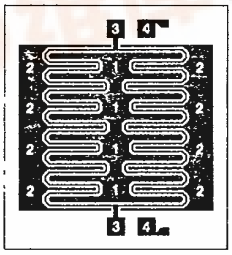
Note 1: Not applicable to chips. Final value depends on mounting.
Note 2: Pulse Test 80μSec, 1% Duty Cycle
Note 3: Free Air
Note 4: Infinite Heat Sink

SCHEMATIC DIAGRAM



(See Package 6)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate 4—Diode
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

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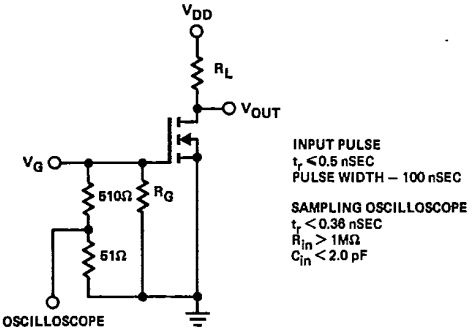
T-35-25

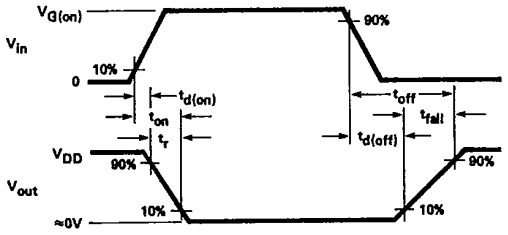
ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DSS} Drain Source Breakdown Voltage		25			V	I_D = 1.0μA, V_{GS} = 0
2	STATIC	$V_{GS(th)}$ Gate Source Threshold Voltage		0.5		2.0	V	I_D = 1mA, V_{DS} = V_{GS}
3	STATIC	$I_{D(on)}$ Drain-Source ON Current		1.0			nA	V_{DS} = 10V (Note 1) V_{GS} = 10V
4	STATIC	I_{DSS} Drain-Source OFF Leakage Current				1.0	nA	V_{DS} = 25V, V_{GS} = 0
5	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance				8.0	ohms	V_{GS} = 5V; I_D = 50mA (Note 1)
6	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance				6.0	ohms	V_{GS} = 10V; I_D = 500mA (Note 1)
7	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance				6.0	ohms	V_{GS} = 10V; I_D = 500mA (Note 1)
8	STATIC	I_{GSS} Gate Body Leakage Current	SD205			1.0	μA	V_{GS} = 20V, V_{DS} = 0
8A	STATIC	I_{GSS} Gate Body Leakage Current	SD204			±10	nA	V_{GS} = ±20V, V_{DS} = 0
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance		100			mmhos	V_{DS} = 15V, I_D = 200mA f = 1KHz (Note 1)
10	DYNAMIC	c_{iss} Common-Source Input Capacitance			11	13	pF	V_{DS} = 10V, V_{GS} = 0 f = 1MHz
11	DYNAMIC	c_{oss} Common-Source Output Capacitance				8.0	pF	V_{DS} = 10V, V_{GS} = 0 f = 1MHz
12	DYNAMIC	c_{rss} Common-Source Reverse Transfer Capacitance				3.0	pF	V_{DS} = 10V, V_{GS} = 0 f = 1MHz
13	DYNAMIC	$t_{d(on)}$ Turn-On Delay Time			<1.0	2.0	nS	V_{DD} = 10V, $V_{G(on)}$ = 10V R_L = 133Ω, R_G = 51Ω
14	DYNAMIC	t_r Rise Time			1.0	3.0	nS	V_{DD} = 10V, $V_{G(on)}$ = 10V R_L = 133Ω, R_G = 51Ω
15	DYNAMIC	t_{off} Turn-off Time			3.0	5.0	nS	V_{DD} = 10V, $V_{G(on)}$ = 10V R_L = 133Ω, R_G = 51Ω
16	DYNAMIC	NF Common-Source Noise Figure				4.5	dB	V_{DS} = 10V, I_D = 100mA f = 300MHz
17	DYNAMIC	G_{PS} Common-Source Power Gain		9.0			dB	V_{DS} = 10V, I_D = 100mA f = 300MHz

SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS



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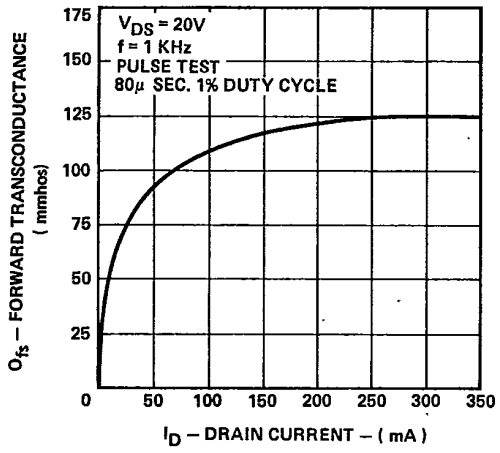
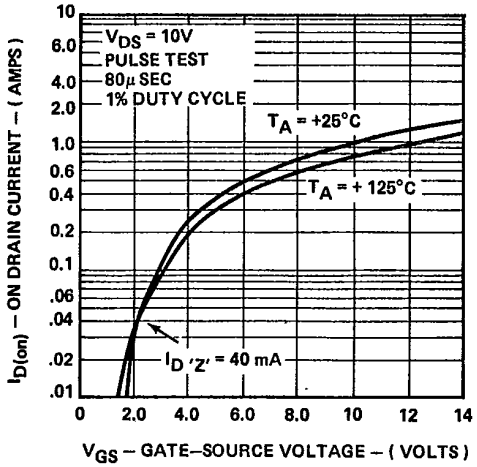
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

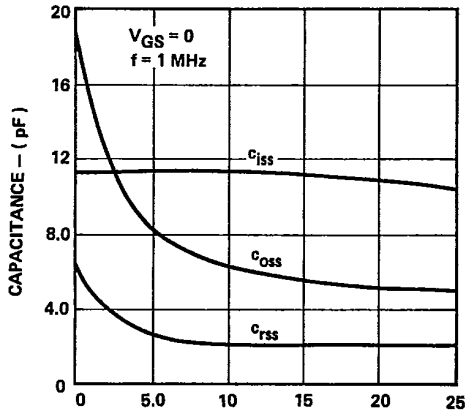
FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT



ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



CAPACITANCES —VS— DRAIN-SOURCE VOLTAGE



DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE