Table of Contents

1. Introduction

The SD73C168 is an 8-Bit microcontroller that contains Prescaler, PLL Frequency Synthesizer and 2 channel A/D converter for Digital Tuning System.
The device is provided with abundant I/O ports and 2 channel serial interface ports (SI/O) controlled by powerful instruction. The package is 80-pin QFP and high performance CPU and internal peripheral allow flexible and easy system design in car-stereo, radio tuner and Hi-Fi audio system.

1.1 Key Features

- CMOS Technology
- Memory Configuration
  - 256 Byte On-Chip RAM Register file plus 128 Byte Peripheral Free RAM
  - Memory-Mapped Ports for Easy Addressing
  - 16K-Byte On-Chip ROM
- On-Chip PLL Frequency Synthesizer with Dual Modules Prescaler
  - Independant Frequency input ports : Max 150MHz at FM, 40MHz at AM
  - Two Types of Frequency Dividing Method : Pulse Swallow and Direct
  - 8 Kinds of reference Frequencies : 1, 5, 6.25, 9, 10, 12.5, 25 and 50KHz
- 2 Channel SIO port
- 2 Channel On-Chip Timer
  - 16-Bit with 5-Bit Prescaler and 16-Bit capture latch, timer outputs
  - Internal interrupt with Automatic timer Reload
- On-Chip A/D Converter
  - 2-channels with 8 bit resolution
  - Ratiometric Conversion
  - 144 Machine-Cycles Conversion time (64us)
- On-Chip IF Counter
  - 17-Bit, Gate Time : Program can select from 1ms to 15ms
  - maximum Input Frequency : FM IF = 20MHz, AM IF = 5MHz
- Easy Interrupt Handling
  - External Interrupts with Schmitt-Trigger Input
  - Software Calls through Interrupt Vectors
  - Software Monitoring of Interrupt Status
  - Precise Interrupt Timing through Capture Latch
- Selectable Beep clock : 417Hz, 1KHz, 1.25KHz, 2.5KHz
- 64 I/O Pins
  - 64 Bidirectional Pins
- Wide Operating Range
  - Voltage(VDD) : 5V ± 10%

- Clock : 4.5MHz
- Temperature : -40 deg to 85 deg
- One Machine Execution Time : 0.44us (with 4.5MHz Crystal Oscillator)

■ Low operating Current

- Halt Mode for Power Savings (Typical : 1uA at OSC stop)
- Warm-up mode for avoid unstable osc operation at the wake time from Halt mode. The warm-up time can be adjustable by S/W.

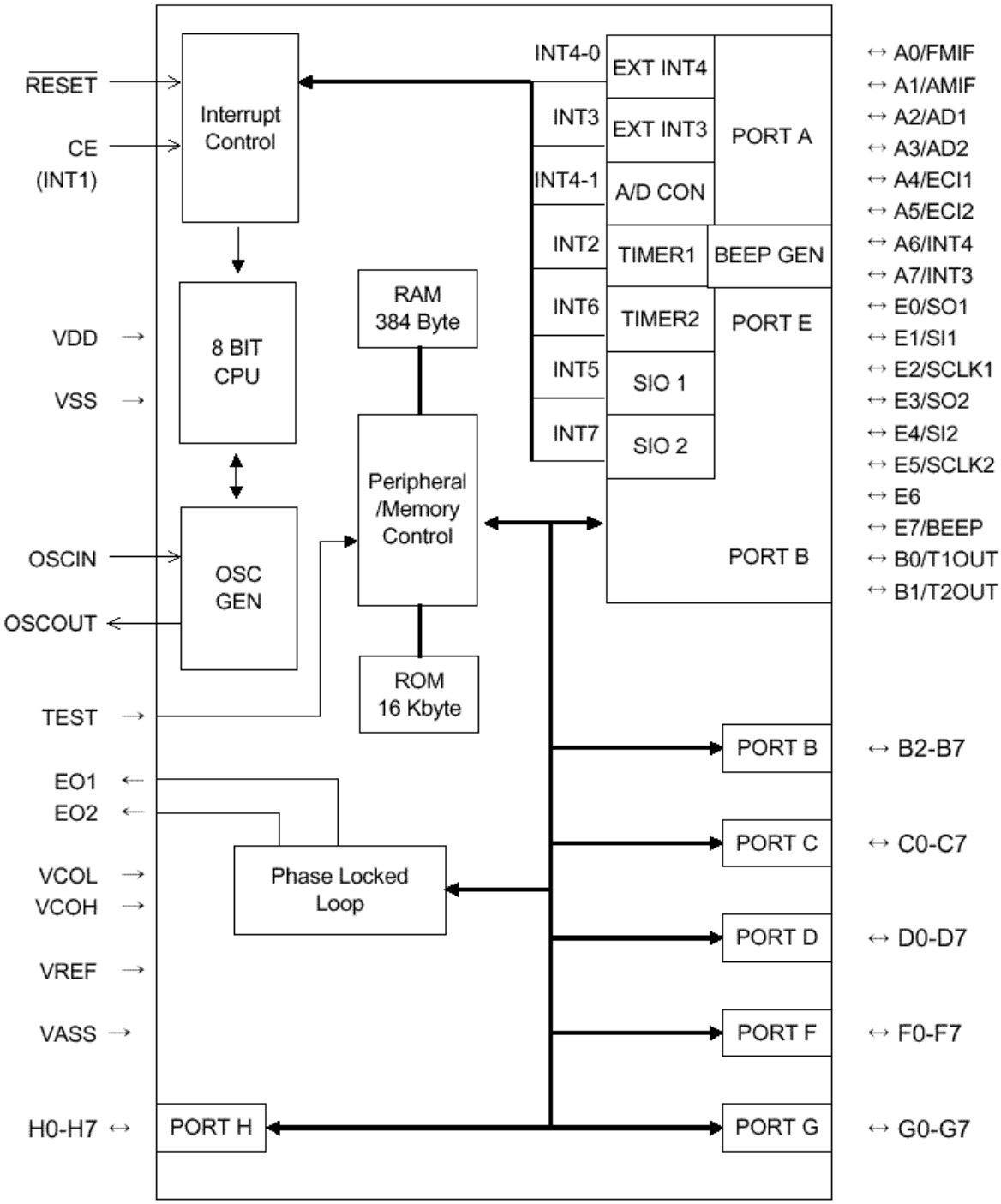
■ Package

- 80 QFP (Quad Flat Package)

■ Development Support

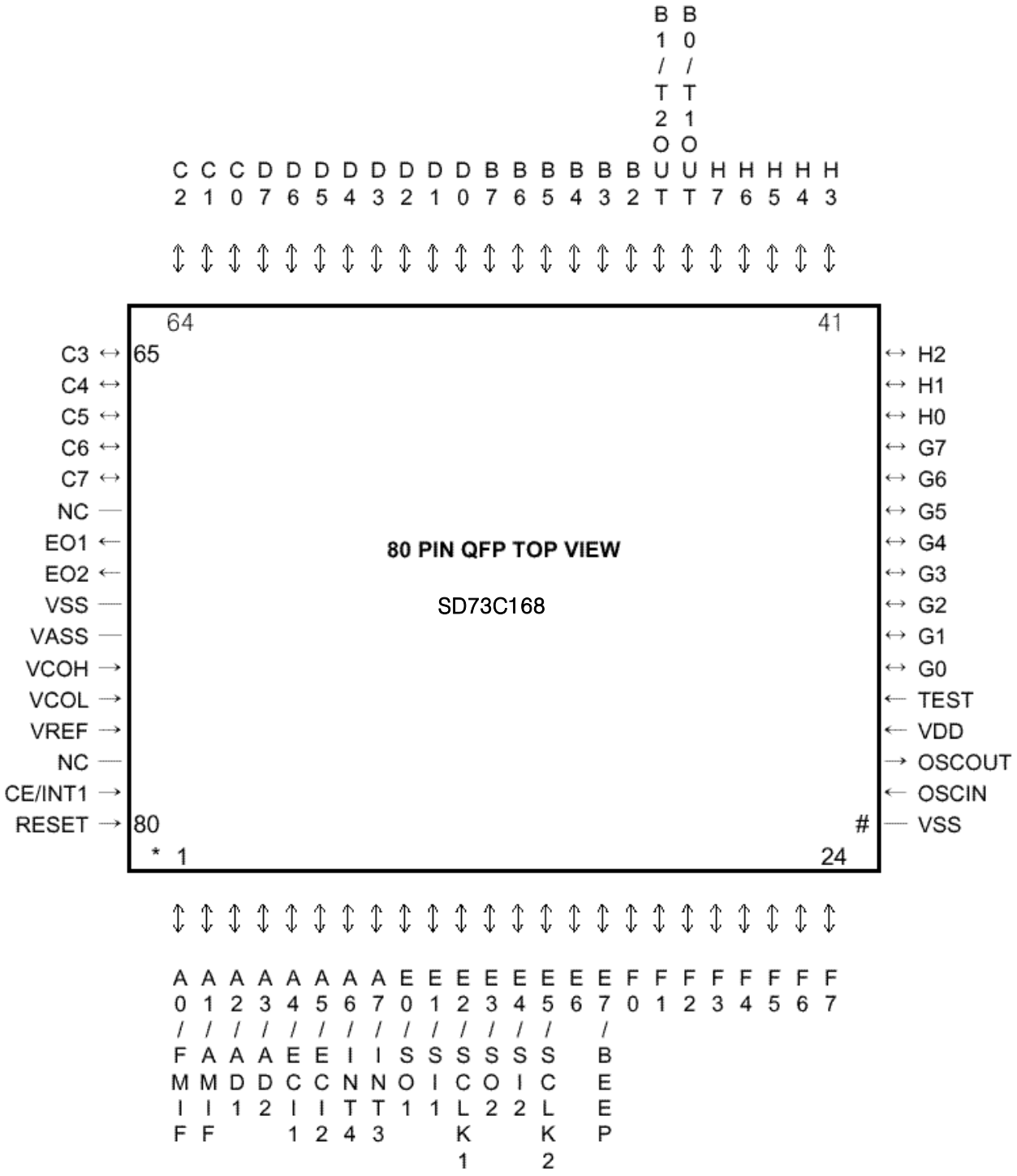
- Evaluation Module : EVM73C00A & ADP73C168
- Assembler/Linker Cross Support for Popular Hosts

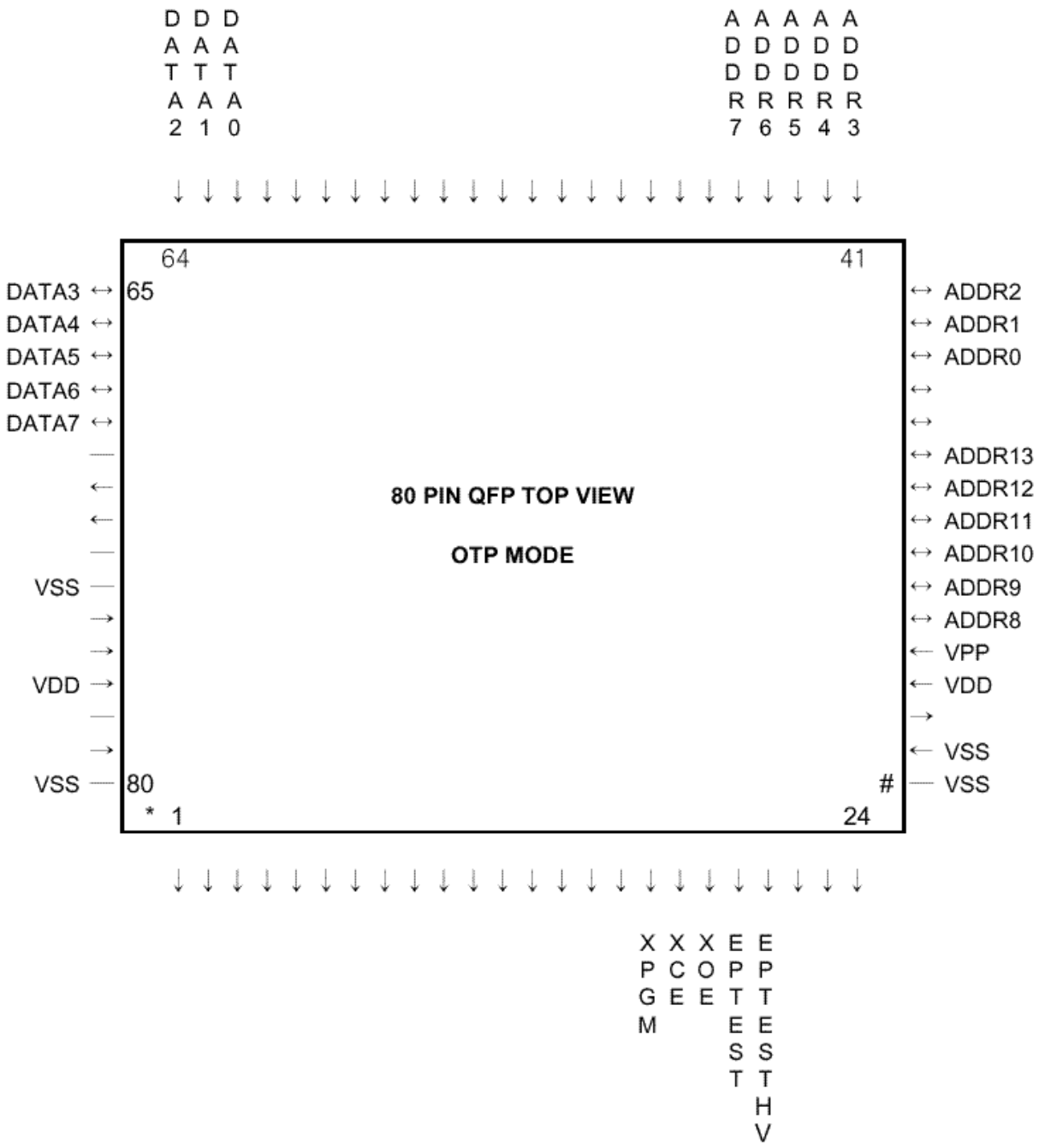
2. SD73C168 Block Diagram



3. PIN Assignment and Description

3.1 SD73C168 Pin Assignment




DATA2
DATA1
DATA0
ADDR7
ADDR6
ADDR5
ADDR4
ADDR3
64
41
DATA3
65
DATA4
DATA5
DATA6
DATA7
ADDR2
ADDR1
ADDR0
ADDR13
ADDR12
ADDR11
ADDR10
ADDR9
ADDR8
VPP
VDD
VSS
VSS
80 PIN QFP TOP VIEW
OTP MODE
VSS
VDD
VSS
80
1
24
#
XPGM
XCE
XOE
EPTEST
EPTESTHV

3.2 Description

NAME	Pin No.	I/O	FUNCTIONAL DESCRIPTION	PORT TYPE
A0/FM IF	1	I/O	Port A is a bidirectional data port.	Analog-IN or
A1/AM IF	2	I/O	These Ports can be selected as universal Counter input. A0 and A1 work as the FM IF and AM IF pin, independently. The maximum input frequency is 5MHz for AM IF (0.1Vp-p) and 20MHz (0.1Vp-p) for FM IF.	Logic-IN/ Push-Pull OUT
A2/AD1	3	I/O	These Posts can be selected for an A/D Converter Input.	Analog-IN or
A3/AD2	4	I/O	2 Channel/8-Bit Analog-to-Digital Converter are used for the Sequential Comparison method by program. Reference Voltage of the A/D Converter is the same level of VDD (5V± 10%)	Logic-IN/ Push-Pull OUT
A4/ECI1	5	I/O	The A4,A5 Port can be used as event counter input 1,2.	
A5/ECI2	6	I/O		
A6/INT4	7	I/O	These Ports can be used as external interrupt pin.	Logic-IN or
A7/INT3	8	I/O		Schmitt-Trigger-IN/ Push-Pull OUT
E0/SO1	9	I/O	Port E is a bidirectional data port.	
E1/SI1	10	I/O	These Ports can be selected as serial interface (SIO) 1.	Logic-IN/
E2/SCLK1	11	I/O	E0, E1 and E2 work as the serial output, serial input and serial clock pin, respectively.	Push-Pull OUT
E3/SO2	12	I/O	These Ports can be selected as serial interface (SIO) 2.	
E4/SI2	13	I/O	E3, E4 and E5 work as the serial output, serial input and	Logic-IN/
E5/SCLK2	14	I/O	serial clock pin, respectively.	Push-Pull OUT
E6	15	I/O		
E7/BEEP	16	I/O	The E7 Port can be used as BEEP output pin.	
F0	17	I/O	Port F is a bidirectional data port.	
F1	18	I/O		Logic-IN/
F2	19	I/O		Push-Pull OUT
F3	20	I/O		
F4	21	I/O		
F5	22	I/O		
F6	23	I/O		
F7	24	I/O		

NAME	PIN NO.	I/O	FUNCTION DESCRIPTION	PORT TYPE
G0	30	I/O	Port G is a bidirectional data port.	Logic-IN/
G1	31	I/O		Push-Pull OUT
G2	32	I/O		
G3	33	I/O		
G4	34	I/O		
G5	35	I/O		
G6	36	I/O		
G7	37	I/O		
H0	38	I/O	Port H is a bidirectional data port.	Logic-IN/
H1	39	I/O		Push-Pull OUT
H2	40	I/O		
H3	41	I/O		
H4	42	I/O		
H5	43	I/O		
H6	44	I/O		
H7	45	I/O		
B0/T1OUT	46	I/O	Port B is a bidirectional data port.	Logic-IN/
B1/T2OUT	47	I/O	Port B0, B1 can be selected as Timer 1 & 2 output ports.	Push-Pull OUT
B2	48	I/O		
B3	49	I/O		
B4	50	I/O		
B5	51	I/O		
B6	52	I/O		
B7	53	I/O		
D0	54	I/O	Port D is a bidirectional data port.	Logic-IN/
D1	55	I/O		Push-Pull OUT
D2	56	I/O		
D3	57	I/O		
D4	58	I/O		
D5	59	I/O		
D6	60	I/O		
D7	61	I/O		
C0	62	I/O	Port C is a bidirectional data port.	Logic-IN/
C1	63	I/O		Push-Pull OUT
C2	64	I/O		
C3	65	I/O		
C4	66	I/O		
C5	67	I/O		
C6	68	I/O		
C7	69	I/O		

NAME	Pin No.	I/O	FUNCTION DESCRIPTION	PORT TYPE
VCOH	75	I	FM VCO input port. Only Pulse swallow method is used for this port. The range of local oscillator output is 10MHz to 150MHz with 0.3Vp-p minimum. The output is required by capacitor coupling because an AC amplifier is contained.	Analog-IN
VCOL	76	I	AM VCO input port. This terminal can be selected by direct-dividing method or pulse-swallow method. In direct-dividing method, the range of local oscillator output is 0.5MHz to 10MHz with 0.3Vp-p minimum, and in pulse-swallow method, the range of local oscillator output is 5MHz to 40MHz with 0.3Vp-p minimum. Input to this port should be coupled by capacitor coupling because and AC amplifier is contained.	Analog-IN
VDD VREF	28 77		Power source port. The terminal supplies 5V ±10% for normal operation. VDD and VREF must be connected to the same electric potential. VDD is a power for logic circuit and V_{REF} is a power for analog circuit in the device.	
NC	70		No connection	
EO1 EO2	71 72	O O	Phase comparison error output ports. The divided frequency of VCO output and the reference frequency are compared in their phase. If divided frequency is higher than the reference frequency, output signal is logic high level. If divided frequency is lower than the reference frequency, output signal is vice versa. When two frequencies are matched, port become a floating state. EO1 and EO2 have the same waveform.	3-State-OUT
TEST	29	I	Internal Chip Test port. It should be connected to VSS.	
VSS VASS	73, 25 74		Ground reference VSS is a ground for logic circuit and VASS is a ground for Analog circuit in the device	
OSCOUT OSCIN	27 26	O I	Crystal oscillator input and output ports. Connect 4.5MHz Crystal.	

NAME	PIN NO.	I/O	FUNCTION DESCRIPTION	PORT TYPE
NC	78		No connection	
RESET	80	I	System reset request input port. The reset pin must be held low for minimum of 5 internal clock cycles to guarantee recognition by the device. The device initialization requires 15 machine cycles.	
CE/INT1	79	I	Device selection Signal input port. External interrupt input port. This port can be used as a Chip Enable input. When activated, CPU resumes its operation from HALT mode	Schimitt-Trigger-IN

4. Architecture

The SD73C168 has a maximum memory address space of 64K bytes and only the Single-Chip moc
On-Chip memory spaces are configured as shown in Table 4.1.
In the sections that follow, the Register File (RF) and the Peripheral File (PF) are described along with three important registers in the CPU : the Stack Pointer (SP), the Status Register (ST), and the Program Counter (PC)

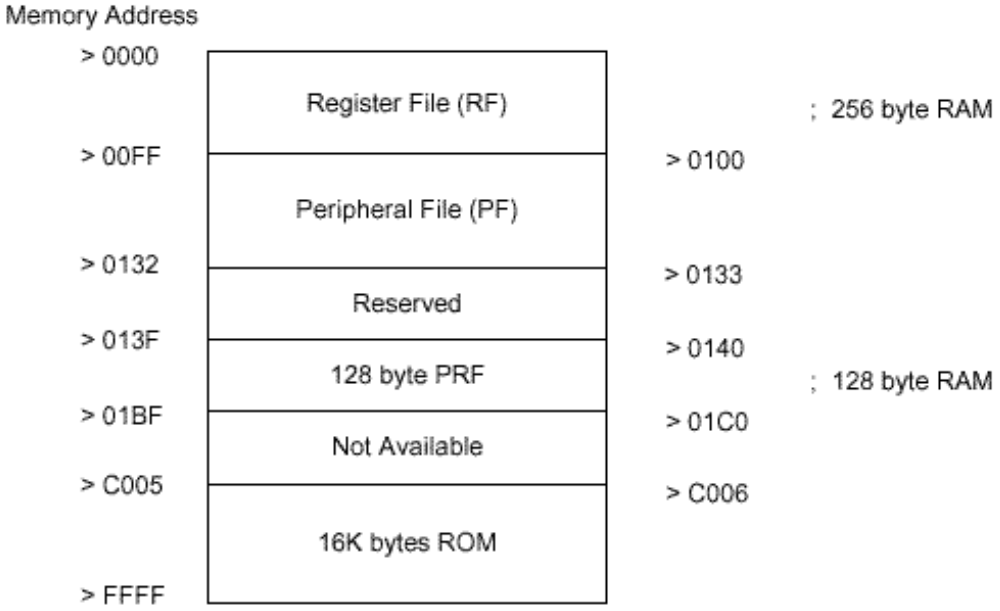


Table 4-1. SD73C168 Memory Map

4.1 Register File (RF)

The 256-byte on chip RAM resides in location >0000 to >00FF ('>' means hex) of the SD73C168's address space and is called the Register File (RF). The RAM is treated as registers by much of the instruction set and numbered R0-R255. The first two registers, R0 and R1, are also called the A and B registers respectively. Several instructions specify A or B as either the source or destination register ; e.g., STSP stores the contents of the Stack Pointer (SP) in the B register.
Except where stated otherwise, any register in the Register File can be addressed as an 8-bit source or destination register. The stack is also located in the Register File. Refer to section 4.3 for information regarding the initialization of the Stack Pointer (SP) and stack definition in the Register File.

4.2 Peripheral File (PF)

The Peripheral File (PF) resides in location >0100 to >0132 of the SD73C168's address space. Peripheral File locations are numbered P0-P50. The PF registers are used for interrupt control, parallel I/O, timer control, PLL, IF counter, BEEP, SIO and A/D converter control.

4.3 Peripheral RAM File (PRF)

The Peripheral RAM file (PRF) resides in location >0140 to >01BF of SD73C168's address space. PRF will act a role P64-P191. Useage is for additional RAM, but addressing method is same as Peripheral File's.

Memory address		
>0100	P0	
	:	Peripheral File
>0132	P50	
>0133	P51	
	:	Not Avail
>013F	P63	
>0140	P64	
	:	128 bytes PRF
>01BF	P191	
>01C0	P192	
	:	Not Avail
>01FF	P255	

Table 4.3 SD73C168 Peripheral File Map

4.4 Stack Pointer (SP)

The Stack Pointer(SP) is an 8-bit register in the CPU that is typically used to hold a pointer in RAM (the Register File). However, the SP can also be used as temporary data storage if a stack is not implemented, or if the SP contents are not needed. When a stack is implemented just before data is pushed onto the stack and automatically decremented immediately after data is poped from the stack. Upon assertion if the RESET function (see Section 4.7) >01 is loaded into the SP. The size of the stack can be changed from the 254-level stack at RESET to a smaller stack by executing a stack initialization program as illustrated in Figure 4.4. The This feature allows the stack to be located anywhere in the Register File. The SP is initialized through the B register (R1).

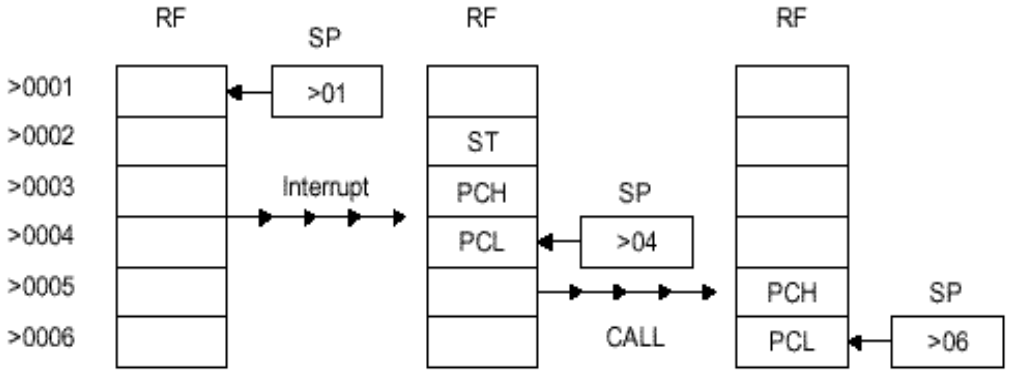
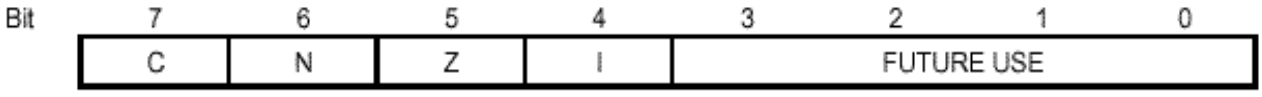


Figure 4.4 Example of Stack Initialization in the Register File

4.5 Status Register (ST)

The Status Register (ST) is an 8-bit register in the CPU that contains three conditional status bits ; Carry (C), Sign (N), Zero (Z), and a global Interrupt Enable bit (I) as shown in Figure 4-5.



C : CARRY OUT
N : SIGN
Z : ZERO
I : INTERRUPT ENABLE

Figure 4-5. Status Register (ST)

The C, N and Z bits are used mostly for arithmetic operations, bit rotating, and conditional branching. The Carry(C) bits is used as the carry-in and carry-out for most of lotate and arithmetic instructions. The Sign(N) bit contains the most significant bit of the destination operand contents after instruction execution. The Zero(Z) bit contains a one when all bits of the destination operand are equal to zero after instruction execution. The C, N and Z status bits also have jump-on-condition instructions associated them. The global Interrupt Enable (I) bit must be set to one by the EINT instruction in

order for any of the individual interrupts (INTn) to be recognized by the CPU. The Interrupt Enable (I) bit can cleared by DINT instruction of by executing a device RESET (see Section 4.7).

4.6 Program Counter (PC)

The SD73C168's 16-bit Program Counter (PC) consists of two 8-bit registers in the CPU which contain the MSB and the LSB respectively of a 16-bit address ; the Program Counter High (PCH) and Low (PCL). The PC acts as the 16-bit address pointer of the opcodes and operands in memory of the currently executing instruction. Upon assertion of the RESET function, the MSB and the LSB of the PC are loaded into the A and B registers of the Register File (see Section 4.7).

4.7 Peripheral File Map

The Peripheral File (PF) resides in locations >0100 to >01BF of the SD73C168's address space as shown in Table 4.7

Table 4.7 Peripheral File Map

REGISTER	ADDRESS	NAME	NOTE	FUNCTION	RESET VALUE
P0	>0100	IOCTL0	1	Interrupt 1,2 and 3 control register	00000000
P1	>0101	IOCTL1	1	Ext-INT 1,3 and 4 input edge select	0000x000
P2	>0102	IOCTL2	1	Interrupt 4,5,6,7 control register	00000000
P4	>0104	T1MSDATA	1	Timer 1 MSB reload register / MSB readout latch	xxxxxxxx
P5	>0105	T1LSDATA	1	Timer 1 LSB reload register / LSB decrementer value	xxxxxxxx
P6	>0106	T1CTL0	1	Timer 1 control register 0 / MSB readout latch	x0xxxxxx
P7	>0117	T1CTL1	1	Timer 1 control register 1 / LSB capture latch value	0x0xxxxx
P8	>0118	T2MSDATA	1	Timer 2 MSB reload register / MSB readout latch	xxxxxxxx
P9	>0109	T2LSDATA	1	Timer 2 LSB reload register / LSB decrementer value	xxxxxxxx
P10	>010A	T2CTL0	1	Timer 2 control register 0 / MSB readout latch	00xxxxxx
P11	>010B	T2CTL1	1	Timer 2 control register 1 / LSB capture latch value	0x0xxxxx
P13	>010D	APSLCT		A port select control register	00000000
P14	>010E	ADCTL	1	A/D converter control register	00xxxxx0
P15	>010F	ADDATA	1	A/D converter data value	00000000
P16	>0110	PLLCTL0		PLL control register 0	00000000

REGISTER	ADDRESS	NAME	NOTE	FUNCTION	RESET VALUE
P17	>0111	PLLCTL1	1	PLL control register 1	0xxx0000
P18	>0112	PLLDATAH		PLL program counter MSB data register	00000000
P19	>0113	PLLDATAL		PLL program counter LSB data register	00000000
P22	>0116	IFCCTL	1	IF counter data register	00000000
P23	>0117	IFCLSD	1	IF counter data register (LSB)	00000000
P24	>0118	IFCMSD	1	IF counter data register	00000000
P25	>0119	IFCHSD	1	IF counter data register (MSB)	xxxxxxx0
P27	>011B	SIO1CTL		SIO 1 control register	0000000x
P28	>011C	SIO1BUF		SIO 1 data register	xxxxxxxx
P29	>011D	SIO2CTL		SIO 2 control register	0000000x
P30	>011E	SIO2BUF		SIO 2 data register	xxxxxxxx
P32	>0120	ADATA		Port A data value	xxxxxxxx
P33	>0121	ADDR		Port A direction register	00000000
P34	>0122	BDATA		Port B data value	xxxxxxxx
P35	>0123	BDDR		Port B direction	00000000
P36	>0124	CDATA		Port C data value	xxxxxxxx
P37	>0125	CDDR		Port C direction register	00000000
P38	>0126	DDATA		Port D data value	xxxxxxxx
P39	>0127	DDDR		Port D direction register	00000000
P40	>0128	EDATA		Port E data value	xxxxxxxx
P41	>0129	EDDR		Port E direction register	00000000
P42	>012A	FDATA		Port F data value	xxxxxxxx
P43	>012B	FDDR		Port F direction register	00000000
P44	>012C	GDATA		Port G data value	xxxxxxxx
P45	>012D	GDDR		Port G direction register	00000000
P46	>012E	HDATA		Port H data value	xxxxxxxx
P47	>012F	HDDR		Port H direction register	00000000
P50	>0132	BEEP		BEEP control register	00000000
P64	>0140			Peripheral RAM	xxxxxxxx
:	:			128 bytes	
:	:				
P191	>01BF				xxxxxxxx

Notes 1 : Be careful when using logical instructions (e.g., ANDP, ORP, XORP) on these registers because of different read/write functions.

2 : 'x' means indeterminate

3 : P3, P12, P20, P21, P26,P31, P48, P49, P51-63 are not implemented.

4.7.1 Peripheral Files detail Description

1) I/O CONTROL REGISTERS

PF NAME : IOCTL0 : I/O CONTROL REGISTER 0

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P0	READ	NOT USED		INT3F	INT3E	INT2F	INT2E	INT1F	INT1E
>0100	WRITE			INT3C	INT3E	INT2C	INT2E	INT1C	INT1E
RESET VALUE		X	X	O	O	O	O	O	O

X = Indeterminate

Read : INTnF : 0 = INTn inactive
1 = INTn pending

Write : INTnE : 0 = INTn disable
1 = INTn enable
INTnC : 0 = No Effect
1 = Clear INTn flag

PF NAME : IOCTL1 : I/O CONTROL REGISTER 1

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P1	READ	INT41F	INT41E	INT40F	INT40E	NOT	INT40S	INT3S	INT1S
>0101	WRITE	INT41C	INT41E	INT40C	INT40E	USED	INT40S	INT3S	INT1S
RESET VALUE		O	O	O	O	X	O	O	O

X = Indeterminate
INT41 = INT4-1
INT40 = INT4-0

Read : INTnF : 0 = INTn inactive
1 = INTn pending
INTnS : 0 = Falling edge sensing
1 = Rising edgi sensing

Write : INTnE : 0 = INTn disable
1 = INTn enable
INTnC : 0 = No Effect
1 = Clear INTn flag

PF NAME : IOCTL2 : I/O CONTROL REGISTER 2

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P2	READ	INT7F	INT7E	INT6F	INT6E	INT5F	INT5E	INT4F	INT4E
>0102	WRITE	INT7C	INT7E	INT6C	INT6E	INT5C	INT5E	X	INT4E
RESET VALUE		O	O	O	O	O	O	O	O

Read : INTnF : 0 = INTn inactive
1 = INTn pending
This bit is automatically cleared
When CPU fetch its vector address.
<< INT4F is not automatically cleared
When CPU fetch vector address>>

Write : INTnE : 0 = INTn disable
1 = INTn enable
INTnC : 0 = No Effect
1 = Clear INTn flag

2) TIMER 1 & 2 CONTROL REGISTERS

PF NAME : T1MSDATA : TIMER 1 MS BYTE DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P4	READ	MSB READOUT LATCH							
>0104	WRITE	MSB READOUT LATCH							
RESET VALUE		X	X	X	X	X	X	X	X

PF NAME : T1LSDATA : TIMER 1 LS BYTE DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P5	READ	LSB DECREMENTER VALUE							
>0105	WRITE	LSB RELOAD REGISTER							
RESET VALUE		X	X	X	X	X	X	X	X

PF NAME : T1CTL0 : TIMER 1 CONTROL REGISTER 0

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P6	READ	MSB READOUT LATCH							
>0106	WRITE	X	T1OUT	X	X	X	X	X	X
RESET VALUE		X	O	X	X	X	X	X	X

T1OUT : Timer 1 toggle output enable bit.
This write bit determines PORT B0 is timer 1 toggle output pin or normal I/O pin.
0 = PORT B0 is normal I/O pin.
1 = PORT B0 is timer 1 toggle output in, and B0 is toggle when Timer 1 decrements through zero value.

PF NAME : T1CTL1 : TIMER 1 CONTROL REGISTER 1

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P7	READ	LSB CAPTURE LATCH							
>0107	WRITE	START1	SOURC1	T1HALT	PRESCALER RELOAD REGISTER (PL)				
RESET VALUE		O	X	O	X	X	X	X	X

Write : SOURC1 : 0 = Internal clock source Fosc/4
1 = External clock source from A4/ECI1
START1 : 0 = Timer 1 is stop, hold current count value and clear INT2 flag.
1 = Timer 1 reloads prescaler and decrementer, begins decrementing.
T1HALT : 0 = Timer 1 remains active when execute IDLE instruction. (WAKE-UP)
1 = Timer 1 will halt when execute IDLE instruction. (HALT)

PF NAME : T2MSDATA : TIMER 2 MS BYTE DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P8	READ	MSB READOUT LATCH							
>0108	WRITE	MSB READOUT REGISTER							
RESET VALUE		X	X	X	X	X	X	X	X

PF NAME : T2LSDATA : TIMER 2 LS BYTE DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P9	READ	LSB DECREMENTER VALUE							
>0109	WRITE	LSB RELOAD REGISTER							
RESET VALUE		X	X	X	X	X	X	X	X

PF NAME : T2CTL0 : TIMER 2 CONTROL REGISTER 0

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P10	READ	MSB READOUT LATCH							
>010A	WRITE	CASCADE	T2OUT	X	X	X	X	X	X
RESET VALUE		O	O	X	X	X	X	X	X

T2OUT : Timer 2 toggle output enable bit.
This write bit determines PORT B1 is timer 2 toggle output pin or normal I/O pin.
0 = PORT B1 is normal I/O pin.
1 = PORT B1 is timer 1 toggle output pin, and B1 is toggle when Timer 2 decrements through zero value.

CASCADE : Timer 2 cascade control bit
0 = Timer 2 is not cascaded with Timer 1, Timer 2 clock is determined by source bit.
1 = Timer 1 and 2 are cascaded, clock source is generated by Timer 1 reload pulse, overrides source bit.

PF NAME : T2CTL1 : TIMER 2 CONTROL REGISTER 1

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P11	READ	LSB CAPTURE LATCH							
>010B	WRITE	START2	SOURC2	T2HALT	PRESCALER RELOAD REGISTER (PL)				
RESET VALUE		O	X	O	X	X	X	X	X

Write : SOURC2 : 0 = Internal clock source Fosc/4
1 = External clock source from A5/ECI2
START2 : 0 = Timer 2 is stop, hold current count value and clear INT6 flag.
1 = Timer 2 reloads prescaler and decrementer, begins decrementing.
T2HALT : 0 = Timer 2 remains active when execute IDLE instruction. (WAKE-UP)
1 = Timer 2 will halt when execute IDLE instruction. (HALT)

3) A/D CONVERTER REGISTERS

PF NAME : APSLCT : PORT A SELECT CONTROL REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P13	READ	INT3SEL	INT40SEL	NOT USED		AD2SEL	AD1SEL	AMIFSEL	FMIFSEL
>010C	WRITE	INT3SEL	INT40SEL	NOT USED		AD2SEL	AD1SEL	AMIFSEL	FMIFSEL
RESET VALUE		O	O	O	O	O	O	O	O

FMIFSEL
AMIFSEL : FM and AM IF input enable bits. This read/write bits disable digital inputs when FM and AM IF inputs are enabled.
0 = PORT A0 and A1 are normal I/O pins.
1 = PORT A0 and A1 are disabled.

AD1SEL
AD2SEL : A/D converter input enable bits. This read/write bits disable digital inputs when A/D converter inputs when A/D converter inputs are enabled.
0 = PORT A2 and A3 are normal I/O pins.
1 = PORT A2 and A3 are disabled.

INT40SEL
INT3SEL : External interrupt 3 and 4-0 input enable bits. This read/write disable Digital inputs when A/D converter inputs are enabled.
0 = PORT A7 and A6 are normal I/O pins.
1 = PORT A7 and A6 are disabled

PF NAME : ADCTL : A/D CONTROL REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P14	READ	READY	START	NOT USED					ADCHS
>010E	WRITE	READYC	START	NOT USED					ADCHS
RESET VALUE		O	O	X	X	X	X	X	O

READ :

READY : 0 = No Operation or Incomplete Conversion
1 = Complete Conversion

WRITE

ADCHS : 0 = A/D Converter Input Channel is PORT A2
1 = A/D Converter Input Channel is PORT A3

START : 0 = Conversion Stop
1 = Conversion Start

READYC : 0 = Ineffect
1 = Clear Ready Flag

PF NAME : ADDATA : A/D CONVERTER DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P15	READ	CONVERSION DATA REGISTER							
>010F	WRITE	NOT USED (INVALID)							
RESET VALUE		O	O	O	O	O	O	O	O

4) PLL (PHASE LOCKED LOOP) REGISTER

PF NAME : PLLCTL0 : PLL CONTROL REGISTER 0

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P16	READ	NOT USED							
>0110	WRITE	INSL1	INSL0	REF2	REF1	REF0	DTM2	DTM1	DTM0
RESET VALUE		O	O	O	O	O	O	O	O

WRITE :

PHASE DETECT TIME SELECT

DTM2	DTM1	DTM0	DETECT TIME
0	0	0	0.44 us
0	0	1	0.55 us
0	1	0	0.66 us
0	1	1	0.77 us
1	0	0	0.88 us
1	0	1	1.00 us
1	1	0	1.11 us
1	1	1	1.22 us

PHASE DETECT TIME SELECT

REF2	REF1	REF0	REF. FREQ
0	0	0	1.0 KHz
0	0	1	5.0 KHz
0	1	0	6.25 KHz
0	1	1	9.0 KHz
1	0	0	10.0 KHz
1	0	1	12.5 KHz
1	1	0	25.0 KHz
1	1	1	50.0 KHz

MODE SELECT

INSL1	INSL0	INPUT MODE
0	0	NOT USED
0	1	AM DIRECT
1	0	AM SWALLOW
1	1	FM SWALLOW

PF NAME : PLLCTL1 : PLL START/STOP CONTROL REGISTER 1

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P17	READ	READY	X	X	X	REFTST	PLLTST	UL1	UL0
>0111	WRITE	PLLEN	X	X	X	REFTST	PLLTST	NOT USED	
RESET VALUE		O	X	X	X	O	O	O	O

READ :

PLL UNLOCK STATUS DETECT :

UL1	UL0	STATUS
0	0	PLL LOCK/STOP/OFF
0	1	REF FREQ > VCO FREQ
1	0	REF FREQ < VCO FREQ
1	1	NOT USED

READY : 0 = NO OPERATION
1 = ACTIVE

WRITE :

PLLTST : PLL TEST BIT (ATTENTION : SHOULD BE SET "0" IN NORMAL OPERATION)
0 = ACTIVE NORMAL
1 = TEST MODE

REFTST : REFERENCE DIVIDER TEST BIT(SHOULD BE SET "0" IN NORMAL OPERATION)
0 = ACTIVE NORMAL OPERATION
1 = REFERENCE TEST MODE

PLLEN : 0 = PLL OFF, PLL STOP
1 = PLL ON, PLL START

PF NAME : PLLDATAH : PLL PC MSB DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P18 >0112	READ / WRITE	PLL PC MSB DATA							
RESET VALUE		O	O	O	O	O	O	O	O

PF NAME : PLLDATAL : PLL PC LSB DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P19 >0113	READ / WRITE	PLL PC LSB DATA				SWALLOW COUNTER VALUE			
RESET VALUE		O	O	O	O	O	O	O	O

5) IF COUNTER REGISTER

PF NAME : IFCCTL : IF CONTROL REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P22	READ	READY	FMIF	AMIF	TSTIF	TP3	TP2	TP1	TP0
>0116	WRITE	START							
RESET VALUE		O	O	O	O	O	O	O	O

READ :

READY : 0 = INACTIVE OR COMPLETE COUNTER
1 = INCOMPLETE OR ACTIVE COUNTER

WRITE :

IF FREQ. COUNTING PERIOD SELECT (TP0, TP1, TP2, TP3)

TP3	TP2	TP1	TP0	COUNT TIME
0	0	0	0	X
0	0	0	1	1 ms
0	0	1	0	2 ms
0	0	1	1	3 ms
0	1	0	0	4 ms
0	1	0	1	5 ms
0	1	1	0	6 ms
0	1	1	1	7 ms
1	0	0	0	8 ms
1	0	0	1	9 ms
1	0	1	0	10 ms
1	0	1	1	11 ms
1	1	0	0	12 ms
1	1	0	1	13 ms
1	1	1	0	14 ms
1	1	1	1	15 ms

TSTIF : IF COUNTER TEST BIT
(ATTENTION : SHOULD BE SET TO "0" IN NORMAL OPERATION)
0 = NORMAL ACTIVE MODE
1 = TEST MODE

AMIF, FMIF : IF COUNTER INPUT SELECT

FMIF	AMIF	COUNTING INPUT
0	0	NOT INPUT
0	1	AMIF
1	0	FMIF
1	1	X

START : IF COUNTER START/STOP
0 = STOP (DISABLE)
1 = START (ENABLE)

PF NAME : IFCLSD : IF COUNTER LSB VALUE

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P23 >0117	READ	IF COUNTER LSB VALUE							
RESET VALUE		O	O	O	O	O	O	O	O

IF Counter LSB data bits
This read bits are LSB 8 bits of 17 bits IF Counter.

PF NAME : IFCMSD : IF COUNTER VALUE

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P24 >0118	READ	IF COUNTER MSB-1 VALUE							
RESET VALUE		O	O	O	O	O	O	O	O

IF Counter MSB data bits
This read bits are MSB 8 bits (from bit-15 to bit-8) of 17 bits IF Counter.

PF NAME : IFCHSD : IF COUNTER MSB VALUE

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P25 >0119	READ	NOT USED							IFD16
RESET VALUE		X	X	X	X	X	X	X	O

IF Counter MSB data bits
This read bits are MSB 1 bits (bit-16) of 17 bits IF Counter.

6) SERIAL I/O REGISTERS

PF NAME : SIO1CTL : SERIAL I/O 1 CONTROL REGISTEI

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P27	READ	SIO1AF	CKSRC1	BAU11	BAU10	SIO1EF	SCLK1E	SO1ENA	X
>011B	WRITE	SIO1ST	CKSRC1			SIO1EC	SCLK1E	SO1ENA	X
RESET VALUE		O	O	O	O	O	O	O	X

SIO1AF : SIO1 operation flag bit.
This read bit determines SIO1 is enabled or not.
0 = SIO1 is stop state
1 = SIO1 is processing state

SIO1ST : SIO1 start enable bit
This write bit determines SIO1 is start or not.
0 = SIO1 is stop
1 = SIO1 is started
* Caution : This bit should be reset to "0" before 8bit transmition for proper SI operation.

CKSRC1 : SIO1 clock source selection bit
This read/write bit determines SIO1 clock source in from external or internal.
0 = SIO1 clock is from internal
1 = SIO1 clock is from external

BAU1n : SIO1 transmission speed select bits.
This read/write bits determine SIO1 transmission speed.

BAU11	BAU10	SCLK FREQ. (Fosc = 4.5MKHz)		
0	0	Fosc/8	=	563 KHz
0	1	Fosc/16	=	281 KHz
1	0	Fosc/32	=	141 KHz
1	1	Fosc/64	=	70 KHz

SIO1EF : Transmission error flag bit
This read bit shows overrun error was occured or not
0 = Overrun error is not occured
1 = Overrun error is occured

SIO1EC : Transmission error flag clear bit
This write bit determines transmission error flag is cleared or not
0 = Transmission error flag is not affected
1 = Transmission error flag is cleared

SCLK1E : SIO1 clock enable bit
This read/write bit determines PORT E2 bit is SIO1 clock output pin or not
0 = PORT E2 is normal I/O port
1 = PORT E2 is assigned SIO1 clock output pin when "CKSRC1" is set.
(Then, PORT E2 direction should be output)

SO1ENA : Serial output enable bit
This read/write bit determines PORT E0 is SO1 pin or not
0 = PORT E0 is normal I/O port
1 = PORT E0 is assigned SO1 pin (Then, PORT E0 direction should be output state)

PF NAME : SIO1BUF : SERIAL I/O 1 DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P28	READ	SIO1 RECEIVING DATA							
>011C	WRITE	SIO1 TRANSMITTING DATA							
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : SIO2CTL : SERIAL I/O 2 CONTROL REGISTEI

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P29	READ	SIO2AF	CKSRC2	BAU21	BAU20	SIO2EF	SCLK2E	SO2ENA	X
>011D	WRITE	SIO2ST	CKSRC2			SIO2EC	SCLK2E	SO2ENA	X
RESET VALUE		O	O	O	O	O	O	O	X

SIO2AF : SIO2 Operation flag bit.
This read bit determines SIO2 is enabled or not.
0 = SIO2 is stop state
1 = SIO2 is processing state

SIO2ST : SIO2 start enable bit.
This write bit determines SIO2 is start or not
0 = SIO2 is stop
1 = SIO2 is start
* Caution : This bit should be reset to "0" before 8bit transmition for proper SI
operation.

CKSRC2 : SIO2 clock source selection bit
This read/write bit determines SIO2 clock source in from external or internal
0 = SIO2 clock is from internal
1 = SIO2 clock is from external

BAU2n : SIO2 transmission speed select bits.
This read/write bits determine SIO2 transmission speed.

BAU21	BAU20	SCLK FREQ. (Fosc=4.5KHz)		
0	0	Fosc/8	=	563 KHz
0	1	Fosc/16	=	281 KHz
1	0	Fosc/32	=	141 KHz
1	1	Fosc/64	=	70 KHz

SIO2EF : Transmission error flag bit
This read bit shows overrun error was occured or not
0 = Overrun error is not occured
1 = Overrun error is occured

SIO2EC : Transmission error flag clear bit
This write bit determines transmission error flag is cleared or not.
0 = Transmission error flag is not affected
1 = Transmission error flag is cleared

SCLK2E : SIO2 clock enable bit
This read/write bit determines PORT E5 bit is SIO2 clock output pin or not
0 = PORT E5 is normal I/O port
1 = PORT E5 is assigned SIO2 clock output pin when "CKSRC2" is set.
(Then, PORT E5 direction should be output)

SO2ENA : Serial output enable bit
This read/write bit determines PORT E3 is SO2 pin or not
0 = PORT E3 is normal I/O port
1 = PORT E3 is assigned SO2 pin (Then, PORT E3 direction should be output state)

PF NAME : SIO2BUF : SERIAL I/O 2 DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P30	READ	SIO2 RECEIVING DATA							
>011E	WRITE	SIO2 TRANSMITTING DATA							
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

7) PORT DATA / DIRECTION REGISTER

PF NAME : ADATA : PORT A DATA REGISTEF

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P32	READ	PORT A DATA VALUE							
>0120	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : ADDR : PORT A DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P33	READ	NOT USED							
>0121	WRITE	PORT A DIRECTION REGISTER							
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT A INPUT MODE 1 : PORT A OUTPUT MODE

PF NAME : BDATA : SERIAL I/O 1 DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P34	READ	PORT B DATA VALUE							
>0122	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : BDDR : PORT B DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P35	READ	NOT USED							
>0123	WRITE	PORT B DIRECTION REGISTER							
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT B INPUT MODE 1 : PORT B OUTPUT MODE

PF NAME : CDATA : PORT C DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P36	READ	PORT C DATA VALUE							
>0124	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : CDDR : PORT C DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P37	READ	NOT USED							
>0125	WRITE	PORT C DIRECTION REGISTER							
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT C INPUT MODE 1 : PORT C OUTPUT MODE

PF NAME : DDATA : PORT D DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P38	READ	PORT D DATA VALUE							
>0126	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : DDDR : PORT D DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P39	READ	PORT D DIRECTION REGISTER							
>0127	WRITE								
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT D INPUT MODE 1 : PORT D OUTPUT MODE

PF NAME : EDATA : PORT E DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P40	READ	PORT E DATA VALUE							
>0128	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : EDDR : PORT E DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P41	READ	PORT E DIRECTION REGISTER							
>0129	WRITE								
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT E INPUT MODE 1 : PORT E OUTPUT MODE

PF NAME : FDATA : PORT F DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P42	READ	PORT F DATA VALUE							
>012A	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : FDDR : PORT F DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P43	READ	PORT F DIRECTION REGISTER							
>012B	WRITE								
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT F INPUT MODE 1 : PORT F OUTPUT MODE

PF NAME : GDATA : PORT G DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P44	READ	PORT G DATA VALUE							
>012C	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : GDDR : PORT G DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P45	READ	PORT G DIRECTION REGISTER							
>012D	WRITE								
RESET VALUE		O	O	O	O	O	O	O	O

0 : PORT G INPUT MODE 1 : PORT G OUTPUT MODE

PF NAME : HDATA : PORT H DATA REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P46	READ	PORT H DATA VALUE							
>012E	WRITE								
RESET VALUE		X	X	X	X	X	X	X	X

X : INDETERMINATOR

PF NAME : HDDR : PORT H DIRECTION REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P47	READ	PORT H DIRECTION REGISTER							
>012F	WRITE								
RESET VALUE		O	O	O	O	O	O	O	O

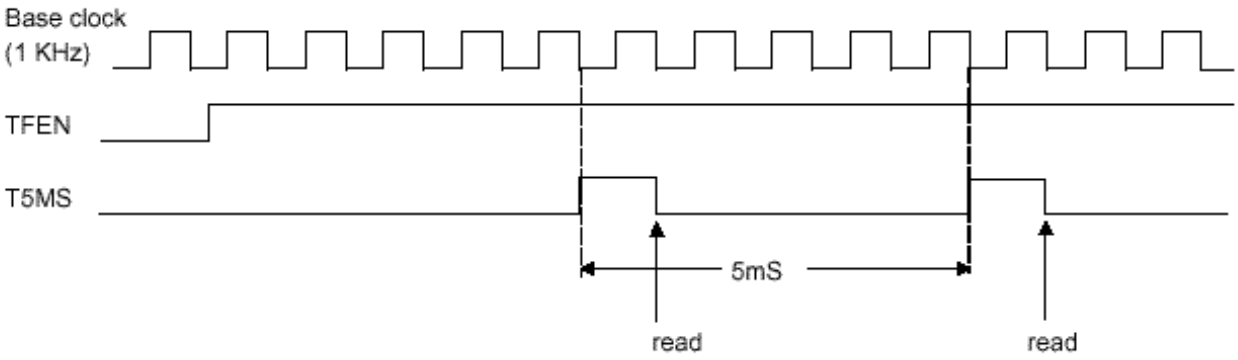
0 : PORT H INPUT MODE 1 : PORT H OUTPUT MODE

8) BEEP REGISTER

PF NAME : BEEP : BEEP CONTROL REGISTER

	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P50	READ	T250MS	T125MS	T100MS	T5MS	TFEN	BPEN	FSEL1	FSEL0
>0132	WRITE	NOT USED		WTSL1	WTSLO	TFEN			
RESET VALUE		O	O	O	O	O	O	O	O

** CAUTION 1 "TFEN" bit must be set "1" before HALT mode.



T250MS, T125MS, T100MS, T5MS : Interval timer flag bit

This read bits is set by warm-up timer after 250ms, 125ms, 100ms, and 5ms respectively after "TFEN" bit is set.
These flags are cleared by read operations.

WTSLn : Warm-up time select bits

WTSL1	WSTL0	WARM-UP TIME
0	0	25 ms
0	1	50 ms
1	0	100 ms
1	1	NO USE

TFEN : Warm-up timer enable bit.
This read/write bit determines warm-up timer is enabled or not
0 = Warm-up timer is disabled.
1 = Warm-up timer is enabled.

BPEN : 0 = Beep out disable
1 = Beep out enable

FSELn : BEEP Frequency select :

FSEL1	FSEL0	BEEP FREQ.
0	0	417Hz (2/3 Duty)
0	1	1KHz (1/2 Duty)
1	0	1.25 KHz (1/2 Duty)
1	1	2.5 KHz (1/2 Duty)

9) Peripheral RAM register

PF NAME : PRAM 0-127 : Peripheral RAM register

P64-P191	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
>140 ~	READ	Peripheral RAM register							
>01BF	WRITE	Peripheral RAM register							
RESET VALUE		X	X	X	X	X	X	X	X

These peripheral RAM region is >140 (hex) to >01BF (hex), and size is 128 bytes.

4.8 Interrupt and Reset Priorities

The SD73C168 has priority servicing of interrupt levels and RESET. These levels are defined as shown in Table 4-8. The TRAP instruction branch to a two bytes location in a reserved section of memory called the TRAP Vector Table. As shown in Figure 4-8, each trap location stores a 16-bit address which references either reset function (TRAP0), one of the seven interrupt service routine (TRAP1-INT1, TRAP2-INT2, TRAP3-INT3, TRAP4-INT4, TRAP5-INT5, TRAP6-INT6, TRAP7-INT7) or a subroutine (TRAP8-23).

Once INTn has been acknowledged by the CPU, the corresponding INTn Flag flip flop is cleared. The CPU then pushes the contents of the Status Register and Program Counter (MSB and LSB) onto the stack and zeros the Status Register, including the global Interrupt Enable (I) bit. the CPU reads an interrupt code from the interrupt logic and branches to the address contained in the corresponding interrupt vector location in memory.

The interrupt service routine can explicitly enable nested interrupt by executing the EINT instruction to directly set I bit in the Status Register to a one, thus permitting nested interrupt to be recognized. When the nested interrupt service routine completes, it returns to the previous interrupt service routine by executing the RETI instruction.

Level	Name	Trigger Factor	Vector	
			MSB	LSB
0	RESET	Active Low/Level Sensitive	>FFFE	>FFFF
1	INT1 External (CE)	Program Selectable	>FFFC	>FFFD
2	INT2 Timer 1	Timer 1 through '>0000'	>FFFA	>FFFB
3	INT3 External	Program Selectable	>FFF8	>FFF9
4-0	INT4 External	Program Selectable	>FFF6	>FFF7

Level	Name	Trigger Factor	Vector	
			MSB	LSB
4-1	INT4 A/D Converter	End of A/D Conversion		
5	INT5 SI/O 1	End of SI/O 1 Frame	>FFF4	>FFF5
6	INT6 Timer 2	Timer 2 through ">0000"	>FFF2	>FFF3
7	INT7 SI/O 2	End of SI/O 2 Frame	>FFF0	>FFF1

Table 4-8. Interrupt and Reset Priorities

ADDRESS	
>FFD0	TRAP23 (A8 - A15)
>FFD1	TRAP23 (A0 - A7)
/	/
/	/
/	/
>FFF0	SI/O2 OR TRAP7 (A8-A15)
>FFF1	SI/O2 OR TRAP7 (A0-A7)
>FFF2	TIMER2 OR TRAP6 (A8-A15)
>FFF3	TIMER2 OR TRAP6 (A0-A7)
>FFF4	SI/O1 OR TRAP5 (A8-A15)
>FFF5	SI/O1 OR TRAP5 (A0-A7)

ADDRESS	
>FFF6	INT4, A/D OR TRAP4 (A8-A15)
>FFF7	INT4, A/D OR TRAP4 (A0-A7)
>FFF8	INT3 OR TRAP3 (A8-A15)
>FFF9	INT3 OR TRAP3 (A0-A7)
>FFFA	TIMER1 OR TRAP2 (A8-A15)
>FFFB	TIMER1 OR TRAP2 (A0-A7)
>FFFC	INT1 OR TRAP1 (A8-A15)
>FFFD	INT1 OR TRAP1 (A0-A7)
>FFFE	RESET OR TRAP0 (A8-A15)
>FFFF	RESET OR TRAP0 (A0-A7)

Figure 4-8. The TRAP Vector Table

5. Description of Each Function

5.1 Input / Output Ports

SD73C168 has 64 I/O pins organized as eight parallel ports labeled Port A,B,C,D,E,F,G,H each Port is mapped 8 bit data value register in the Peripheral File (PF). The data value registers are usually called APORT, BPORT, CPORT, DPORT, EPORT, FPORT, GPORT and HPORT in a program.
All Ports are implemented as bidirectional I/O Ports.
Each Bidirecitional ports has a corresponding 8 bit Data Direction Register (DDR) that programs each ports as input or output. A bit set to one in the DDR will cause the corresponding pin to be an output, while a zero in the DDR will cause the pin to be a high impedance input.
Upon RESET, the DDR file-flop register are set to zero by the on-chip circuitly, forcing them to become inputs. And output data register ports (A,B,C,D,E,F,G and H) are indeterminate data set. After RESET, if '1' s are written to the DDR register sometime before the output data register is changed then the corresponding I/O pins will output a "1". For this reason, it is good practice that ports A,B,C,D,E,F,G,H output data register is loaded with the desired value before any bits are configured as outputs.
The logic for each bidirectional I/O line is shown in Figure 5-1.

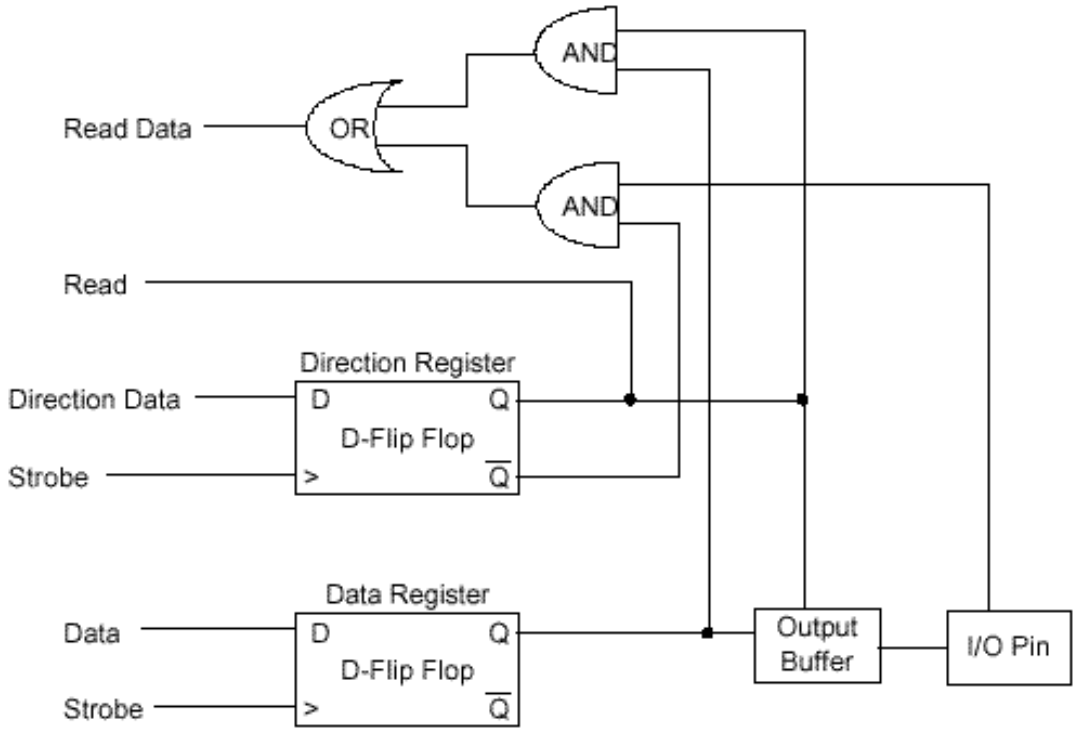


Figure 5-1. Bidirectional I/O Logic

Port Port A is an 8-bit bidirectional I/O port where any of its eight pins may be individually programmed as an input or output under software control. Reading port A data register (P32) returns either the current value at the pin (input mode) or the current value of port A data register (output mode). And also port A can be used as A/D converter AM and FM IF input.

Port Port B is an 8-bit bidirectional I/O port where any of its eight pins may be individually programmed as an input or output under software control. Reading port A data register (P34) returns either the current value at the pin (input mode) or the current value of port B data register (output mode). And also port B can be used as Timer output ports.

Port C,D,F,G,H : Port C,D,F,G,H is an 8-bit bidirectional I/O port where any of its eight pins may be individually programmed as an input or output under software control. Reading port C,D,F,G,H data register (P36, P38, P42, P44, P46) returns either the current value at the pin (input mode) or the current value of port C,D,F,G,H data register (output mode).

Port Port E is an 8-bit bidirectional I/O port where any of its eight pins may be individually programmed as an input or output under software control. Reading port E data register (P40) returns either the current value at the pin (input mode) or the current value of port E data register (output mode). And also port E can be used as SI/O data and clock inputs or outputs and BEEP output port.

5.2 Device Initialization

Interrupt level 0 (RESET) cannot be masked and will be recognized immediately even in the middle of instruction. To execute the level 0 interrupt, the RESET pin must be held low for minimum of 5 internal clock cycles to guarantee recognition by the device. During assertion of the RESET pin, the following operations are performed prior to the first instruction acquisition.

1) All zeros are written to the IOCTL0 Register and Status Register. And zero is written to the IOCTL1, and IOCTL2. This disables all interrupt and clears all interrupt flags.
2) The initialize data are written to the Peripheral Registers. And all zeros are written to the APSLCT, ADDR, BDDR, CDDR, DDDR, EDDR, FDDR, GDDR and HDDR.
3) The MSB and LSB values of the Program Counter Just before RESET are stored in R0 and R1 (A and B Register) respectively.
4) The Stack Pointer is initialized to >01.
5) The MSB and LSB of the Reset Vector are fetched location >FFFE and >FFFF respectively (see Table 4-8) and loaded into the Program Counter.
6) Program execute begins from the address placed in the Program Counter.

5.3 I/O Control Register

The I/O control register are located in the Peripheral File and are responsible for interrupt control. The SD73C168 contains the I/O Control 0 (IOCTL0), I/O Control 1 (IOCTL1), I/O Control 2 (IOCTL2). The I/O control register are mapped into locations P0 (IOCTL0), P1 (IOCTL1), P2 (IOCTL2) of the Peripheral File as shown in Figure 5-3A, 5-3B and 5-3C. The individual interrupt mask and resets are controlled through these registers. The interrupt sources may also be individually tested by reading the interrupt flags. The interrupt flag values are independent of the interrupt enable values. The INTn FLAG values are independent of the INTn ENABLE values. Writing a '1' to the INTn CLEAR bit will clear the corresponding INTn FLAG, but writing a '0' to the INTn CLEAR bit has no effect on the bit. If INTn is to be recognized by the CPU, three conditions must be met as follow.

1) A one must be written to the INTn ENABLE BIT IN THE IOCTL0, IOCTL1 or IOCTL2 Register.
2) The global INTERRUPT ENABLE bit, IE., bit4 in the Status Register, must be set to one by the EINT instruction.
3) INTn must be the highest priority interrupt asserted within an instruction boundary.

Setting '1' to both INTnFLAG and INTnENABLE bit clears the INTnFLAG first, and then sets '1' to INTnENABLE bit.

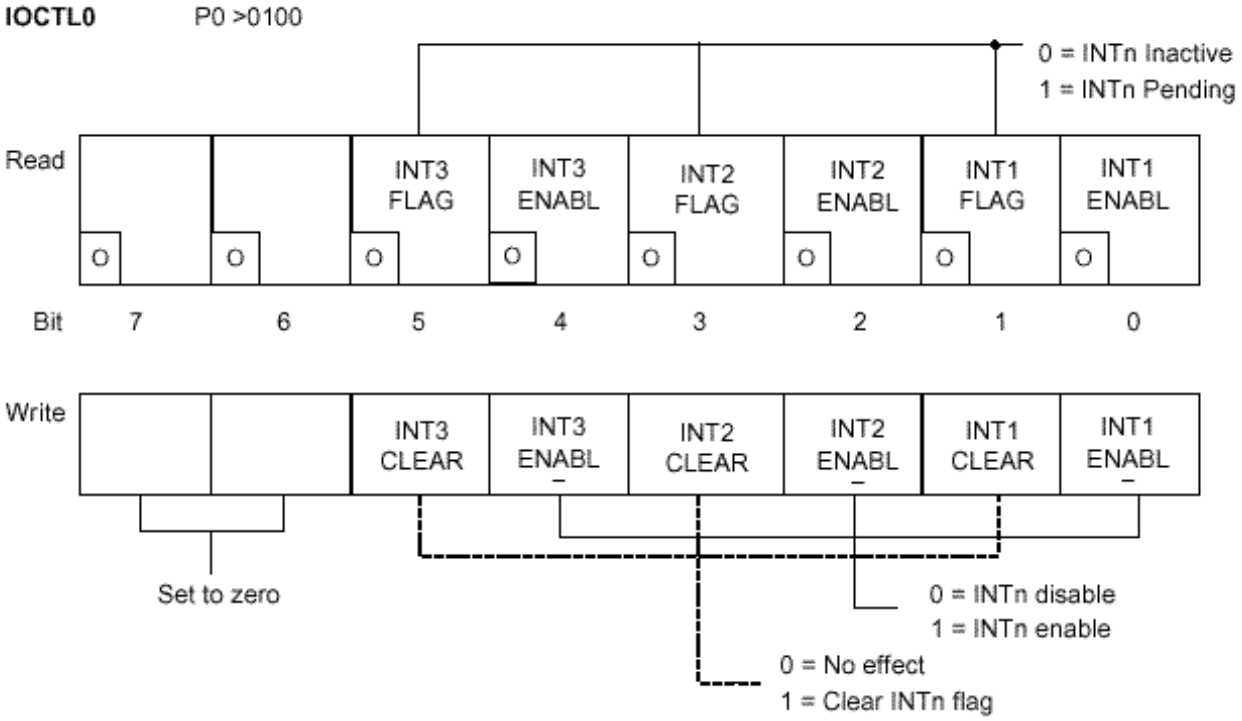
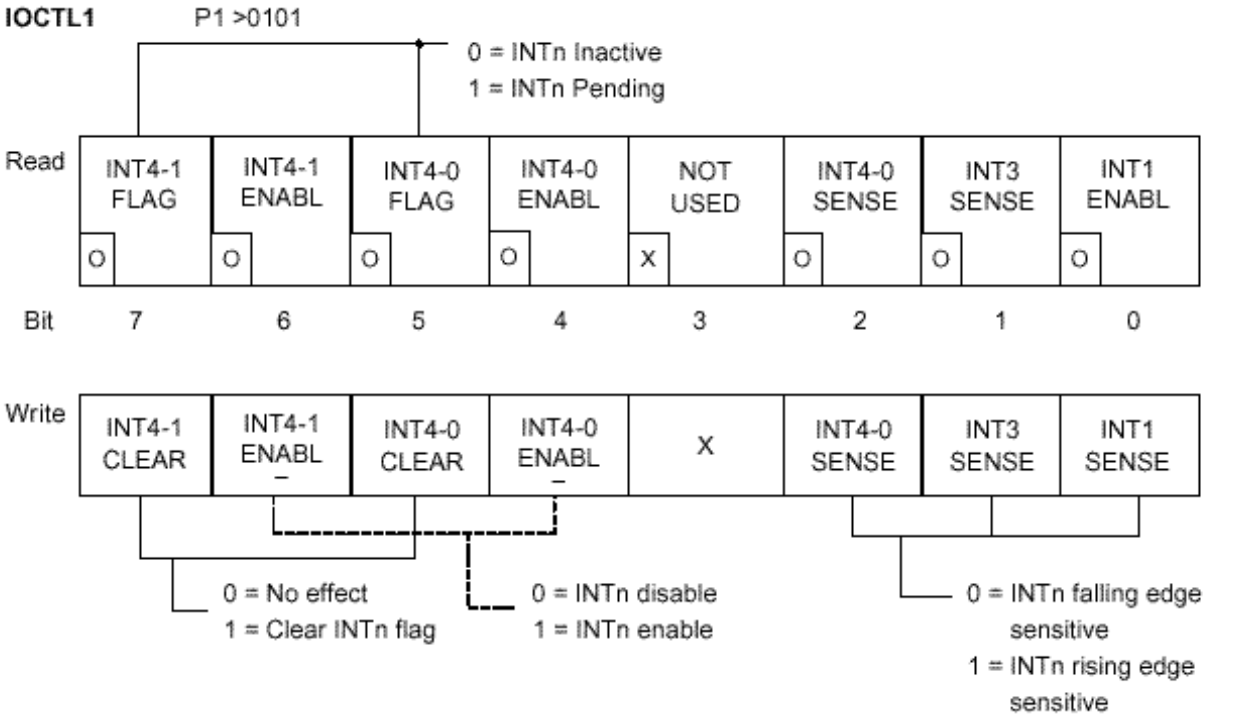


Figure 5-3A I/O Control Register 0 (IOCTL0)



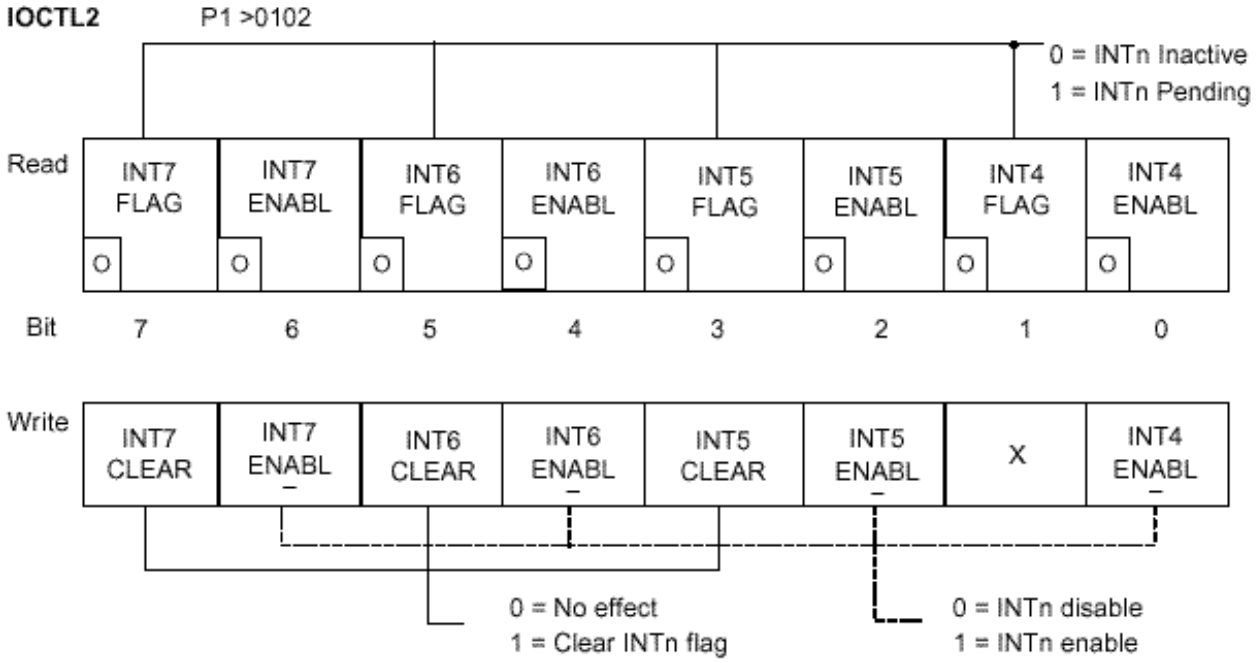


Figure 5-3C I/O Control Register 2 (IOCTL2)

5.4 Interrupt Logic and External Interrupt

The internal interrupt logic for each eight maskable interrupt of SD73C168 is shown in Figure 5-4A-1, 54A-2. This interrupt logic will detect the output of each corresponding interrupt and latch the interrupt Flag.

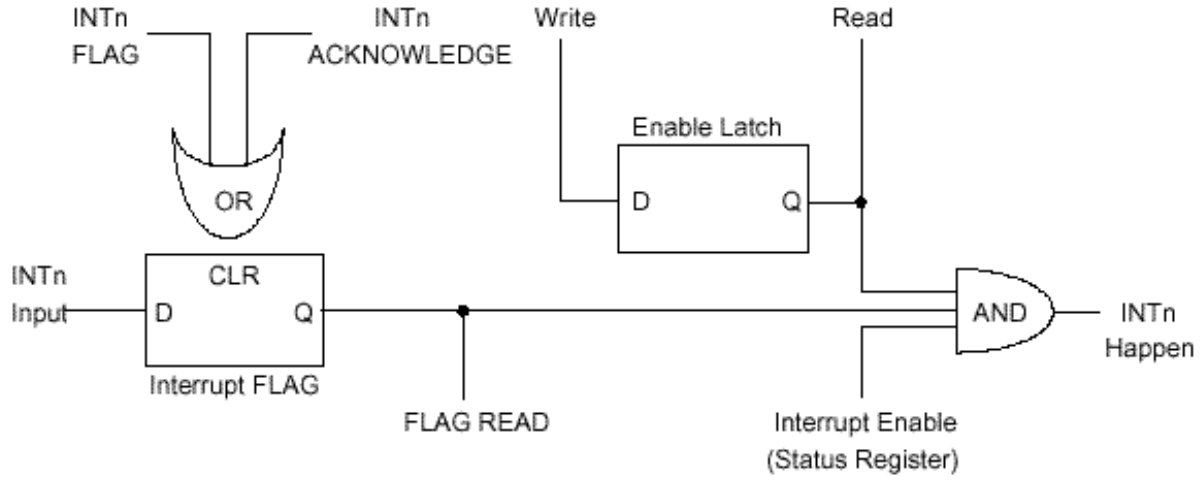


Figure 5-4A-1. Interrupt Logic

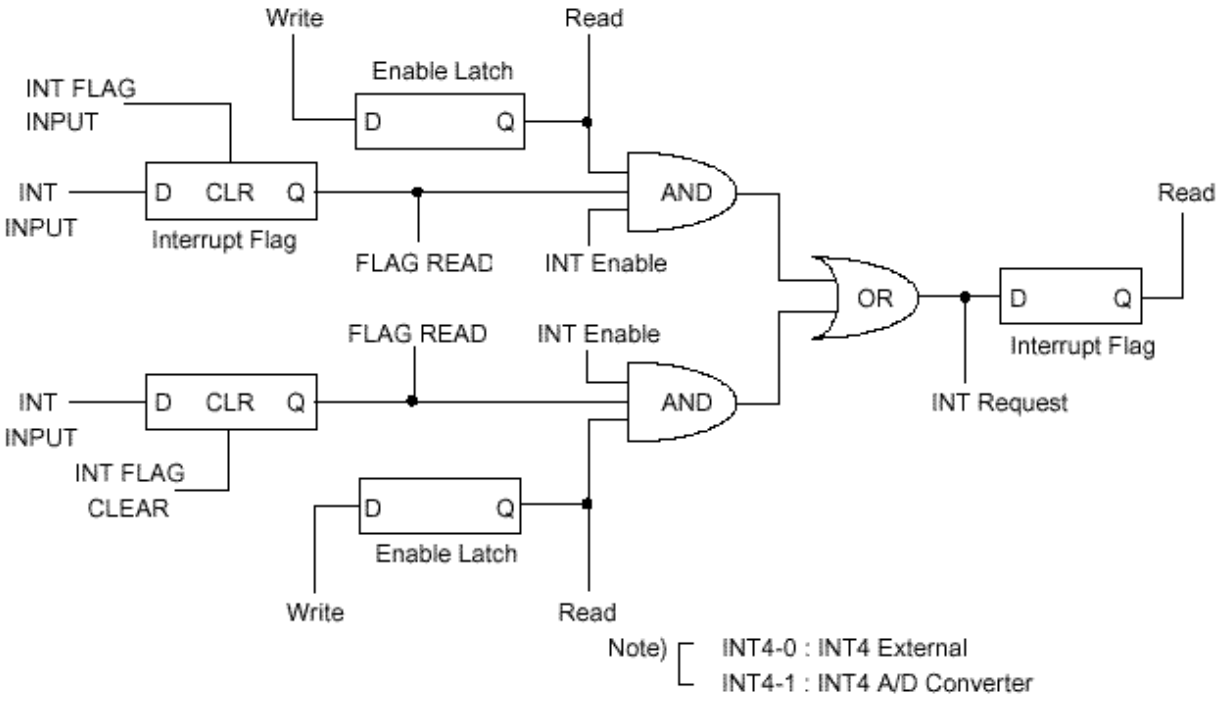


Figure 5-4A-2. Interrupt 4 Logic

To even further conserve the already low power requirement, two low power modes are provided. These modes are called Halt and Wake up and entered by executing a IDLE instruction. Either an external interrupt or the timer interrupt will release the device from the low power depending on whether it is in the Halt or Wake-up mode. See Section 5.12 for a complete description of the modes and interrupts.
When an external interrupt is first asserted, its level is gated into interrupt Flag. In order for an interrupt signal to be detected the signal width must be a minimum of 5 internal clock cycles. The interrupt Flag will be set to '1'. If INTn is removed before the interrupt is recognized, its occurrence is latched in by the INTn Enable Flag. The INTn Enable bit is used separately to individually mask the interrupt levels. This bit must be 1 before the interrupt to be recognized.
As previously stated, all interrupt control bits are implemented in the IOCTL0, IOCTL1 and IOCTL2 registers in the Peripheral File. I/O instructions may simply read from and write to each INTn Enable bit. By the INTn input, the interrupt Flag is set to one at falling edge and become active through interrupt is enabled. The interrupt service routine is executed after the currently executing instruction is completed. the value of the Status Register and Program Counter (MSB and LSB) respectively moves onto the stack and zeros the Status Register (see Section 4.3). The corresponding vector address is loaded into the Program Counter and interrupt service routine is executed. The corresponding interrupt Flag is automatically cleared. (But INT4F, INT40F, INT41F flags are not automatically cleared, because they used same interrupt vector address. These flags are cleared by only program.)
The External interrupts, INT1, INT3 and INT4-0 have schmitt Trigger inputs and can be used as zero-cross detector.
The following attention have to be paid due to using both as the External interrupt pins and general purpose I/O pins.

1) The port (A7/INT3, A6/INT4) used as the interrupt input should be input mode. The output mode may cause to damage the device. If the content of the corresponding output port is changed '1' to'0', the interrupt flag will also set to '1'.

2) If not used as the interrupt input, the corresponding Interrupt enable should be disabled, but even if this interrupt Enable being disabled, the Interrupt Flag will be changed.

The External interrupt timing is shown in Figure 5-4B. And it needs an biditional circuitry when INT1, INT3, INT4-0 are used as zero cross detector as shown in Figure 5-4C and the following conditions are to be satisfied.

1) The External interrupt level should be range from VDD+0.3V to VSS, and it is necessary for input current not to exceed the specification.

2) The noise on interrupt signal should be minimized because the noise debounce logic is not implemented on chip. So the function may be failed due to the continuous interrupt.

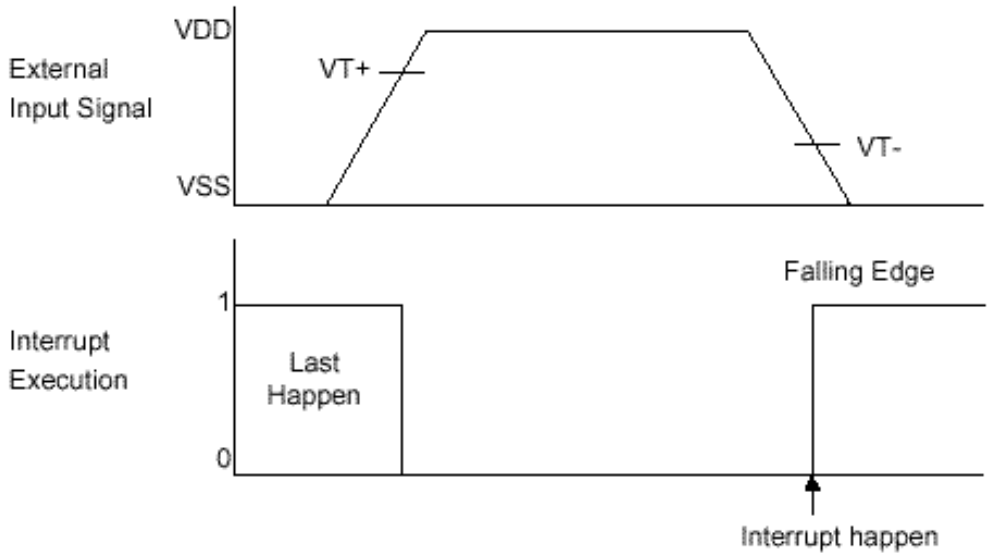


Figure 5-4B External Interrupt Timing

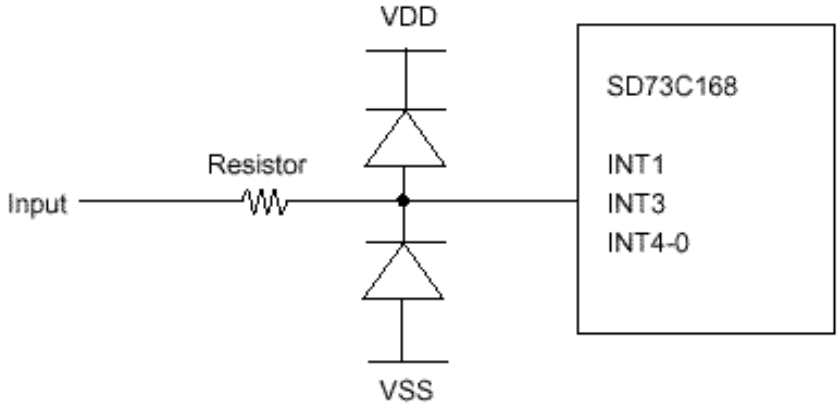


Figure 5-4C Additional Circuitry for External Input

5.5 Programmable Timer / Event Counter

SD73C168 features two on-chip timers with individual start and stop bits. Timer1 and Timer2 (shown in Fig. 5-5 & Fig 5-6) consist of a 16 bit capture latch, and a 5-bit non-readable prescaler with a 5-bit reload register.

The clock source of Timer1 and Timer2 shown in Table 5-1 is determined by bit 6 (SOURCE) of T1CLT1 and T2CTL1 respectively. A SOURCE bit of 0 selects the internally generated Fosc/4 clock and places the Timer/Event Counter in the Real Timer Clock (RTC) mode. A SOURCE bit of 1 selects the external clock source and places the Timer/Event Counter in the Event counter mode. In the external mode, the clock source for Timer 1 and 2 are input on the two least significant Bits of I/O Port A(A4) and (A5) respectively. Bit 7 of the timer control registers is the START bit for the respective programmable timers. When a 0 is written to the START bit, regardless of whether it was a 0 or 1 before, the prescaler and counter decrementers are loaded with the corresponding latch values, and the Timer/Event Counter operation begins. When the prescaler and counter decrement through zero together, an interrupt flag is set and the prescaler and counter decrementers are immediately and automatically reloaded with the corresponding latch values.

The interrupt levels generated by the timers are INT2 for Timer1 and INT6 for Timer2. Timer1 and Timer2 each have a 16-bit Capture Latch (CL) associated with them which capture the current value of the counter whenever INT3 for Timer1 and INT1 for Timer2 are triggered. The capture latch will store the Timer value even when INT1/INT3 are disabled. Both capture latch is disabled during the IDLE instruction when their corresponding timer HALT bits are 1.

Table 5-1. Timer 1 & Timer 2 clock Sources

Timer	Mode	Source Bit	Cascade Bit	Clock Source	Capture Latch Trigger	Interrupt
1	RTC	0	-	Fosc/4	$\overline{INT3}$	INT2
	EC	1	-	External Port A4		
2	RTC	0	-	Fosc/4	$\overline{INT1}$	INT6
	EC	1	-	External Port A5		
	CASCADE	-	1	Timer1		

In the Timer1 and Timer2, most significant byte readout latch is shared between the most significant byte (MSB) of the decrementer and the MSB of the capture latch. It allows the complete 16-bit value of the decrementer or the capture latch to be sampled at one moment. The least significant byte (LSB) must be read first, which causes the MSB to be simultaneously loaded into the readout latch.

There is only one readout latch for each timer, but the some latch can be read from two address for easier programming (see the diagrams for Timer1 and Timer2)

Timer1 MSB readout latch can be read from both P4(>0104) P6(>0106).

Similarly, Timer2 MSB readout latch can be read from both P8(>0108) and P10(010A)

Reading the LSB of the decrementer or capture latch will always update the contents of the readout latch. In order to correctly read the entire 16-bit value of the decrementer or capture, the LSB must be read first, which will load the MSB readout latch. The MSB readout latch must be read and stored before reading the LSB of either the decrementer or capture latch.

The order of 16-Bit read operations should be :

Timer1 : Decrementer : P5 then P4, or P5 then P6
Capture latch : P7 then P6, or P7 then P4

Timer2 : Decrementer : P9 then P8, or P9 then P10
Capture latch : P11 then P10, or P11 then P8

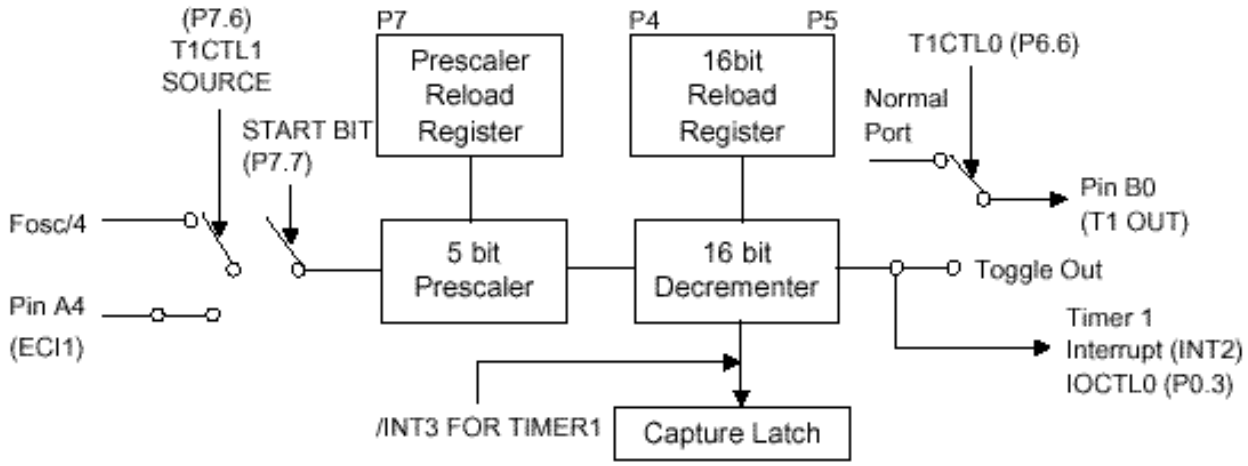


Figure 5-5. Timer 1 Schematic Diagram

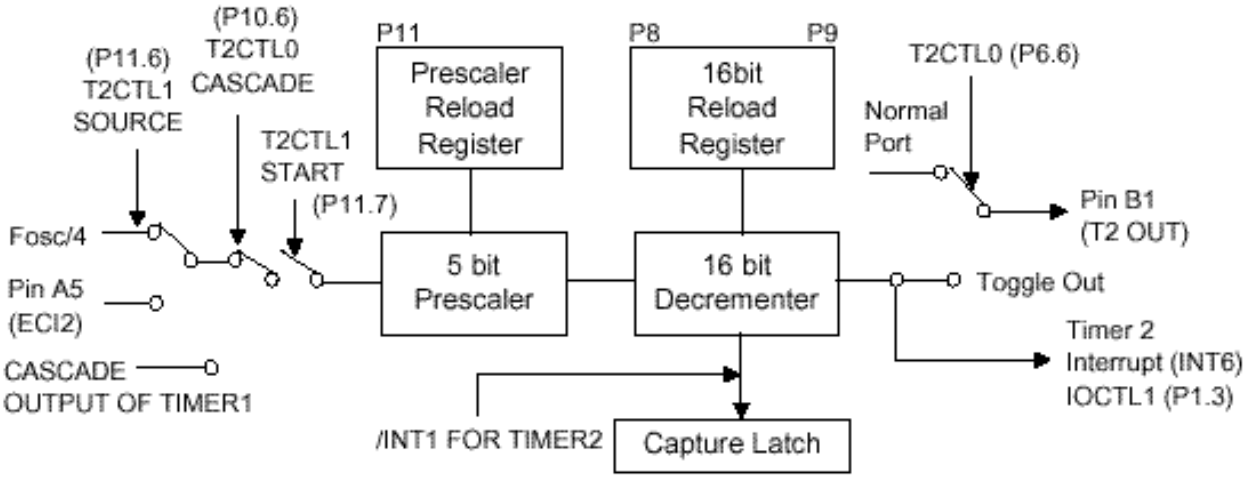


Figure 5-6. Timer 2 Schematic Diagram

5.5.1 Timer Control Registers

The Timer Control registers are shown in Figure 5-5 for Timer1 and Figure 5-6 for Timer2.

P4 >0104 T1MSDATA Timer 1 MS Data

	7	6	5	4	3	2	1	0
R	16 bit TIMER MSB DECREMENTER VALUE							
W	16 bit TIMER MSB RELOAD REGISTER							
RESET	X	X	X	X	X	X	X	X

Bit 0 - 7 : decrementer value MSB

P5 >0105 T1LSDATA Timer 1 LS Data

	7	6	5	4	3	2	1	0
R	16 bit TIMER LSB DECREMENTER VALUE							
W	16 bit TIMER LSB RELOAD REGISTER							
RESET	X	X	X	X	X	X	X	X

Bit 0 - 7 : decrementer value LSB

P6 >0106 T1CTL0

	7	6	5	4	3	2	1	0
R	MSB CAPTURE LATCH VALUE							
W	X	T1OUT	X	X	X	X	X	X
RESET	X	O	X	X	X	X	X	X

READ Bit 0 - 7 : Capture latch value MSB
WRITE B 6 T1OUT Toggle out CNTC for B0 Port
0 : B0 is a normal I/O port
1 : T1OUT ; toggles B0 when T1 decrements through 0

P7 >0107 T1CTL1

	7	6	5	4	3	2	1	0
R	LSB CAPTURE LATCH VALUE							
W	START1	SOURC1	T1HALT	PRESCALER RELOAD REGISTER				
RESET	O	X	O	X	X	X	X	X

READ

Bit 0 - Bit 7
Provide the LSB value of Capture Register which contains the decrementer register value at the time of INT1 was happened lately.

WRITE

Bit 1 - Bit 4 : Reloads the 5bit PRESCALER RELOAD REGISTER.

Bit 5 : T1HALT
0 - Timer 1 remains active during IDLE.
1 - Timer 1 will halt during IDLE

Bit 6 : SOURC1
0 - Internal clock source fosc/4
1 - External clock source from Port A4/ECI1.

Bit 7 : START1 : Timer 1 Start/Stop control
0 - Stop the Timer 1, hold current count value and clear INT2 FLAG.
1 - Reloads prescaler and decrementer and begin decrementing

CAUTION ! ! ! - START1 bit must set to be "0" before into HALT mode.

P8 >0108 T2MSDATA Timer 2 MS Data

	7	6	5	4	3	2	1	0
R	16 bit TIMER MSB DECREMENTER VALUE							
W	16 bit TIMER MSB RELOAD REGISTER							
RESET	X	X	X	X	X	X	X	X

Bit 0 - 7 : decrementer value MSB

P9 >0109 T2LSDATA Timer 2 LS Data

	7	6	5	4	3	2	1	0
R	16 bit TIMER LSB DECREMENTER VALUE							
W	16 bit TIMER LSB RELOAD REGISTER							
RESET	X	X	X	X	X	X	X	X

Bit 0 - 7 : decrementer value LSB

P10 >010A T2CTL0

	7	6	5	4	3	2	1	0
R	MSB CAPTURE LATCH VALUE							
W	CASCADE	T2OUT	X	X	X	X	X	X
RESET	O	O	X	X	X	X	X	X

READ

Bit 0 - Bit 7 : Capture latch value MSB

WRITE

Bit 6 : T2OUT ; T2 Toggle out CNTC for B1 Port

0 - Toggle output disable.

1 - T2OUT ; toggle B1 when T2 decrements through 0

Bit 7 : CASCADE

0 - Clock determined by SOURCE bit.

1 - Clock source is Timer 1 reload signal, overrides SOURCE bit

P11 >010B T2CTL1

	7	6	5	4	3	2	1	0
R	LSB CAPTURE LATCH VALUE							
W	START2	SOURC2	T2HALT	PRESCALER RELOAD REGISTER				
RESET	O	X	O	X	X	X	X	X

READ

Bit 0 - Bit 7 : Capture latch value LSB

WRITE

Bit 0 - Bit 4 : Reloads the 5 bit PRESCALER RELOAD REGISTER

Bit 5 : T2HALT

0 - Timer 2 remains active during IDLE

1 - Timer 2 will halt during IDLE

Bit 6 : SOURC2

0 - Internal clock source fosc/4

1 - External clock source from Port A5/ECI2

Bit 7 : START2 ; Timer 2 Start/Stop control

0 - Stop the Timer 2, hold current count value and clear INT6 FLAG.

1 - Reloads prescaler and decrementer and begin decrementing

CAUTION ! ! ! : START2 bit must set to be "0" before into HALT mode.

5.5.2 Real Time Clock mode (RTC)

In the Real Time Clock mode, Fosc/4 which is internally generated is the decrementer clock source. Each positive pulse transition of the Fosc/4 period signal decrements the count chain.

5.5.3 Event Counter mode (EC)

When Timer1 or Timer2 is selected to use in the EC mode, pin A4 and A5 operate as clock source decrementers for Timer1 and Timer2, respectively. The maximum clock frequency on A4 and A5 in the EC mode must not be greater than fosc/4. The minimum pulse width must not be less than 1.24 state clock cycles. Each positive pulse transition decreases the count chain.

5.5.4 Timer and Prescaled Clock

The timer clock, whether internal or external, is prescaled by a 5-bit module-N counter. The actual prescaling value is determined by the least significant five bits of the timer control register, and the actual prescaling value is equal to the timer control latch value plus one.
An INT2 interrupt for Timer1 and INT6 interrupt for Timer2 are momentarily pulsed when both the prescaler and counter is decreased to zero value together. This sets the INT2 or INT6 flag flip-flop. The prescaler and counter and then immediately reloaded with the contents of the prescale latch (PL) and the timer latch (TL) and the timer will start decreasing with the PL and TL value.

5.5.5 Timer Interrupt Pulses

The period of the timer INT2 and INT6 interrupt pulses may be calculated by following formula :

$$tINT = tCLK * (PL + 1) * (TL + 1)$$

where
tINT = period of timer interrupt
tCLK = 4/Fosc for internal Real Time Clock mode or the period of input external EC mode
PL = Prescaler Latch value
TL = Timer Latch value

At the falling edge of the INT3 and INT1 input, the Timer1 and Timer2 values are loaded into the corresponding Capture Latch (CL), when read Timer1 and Timer2 control register contain the CL value. This feature provides the capability to determine when an external event occurred relative to the internal timer.

5.5.6 Timer Output Function

Timer1 and Timer2 can be cascaded together to form one large timer by setting the CASCADE bit of T2CTL0 (P10) to "1". The CASCADE bit of 1 selects the output generated by Timer1 reload pulse as the clock input to the prescaler of Timer 2.
The CASCADE bit overrides the SOURCE bit, that is, if the CASCADE bit is "1", the SOURCE

bit of Timer2 has no effect. For right cascading operation, Timer2 is requested to be started first and then Timer1.
A Timer output function exists on both Timer1 and Timer2 that allows the B0 and B1 outputs, respectively, to be toggled every timer decrementing through zero.
This function is enabled by the T1OUT bit and T2OUT bit (bit6) in the timer control register T1CTL0 and T2CTL0.
When operating in the timer output mode, the B0 and/or B1 output can not be changed timer's START bit will reload and start the timer, but will not toggle the output. The output will toggle only when the timer decreses through "0". The timer output feature is independent of INT2 and INT6 and, therefore, will operate with INT2 and INT6 enabled or disabled.
Also, if the timer is active during the IDLE instruction, the timer output feature will continue to operate. Whenever the T1OUT bit is returned to "0".
B0 or B1 will become an output-only pin like G0. The value in the B0 or B1 data register will be the last value output by the timer output function. So that B0 or B1 data register will be the last value output by the timer output function, so that B0 or B1 will not change as the T1OUT or T2OUT BIT is returned to "0".
Whenever a read of B port is perfomed, the value on the B1 pin will always be returned, so the current timer output value can be read by reading the B port.
The T1OUT and T2OUT bits are set to 0 by a reset, so the timer output function will not be enabled unless the user sets T1OUT or T2OUT to 1.

5.5.7 Notes for Timer Usage

In the Timer1 and Timer2, most significant byte readout latch is shared between the most significant byte (MSB) of the decrement and the MSB of capture latch to be sampled at on moment. Timer 1 MSB readout latch can be read from both P4 and P6. Similarly, Timer2 MSB readout latch can be read from both P8 and P10. Reading the LSB of the decrement or capture latch will always update the content of the readout latch. In order to correctly read the entire 16 bit value of the decrementer or capture latch, the LSB must be read first, which will load the MSB readout latch. The MSB readout latch must be read and stored after reading the LSB of either the decrementer or capture latch.

5.6 A/D Converter

The key features of A/D converter are as follows.

- Total Unadjustabled Error	±1 LSB Max
- Analog input	2 channels
- Analog input range	VSS to VDD
- Conversion	Ratiometric Conversion
- Resolution	8 bit
- Conversion time	144 CPU machine cycles (1 machine cycle = 2/fosc)

The A/D Converter can be controlled by the three register on the Peripheral File.
The function block diagram is shown in Figure 5-7.

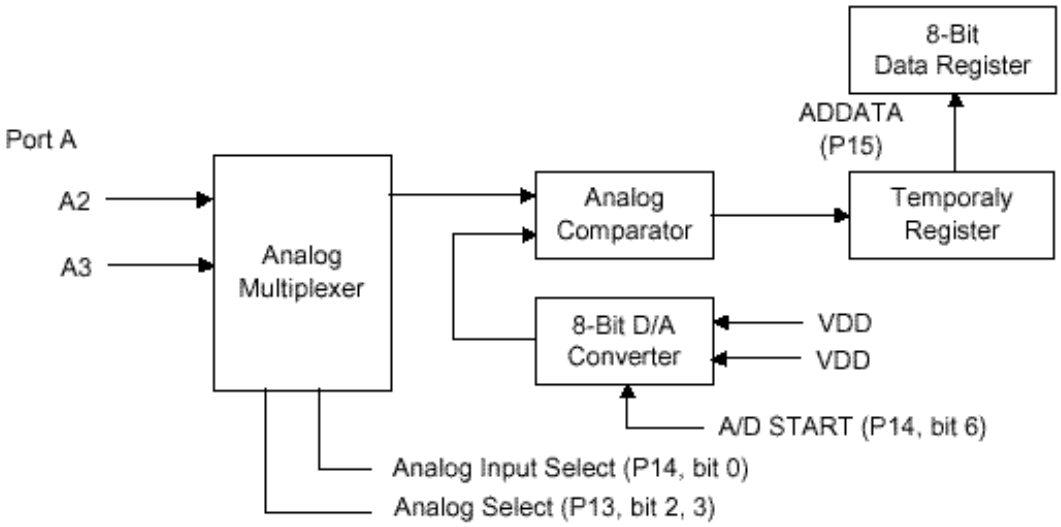


Figure 5-7. A/D Converter Function Block Diagram

5.6.1 A/D Converter Control / Data Registers

P15 >010F ADDATA

	7	6	5	4	3	2	1	0
R	CONVERSION DATA REGISTER							
W	I N V A L I D							

Note : After reset, all bits have "0"
Bit 0 - Bit 7 A/D CONVERSION DATA (0 - 255)

P14 >010E ADCNTL

	7	6	5	4	3	2	1	0
R	READY	START	NOT USED					ANALOG CHANNEL SELECT
W								

Bit 0 : ANALOG CHANNEL SELECT
ANALOG CHANNEL SELECT is determined by the value of P14 bit 0 at the beginning of conversion. If a new value is loaded to these bits during A/D conversion, it is effective for next conversion cycle.

PORT	BIT0
A2	0
A3	1

Bit 1 : Bit 5 Not used.

Bit 6 : START FLAG

Even through the START FLAG is set to "1" or "0" during A/D conversion, the START FLAG is ignored till the current conversion is completed.

WRITE

START A/D Converter Start/Stop Control bit.

0 = Stop A/D conversion

1 = Start A/D conversion

Bit 7 : READY FLAG

When the analog conversion data is set to ADDATA register (P16), the READY FLAG will be set to "1". Then the ADDATA register can be read by software. After the ADDATA register is read, the READY FLAG will be set to "0" automatically.

READ

0 = No operation or Incomplete conversion

1 = Complete conversion

WRITE

0 = Ineffect

1 = Clear READY FLAG

P13 >010D APSLCT

	7	6	5	4	3	2	1	0
R W	INT3SE	INT40SE	NOT USED		AD2SEL	AD1SEL	AMIFSE	FMIFSE

Note : After reset, all bits have "0"

Bit 2 - Bit 3 : ANALOG INPUT ENABLE

BIT2 (AD1SEL) : AD1/PORT A2

BIT3 (AD2SEL) : AD2/PORT A3

Before the A/D Converter operation starts, the corresponding bits of ANALOG INPUT ENABLE should be set to "1".

5.6.2 A/D Converter Operation

The A/D converter operation procedure is as follows.

1) Set the corresponding bits of ANALOG INPUT ENABLE register to "1".
2) Load the analog channel value to the ANALOG CHANNEL SELECT register bit 0.

3) Set the START FLAG (ADCNTL register bit 6) to "1"
   Then A/D conversion starts.
4) The conversion data is transfered to the ADDATA register, after A/D conversion completed.
   Then the READY FLAG (ADCNTL register bit 7) set to "1" automatically.
5) Can read the ADDATA register.

If the START FLAG is set to "0" during A/D conversion, the A/D converter operation is terminated, after the A/D converter is completed, this timing is shown in Figure 5-8 for the single conversion and Figure 5-9 for the continous conversion. If the READY FLAG is set to occured as other Interrupt.

5.6.3 Notes for A/D Converter usage

1) When the Port A2, A3 is defined as analog input function by the ANALOG INPUT ENABLE register, reading the Port A2, A3 data register is "0". Each bit of the Port A2, A3 can be defined individually by the ANALOG INPUT ENABLE register.

2) When the Port A2, A3 is used as analog input, the direction of Port A2, A3 should be set to input mode by using the Port A Direction register.

3) The precision of the conversion value is influenced by the stability of VDD and VSS during A/D conversion.

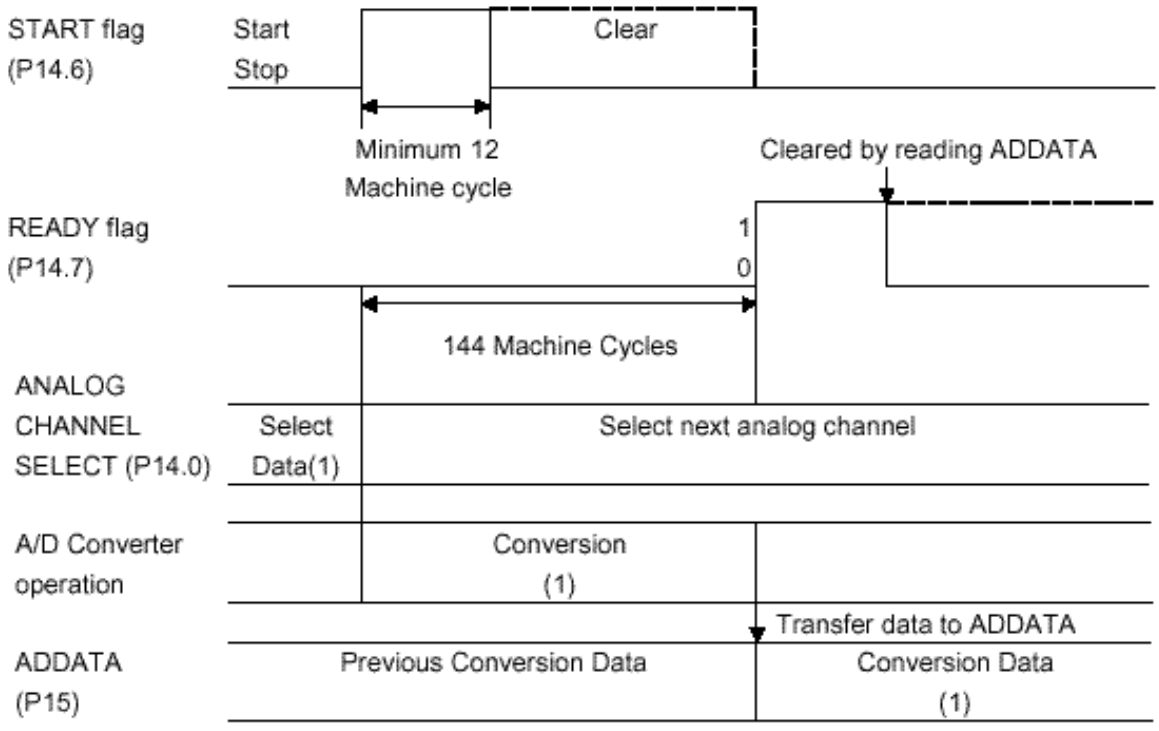


Figure 5-8. Single A/D Conversion

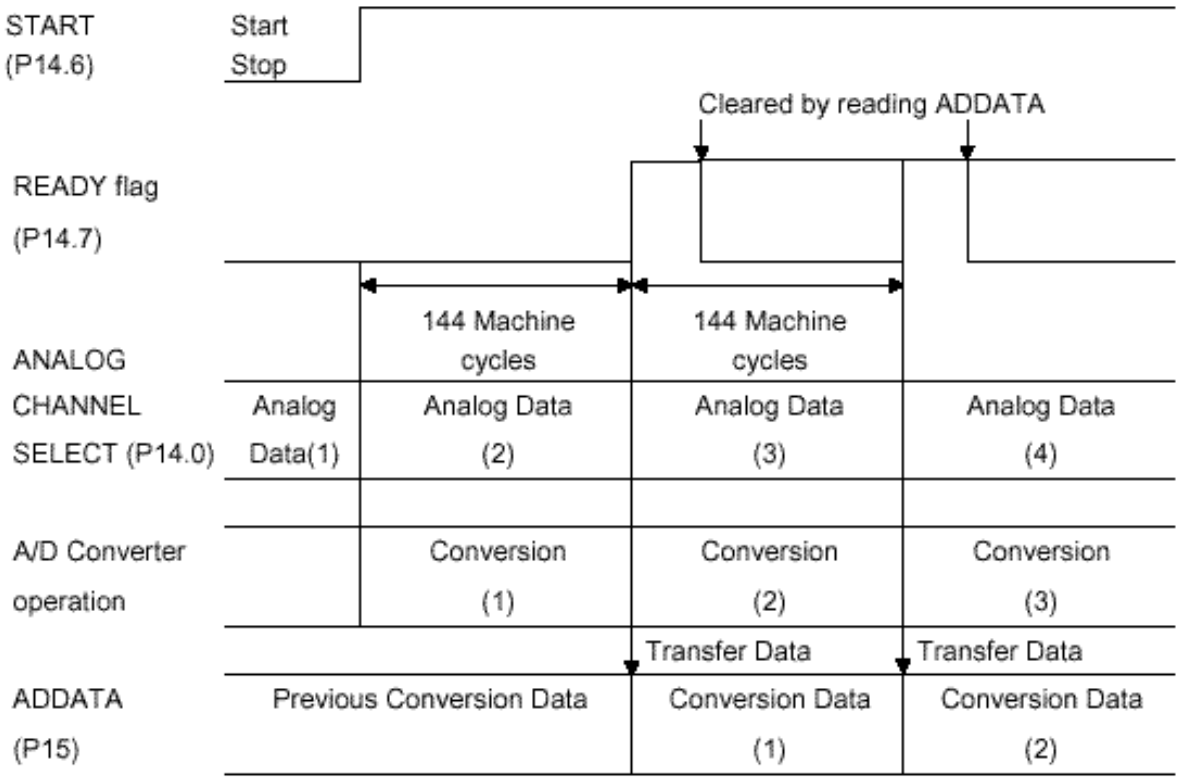


Figure 5-9 Continous A/D Conversion

5.7 PLL

The ON-CHIP Phase Locked Loop (PLL) has reference frequency divider, two module prescaler. 4bit swallow counter, 12bit programmable counter. Phase detector and exclusive PLL ports like VCOH, VCOL, EO1, CO2. Figure 5.7 shows PLL block diagram.

5.7.1 Reference Frequency Divider

The reference frequency divider consists of the crystal oscillator wich has connected external crystal (4.5MHz). This frequency divider generates 8 kinds of reference frequencies I.e. 1KHz, 5KHz, 6.25KHz, 9KHz, 10KHz, 12.5KHz, 25KHz and 50KHz.
One of reference frequencies can be selected by the program (By setting peripheral file : P16, bit 5, 4, 3).

5.7.2 PLL Control register

PLL control register are located in the two peripheral registers, P16 and P17. Figure 5-7-1 shows how to set each bit of PLL control register for PLL lock detection time, Reference frequency and AM/FM band Mode.

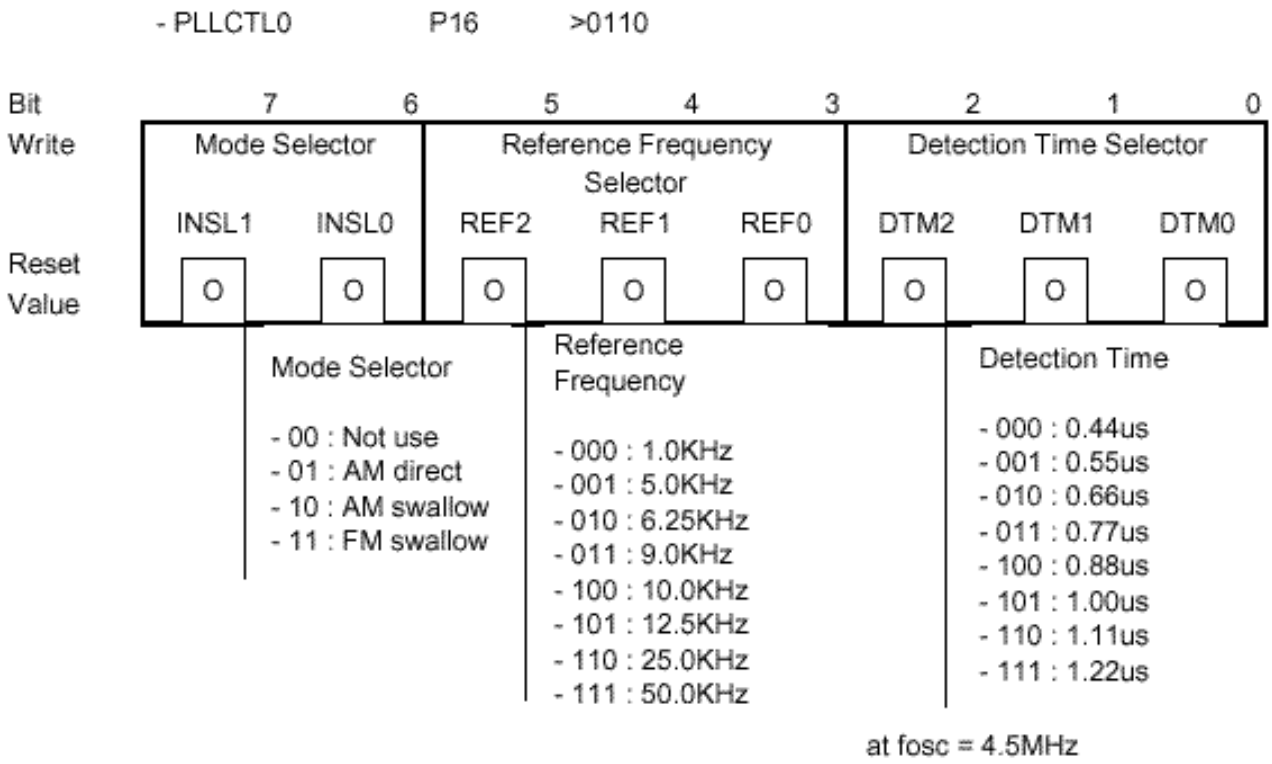


Figure 5-7-1 PLL Control Register

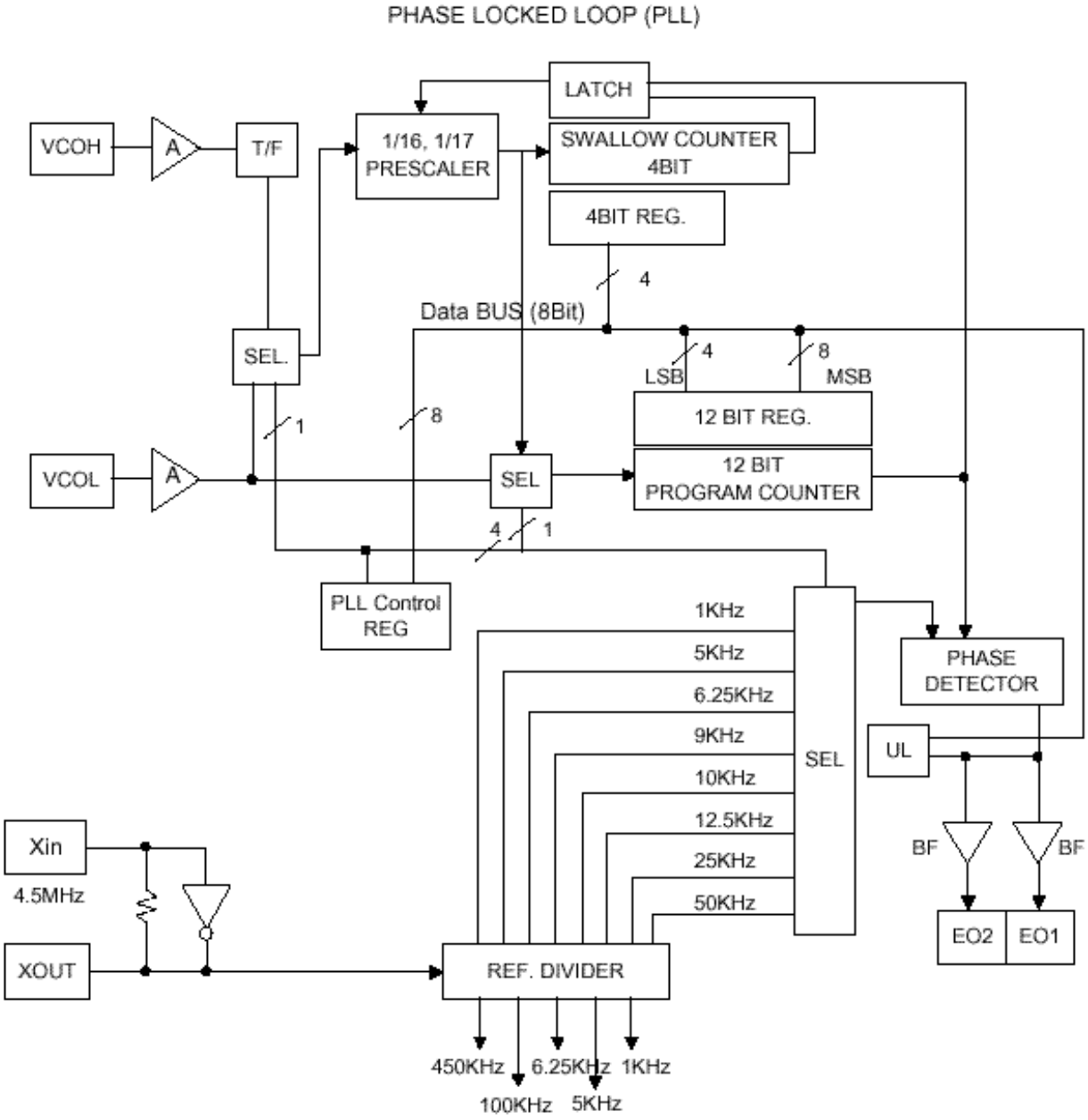


Figure 5-7 PLL Block Diagram

- UNLOCK F/F DETECTION TIME SELECTOR BIT

This bit must be set to satisfy your applied UNLOCK F/F detection time specification.
UNLOCK F/F detects the PLL Locking status affer detection time duration.

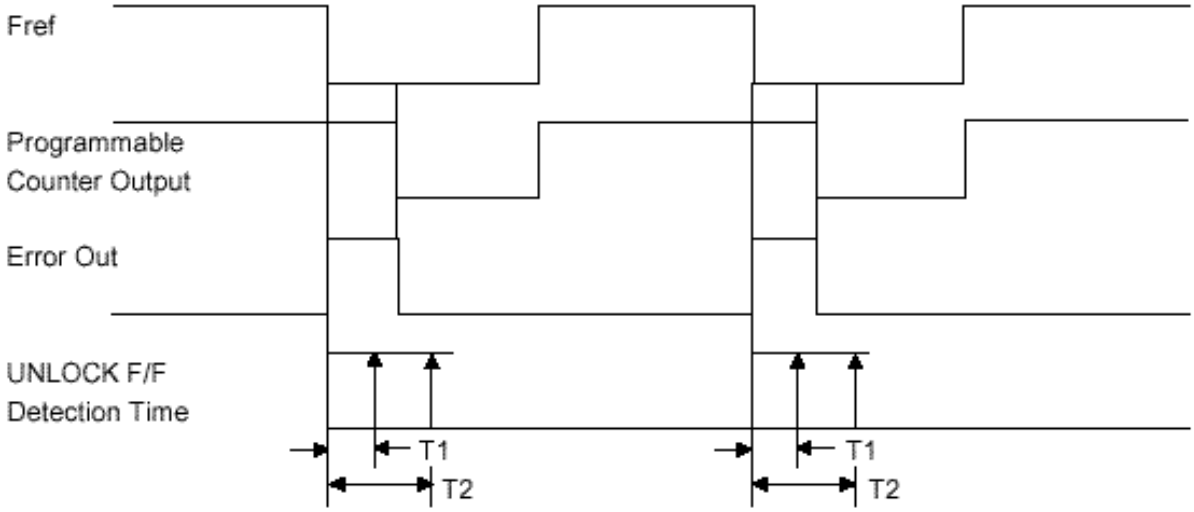


Figure 5-7-2. UNLOCK F/F DETECTION TIME

For example, if you select detection time - T1, UL F/F output is UNLOCK STATES, but you select Detection time - T2, UL F/F output is Lock status under the same Error output conditions. This is very useful to compensate for mechanical oscillation of VCO. Figure 5-7-2 shows two kinds of detection time (T1 and T2) as for example.

- REFERENCE FREQUENCY SELECTOR BIT

These bits select reference frequency specification which is inputs to phase detector to compare the phase difference with the VCO output divided by the programmable divider.

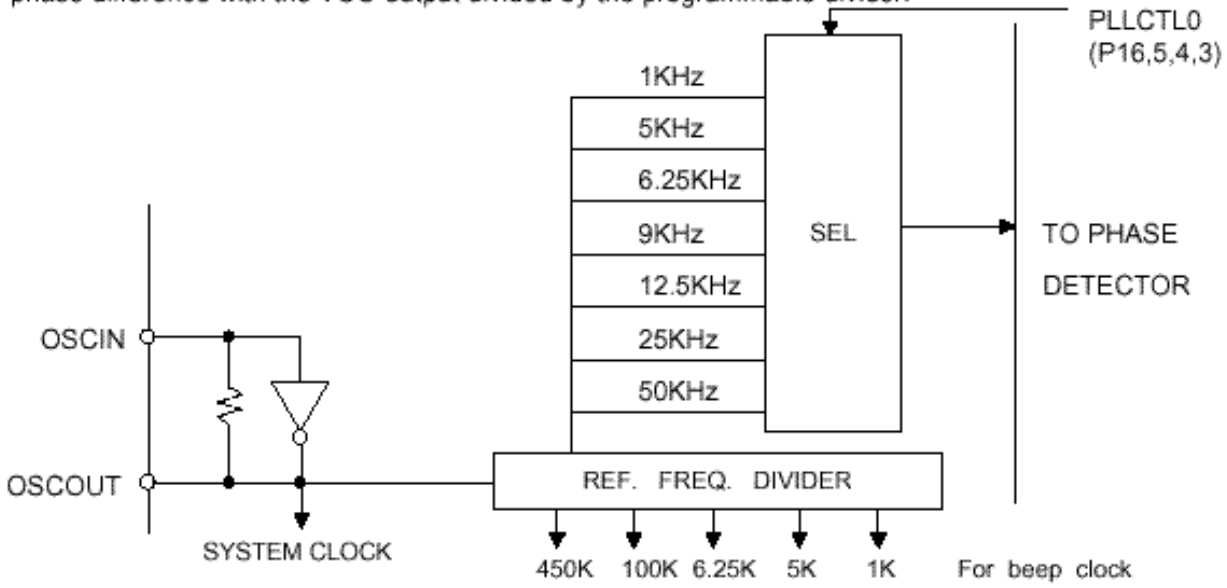


Figure 5-7-3. REFERENCE FREQUENCY SELECTOR BIT

- MODE SELECTOR BIT (AM, FM)

These bits selects dividing method whether pulse swallow dividing type or direct dividing type.
According to the input frequency band three combinations are available as follows.

INSL1	INSL0	Freq. Dividing Types	Input Freq. Range	Input Port	Freq. Div Number
0	0	NOT USE			
0	1	Direct Dividing	0.5 - 10MHz LW MW SWL	VCOL=ACTIVE VCOH=PULL-DOWN	M
1	0	(1/16, 1/17) Pulse swallow type	5 - 40MHz SWH	VCOL=ACTIVE VCOH=PULL-DOWN	(16M+S)
1	1	(1/2x1/16, 1/17) Pulse swallow type	10 - 150MHz FM	VCOH=ACTIVE VCOL=PULL-DOWN	2(16M+S)

Figure 5-7-4. Mode Selector Bit

(Note) : M represents program counter dividing numeral value
S represents swallow dividing numeral value

- PLLCTL1 P17 >0111

Bit	7	6	5	4	3	2	1	0
Read	READY	NOT USED			PLL TEST		UNLOCK DETECTOR	
							UL1	UL0
Reset Value	O	X	X	X	O	O	O	O

- 0 : No operation
- 1 : Active

- * ATTENTION

UNLOCK DETECTOR

- 00 : PLL LOCK/STOP/OFF
- 01 : REF FREQ>VCO FREQ
- 10 : REF FREQ<VCO FREQ
- 11 : NOT USED

Bit	7	6	5	4	3	2		
Write	PLLEN	NOT USED			PLL TEST			
Reset Value	O	X	X	X	O	O	O	O

- 0 : No operation
- 1 : Active

- * ATTENTION
These bits must be set to "0" in normal program operation

Figure 5-7-5. PLL Control Register

○ READY

This bit must be set to satisfy The PLL conditions between PLL ON/START STATUS and PLL OFF/STOP STATUS by programming.

○ PLLEN BIT

When the PLL ON/START (PLLEN=1) OR PLL OFF/STOP (PLLEN=0) is set to PLLCTL1 register (P17), the READY bit will be set to 1 or 0 accordingly.

○ UNLOCK DETECTOR BIT

This bit is automatically set by phase detector conditions.
Both the UL1 bit and UL0 bit are automatically set under conditions of PLL LOCK/STOP/OFF. When reference frequency leads VCO frequency which is divided by programmable divider (Fref>VCO/N), the UL1 bit is set to 0 and the UL0 bit is set to 1. When reference frequency lags VCO frequency which is divided by programmable divider (Fref>VCO/N), the UL1 bit is set to 1 and the UL0 bit is set to 0.

5.7.3 PLL Data Register

PLL data register are located in two peripheral registers as PF (18) and PF (19).

- PLLDATAH P18 >0112 : PLL PC MSB DATA REGISTER

Bit	7	6	5	4	3	2	1	0
Write	PLL PC MSB DATA							
Reset Value	O	X	X	X	O	O	O	O

- PLLDATAL P19 >0113 : PLL PC LSB DATA REGISTER

Bit	7	6	5	4	3	2	1	0
Write	PLL PC LSB DATA				SWALLOW COUNTER VALUE			
Reset Value	O	X	X	X	O	O	O	O

Figure 5-7-6. PLL DATA REGISTER

5.7.4. Programmable Divider

Programmable divider is composed of two modules prescaler, 4bit swallow counter and 12 bit binary programmable counter.
In pulse swallow dividing type, 1/16, 1/17 - modules prescaler is active in case of FM BAND and 1/2 divider is added to the front stage of prescaler.

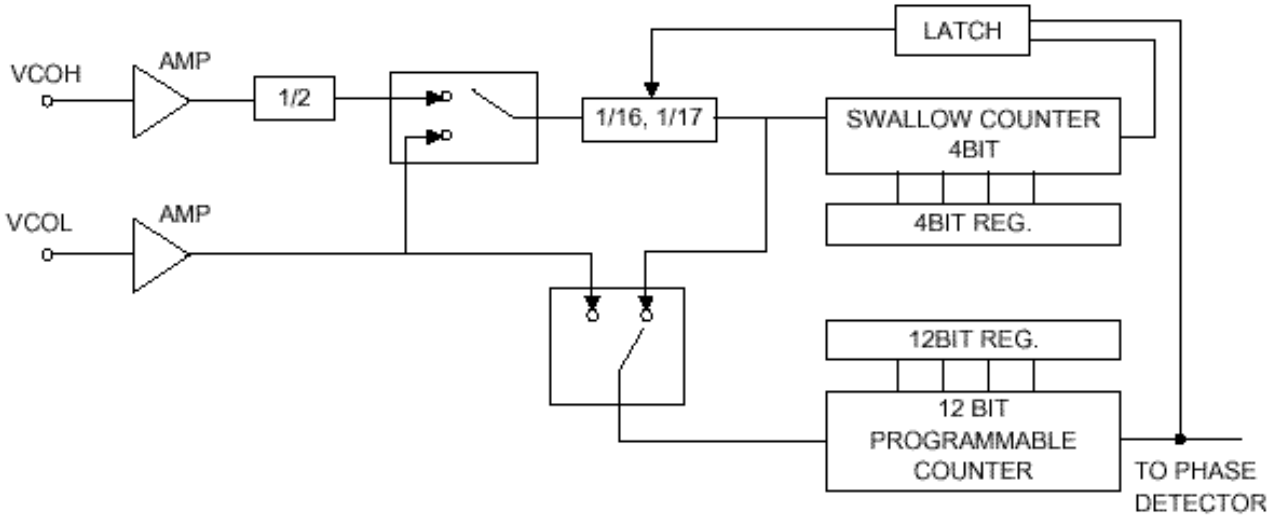


Figure 5-7-7. Circuit Diagram of Programmable Divider

In direct dividing type, input frequency (VCOL) is transfered to programmable counter directly. Both VCOH and VCOL ports have built-in AC AMP, INPUT signal must be cut by coupling capacitor.

5.7.5. Phase Detector

Phase detector detects the difference of phased between the reference frequency(Fref) and programmable counter output (VCO/N).
The output of this circuit puts out its error compoment to the EO1 and EO2 pins. Output from EO1, EO2 can be feedback to VCO through low pass filter.

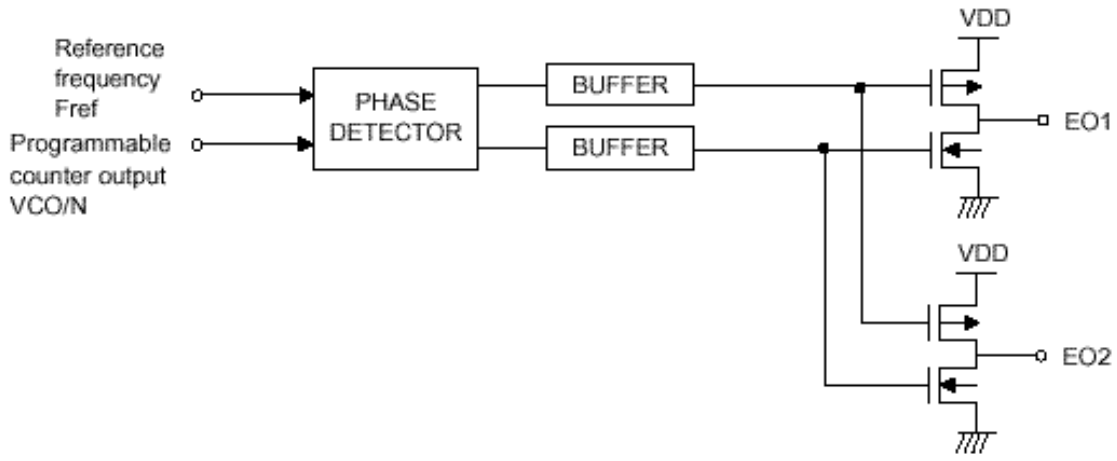


Figure 5-7-8. Phase Detector Circuit Diagram

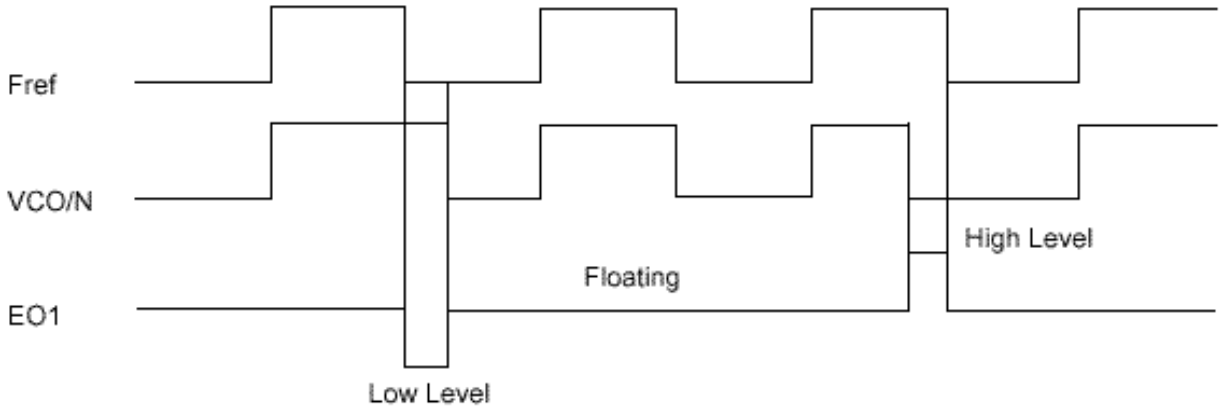


Figure 5-7-9, Error Output Time Chart

i) Fref > VCO/N : low level
ii) Fref < VCO/N : high level
iii) Fref = VCO/N : floating

Two Error output EO1, EO2, ports have the exactly same characteristics to optimize the design of low pass filter constant for each FM/AM BAND.

5.7.6. Setting of Frequency Dividing Number

The relation between VCO and Fref is as follows.

VCO = { (m+1)S + m(M-S) }Fref (put N = mM + S)
= (mM + S)Fref

$$N = \frac{VCO}{Fref}$$

VCO : Input frequency to pin VCOH/VCOL
Fref : Reference frequency
m : STANDARD Prescaler Ratio (=16)
s : The bit number of swallow counter
M : The bit number of programmable counter

1) Direct dividing type

- Frequency dividing number setting range

$N = 16 \sim (2^{12} - 1)$ => 10 ~ >FFF

Example : Reception of MW
(Reception frequency : 1440KHz, Reference frequency : 9KHz, IF frequency : 450KHz)

$$N = \frac{(1440+450) \times 10^3}{9 \times 10^3} = 210$$

= >0D2

- PLL DATA REGISTER

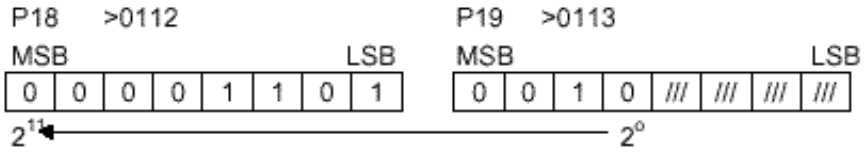


Figure 5-7-10.

2) Pulse Swallow Type

- Frequency dividing number setting range

$$N = 256 - (2^{16} - 1)$$

Example : Reception of FM

(Reception frequency : 125MHz, Reference frequency : 25KHz, IF frequency : 10.7MHz)

In case of FM band, 1/2 divider is added to the front stage of prescaler.

$$N = \frac{(125+10.7) \times 10^6}{2 \times 25 \times 10^3} = 2714 = 16M + S$$

M : 169[10] = 0A9h

S : 10[10] = 0Ah

= >A9A

- PLL DATA REGISTER

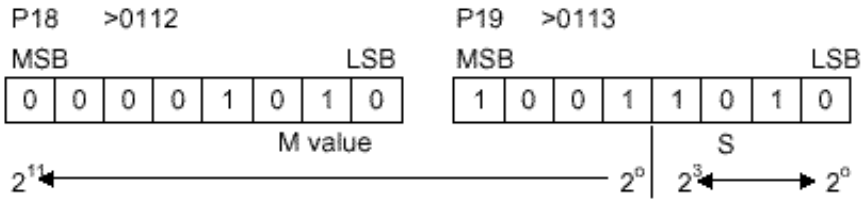


Figure 5-7-11.

5.8 IF Counter

The SD73C168 has on-chip IF counter function to measure FMIF or AMIF frequencies.
The IF counter consists of 17 bits and is mainly used to detect the stop signal during auto search tuning. If the desired IF frequency is counted by measuring frequencies input to pins PA0/FMIF and PA1/AMIF during auto search tuning, a broadcast station can be considered to exist on the reception frequency at that time.
Thus, by using the IF counter function to detect the stop signal, auto search tuning operation can be accomplished with smaller channel spacings such as 25KHz/step in the FM band 1KHz/step in the AM band.

5.8.1. IF Counter Block Diagram

IF COUNTER is shown in Figure 5.8.1.

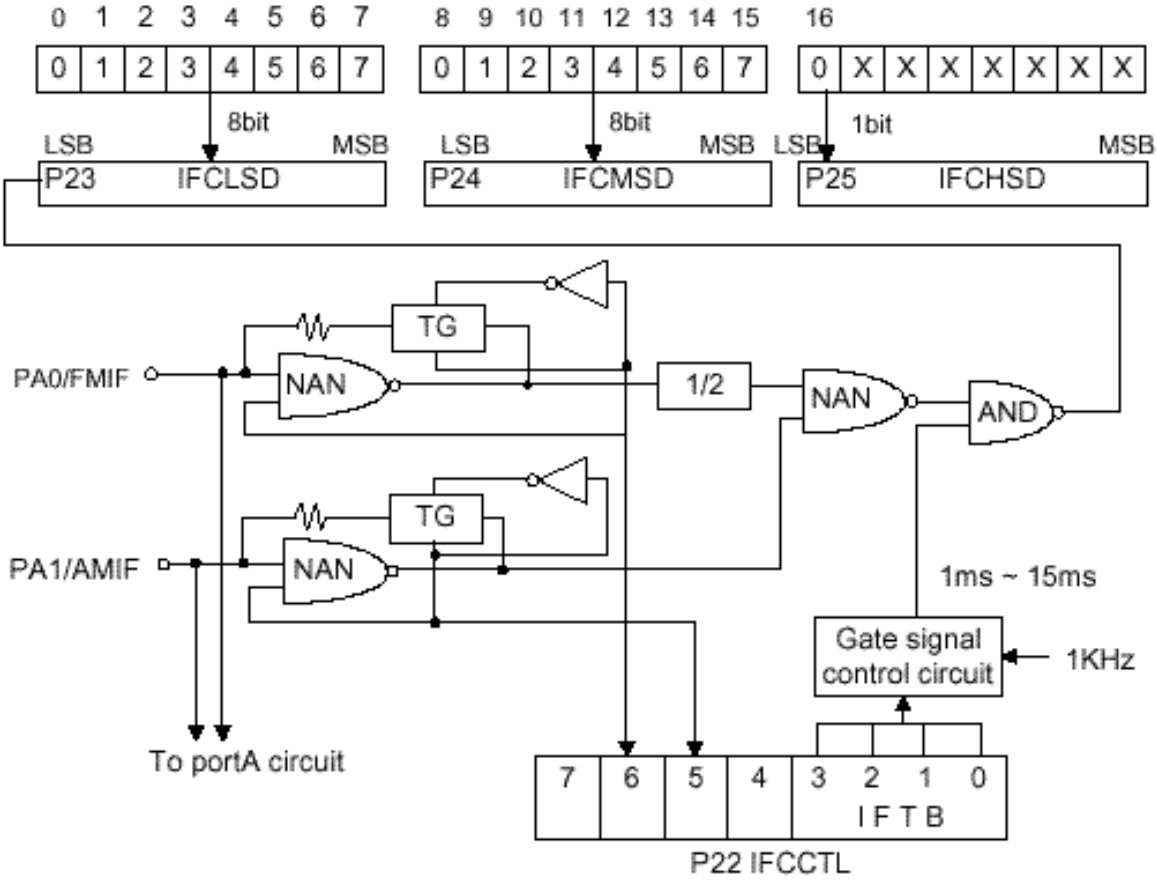


Figure 5-8-1. Configuration of IF counter

The IF counter of the SD73C168 is 17bit binary counter and its value can be read the IFCLSD (P23), IFCMSD (P24) and IFCHSD (P25).

IFCLSD, IFCMSD and IFCHSD are Registers for reading only, and data cannot be set in the IF counter through these Registers.

One of the fifteen following count times (gate signals) of the IF counter can be selected by the IF counter time bits (IFTB) : From 1msec to 15msec.

The frequency input to pin PA0/FMIF or pin PA1/AMIF can be countered by deciding the number of pulses input to the IF counter within the above-mentioned times.

The IFCCTL can also select A0/FMIF or A1/AMIF (P22;bit6/5).

If one pin is selected the other pin is internally pulled down automatically through a resister.

The maximum frequency that can be input to pin A0/FMIF is 20MHz (Vin=0.1 Vp.p) and that of pin A1/AMIF is 5MHz (Vin=0.1 Vp.p)

The signal input to pin A1/AMIF is input directly to the IF counter.

The signal input to pin A0/FMIF is input to the IF counter internally through the 1/2 frequency divider.

Therefore, the value of the IF counter will be 1/2 to the actual frequency to be input to pin A0/ FMIF if pin A1/AMIF is selected. The IF counter is reset during power ON reset (VDD = low to high) and IF counter holds the present values when the counter is stopped. This values can be cleared by program (IFCCTL;bit7). When the IF counter enters a halt mode, it maintains the state before the halt state.

5.8.2. IF Counter Control Register (IFCCTL)

The IF counter register IFCCTL designates the input pin and input gate signal time of the IF counter. The IFCCTL consists of 8bit Flip Flops and is set by the IFCCTL instruction.
IF COUNTER CONTROL REGISTER is Shown in figure 5-8-2. All the bits of the IF counter control register are reset to "0" during power On reset (VDD = low to high) or when the clock is stopped.

IFCCTL P22 >0116

Bit Write	START	FMIF	AMIF	TSTIF	TP3	TP2	TP1	TP0

IFTB				Count Time (at 4.5MHz fosc)
3	2	1	0	
0	0	0	0	Not USED
0	0	0	1	1 mSec
0	0	1	0	2 mSec
0	0	1	1	3 mSec
0	1	0	0	4 mSec
0	1	0	1	5 mSec
0	1	1	0	6 mSec
0	1	1	1	7 mSec
1	0	0	0	8 mSec
1	0	0	1	9 mSec
1	0	1	0	10 mSec
1	0	1	1	11 mSec
1	1	0	0	12 mSec
1	1	0	1	13 mSec
1	1	1	0	14 mSec
1	1	1	1	15 mSec

Must be set to "0"

Bit6	Bit5	Input signal selection
0	0	Neither will be selected
0	1	AMIF input
1	0	FMIF input
1	1	not used

Bit7	Start/Stop
0	Inactive or counter is stopped
1	Start

Figure 5-8-2. IF Counter Control Register

5.8.3. Gate Signal

The gate signal time of the IF counter is designated by the IF Time bits (IFTB) of the IF counter control Register (IFCCTL). The basic clock of it is a 1ms pulse signal which is not synchronous to the instruction.
Gate signals of 1mSec to 15mSec are generated based on this basic clock (1mSec).
For this reason, the IF counter starts immediately when the basic clock falls after the execution of the IFCCTL instruction is generated. Figure 5-8-3 shows an example when a gating time of 1ms is designated.

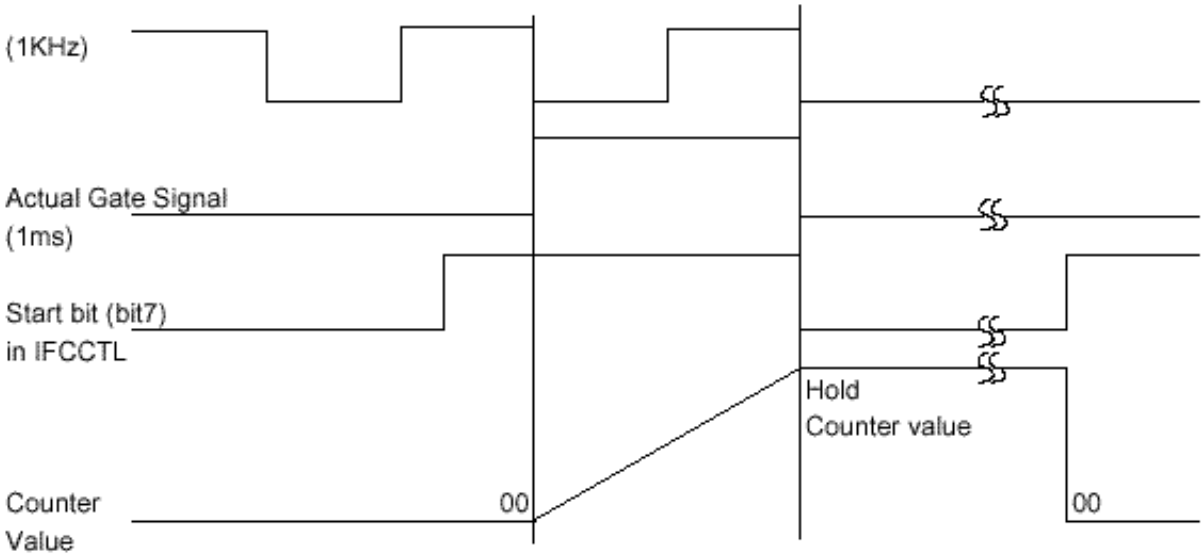


Figure 5-8-3. IF Counter Timing Chart.

As the timing chart in Figure 5-8-3 shows the delay time from the point counter start instruction to the point of actual counting by the IF counter is 1 msec maximum.

5.8.4. Error

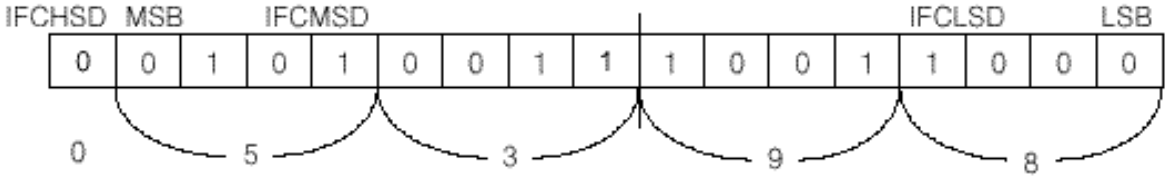
IF counter errors can be classified as gating time errors and counting errors. The gating time error depends on the oscillation frequency of the 4.5MHz crystal resonator connected externally. This because the basic pulse signal that decides the gating time is generated by dividing the 4.5MHz frequency.
Counting errors will be 0 to +1 (IFCCTL;Bit0) at maximum. When pin PA0/FMIF is selected, pin PA0/FMIF is regarded equivalently as low if the gate closes with the input signal remaining in a "high" state (or if pin PA0/FMIF becomes non-selective), and is counted larger by 1.
When pin PA1/AMIF is selected the signal of low to high is equivalently input to the counter and is counted one more when the gate opens (or when pin PA1/AMIF is selected during counting) if the level of pin PA1/AMIF is already high.

5.8.5. Examples of IF Counter Data Calculations

(1) When pin FMIF is selected as IF counter input pin. The frequency input to pin PA0/FMIF is input to the IF counter through the 1/2 frequency divider. For this reason, the data vlaue of the IF counter will be 1/2 of the frequency input to pin PA0/FMIF.

Example : FMIF freuqency (fFMIF) : 10.7MHz
Gate signal (Tg) : 4ms
IF counter value (N)

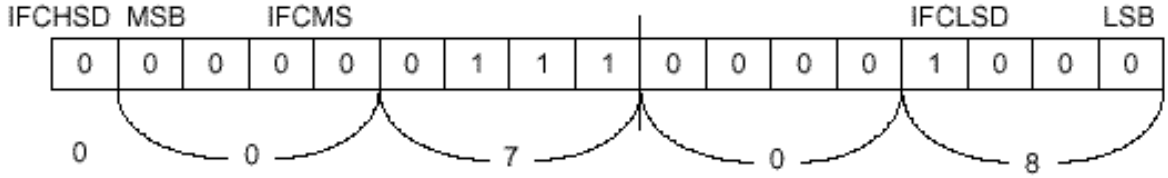
$N = 1/2\ (fFMIF \times Tg) = 2/1 \times 10.7 \times 10^{6} \times 4 \times 10^{-3}$
$= 21400$
$= >5398$



(2) When pin AMIF is selected as IF counter input pin.
The frequency input to pin PA1/AMIF is directly input to the IF counter.

Example : AM IF frequency (fAMIF) : 450MHz
Gate signal (Tg) : 4ms
IF counter value (N)

$N = fAMIF \times Tg = 450 \times 10^{3} \times 4 \times 10^{-3}$
$= 1800$
$= >708$



5.9. Serial Communication I/O Port : SIO1, SIO2

SD73C168 contain 2 sets of full duplex serial communication port synchronized by an internal or external clock (SCLK1, SCLK2) that consists of a double buffered receiver, double buffered transmitter as shown in Figure 5-9A, 5-9B.
Figure 5-9-2 shows the serial communication frame format. One frame consists of eight bits data only with eight bits fixed length. The period equals the SCLK period. LSB (=bit0) is received or transmitted first, and subsequently bit 1, 2, 3, 4, 5, 6, 7.
The receiver (RX) receives data from E1 (E4) pin on the rising SCLK1 (SCLK2) edges and the transmitter (TX) transmits data to E0 (E3) pin on the falling SCLK1 (SCLK2) edges as shown in Figure 5-9-3.

The transmitter and receiver process each data at the same bit position during the same SCLK1 (SCLK2), so an INT5 (INT7) interrupt by the transmitter is generated at the same time an INT5 (INT7) interrupt by the receiver.

SHIFT CLOCK	INTERNAL SCLK	EXTERNAL SCLK
SCLK Source	Fosc	E2 (SCLK1), E5 (SCLK2)
Band Rate	Fosc/8, Fosc/16, Fosc/32, Fosc/64	Fosc/8 Max
E2:SCLK1,E5:SCLK2	SCLK1, 2 Output or I/O Port	SCLK1, 2 Input
Character Length	8bit fixed length	
Error Detection	Overrun	

Table 5-9. SI/O Feature (Fosc : Xtal Oscillation Frequency)

* 1 SCLK1E (P27,2)

0 : E2 Normal I/O
1 : - P41.2 = 0 : E2 External SCLK1 input
- P41.2 = 1 : E2 Internal SCLK1 output

SCLK2E (P29,2)

0 : E5 Normal I/O
1 : - P41.5 = 0 : E5 External SCLK1 input
- P41.5 = 1 : E5 Internal SCLK1 output

* 2 SO1ENA (P27.1)

0 : E0 Normal I/O
1 : E0 Serial data output SO1 (P41, 0 = 1)

SO2ENA (P29.1)

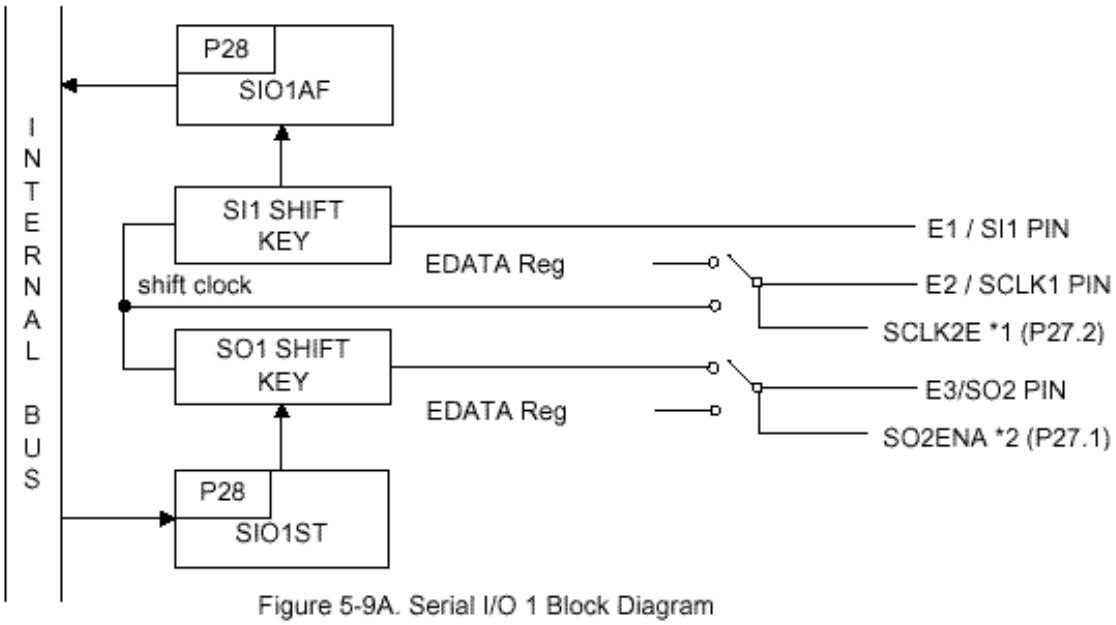


Figure 5-9A. Serial I/O 1 Block Diagram

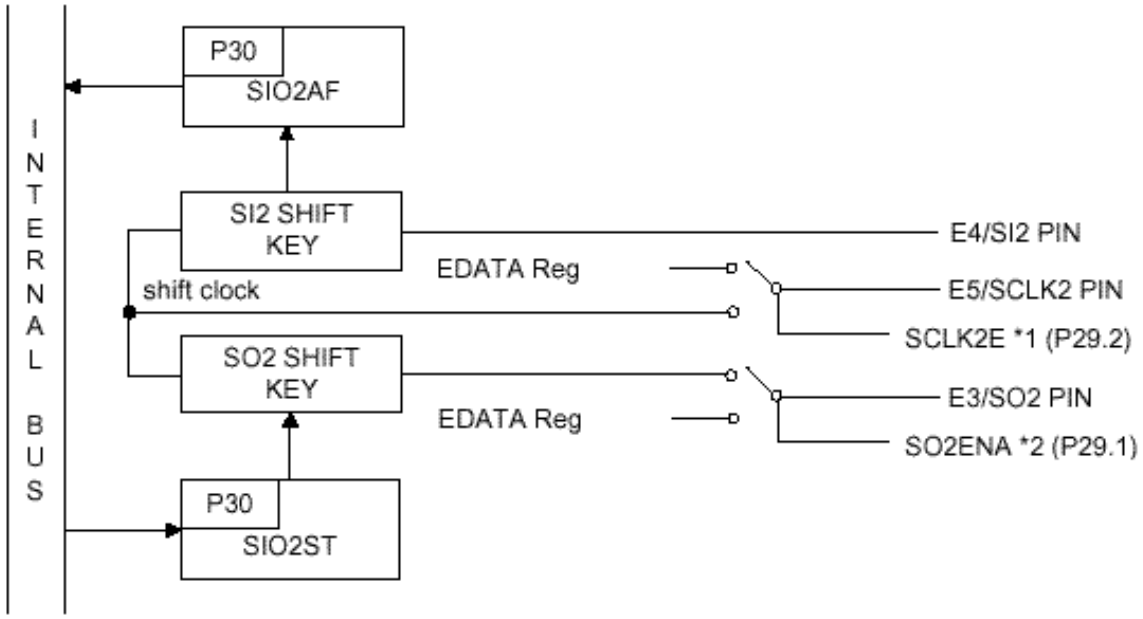


Figure 5-9B. Serial I/O2 Block Diagram

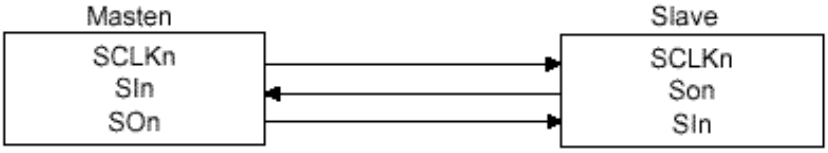


Figure 5-9-1. Master-Slave Connection Example

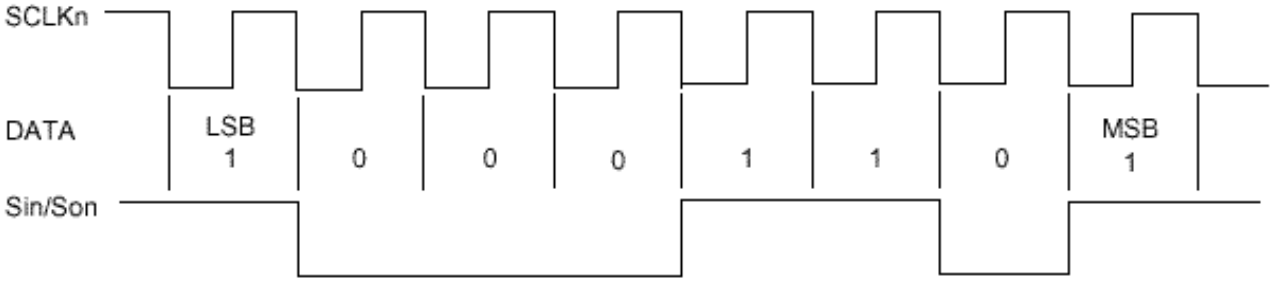


Figure 5-9-2. Serial Communication Format

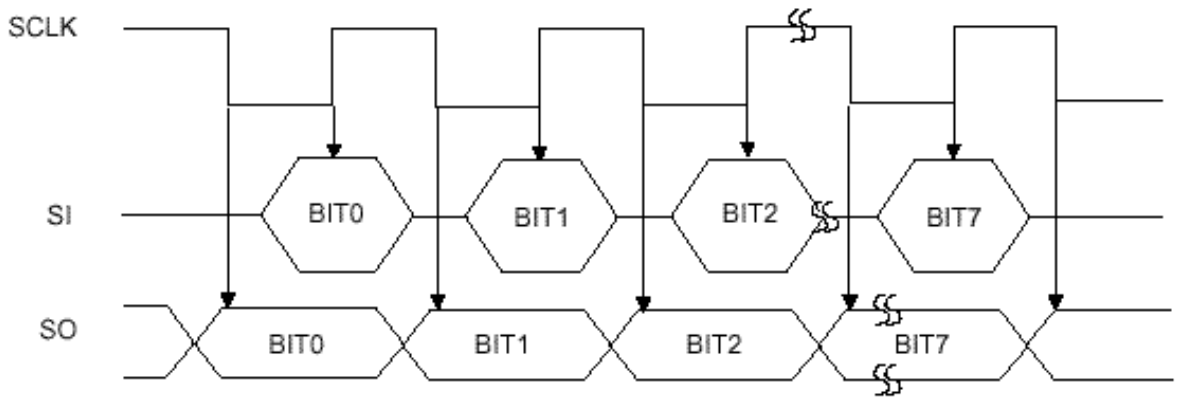


Figure 5-9-3. Serial I/O Timing

6. OTP Device Specification

6.1 Pin Assignment of OTP and OTP Programming Adapter Board

The OTP Device can be programmed like any Texas Instruments Device on a wide variety of PROM programmers. Programming the OTP Device requires a 80QFP to 28DIP adapter socket with the XRESET and OSCIN pins grounded. The following diagram shows the connections needed to be made on the 80QFP to 28DIP pin socket.

	OPERATING MODE		EPROM MODE			OPERATING MODE		EPROM MODE	
PIN NO.	PIN NAME	I/O	PIN NAME	I/O	PIN NO.	PIN NAME	I/O	PIN NAME	I/O
1	A0/FMIF	I/O			36	G6	I/O		
2	A1/AMIF	I/O			37	G7	I/O		
3	A2/AD1	I/O			38	H0	I/O	ADDR0	I
4	A3/AD2	I/O			39	H1	I/O	ADDR1	I
5	A4/ECI1	I/O			40	H2	I/O	ADDR2	I
6	A5/ECI2	I/O			41	H3	I/O	ADDR3	I
7	A6/INT4	I/O			42	H4	I/O	ADDR4	I
8	A7/INT3	I/O			43	H5	I/O	ADDR5	I
9	E0/SO1	I/O			44	H6	I/O	ADDR6	I
10	E1/SI1	I/O			45	H7	I/O	ADDR7	I
11	E2/SCLK1	I/O			46	B0/T1OUT	I/O		
12	E3/SO2	I/O			47	B1/T2OUT	I/O		
13	E4/SI2	I/O			48	B2	I/O		
14	E5/SCLK2	I/O			49	B3	I/O		
15	E6	I/O			50	B4	I/O		
16	E7/BEEP	I/O			51	B5	I/O		
17	F0	I/O	XPGM	I	52	B6	I/O		
18	F1	I/O	XCE	I	53	B7	I/O		
19	F2	I/O	XOE	I	54	D0	I/O		
20	F3	I/O	EPTEST	I	55	D1	I/O		
21	F4	I/O	EPTESTHV	I	56	D2	I/O		
22	F5	I/O			57	D3	I/O		
23	F6	I/O			58	D4	I/O		
24	F7	I/O			59	D5	I/O		
25	VSS		VSS		60	D6	I/O		
26	OSCIN	I	VSS		61	D7	I/O		
27	OSCOUT	O			62	C0	I/O	DATA0	I/O
28	VDD		VDD		63	C1	I/O	DATA1	I/O
29	TEST	I	VPP		64	C2	I/O	DATA2	I/O
30	G0	I/O	ADDR8	I	65	C3	I/O	DATA3	I/O
31	G1	I/O	ADDR9	I	66	C4	I/O	DATA4	I/O
32	G2	I/O	ADDR10	I	67	C5	I/O	DATA5	I/O
33	G3	I/O	ADDR11	I	68	C6	I/O	DATA6	I/O
34	G4	I/O	ADDR12	I	69	C7	I/O	DATA7	I/O
35	G5	I/O	ADDR13	I	70	NC			

	OPERATING MODE		EPROM MODE			OPERATING MODE		EPROM MODE	
PIN NO.	PIN NAME	I/O	PIN NAME	I/O	PIN NO.	PIN NAME	I/O	PIN NAME	I/O
71	EO1	O			76	VCOL	I		
72	EO2	O			77	VREF		VDD	
73	VSS				78	NC			
74	VASS		VSS		79	CE/INT1	I		
75	VCOH	I			80	RESET	I	VSS	

Note 1) Important notice

A. EPTESTHV PIN Assigned to F4 and EPTEST PIN Assigned to F3.

EPTEST	EPTESTHV	OPERATION
0	0	PGM, PGM VERIFY, READ
1	0	Word Line Stress, Bit Line Stress
1	1	Other Function Test Mode

B. VPP Pin assigned to test pad.

C. ADDR (0 to 13) was assigned to HPORT (0 ~ 7), EPORT (0 ~ 5)

D. EPROM I/O DATA (8) was assigned to CPORT

Note 2) EPORM related pins

TOTAL 31 PIN

○ DATA LINE	:	8 PIN
○ ADDRESS	:	14 PIN (ADDR0 ~ ADDR13)
○ CONTROL	:	5 PIN (XCE, XOE, XPGM, EPTEST, EPTESTHV)
○ VPP	:	1 PIN
		28 PINS
○ OTHER PIN	:	4 PIN (XRESET, OSCIN, VDD, VSS)
TOTAL		32 PINS

7. Electrical Specification

7.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range

(unless otherwise noted *)

PARAMETER		SYMBOL	RATING	UNIT
Supply voltage range (see Note 1)		VDD Vref	-0.3 ~ 7.0	V
Input voltage range	Port A,B,C,D,E,F,G,H, RESET, INT4-0, INT3, CE, OSCIN, VCOH, VCOL	VI	-0.3 ~ VDD+0.3	V
Output voltage	Port A,B,C,D,E,F,G,H, EO1, EO2	VO	-0.3 ~ VDD+0.3	V
Input current		II	± 10	mA
Output current		IO	± 10	mA
Total low-level output current		∑IOL	Max 80	mA
Power dissipation		PD	0.5	W
Storage temperature range		TSTG	-55 ~ 125	℃

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operating of the device at those or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximumrated conditions for extended periods may affect device reliability.

Notes :

1. Unless otherwise noted, all voltages are with respect to VSS.
2. Test pin must connect to VSS.

7.2 Recommended Operating Conditions

(Vss = 0V, Topr = -40 to 85℃)

PARAMETER	SYMBOL	CONDITION	MIN	TYPE	MAX	UNIT
Supply voltage	VDD1	CPU/PLL ON	4.5	5	5.5	V
	VDD2	CPU ON/PLL STOP	3.5	5	5.5	V
Memory Retention voltage	VDDR	OSC STOP	2.5	5	5.5	V
Analog supply voltage	VASS		-0.3	0		V
	VREF			VDD	VDD+0.3	V
Input oscilation voltage	VIN-VCO	VCOL, VCOH	0.3			Vp-p
	VIN-IF	AMIF, FMIF	0.1			
Operation free air temperature range	TOPR (Note3)		-40		85	℃
High level input voltage	VIH	Port A, B, C, D, E, F, G, H, OSCIN VDD=2.5 ~ 5.5V	0.7VDD		VDD	V
Low level input voltage	VIL	Port A, B, C, D, E, F, G, H, OSCIN VDD = 5V ±10%	VSS		0.3VDD	V
Positive-going threshold voltage	VT+ (see Note3)	INT1 (CE) RESET INT3, INT4-0	3.0		4.0	V
Negative-going threshold voltage	VT- (see Note3)	INT1 (CE) RESET INT3, INT4-0	1.0		2.0	V
Hysterisis	VT+ ~ VT- (see Note3)	INT1 (CE) RESET INT3, INT4-0	1.5		2.5	V
INT input current	IINT	INT1 (CE) RESET INT3, INT4-0			10.0	uA

Notes : 3. VDD = 5.0V

7.3 Electrical Characteristics Over Full Range of Operation

(Vss = 0V, Topr = -40 to 85℃)

PARAMETER		TEST CONDITION		MIN	NON	MAX	UNIT
Input current	II	VCOH, VCOL OSCIN	Vi = VSS ~ VDD			±20.0	uA
High level output current	IOH	PORT A, B, C, D, E, F, G, H, EO1, EO2	VDD = 5V ±10% VOH = VDD - 0.5V	-0.3	-1.2		mA
			VDD = 2.5 ~ 5.5V VOH = VDD - 0.5V	-0.1	-0.5		
Low level output current	IOL	PORT A, B, C, D, E, F, G, H, EO1, EO2	VDD = 5V ±10% VOL = 0.4V	0.4	0.6		mA
			VDD = 2.5 ~ 5.5V VOL = 1.0V	1.7	2.4		
High level output voltage	VOH	PORT A, B, C, D, E, F, G, H, EO1, EO2	VDD = 5V ±10% IOH = -1.0mA	VDD-0.5		VDD	V
			VDD = 2.5 ~ 5.5V IOH = -0.3mA	VDD-0.5		VDD	
Low level output voltage	VOL	PORT A, B, C, D, E, F, G, H, EO1, EO2	VDD = 5V ±10% IOL = -1.7mA			0.5	V
			VDD = 2.5V ±10% IOL = -0.4mA			0.4	
Output leakage current	Ileak	EO1, EO2	VO = VSS ~ VDD				nA
Input	Ci					15	pF
Supply current (Note 4)	ICC	Operating mode (PLL active)	fosc = 4.5MHz		20.0	40.0	mA
		Wake-up mode (Timer active)	fosc = 4.5MHz		1.5	3.0	mA
		Halt mode (OSC active)	fosc = 4.5MHz		500	900	uA
		Halt mode (OSC stop)	VDD = 5V		1	5	uA
			VDD = 3V		0.5	1	

Notes : 4. All I/O terminals which except OSCIN are open. And VDD = 5V

7.4 AC Characteristics for Input/Output Ports

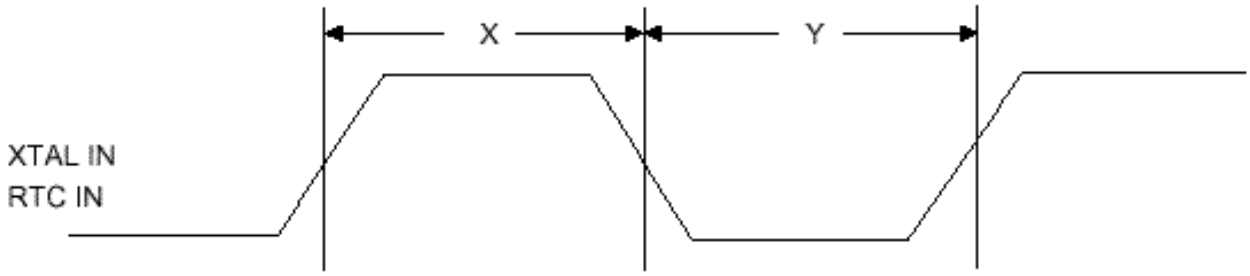
7.4.1 AC Characteristics for Input/Output Ports

(Vss = 0V, V_{DD} = 4.5 ~ 5.5V, Topr = -40 to 85℃)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
VCOH operating frequency	VCOH	Vin = 0.3 Vp-p	10		150	MHz
VCOL Operating frequency	VCOL	Vin = 0.3 Vp-p	0.5		40	MHz
FMIF operating freuquency	FMIF	Vin = 0.1 Vp-p	1		20	MHz
AMIF operating freuquency	AMIF	Vin = 0.1 Vp-p	0.1		5	MHz

7.4.2 AC Characteristics for clock I/O

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
Clock pulse rise time	tr (c)				20	nS
Clock pulse hold time	tf (c)				10	nS
Clock pulse duty cycle	dty (c)		45	50	55	%



$$DUTY(\%) \quad \frac{X \text{ OR } Y}{T(c)} \quad x \ 100 \qquad T(c) = X + Y$$

Note : Timing points are 90% (high) and 10% (low)

Figure 7-1. External driven clock waveform

7.5 A/D Converter Characteristics

(Vss = 0V, V_{DD} = 4.5 ~ 5.5V, Topr = -40 to 85℃)

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
Resolution				8	bit
Non-Linearity					
Zero error			±1	±2	LSB
Full-scale error					
Conversion time	4.5 MHz		64		us

7.6 AC Characteristics for Serial I/O ports

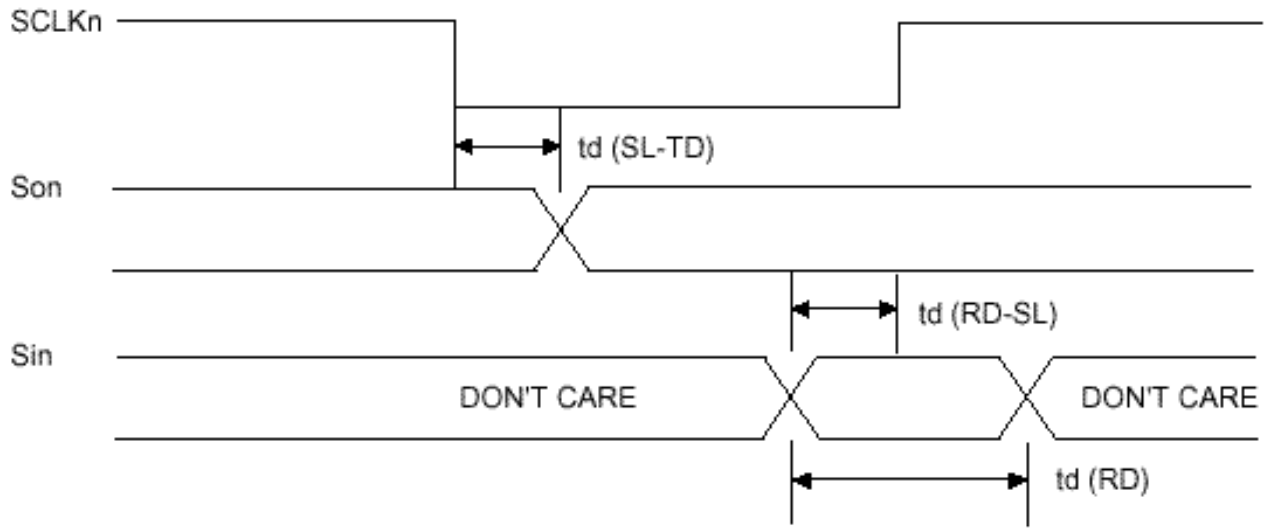


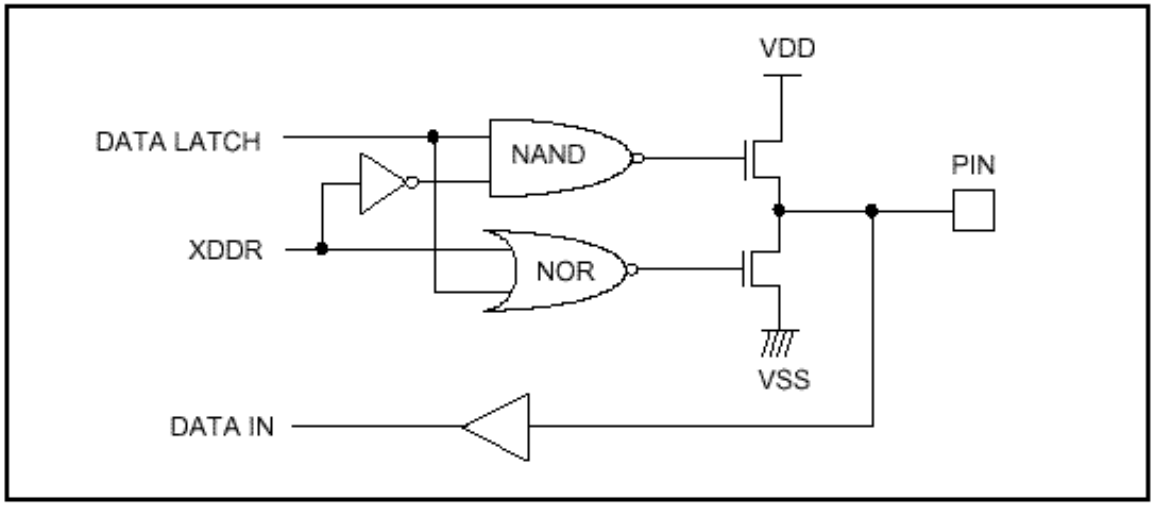
Figure 7.2 AC Characteristics for Serial I/O ports

PARAMETER		MIN	NOM	MAX	UNIT
td (SL-TD)	SCLKn low to new Son data		tc (c)		sec
td (RD-SL)	Sin data valid before SCLKn high		tc (c)		
td (RD)	Sin data valid time		4t (c)		

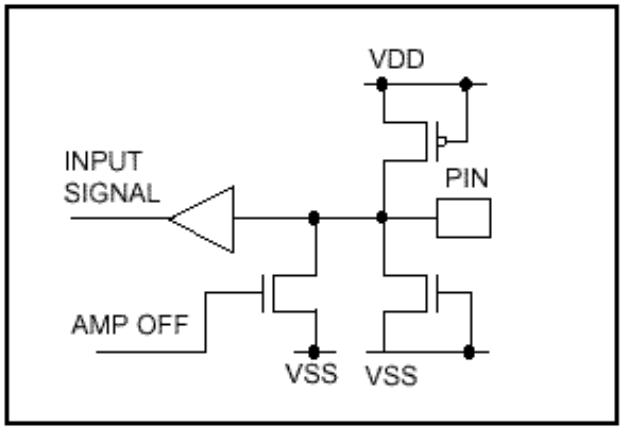
Note : VDD = 5V ±10%, tc(c) = 2/Fosc

7.7 Schematic of Inputs/Outputs

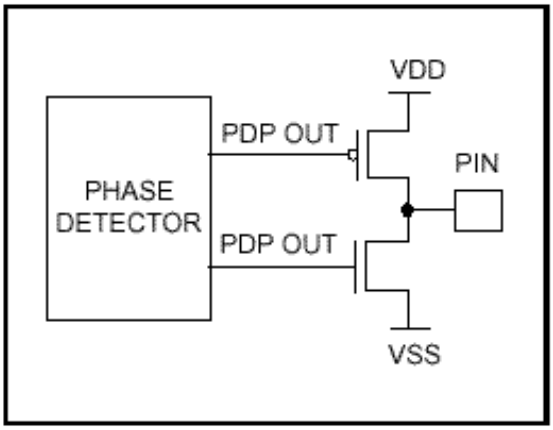
Port A, B, C, D, E, F, G, H



VCOH, VCOL

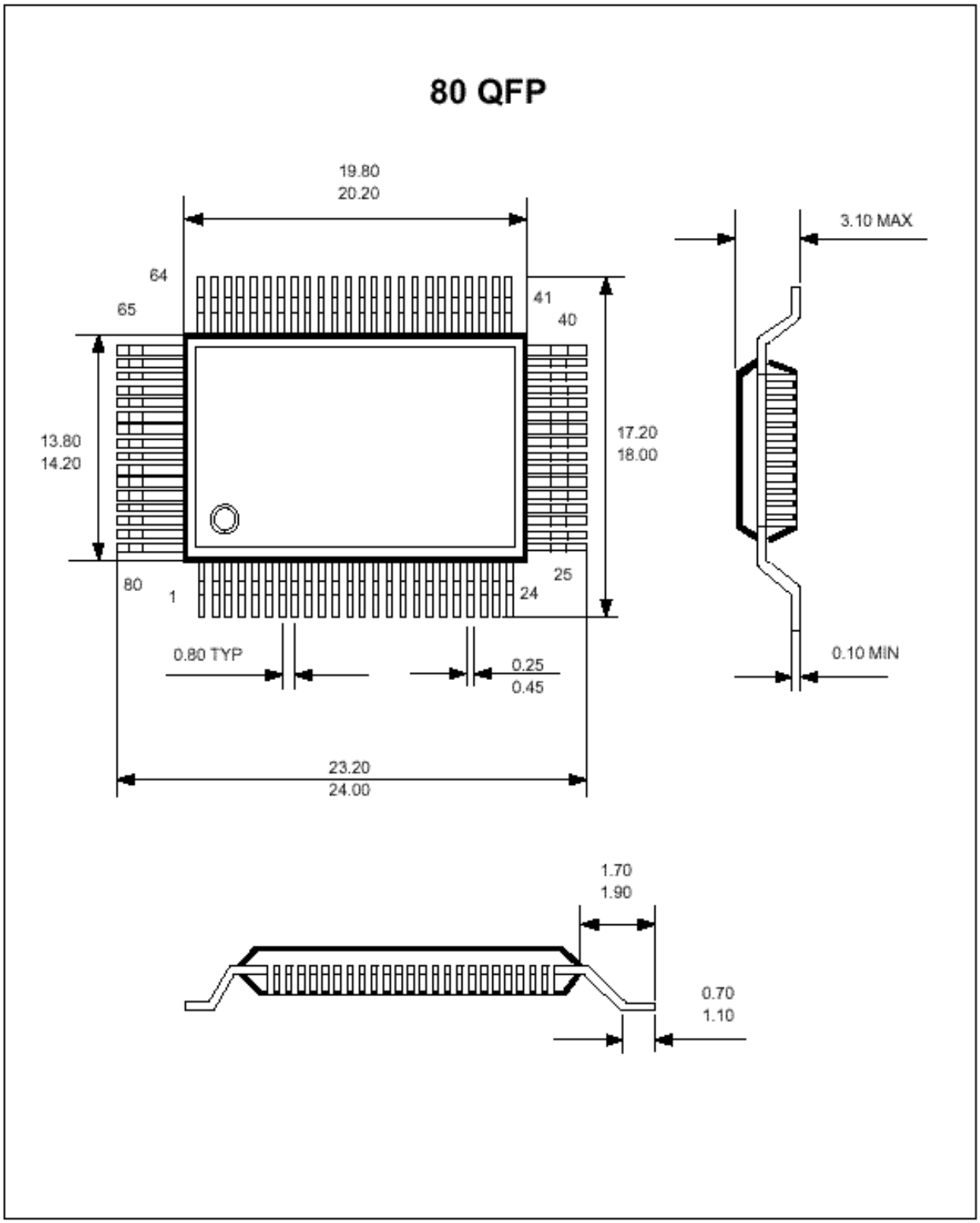


EO1, EO2



7.8 80 Pin Plastic Flat Package (Mechanical Data)

[Unit : Milimeter]



* APPENDICES

A. SD73C168 Table

B. Development Support

C. OTP Programming

Appendix A. SD73C168 Table

		SD73C168
TECHNOLOGY		CMOS
ROM SIZE		16K BYTE
RAM SIZE		384 BYTE
A/D CONVERTER		8BIT x 2CH
TIMER		2
SERIAL I/O		2
I/O	PORT	64
	INPUT	-
	OUTPUT	-
	I/O	64
DISPLAY DRIVER		-
EVENT COUNTER		2
OPEN DRAIN PORT		-
MAX IN FREQ.		
	FM	150MHz
	AM	40MHz
INTERRUPT		
	EXTERNAL	3
	INTERNAL	5
PACKAGE		80 QFP
IF COUNTER		17 BIT

Appendix B. Development Support

B.1 H/W Tool

B.1.1. EVM73C00(A)

EVM73C00(A) is a SD73CXX evaluation module, referred to throuthout this manual as the EVM. It is designed to emulate the SINGLE-CHIP MODE of the SD73CXX families. It provides all the signals that would be available from masked ROM parts. The EVM provides the ability to develop, debug, and test programs prior to factory masking.

Note : The EVM does not support the expansion modes of the SD73CXX family of processors.

B.1.2 Functional Overview

The EVM is a single-board development system capable of emulating the single-chip of the SD73CXX family or microcomputers.

The EVM stands alone as a development system using the text editor for creation of SD73CXX assembly language text files and can also accept text files from a host CPU through either of the two EIA ports. In both situations the resident assembler will convert the incoming text into excutable code in the second pass after resolving labels from the first assembly pass.
The EVM firmware supports two ports in the operations of loading and dumping data (text and object code) for storage and display. Port1/2 conform to the EIA RS-232C standard.

PORT1/PORT2	User terminal / terminal emulator
	Uplink / downlink to/from host CPU

The EVM supports the following baud rates :
300, 600, 1200, 2400, 4800, 9600
First, we set baud rate as 9600 bps. But if you want to set another value, you can change this by means of changing jumper (baud rate) on the EVM.
The EVM firmware is contained in 24K bytes of EPROM. The unused portion of the U45 EPROM is accessed with the monitor commands U0 through U9.
The EVM requires 2K bytes of system RAM that is separate from the 32K bytes of user RAM.
A wire-wrap development area, with all required signals provided and labeled, is available for additional logic. Since the EVM is intended to be a development tool by using the emulation cable, the crystal frequency of the EVM can be altered to fit the needs of the target system.

B.1.3 Operating System

The EVM operating system firmware resides in 24K bytes of EPROM and can be devided into three major parts.
- Debug monitor and EPROM programmer
- Text editor
- Assembler

All the software is designed to interact with the user to provide a complete, powerful, and easy to used development tool. During assembly and debug operations, the EVM RAM can be configured to emulate all SD73CXX family members. For emulation of the SD73CXX devices, the EVM allows assembly of text files from RAM, leaving the text intact for immediate editing after execution. After assembly of the text editor output, breakpoints can be set based on either addresses or line numbers. During execution, several modes of fixed displays are available, providing a hex display of the entire register and peripheral files or a binary display of the peripheral ports. During a fixed display, subsequent execution to a breakpoint or execution of a single instruction step will overwrite the old data on the screen with new data.
A programmable line of up to six register or peripheral locations is provided for display with breakpoints and instruction steps. The text editor is cursor and line number, duplicate line, and find string commands. The cursor oriented edit capability simulates a screen editor by allowing editing of the previous or next line moving the cursor up or down.

B.1.4 Overview of Tool

*** The Tool of DTS Application Micom ***

DEVICE	SD73C168
OTP	TMX73CE168
OTP ADAPTER	RWB73CE168QFP
ADP	ADP73C168
EVM	EVM73C00(A)
OTP WRITER	EVM73C00(A)

Note 1 : If you have any question, please call to Daewoo Electronics.
Note 2 : When you use EVM73C00, read the user's manual of EVM73C00 first, and then use EVM73C00.
Note 4 : EVM73C00A is a new version of EVM73C00.

B.2 S/W Tool

B.2.1. Assembler

SD73CXX assembly language instructions are mnemonic operation codes (or mnemonics) that correspond directly to binary machine instructions. An assembly language program(source program) must be converted to a machine language program (object program) by a process called assembling becore a computer can execute it. Assembling converts the mnemonics to binary values and associates those values with binary addresses, creating machine language instructions. Assembler directives control this process, place data in the object program, and assign values to the symbols used in the object program.
SD73CXX assembly language is processed by a two-pass macro assembler that executed on a host computer.

During the first pass the assembler :

1) Maintains the location counter,
2) Builds a symbol table, and
3) Produces a copy of the source code.

During the first pass the assembler :

1) Reads the copy of the source code and
2) Assembles the object code using the opcodes and symbol table produced during the first pass.

Note :
There are some version in assembler software such as "asm7.com" and "asm700.exe".

asm7.com : can support program which use many labels but can't support macro.
asm700.exe : can support macro instruction but can't be used in program with many labels

```
TYPE FILENAME.ASM
A0RG >C006                    ; absolute address (16K byte rom size)
**** PROGRAM ****
END

ASM7 FILENAME.ASM             ----> ENTER KEY
Listing File [FILENAME.LST]   ----> ENTER KEY
Object File [FILENAME.MPO]    ----> ENTER KEY
NO ERROR, NO WARNING
```

The filemane.mpo is object file of TI hex format which can be downloaded into EVM.

B.2.2. Linker

The SD73CXX assembler creates both absolute and relocatable object code that can be linked to form executable programs from separately assembled modules. An entire program need not be assembled at one time. A long program can be divided into separately assembled modules, avoiding a long assembly and reducing the symbol table size. Caution must be observed when assembling a long program with excessive labels ; this may cause an assembler error from symbol table overflow. Modules that are common to several programs can be assembled once and accessed when needed. These separately generated modules can be linked together by the link editor, forming a single linked object module that is stored in a library and/or loaded as required.

Note : See the below simple example.

```
DIR C:
HA0.ASM   HA1.ASM   HA2.ASM   HA0.MPO   HA1.MPO   HA2.MPO   HA.CTL

TYPE HA0.ASM
TYPE HA1.ASM
PSEG
****  PROGRAM  ****
END

TYPE HA2.ASM
DSEG
DATA RESET              ; If this program size is 16K byte, reset
END                     ; address is C006 (trap 0)
```

```
TYPE HA.CTL
TASK HA
PROGRAM >C006          ; program start address
DATA        >FFFE      ; data start address which is trap vector (reset)
INCLUDE HA0.MPO        ;
INCLUDE HA1.MPO        ;
INCLUDE HA2.MPO        ;
END

LINKER HA.CTL
MAPFILE [HA.MAP]
LOADFILE [HA.LOD]
```

The filename of HA.LOD is object file of this.

Note : The data format of filename.lod is same as filename.mpo.
So you can use each file although it is filename.mpo or filename.lod to download to EVM.

APPENDIX C. OTP PROGRAMMING

* Recomendation for TMX73CE168 Adapter (RWB73CE168QFP)

C-1. Program Flow

STEP 1) EVM Power Off
STEP 2) EVM Power On
STEP 3) Set-up EVM Environment (HS/DV)

```
HS  1
DV  5            ; 16K Byte ROM Size
```

STEP 4) Download your MPO File on EVM Board

```
LM 1
INITIALIZE (Y)
------ FILE.MPO TRANSFER ------
```

STEP 5) Insert OTP (TMX73CE168) into Adapter Socket
STEP 5.1) Insert Adapter Socket into EPROM Socket on EVM

* If you use EVM73C00A (Not EVM73C00), Goto the Step 6-1.

STEP 6) Check Device Blank Areas you want to use (EX ; VE 0 3FFF 4)

```
VE  0  3FFF  4          ; VE : Blank Check, >0 : Device Start Address
                        ; >3FFF : Device end Address, 4: ROM Size = 16K Byte,
                        ;         VPP = 13.0V  (TMX73CE168 : 0000H - 3FFFH)
                        ; 0000H - 3FFFH (C000H - FFFFH) ; DV  4   16K
```

If error happen, try again from Step 7.

STEP 7¦ Program Device

```
PE   6  3FFF  C006   4    ; TMX73CE168
                ; PE : Program OTP,  >6 : Device Start Address
                ; >3FFF : Device End Address,  4 ; ROM Size = 16K Byte,
                ; VPP = 13.0V
```

STEP 8¦ Compare Device with your MPO File.
If error happen, try again from Step 7.

STEP 9¦ Take off Adapter Sock from EPROM Sock on EVM.
If you want to program another device, you have to do repeatedly from Step 5 to Step 9.
If you use EVM73C00A (Not EVM73C00), you may use below "One Line" batch command.

STEP 6-1) Enter "AU" : Batch Command for VE & PE & CE

AU <CR>

Then VE, PE, SE operations are automatically operated, and displayed below line in monitor.

VE
PE
CE

ANOTHER DEVICE (Y/N) ?

If you want to program another device (OTP) continuously, change device with new one in OTP Writer Board and type "Y". When you type "N", This process goes to end.

* Important

If you replace programmed device with new device on EVM Power On, some error may happen in access to EPROM area on TMX73CE168 because VCC of EPROM Socket is still asserted.
In case of this mentioned error, if you don't want to do repeatedly from Step 1, get rid of adapter sock from EVM and then insert adapter socket to EVM again.