SIEMENS

Prescaler 1: 64 / 1: 256 for 1.3 GHz

SDA 4212

Bipolar IC

Features

- Pin programmable prescaler ratio of 1:64 or 1:256
- Symmetrical push-pull input
- Low harmonic wave
- Minimal current consumption of 23 mA

Type	Ordering Code	Package
SDA 4212	Q67000-A8049	P-DIP-8
SDA 4212-X	Q67000-A8145	P-DSO-8

Circuit Description

The SDA 4212 has been designed for application in television receivers operating according to the frequency synthesis tuning principle. The component includes a preamplifier and an ECL prescaler stage with symmetrical ECL push-pull outputs. It can be operated with a prescaler ratio of 1:64 or 1:256.
The component has been designed for a max. input frequency of 1.3 GHz.

The preamplifier of the component has been designed with symmetrical push-pull inputs. During the asymmetrical drive of one of the inputs, the other input has to be decoupled to ground by a capacitor (approx. 1.5 nF) of low series inductance.

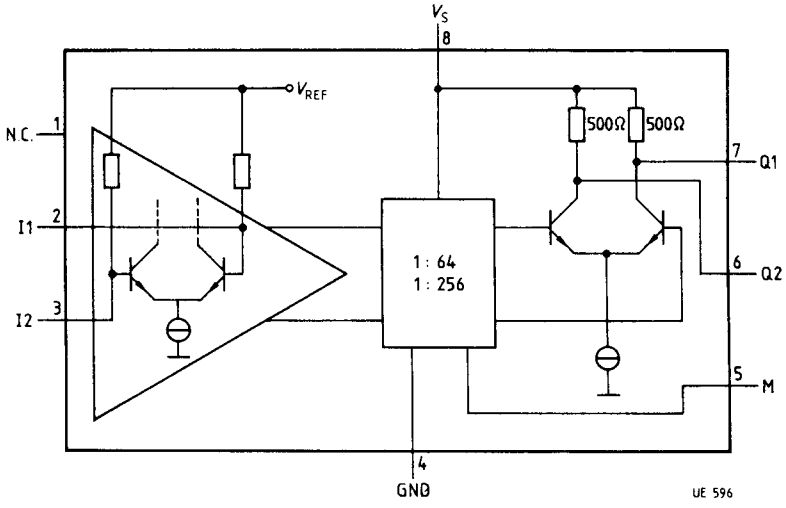
The prescaler stage of the component is comprised of several status controlled master slave flipflops. Their prescaler ratio can be set with the switch-over input M as follows:

M to V_S = 1:64
M to ground = 1:256

The symmetrical push-pull outputs of the prescaler include an internal resistor of 500 Ω each. The DC voltage level at the outputs is connected to the supply voltage V_S (output "High" = V_S). Typical output deviation is 1.0 V_{pp}.

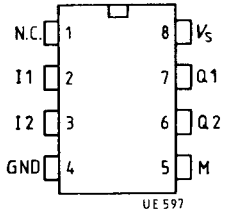
The typical output modulation is 0.6 V_{pp}.

Block Diagram

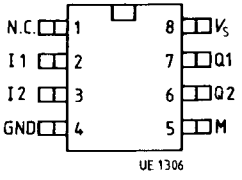


Pin Configuration
(top view)

P-DIP-8



P-DSO-8



Pin Definitions and Functions

Pin No.	Symbol	Function
1	N.C.	Not connected
2	I 1	Input
3	I 2	Input
4	GND	Ground
5	M	Switch-over input M for prescaler ratio
6	Q2	Output
7	Q1	Output
8	V_S	Supply voltage

Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Remarks
		min.	max.	Unit	
Supply voltage	V_S	– 0.3	6	V	
Input voltage (pin 2, pin 3)	V_I		2.5	V_{PP}	
Output voltage (pin 6, pin 7)	V_Q		V_S	V	
Output current (pin 6, pin 7)	$-I_Q$		10	mA	
Input voltage (pin 5)	V_M	– 0.3	V_S	V	
Junction temperature	T_j		125	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance (system-air)	$R_{th\ SA}$		105	K/W	P-DIP-8 package
Overload resistance (ESD protection single discharge of 100 pF capacitor through a1.5 kΩ resistor to each pin)	V_{MOS}	– 2000	2000	V	not required pins float; pin 4 and pin 8 always to ground

Operating Range

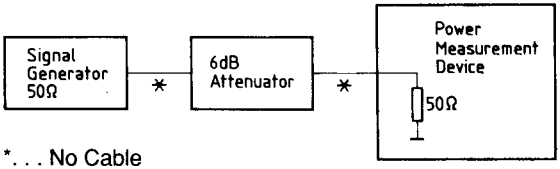
Supply voltage	V_S	4.5	5.5	V	
Input frequency	f	70	1300	MHz	
Ambient temperature	T_A	0	80	°C	

Characteristics
V_S = 5 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Current comsumption	I_S		23.5	29.5	mA	inputs decoupled outputs n.c.; M n.c.	
Input level ("input sensitivity")	V_I	– 26/11		3/315	dBm/mV	70 MHz	1
		– 27/10		3/315	dBm/mV	80 MHz	1
		– 30/7		3/315	dBm/mV	120 MHz	1
		– 32/5.5		3/315	dBm/mV	250 MHz	1
		– 27/10		3/315	dBm/mV	600 MHz	1
		– 27/10		3/315	dBm/mV	1000 MHz	1
		– 22/18		3/315	dBm/mV	1100 MHz	1
		– 15/40		3/315	dBm/mV	1200 MHz	1
		– 9/80		3/315	dBm/mV	1300 MHz	1
Output volt. deviation	V_Q	0.4	0.6		V_{PP}	$C_L \leq 15$ pF; $f \leq 1000$ MHz	1
		0.8	0.9		V_{pp}	$C_L \leq 15$ pF; $f \leq 1$ GHz	1
DC voltage offset of outputs	ΔV_Q			100	mV		3
M-input current "LOW" (prescaler ratio 1:256)	I_M		2	100	µA	M = ground	1
M-input current "HIGH" (prescaler ratio 1:64)	I_M		0	50	µA	M = V_S	1
M-input voltage "HIGH"	V_{MH}	3.0			V		1
M-input voltage "LOW"	V_{ML}			0.2	V		1
Amplitude of the 3rd harmonic at output (referenced to 1st harmonic)	A_3		– 30		dB	f = 700-900MHz;	1,4
			– 35		dB	M = V_S	2,4

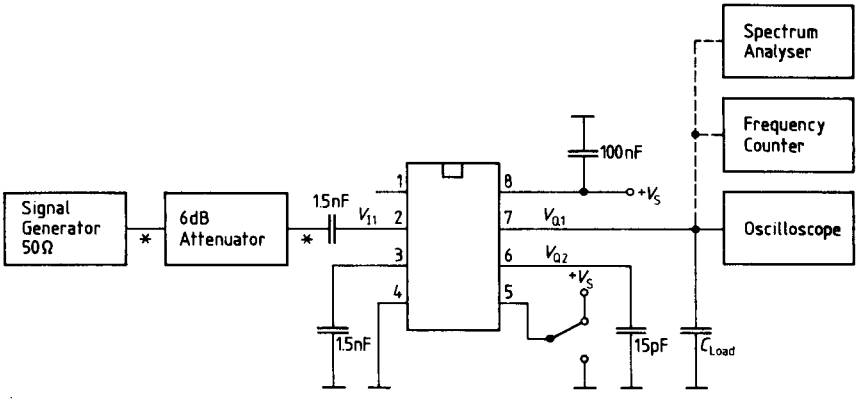
Test Circuit 1

Calibration of Signal Generator



*. . . No Cable

Measurement Configuration for Input Sensivity and Output Voltage Deviation

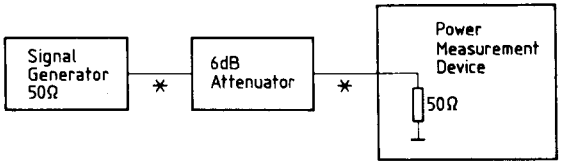


*. . . No Cable

C_{Load}+capacities of the measurement devices = 15 pF (for measurement of the output voltage deviation)

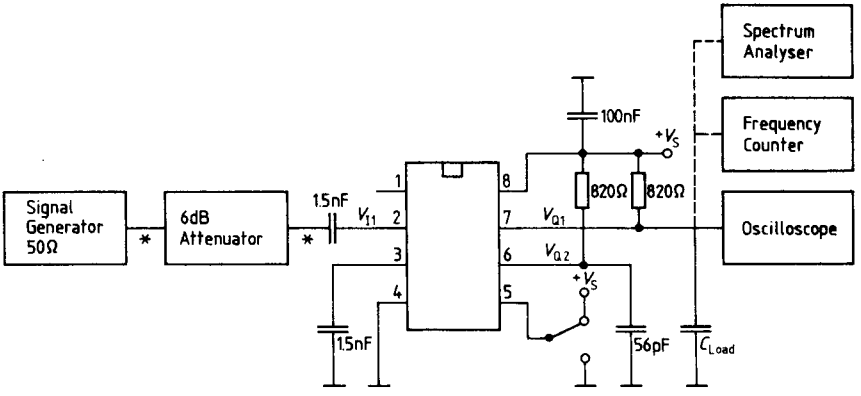
Test Circuit 2

Calibration of Signal Generator



*. . . No Cable

Measurement Configuration for Input Sensivity and Output Voltage Deviation

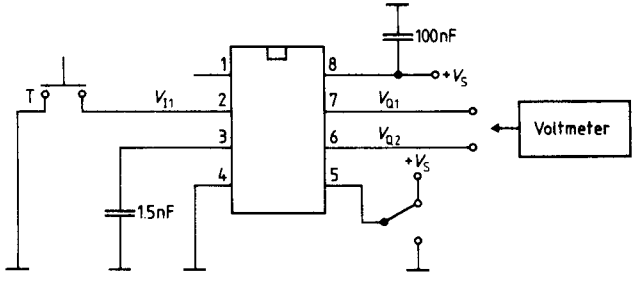


*. . . No Cable

C_{Load}+capacities of the measurement devices = 15 pF (for measurement of the output voltage deviation)

Test Circuit 3

DC Voltage Offset Measurement of Outputs



Note: press key T until outputs turn over