SIEMENS

Analog-Digital-Interface for Inserted Picture

SDA 9087

Preliminary Data

MOS IC

Features

- 3 separate A/D converters
- Resolution: 5 bit
- Sampling rate: 13.5 MHz, 3.375 MHz
- Clamping crcuit for the inut sgnals
- Adjustable delay for the luminance signal (9 steps)
- Color difference signals Y and V can be inverted
- Multiplexed output interface (DMSD compatible)
- Internal clock synchronization by sandcastle signal
- System clock generation for picture insertion processor
- BLN synch signal

Type	Ordering Code	Package
SDA 9087	Q67100-H8707	P-DIP-28

Description

Together with an analog color decoder and a sync separator for the H, V sync signals, the SDA 9087 forms an analog picture channel on whose input the analog CVBS signal is applied. This output produces the digital components Y, U, V plus the sync signals of this CVBS signal. The resolution of the digital output signals is 5 bit.

Furthermore, with the aid of PLL, the SDA 9087 generates the line locked clock LL3 (nom. 13.5 MHz) and the blanking signal BLN.

The picture channel described can replace a high-grade and costly digital picture channel consisting of the devices 7-bit ADC, digital multi-standard decoder (DMSD) and central clock generator (CCG).However, the quality of the picture is reduced , and for this reason the more obvious application is as a picture channel for the inset picture that is inserted in a picture-in-picture (PIP) system.

Y, U and V are digitized by 5-bit flash converters and output in a format that matches the interface of the PIP processor. The PLL synchronizes to an external, horizontal sync signal that is derived from the CCV signal of the inset picture.

Circuit Description

The luminance signal Y and the chrominance signals U, V are fed to the SDA 9087 by means of coupling capacitors. The black level of Y is clamped to V_{REFL}; the color subcarrier must be filtered out of Y.

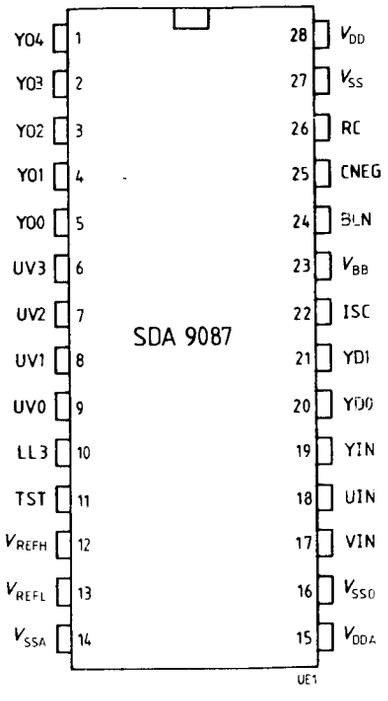
The three signals components are digitized by 5-bit A/D flash converters; the sampling rate is determined by LL3. Y is output as binary offset code. The digitized Y signal is delayed in a delay block. This delay can be varied in increments of two LL3 cycles in a range of 0 through 16 LL3 cycles on pins YD0,1 to compensate for different delays in the preceding luminance and chrominance decoders.

The white level of U and V is clamped to 0.5 x (V_{REFH} + V_{REFL}). U, V are then converted into a 5-bit two's complement code. The digitized U, V signals can be inverted via CNEG control input. A multiplexer selects every fourth U, V sample and applies this 10-bit information in four clock cycles in a nibble format to pins UV (0:3).

The horizontal PLL, consisting of a horizontal timer, phase comparator and VCO, generates the line-locked picture-in-picture system clock LL3 and the internal chip timing.

The horizontal timer divides the LL3 clock by 864 (the same for PAL and NTSC) and applies this signal as a horizontal reference signal to the phase comparator (PC). The external horizontal signal is decoded from the sandcastle signal and matched in its pulse width (= 345 LL3 cycles) to the reference signal. The digital phase comparator is frequency- and phase-sensitivite (type 4) and produces current pulses at its output. The up/down pulses of the phase comparator are filtered on pin RC. The filtered signal is the control voltage of the VCO. The horizontal timer also determines the start time and the width of the clamping pulse as well as the location of the blanking signal BLN, which in turn defines the horizontal duration of the picture information on the Y output and should be synchronous with it. BLN is consequently delayed to the same degree as Y.

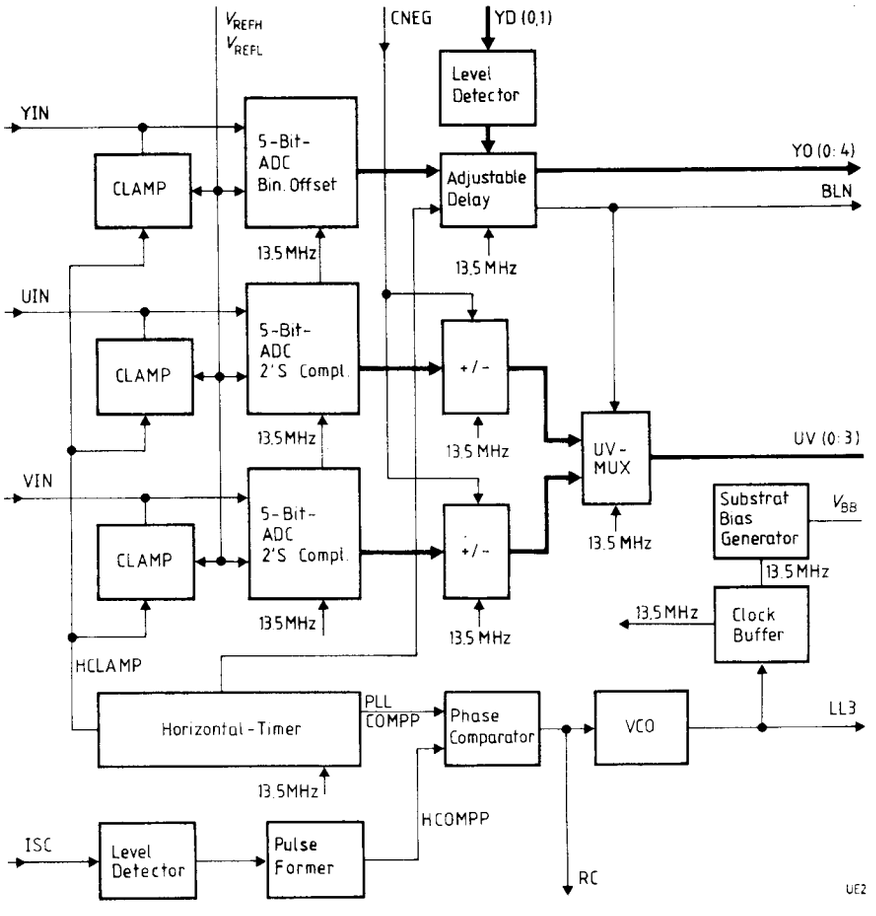
Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1-5	YO (4:0)	O	Digital Y output signal (Index 0 = LBS)
6-9	UV (3:0)	O	Digital Chrominance signal (nibble format)
10	LL3	O	Output of the line locked system clock (nom. 13.5 MHz)
11	TST	I	Test pin, to be switched at V_{SS} or open no wiring = L level
12	V_{REFH}		High reference voltage for the A/D converter
13	V_{REFL}		Low reference voltage for the A/D converter
14	V_{SSA}		Analog ground
15	V_{DDA}		Analog 5 V supply voltage
16	V_{SSO}		V_{SS} connection for the oscillator
17	VIN	I	Analog input for the V signal
18	UIN	I	Analog input for the U signal
19	YIN	I	Analog input for the Y signal
20, 21	YD0, YD1	I	To adjust the Y delay No wiring = L level
22	ISC	I	Input for the sandcastle-synchronous signal of the gate signal
23	V_{BB}		Substrate bias (internally produced)
24	BLN	O	Blanking signal output
25	CNEG	I	Color negated. By H level the crominance signals are multiplied by 1 and are output. No wiring = L level
26	RC	O	Pin to the analog loop filter connection of the PLL
27	V_{SS}		Digital ground
28	V_{DD}		Digital 5 V supply voltage

Block Diagram



Absolute Maximum Ratings
T_A = 0 to 70 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
	V_{DDA}	– 0.3	6	V
Voltages at I/O pins	V_{IN}	– 0.3	7	V
Voltages differences between $V_{REF\,H}$ and $V_{REF\,L}$	ΔV_{REF}	– 4	4	V
Ambient temperature	T_A	– 20	70	C
Storage temperature	T_{stg}	– 20	125	C
Power dissipation	P_{tot}		0.8	W

Operating Range

Supply voltages	V_{DD}	4.5	5.5	V
	V_{DDA}	4.5	5.5	V
Ambient temperature	T_A	0	70	°C
Reference voltage	$V_{REF\,H}$	2.5	3.5	V
	$V_{REF\,L}$	1.5	2.5	V

Characteristics
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Voltages	V_{DD} V_{DDA}	4.5 4.5	5 5	5.5 5.5	V V	
Current consumption	I_{DD} total		100	120	mA	
Digital Output Y0 (0:4), UV (0:3), BLN, LL3						
Load capacitance	C_L	0		20	pF	
Low level High level	V_{QL} V_{QH}	0 2.4		0.4	V V	I_{QL} = 1.6 mA I_{QH} = – 0.2 mA
Delay to the negative transition of LL3	t_d			14	ns	LL3 = V_{QL}
LL3 Pulse Form						
Rise time	t_{LL3R}	0		7	ns	
Fall time	t_{LL3F}	0		5	ns	
H-pulse widh	t_{LL3H}	28			ns	T_{LL3} = 68 ns
L-pulse widh	t_{LL3L}	28			ns	T_{LL3} = 68 ns
LL3 period duration	T_{LL3}	< 68	74	< 80.6	ns	
Digital Input						
CNEG						
Low level High level	V_{CNL} V_{CNH}	 2.0		0.8	V V	
Input current	I_{CN}			30	µA	V_{CNH} = 5 V
YD (0,1)						
Low level Mid level High level	V_{YDL} V_{YDM} V_{YDH}	 2.0 4.0		0.8 0.55 V_{DD}	V V V	
Input current	I_{CN}			30	µA	V_{CNH} = 5 V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Sandcastle Input ISC						
High level	V_{HSC}	3.5		V_{DD}	V	
Mid level	V_{ASC}			2.5	V	
Low level	V_{VSC}	0		V_{ASC}	V	
Switching threshold for High level			0.6 V_{DD}			
VCO **Sandcastle input ISC**						
Frequency range		< 12.4	13.5	> 14.7	MHz	
		< 12.4			MHz	V_{RC} = 1.0 V V_{DD} = 4.5 V T_A = 0 °C
				> 14.7	MHz	V_{RC} = 3.8 V V_{DD} = 5.5 V T_A = 70 °C
Phase Detector						
Pulse current	I_{PD}		160		µA	V_{DD} = 5 V
PLL Loop Filter (recommended value)						
R_1			3.8		kΩ	see application circuit
C_1			2.2		µF	
C_2			0.1		µF	
Analog Input YIN, UIN, VIN						
The dynamic range of the converter goes from $V_{REFL\text{-}intern}$ to $V_{REFH\text{-}intern}$ with:						
$V_{REFH\text{-}intern}$	= V_{REFH} – 30 mV typ.					
$V_{REFL\text{-}intern}$	= V_{REFL} + 30 mV typ.					
Clamping level YIN	= $V_{REFL\text{-}intern}$ +/–10 mV					
Clamping levels UIN, VIN	= 0.5 × ($V_{REFH\text{-}intern}$ + $V_{REFL\text{-}intern}$) +/–10 mV					

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input capacitance	C_{IN}		35		pF	
Leakage current at YIN, UIN, VIN	I_L		1.0		µA	$V_{YIN} = V_{UIN} = V_{VIN} = 3.0$ V $V_{REFH} = 3.0$ V $V_{REFL} = 2.0$ V
Internal resistance in clamping time for R_I of V_{REFH} and $V_{REFL} = 0\ \Omega$	R_{CU} = R_{CV} R_{CY}		 2.4 0.5	 3.0 1.0	 kΩ kΩ	$V_{REFH} = 3.0$ V $V_{REFL} = 2.0$ V
Start of the clamping pulse refer to the transmission of the horizontal ISC burst pulse	t_C		1.4*		µs	
Clamping pulse duration	t_{CPD}		0.666**		µs	
Coupling capacitor for YIN, UIN, VIN	C_U, C_V, C_Y		10		nF	

* (= 19 LL3 period)
** (= 9 LL3 period)

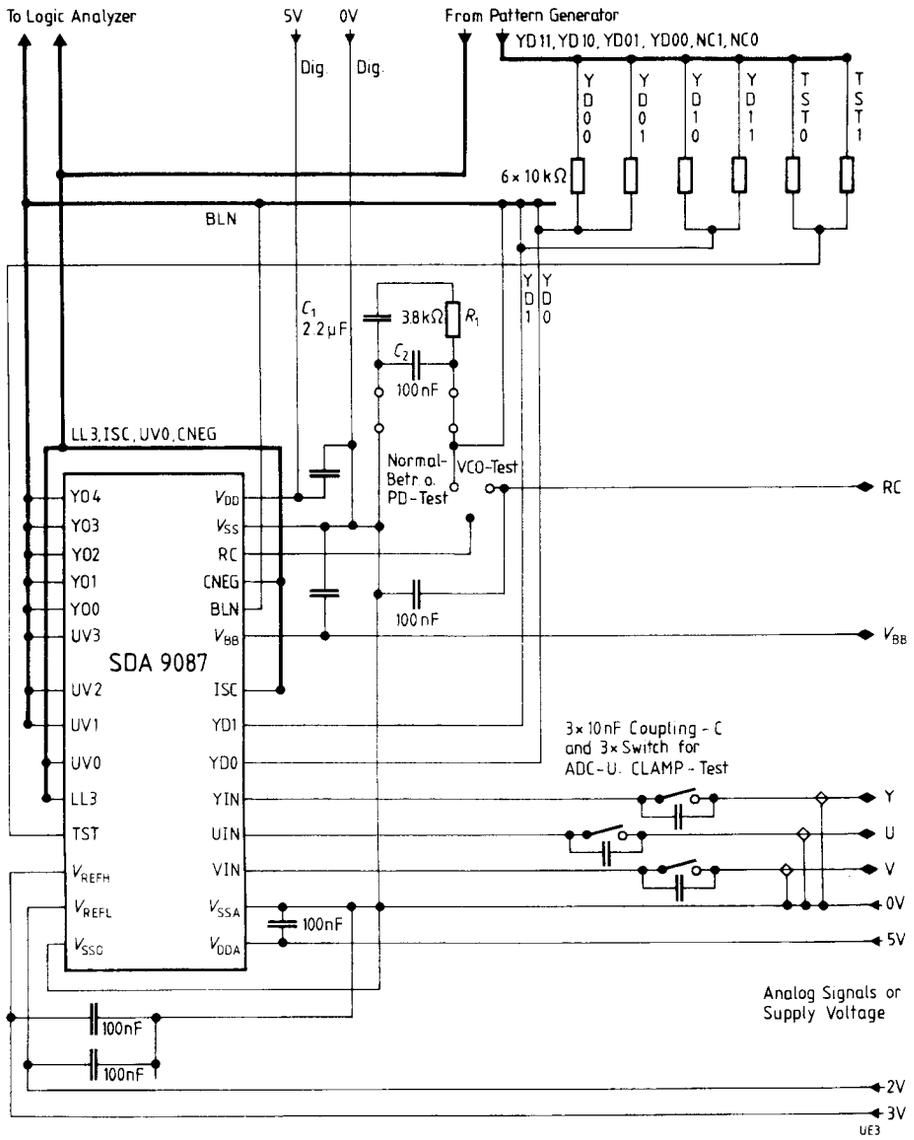
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic range of the converter ($V_{REF\,L}$ intern to $V_{REF\,H}$ intern)			0.95 × (V_{REFH} – V_{REFL})			
DC-Transfer-F Function of the A/D Converter						
Integral non-linearity*				+/- 1	LSB	$V_{REF\,H}$ = 3.0 V $V_{REF\,L}$ = 2.0 V
Differential non-linearity*				+/- 0.5	LSB	
Reference Voltage V_{REFH}, V_{REFL}						
Current consumption	$I_{REF\,H}$ $I_{REF\,L}$			2.5 – 2.5	mA mA	$V_{REF\,H}$ – $V_{REF\,L}$ = 1 V
$V_{REF\,H}$ $V_{REF\,L}$		2.5 1.5	3.0 2.0	3.5 2.5	V V	
Substrate Bias V_{BB}						
V_{BB}		– 2.6		– 1.6	V	V_{DD} = 5.0 V R_L between V_{BB} and V_{SS}> 100 kΩ

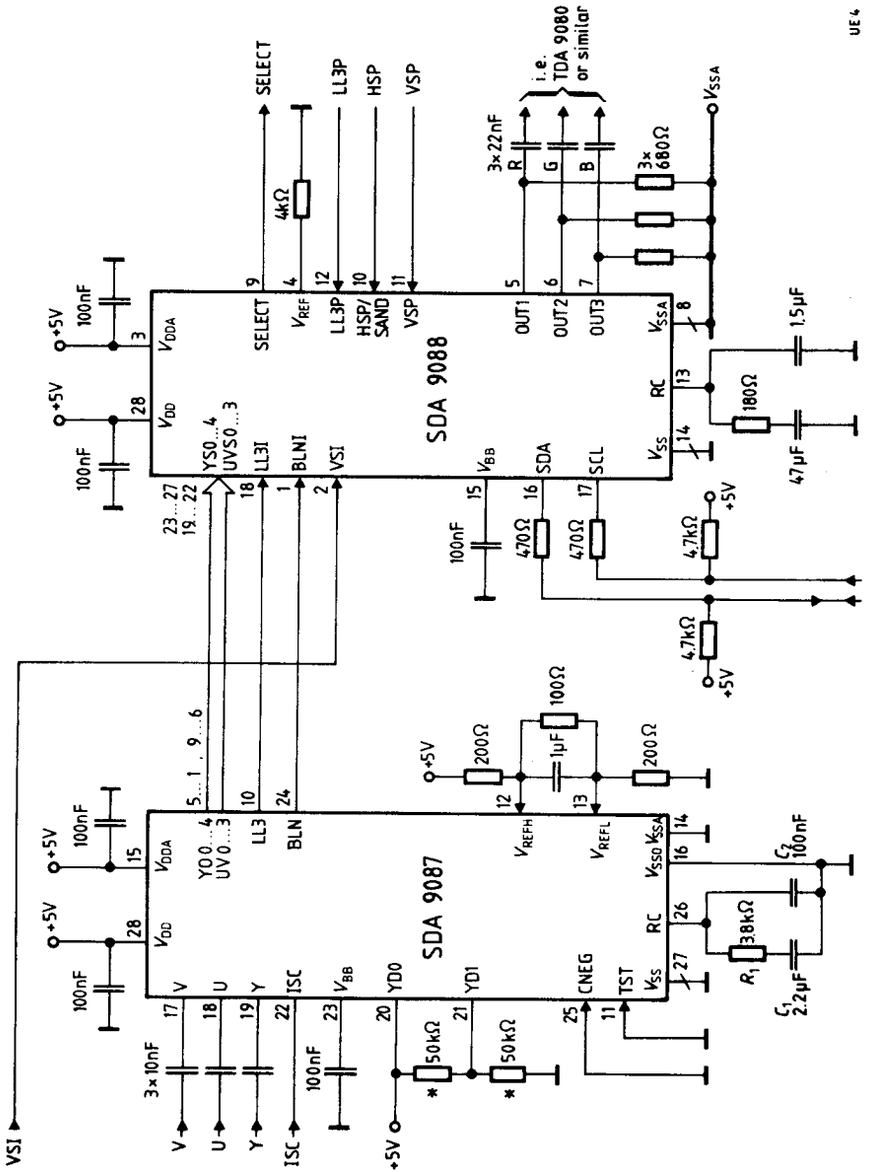
* The absolute tolerance of the coupling level and the converter characteristic line are not influenced by the difference V_{REFH} – V_{REFL} (dynamic range of the converter) which lead to big errors by

Measuring Circuit

Digital Signal or Supply Voltages

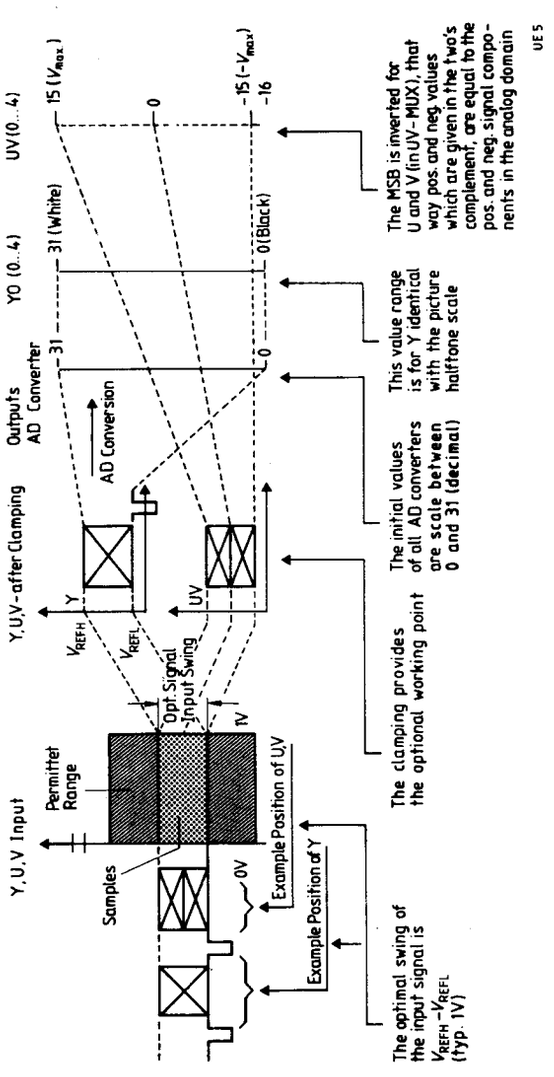


Application Circuit

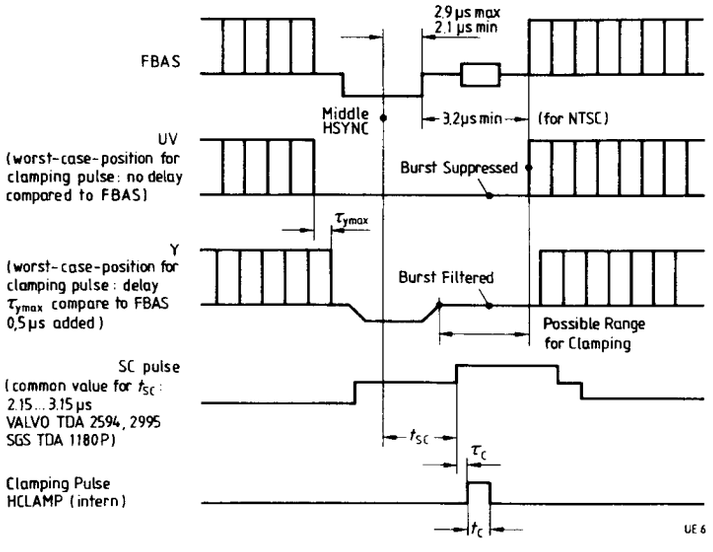


Pulse Diagram

Input Voltage Range of Y, U and V and them Translation in Initial Values ("Digital Values")



Clamping Pulse Timing



Leading edge at clamping pulse

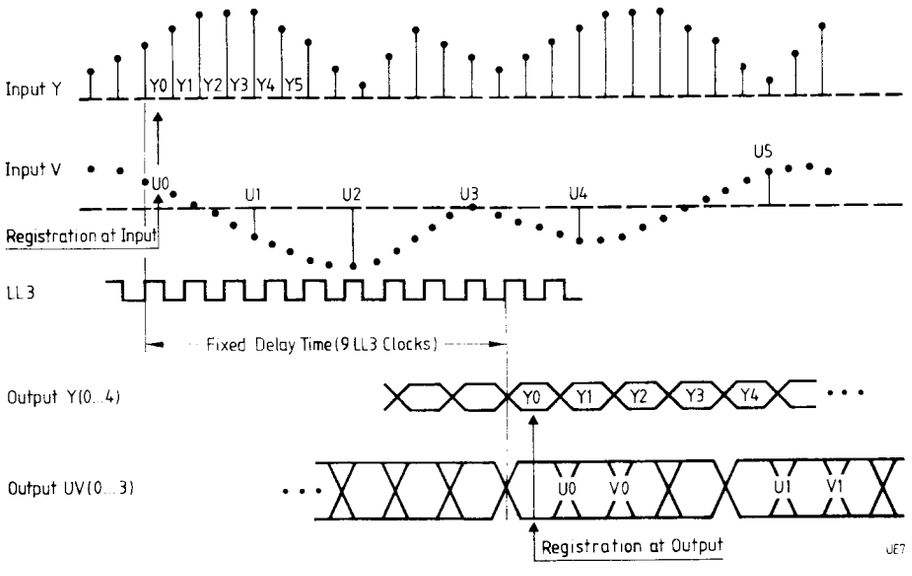
$t_{SC\,min} + \tau_C > 2.9\ \mu s + \tau_{ymax} \approx 3.4\ \mu s$
chosen: $\tau_C = 1.4\ \mu s$ (19 LL3 clocks)

Tailing edge at clamping pulse

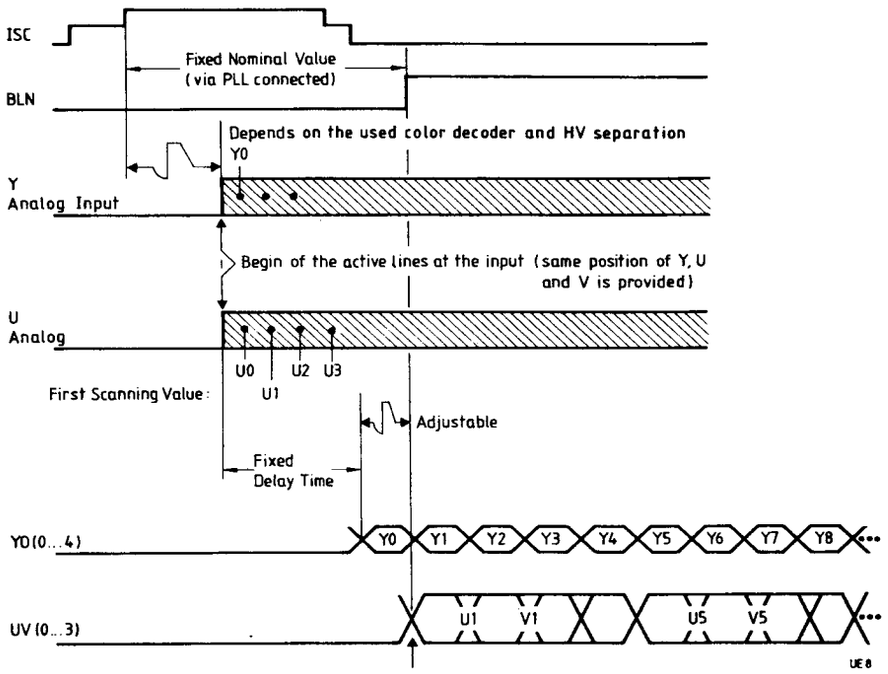
$t_{SC\,max} + \tau_C + t_C < 5.3\ \mu s = 3.2\ \mu s + 2.1\ \mu s$
chosen: $t_C = 0.7\ \mu s$ (9.5 LL3 clocks)

Signal Delay Time for U, V and Y
(used indication: number of scanning values).

Additionally programmable delay time in DELAY-Block-0.

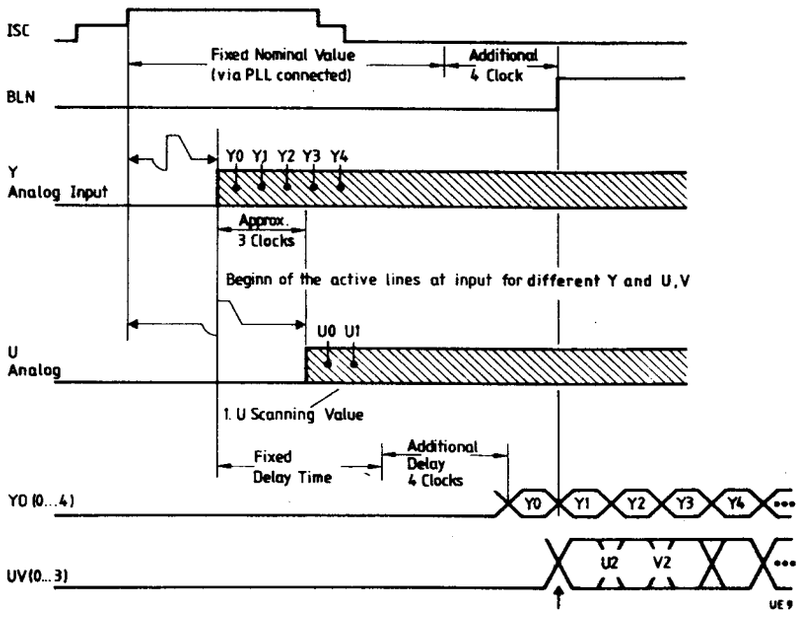


Relation between SC, BLN and Y and UV
(used indication: number of pixels)



- Y, U, V have no delay time differences.
- Delay between SC and Y, U, V is smaller than provided for the optimal case.

Relation between SC, BLN and Y and UV
(used indication: number of pixels)



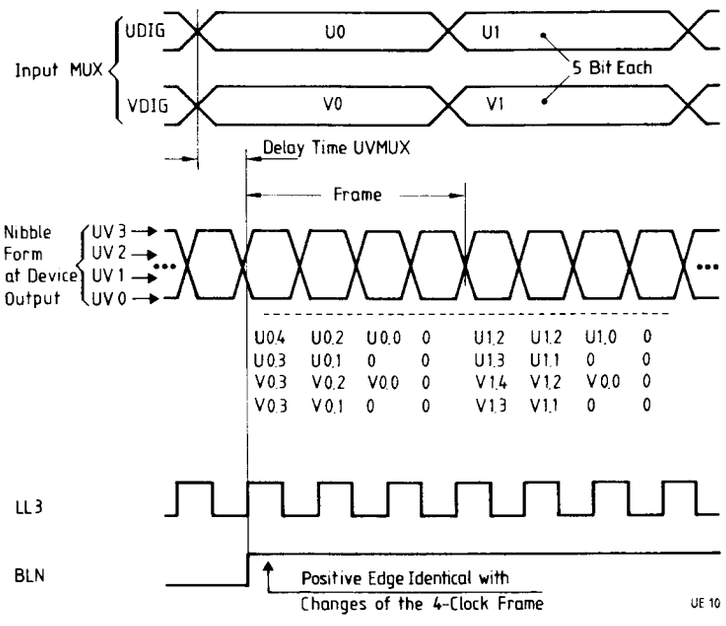
U, V are delayed approx. 3 LL3 clocks compare to Y;

Compensation through an additional Y-delay of 4 clocks.

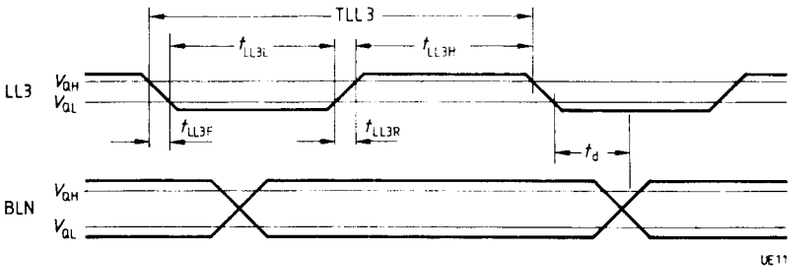
- BLN edge and raster correspond to each other;
- Begin of the active lines of Y0 (0 ... 4) and UV (0 ... 3) is moved.
- Registration errors still 1 clock (Y value 1 clock to late, because of 4 clocks delay, U-delay but only 3 clocks).

Conversion of U and V in a Nibble Form with 13.5 MHz, 4 Bit

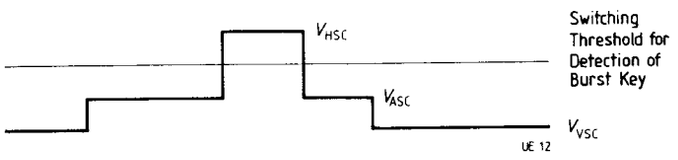
It means: 1. index: number of scanning value (pixels)
2. index: number of bits; 4 = MSB



Specification of Edges



Sandcastle Pulse



Adjusting of Y-Delay via YD0, YD1

Level Range		Additional Delay for Y and BLN	
PIN YD1	Pin YD0		
		LL3 clocks	typ. value
1	1	0	0
1	2	2	148 ns
1	3	4	296 ns
2	1	6	444 ns
2	2	8	592 ns
2	3	10	740 ns
3	1	12	888 ns
3	2	14	1.04 µs
3	3	16	1.18 µs

Level range:
1 = V_{YDL}
2 = V_{YDM}
3 = V_{YDH}

Function of SC Pulse Extention and Phase Comparison
(PLL is unlocked, behind the external H phase)