



SE4100L
PointCharger™ GPS Receiver IC
Preliminary Information

Applications

- Mobile phone & PDA accessories
- Portable navigation
- Personal security
- Security systems
- Asset tracking
- Telematics equipment

Features

- 30 mW power consumption
- 4x4mm 24 pin LPCC package
- Single conversion radio with integrated IF filters
- On-chip, Gain switchable LNA
- Low LNA noise figure, 1.3dB typ.
- On chip crystal oscillator can be powered up independently
- Fully integrated VCO, VCO tank circuit and PLL.
- Remote antenna current detection

Ordering Information

| Type | Package | Remark |
|-----------|-------------|------------------------|
| SE4100L-R | 24 Pin LPCC | Shipped in Tape & Reel |

Product Description

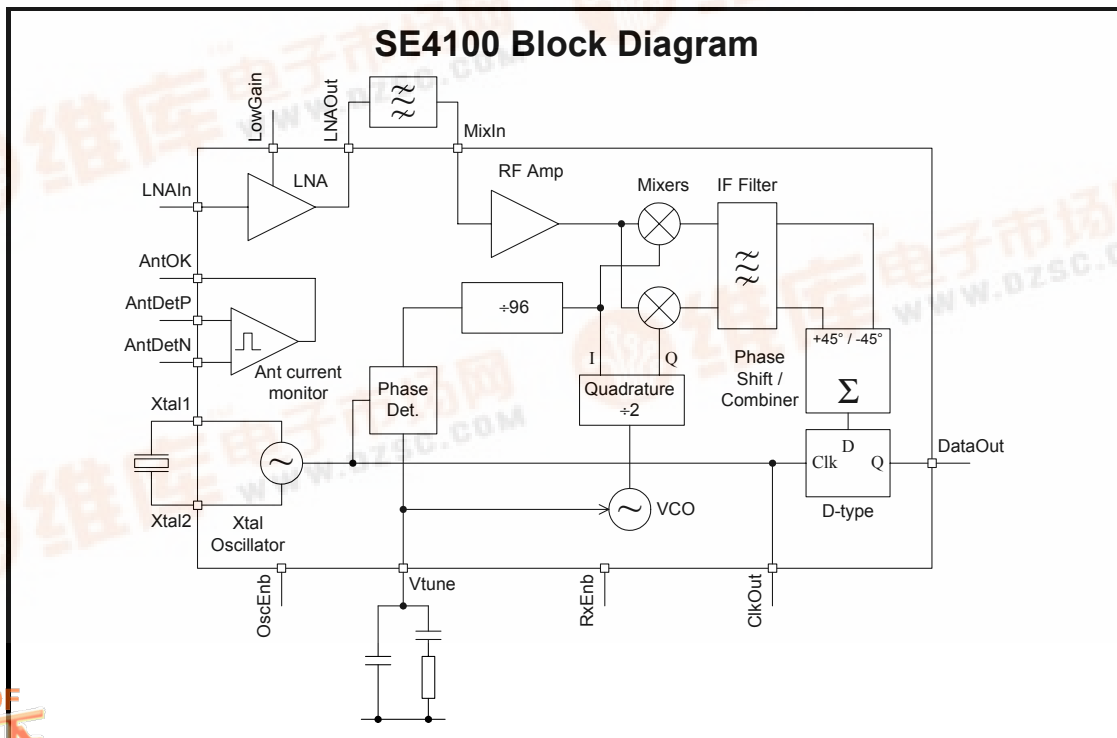
The SE4100 is an integrated GPS receiver designed to receive the L1 signal at 1575.42MHz. The receiver has a low IF architecture, and integrates all of the amplifier, oscillator, mixer and demodulation functions.

The external component count is low, requiring just a 16.368MHz crystal and 11 passive components in its minimum configuration. This and the 24 pin LPCC package result in a very small circuit footprint, which is complemented by just 30mW operating power.

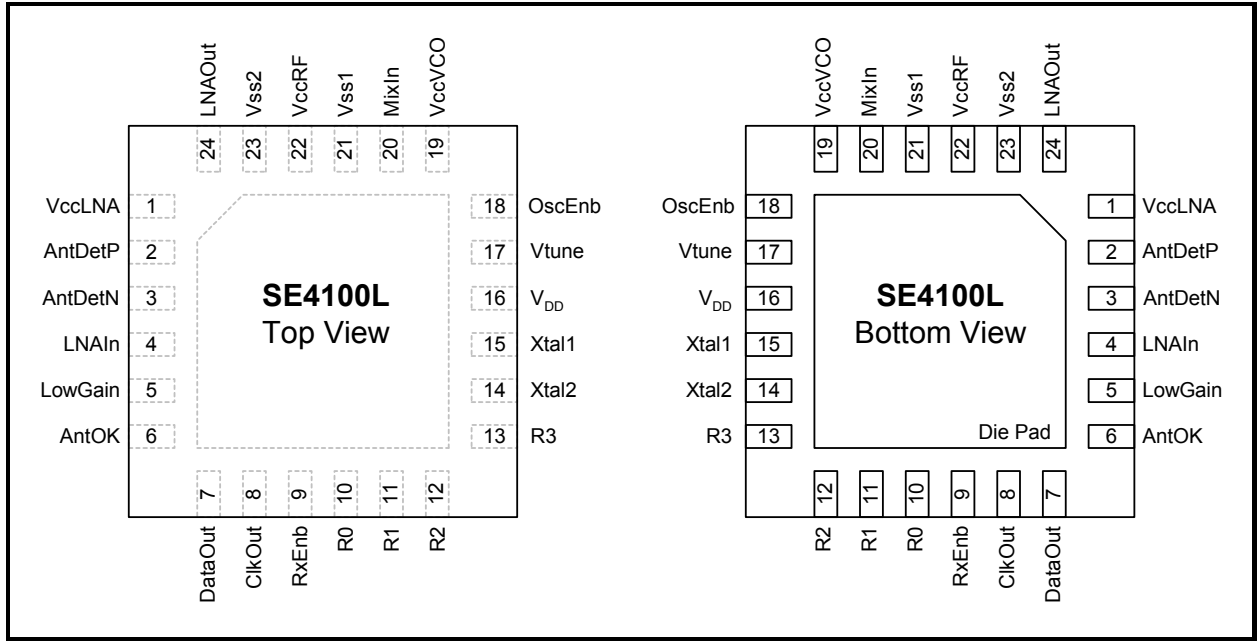
Two digitally controlled shutdown modes enable either to part to be powered down entirely or for just the 16 MHz clock supply to the baseband processor to be maintained.

A switchable gain LNA enables the SE4100 to be used with a local passive antenna or with a remote active antenna without changing the circuit configuration. The on-chip VCO and PLL generates the required LO frequency from the external 16.368MHz crystal. All of the VCO and LO chain is integrated. An image reject mixer downconverts the RF signal to a 4.092MHz IF. The integrated IF filter feeds a combiner, limiter and output latch. The output signal is a 1-bit quantized 4.092 MHz digital IF at CMOS levels.

Functional Block Diagram



Pin Out Diagram



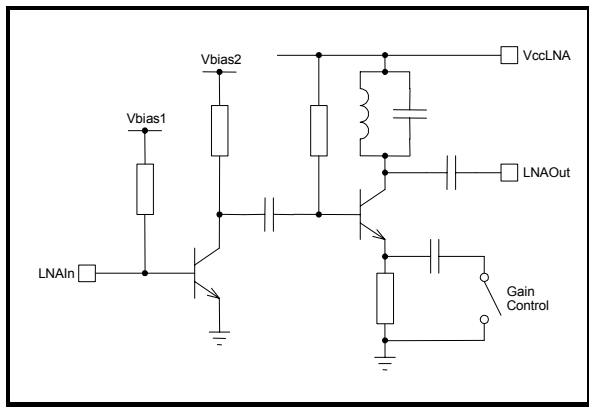
Pin Out Description

| Pin No. | Name | Description |
|---------|---------------------|--|
| 1 | VccLNA | Power supply connection for LNA |
| 2 | AntDetP | Connection to battery side of antenna current sensing resistor |
| 3 | AntDetN | Connection to antenna feed side of antenna current sensing resistor |
| 4 | LNAIn | LNA Input |
| 5 | LowGain | LNA Gain control, High = low gain |
| 6 | AntOK | Antenna OK output flag (high = antenna current OK) |
| 7 | DataOut | Data Output |
| 8 | ClkOut | Buffered version of Xtal Osc output / D-type clock |
| 9 | RxEnb | Enable control for Receiver (all circuits except Reference oscillator and Data Registers), active high input |
| 10 | R0 | Reserved internal connection, must be tied to V _{DD} for normal operation |
| 11 | R1 | Reserved internal connection, must be tied to V _{DD} for normal operation |
| 12 | R2 | Reserved internal connection, must be tied to V _{DD} for normal operation |
| 13 | R3 | Reserved internal connection, must be tied to V _{DD} for normal operation |
| 14 | Xtal2 | Connection to crystal |
| 15 | Xtal1 | Connection to crystal |
| 16 | V _{DD} | Power supply for digital circuits (Xtal Oscillator, Data Registers and Bias circuits) |
| 17 | Vtune | Charge pump output / VCO control voltage input |
| 18 | OscEnb | Enable control for Reference oscillator, active high input |
| 19 | V _{CC} VCO | Decoupling connection for VCO power supply |
| 20 | MixIn | Mixer input signal, 50Ω single ended |
| 21 | V _{SS} 1 | Ground |
| 22 | V _{CC} RF | Power supply connection for all RF circuits except the LNA |
| 23 | V _{SS} 2 | Ground |
| 24 | LNAOut | LNA Output, 50Ω single ended |
| Die Pad | Gnd | Ground connection for all circuits via die pad |

Functional Description

LNA

The internal LNA consists of two transistors cascaded. The biasing, gain switching circuit and output matching to 50Ω is contained on the IC. A conceptual diagram of the internal circuit is shown below.



The input match to 50Ω requires three external components, two capacitors and an inductor. The inductor should be a high Q type, e.g. wirewound or microstrip; otherwise the low noise figure of the LNA will not be obtained.

The output match is optimized to allow for a short length of narrow track between the IC package and a filter. Exact lengths and track widths will depend on the board material and thickness.

The gain of the amplifier is switched between high and low settings by the CMOS level compatible LowGain input pin. Internally, this reduces the gain of the second stage only in the low gain setting, which maintains a low noise figure for the amplifier.

The power supply for the amplifier is provided through the VccLNA pin. Care should be taken with the PCB layout to ensure that the power supply cannot act as a bypass around any filter between the LNA output and the mixer input.

Antenna Current Monitor

The antenna current monitor is a window comparator designed to operate with common mode input voltages above the chip V_{CC}. It is designed to monitor the supply current to an external active antenna and provide a logic output indicating if the current is within the desired range.

The state of the logic output on the AntOK pin is dependent on the voltage drop between AntDetP and AntDetN pins, AntDetP being the higher dc voltage. The current setting this voltage is adjusted by changing the value of the external current sense resistor between these pins.

| Voltage between AntDetP and AntDetN (ΔV_{ANT}) | Logic Output AntOK |
|--|--------------------|
| <0.125 | Low |
| 0.25 > ΔV > 0.5 | High |
| >0.75 | Low |

The AntOK pin is a CMOS output designed to interface directly to the LowGain input pin, so that in the event the supply to the external active antenna is either shorted or open circuited, the internal LNA gain is switched to the high gain setting.

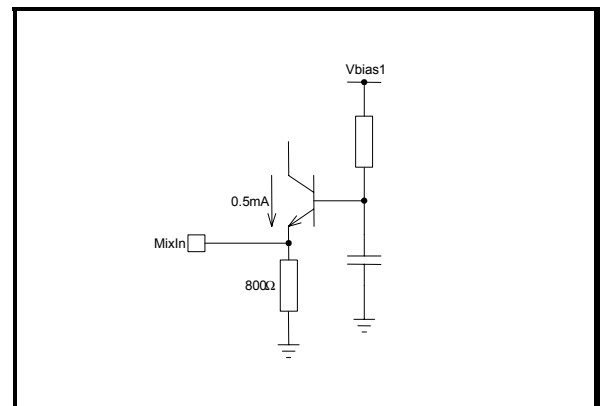
The external current sense resistor should be chosen according to the typical current of the external antenna I_{ANT}, using the formula:

$$R_{EXT} = \frac{0.375}{I_{ANT}}$$

Mixer RF Input

The mixer RF input pin, MixIn, is a single ended 50Ω input, designed to either interface to the LNAOut pin or to the output of an external filter using only a dc blocking capacitor, and without additional matching components.

The input is a common base configuration providing a wideband 50Ω termination. A conceptual diagram of the input circuit is shown below:



The filter type chosen should require a termination impedance of $50+j0\Omega$. Examples of suitable types are shown on the application schematic diagram.

The PCB layout should keep the track from the filter to the MixIn pin as short as possible to minimize pickup and mismatch (if the track is not 50Ω). A dc blocking capacitor should be used, even if the filter does not present a dc path, as the MixIn pin has 0.4V dc present which may be detrimental to the filter.

A filter will improve the performance of the receiver in the presence of out of band blocking signals, but is not essential if operation in the presence of such signals is not critical. If the filter is not fitted, the LNAOut pin should be connected to the MixIn pin via a coupling capacitor.

PLL and Loop Filter

The entire phase-locked loop generating the local oscillator for the mixer is contained on-chip, with the exception of the loop filter.

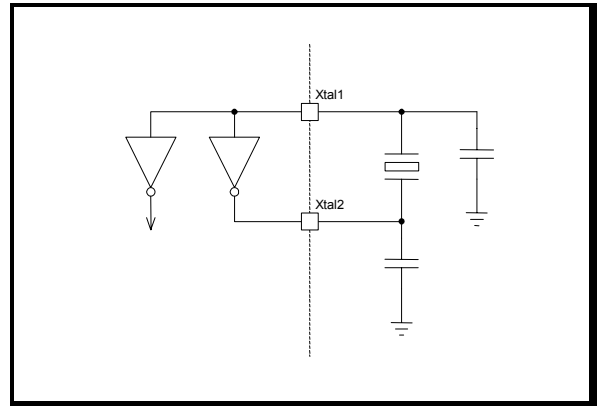
Values provided on the application circuit should be used, as these will provide optimum performance under all conditions.

The capacitors may be ceramic dielectric types, with either COG/NP0 or X7R dielectric. Higher capacitance per unit volume dielectrics should be avoided as the absolute tolerance and temperature stability may compromise system performance.

The PCB layout should keep the track from the Vtune pin to the loop filter as short as possible to minimize noise pickup.

Crystal Oscillator

The crystal oscillator is a Pierce configuration, as shown in the diagram below. The application circuit is designed to work with parallel resonant crystals with a load capacitance of 12pF.



The PCB layout should minimize the lengths of the tracks to Xtal1 and Xtal2 pins. The capacitors at each terminal of the crystal should be mounted adjacent to the crystal and have a low impedance connection to the ground plane.

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below.

This device is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

| Symbol | Parameter | Min. | Max. | Unit |
|----------------------------|---|------|--------------|------|
| V_{CC}, V_{DD} | Supply Voltage | -0.3 | +4.6 | V |
| | Voltage On Any Pin With Respect To V_{SS} except AntDetP and AntDetN Pins | -0.3 | $V_{DD}+0.3$ | V |
| $V_{AntDetP}, V_{AntDetN}$ | Voltage On AntDetP and AntDetN Pins With Respect To V_{SS} | -0.3 | +6.0 | V |
| T_{STG} | Storage Temperature Range | -65 | +150 | °C |

Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|-----------------------|------|------|------|------|
| T_A | Operating Temperature | -40 | +25 | +85 | °C |
| V_{CC}, V_{DD} | Supply Voltage | 2.7 | | 3.6 | V |

DC Electrical Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| I_{CC} | Total Supply Current, All Circuits Active | | 9 | | mA |
| $I_{CC(OSC)}$ | Supply Current, Oscillator Only Active | | 1.0 | | mA |
| $I_{CC(OFF)}$ | Supply Current, No Circuits Active | | | 10 | μA |

AC Electrical Characteristics

| LNA | | | | | | |
|--------------------|--|------|----------------------|--------|------|------|
| Symbol | Parameter | Note | Min. | Typ. | Max. | Unit |
| V _{CCLNA} | LNA Supply Voltage | | 2.7 | | 3.6 | V |
| I _{CC} | Supply Current , RxEnb = '1' | | | 1.2 | | mA |
| S ₂₁ | Forward Gain, f _{RF} =1570MHz to 1580MHz, LowGain = '0', P _{in} = -80dBm | | | 20 | | dB |
| NF | Noise Figure, f _{RF} =1570MHz to 1580MHz, LowGain = '0' | | | 1.3 | | dB |
| S _{21LOW} | Forward Gain, f _{RF} =1570MHz to 1580MHz, LowGain = '1', P _{in} = -80dBm | | | 7 | | dB |
| NF | Noise Figure, f _{RF} =1570MHz to 1580MHz, LowGain = '1' | | | 2.5 | 4 | dB |
| Z ₁₁ | Input Impedance, Single Ended Input, With External Matching Circuit | | | 30-j75 | | Ω |
| S ₂₂ | Output Return Loss, 50Ω system, Single Ended Output | | | | -10 | dB |
| IIP _{3H} | High Gain Mode Input IP3, Tones At 1575 ± 5MHz @ -60dBm | | | -25 | | dBm |
| IIP _{3L} | Low Gain Mode Input IP3, Tones At 1575 ± 5MHz @ -60dBm | | | -15 | | dBm |
| P1dB | Input Power At Which Gain Falls By 1dBm | | | -34 | | dBm |
| t _R | Recovery Time From -3dBm Input Overload Signal | | | 4 | 10 | μsec |
| V _{IL} | Input Low Level, LowGain Input | | | | 0.6 | V |
| V _{IH} | Input High Level, LowGain Input | | V _{DD} -0.6 | | | V |
| I _{IN} | LowGain Input Current | | -0.1 | | 0.1 | μA |

| Receiver | | | | | | |
|-----------------|---|------|------|-------|------|------|
| Symbol | Parameter | Note | Min. | Typ. | Max. | Unit |
| I _{CC} | Supply Current , RxEnb = '1' | | | 8.0 | | mA |
| NF | Noise Figure, f _{RF} =1570MHz To 1580MHz, Input to 'MixIn' | | | 10 | | dB |
| IIP3 | Input IP3, Tones 1575 ± 5MHz @ -40dBm (Mixer and IF Filter Only) | | | -15 | | dBm |
| S11 | Input Return Loss, 50Ω System | | | | -10 | dB |
| t _R | Recovery Time From -30dBm Input Overload Signal | | | 4 | 10 | μsec |
| f _{IF} | IF Centre Frequency | | | 4.092 | | MHz |
| BW | -3dB Bandwidth | | | 2.0 | | MHz |
| ΔT _g | Group Delay Variation, f _C ± BW/2 | | | 0.1 | | μsec |
| AV ₂ | Attenuation At f _C ± BW | | | 11 | | dB |
| AV ₄ | Attenuation At f _C ± 2.BW | | | 27 | | dB |

| VCO and Local Oscillator | | | | | | |
|--------------------------|-------------------------------------|------|------|----------|------|--------|
| Symbol | Parameter | Note | Min. | Typ. | Max. | Unit |
| f _{VCO} | VCO Centre frequency | | | 3142.656 | | MHz |
| L _{1k} | LO SSB Phase noise at 1kHz offset | | | | -65 | dBc/Hz |
| L _{10k} | LO SSB Phase noise at 10kHz offset | | | | -65 | dBc/Hz |
| L _{100k} | LO SSB Phase noise at 100kHz offset | | | | -85 | dBc/Hz |

| Crystal Oscillator | | | | | | |
|--------------------|---|------|------|----------------|------|------|
| Symbol | Parameter | Note | Min. | Typ. | Max. | Unit |
| I _{CC} | Supply Current, Crystal Oscillator And Clock Buffers, OscEnb = '1' | | | 1.0 | | mA |
| f _{XTAL} | Oscillator Frequency | | | 16.368 | | MHz |
| | Crystal Parameters | | | | | |
| | Mode | | | Parallel fund. | | |
| | Frequency | | | 16.368 | | MHz |
| | ESR | | | | 50 | Ω |
| | C _{LOAD} | | | 12 | | pF |
| t _{START} | Oscillator Startup Time To 95% Of Final Amplitude And Within 10ppm Of Final Frequency | | | | 100 | μsec |

| Antenna Current Monitor | | | | | | |
|-------------------------|--|------|---------|------|-------|------|
| Symbol | Parameter | Note | Min. | Typ. | Max. | Unit |
| ΔV_{ANT} | Voltage Between AntDetP And AntDetN For AntOK = High | | 0.25 | | 0.5 | V |
| ΔV_{ANT} | Voltage Between AntDetP And AntDetN For AntOK = Low For Low Current Condition | | | | 0.125 | V |
| ΔV_{ANT} | Voltage Between AntDetP And AntDetN For AntOK = Low For High Current Condition | | 0.75 | | | V |
| $V_{AntDetP}$ | Voltage Range On AntDetP For Normal Operation | | Vcc-0.5 | | 5.25 | V |
| V_{AntOK} | AntOK Output Voltage, Antenna OK, 1mA Current Source | | Vcc-0.5 | | Vcc | V |
| V_{AntOK} | AntOK Output Voltage, Antenna Not OK, 1mA Current Sink | | 0 | | 0.5 | V |

Timing Characteristics

| Symbol | Parameter | Note | Min. | Typ. | Max. | Unit |
|-------------|----------------------------|------|------|------|------|------|
| t_{PER} | Clock Period | | 60 | | | nsec |
| t_{PWL} | Clock Low Width | | 20 | | | nsec |
| t_{PWH} | Clock High Width | | 20 | | | nsec |
| t_{DEL} | Clock To Data Delay Time | | | | 5 | nsec |
| t_{SETUP} | Setup Time | | 21 | | | nsec |
| t_{HOLD} | Hold Time | | 26 | | 31 | nsec |
| t_R | Rise Time, 10-90% | | | | 8 | nsec |
| $t_{R/F}$ | Rise and Fall Time, 10-90% | | | | 8 | nsec |

Output Data Timing Diagram

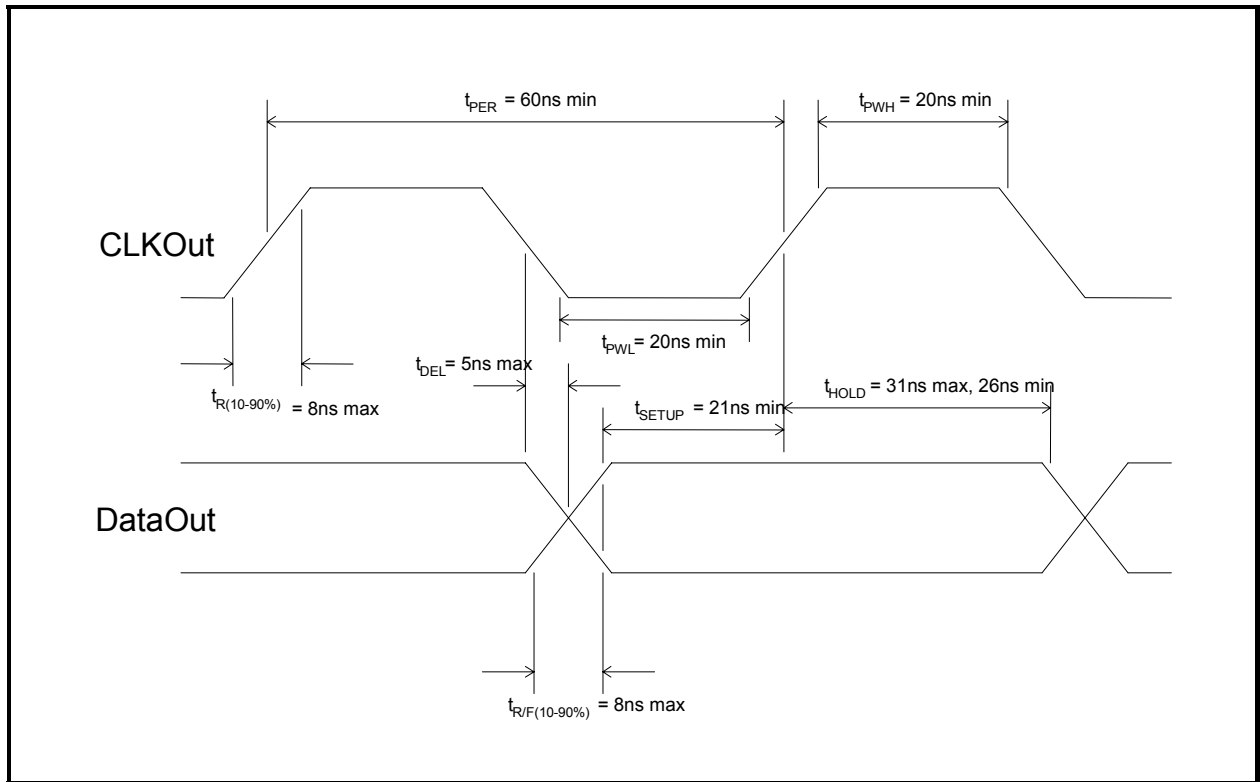


Figure 1: Typical Schematic Diagram

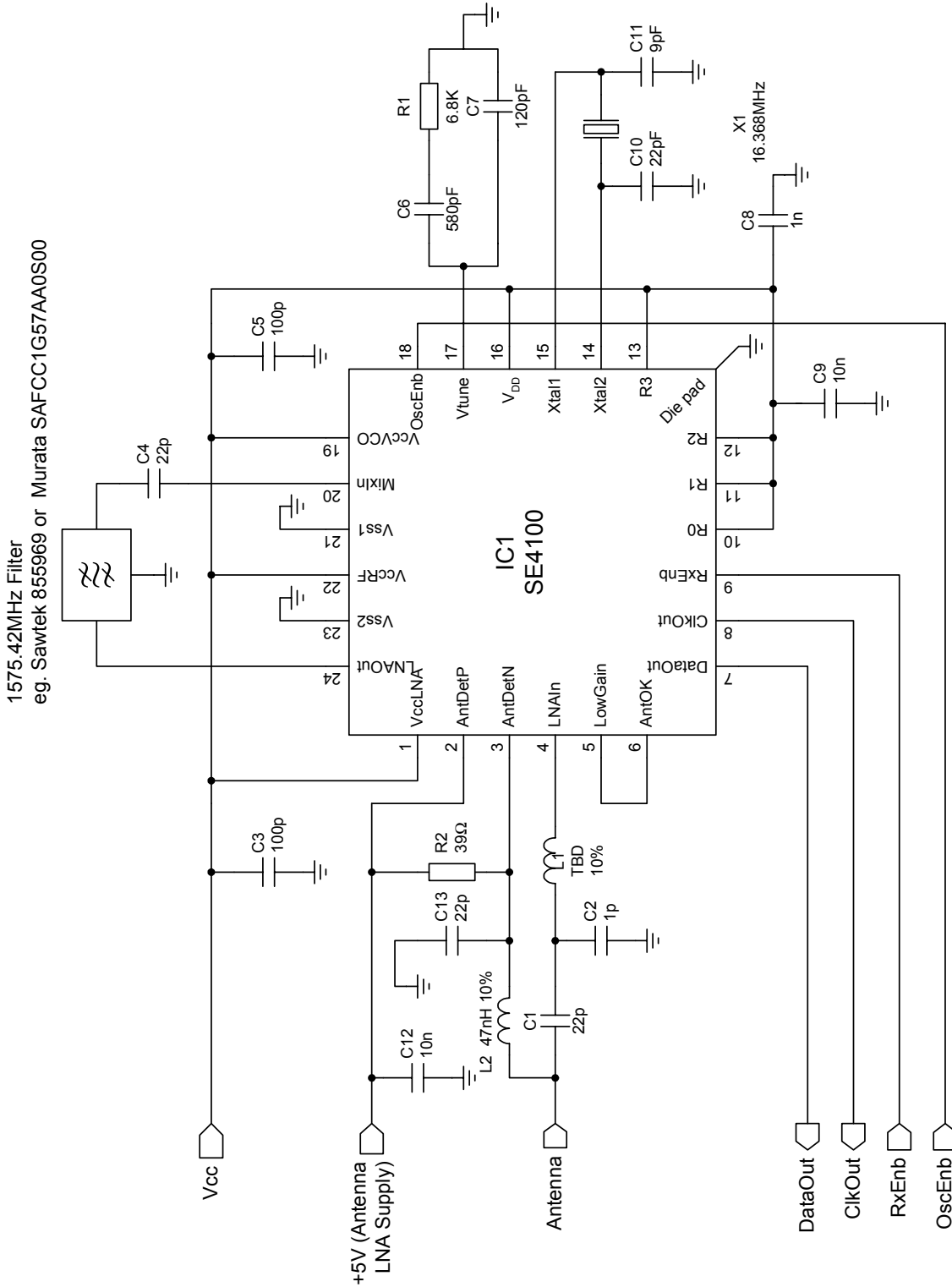
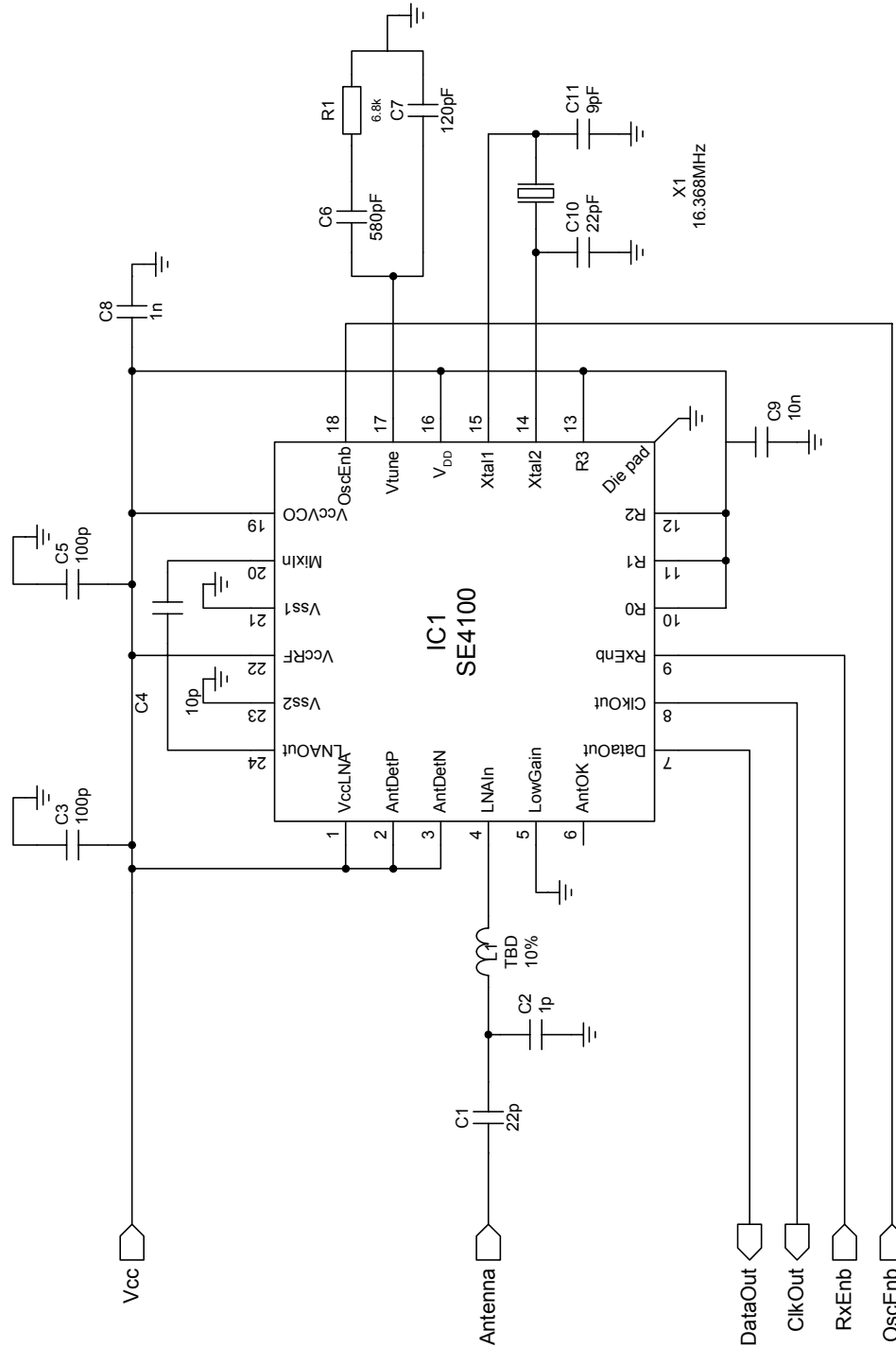
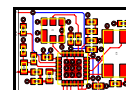
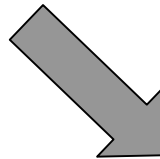
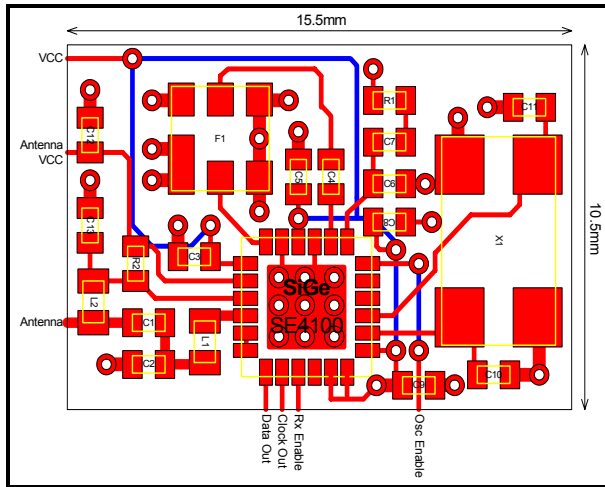


Figure 2: Minimum Component Count Application Schematic Diagram



Typical PCB Layout (With Filter And Antenna Current Sensing)

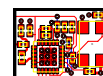
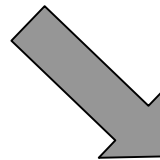
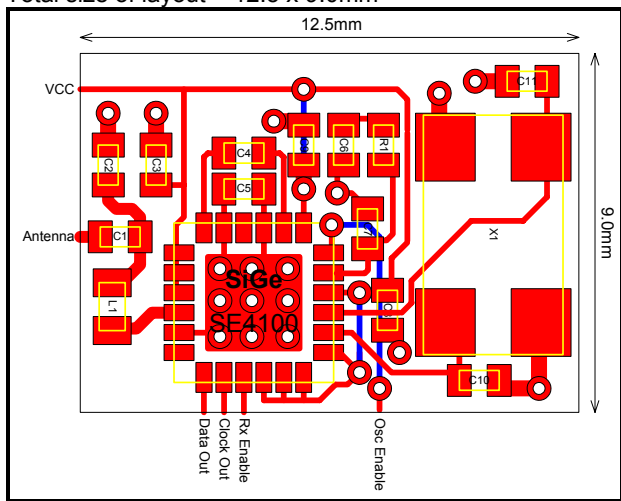
Total size of layout = 15.5 x 10.5mm



Actual size

Typical PCB Layout (Minimum Component Count)

Total size of layout = 12.5 x 9.0mm



Actual size

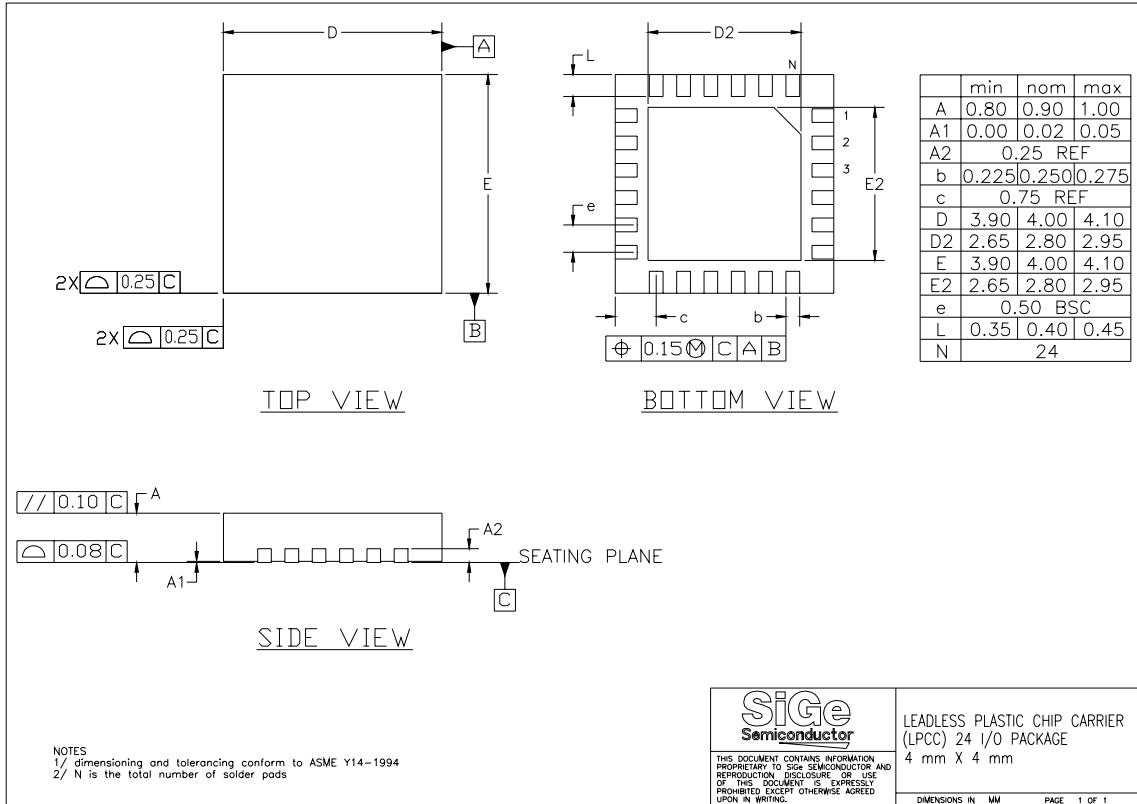
(R2, C12, C13, L2, F1 not used)

Note: These layouts are for illustration purposes only. Reference designs and layout information are available from SiGe Semiconductor.

Typical Bill Of Materials for Application PCB Layout

| Component | Value | Type | Manufacturer |
|-----------|------------|--------------|--------------|
| IC1 | | SE4100 | SiGe |
| C1 | 22pF | 0402 ceramic | |
| C2 | 1pF | 0402 ceramic | |
| C3 | 100pF | 0402 ceramic | |
| C4 | 22pF | 0402 ceramic | |
| C5 | 100pF | 0402 ceramic | |
| C6 | 580pF | 0402 ceramic | |
| C7 | 120pF | 0402 ceramic | |
| C8 | 1nF | 0402 ceramic | |
| C9 | 10nF | 0402 ceramic | |
| C10 | 22pF | 0402 ceramic | |
| C11 | 9pF | 0402 ceramic | |
| C12 | 10nF | 0402 ceramic | |
| C13 | 22pf | 0402 ceramic | |
| L1 | TBD 10% | 0402CS-??NXJ | Coilcraft |
| L2 | 47nH, 10% | 0402CS-47NXX | Coilcraft |
| R1 | 6.8kΩ | 0402 | |
| R2 | 39Ω | 0402 | |
| F1 | 1575.42MHz | 855969 | Sawtek |
| X1 | 16.368MHz | KSX series | AVX |

Package Information





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Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Preliminary Information

The datasheet contains information from the design target specification. SiGe Semiconductor Inc. reserves the right to change information at any time without notification.

Final

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