

SED1520/21

DOT MATRIX LCD DRIVER

S-MOS Systems, Inc.

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Version 1.0 (Preliminary)



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1.0 GENERAL DESCRIPTION

1.1 DESCRIPTION

The SED1520 is a dot matrix LCD driver LSI intended for display of characters and graphics. The bit-addressable display data, which is sent from a microcomputer, is stored in a built-in display data RAM and generates the LCD drive signal.

The SED1520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. With these features, the SED1520 permits the user to implement high-performance handy systems operating from a miniature battery.

In order for the user to adaptively configure his system, the SED1520 family offers two application forms. One form allows an LCD display of 12 characters × 2 lines with an indicator with a single chip. The other is dedicated to driving a total of 80 segments, enabling a medium-size display to be achieved by using a minimum number of drivers.

1.2 FEATURES

- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- Segment output 61 outputs
- Common output 16 outputs
- Duty cycle . . SED1520 . . . 1/16 to 1/32
 SED1521 . . . 1/8 to 1/32
- Built-in display data RAM . . . 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Recommended expansion segment driver: 80 bit
- Master/slave operation is supported
- Low power consumption . . . 30μW
- LCD voltage 3.5 to 13V
- Single power supply 2.4 to 7.0V
- Package QFP5-100 pin (FOA, FAA)
 QFP15-100 pin (FOC, FAC)
 Al pad (DOA, DAA)
 Au bump (DOB, DAB)
 TAB (TOA)

1.3 SED1520 FAMILY SPECIFICATIONS

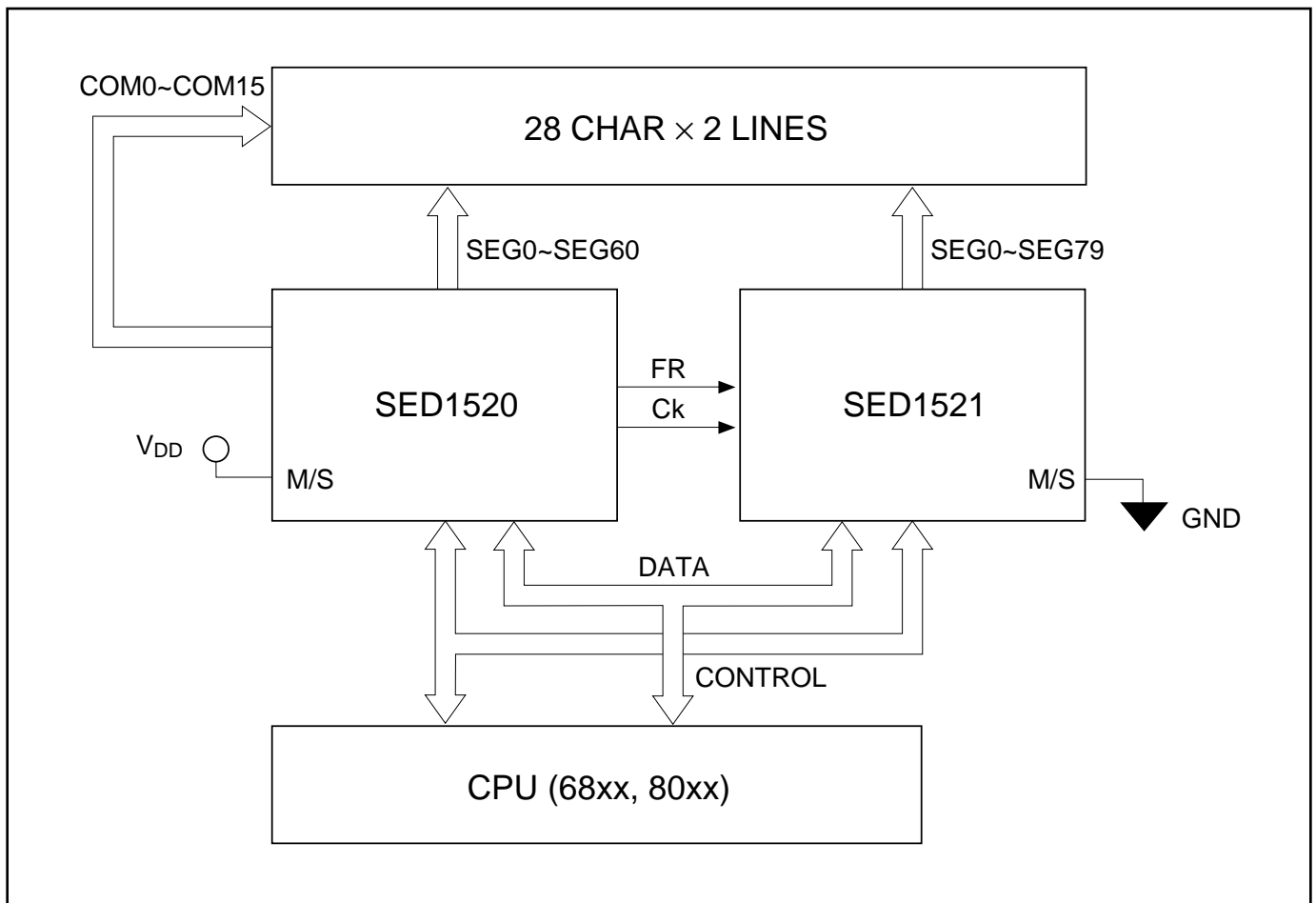
| Product Name | Clock Frequency | | Applicable Driver | No. of SEG Drivers | No. of COM Drivers |
|--------------|-----------------|----------|---|--------------------|--------------------|
| | On Chip | External | | | |
| SED1520FOA | 18kHz | 18kHz | SED1520FOA, SED1521FOA | 61 | 16 |
| SED1521FOA | — | 18kHz | | 80 | 0 |
| SED1520FAA | — | 2kHz | SED1520FAA, SED1521FAA, HD44103CH | 61 | 16 |
| SED1521FAA | — | 2kHz | | 80 | 0 |

1.4 MODEL CLASSIFICATION

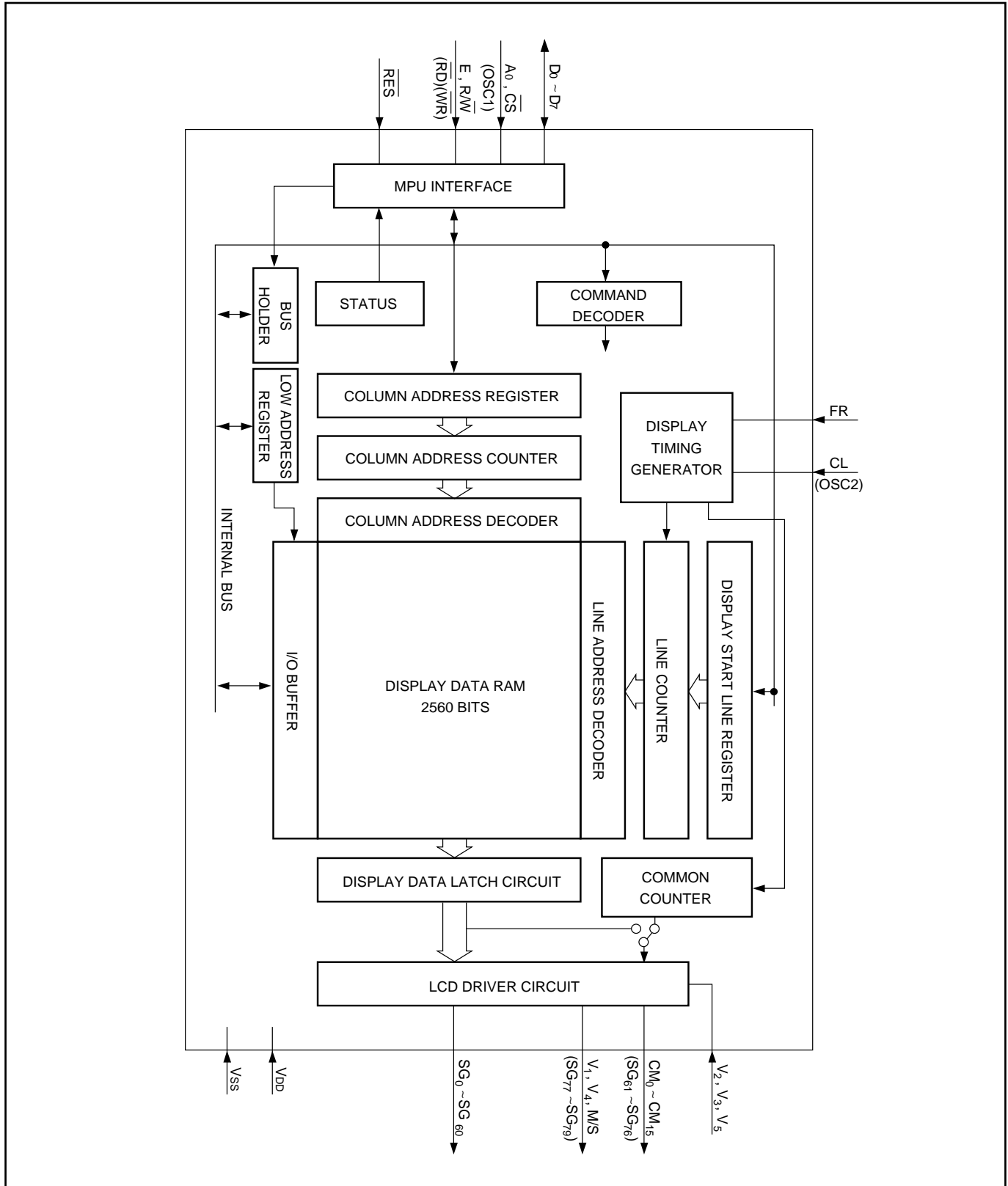
| Model Name | Operating Clock | | Connectable Drivers | SEG Driver | COM Driver |
|------------|---------------------|----------------|------------------------|------------|------------|
| | Internal oscillator | External clock | | | |
| SED1520Fo* | 18KHz | 18KHz | SED1520Fo*, SED1521Fo* | 61 ports | 16 ports |
| SED1520FA* | — | 2KHz | SED1520FA*, SED1521FA* | 61 ports | 16 ports |

2.0 BLOCK DIAGRAMS

2.1 SYSTEM BLOCK DIAGRAM



2.2 BLOCK DIAGRAM



2.3 DESCRIPTION OF CIRCUIT BLOCKS

2.3.1 MPU Interface

2.3.1.1 Selection of Interface Type

The SED1520 Series uses 8 bits of bi-directional data bus (D0–D7) to transfer data. The reset pin is capable of selecting MPU interface; setting the polarity of \overline{RES} to either “H” or “L” can provide direct interface of the SED1520 with a 68 or 80 family MPU (see Table 1 below).

With \overline{CS} at high level, the SED1520 is independent from the MPU bus and stays in standby mode. In this mode, however, the reset signal is input independently of the internal status.

Table 1

| Polarity of \overline{RES} | Type | A0 | E | R/W | \overline{CS} | D0–D7 |
|------------------------------|--------|----|-----------------|-----------------|-----------------|-------|
| “L” active | 68 MPU | ↑ | ↑ | ↑ | ↑ | ↑ |
| “H” active | 80 MPU | ↑ | \overline{RD} | \overline{WR} | ↑ | ↑ |

2.3.1.2 Identification of Data Bus Signals

The SED1520 uses a combination of A0, E, R/W, (\overline{RD} , \overline{WR}) to identify a data bus signal.

Table 2

| Common | 68 MPU | 80 MPU | | Function |
|--------|--------|-----------------|-----------------|--------------------------------------|
| A0 | R/W | \overline{RD} | \overline{WR} | |
| 1 | 1 | 0 | 1 | Read display data |
| 1 | 0 | 1 | 0 | Write display data |
| 0 | 1 | 0 | 1 | Read status |
| 0 | 0 | 1 | 0 | Write to internal register (command) |

2.3.1.3 Access to Display Data RAM and Internal Register

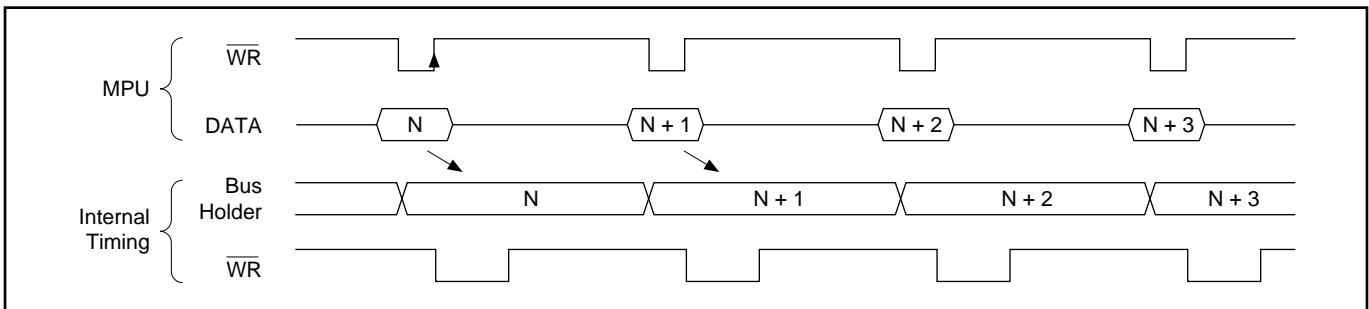
In order to make matching of operating frequencies between the MPU and the display data RAM or internal register, the SED1520 performs a sort of LSI–LSI pipelining via the bus holder attached to the internal data bus.

Consider the case where the MPU reads the content of the display data RAM. In the first data read cycle (dummy), the data is stored on the bus holder. In the next data read cycle, the data is read from the bus holder to the system bus.

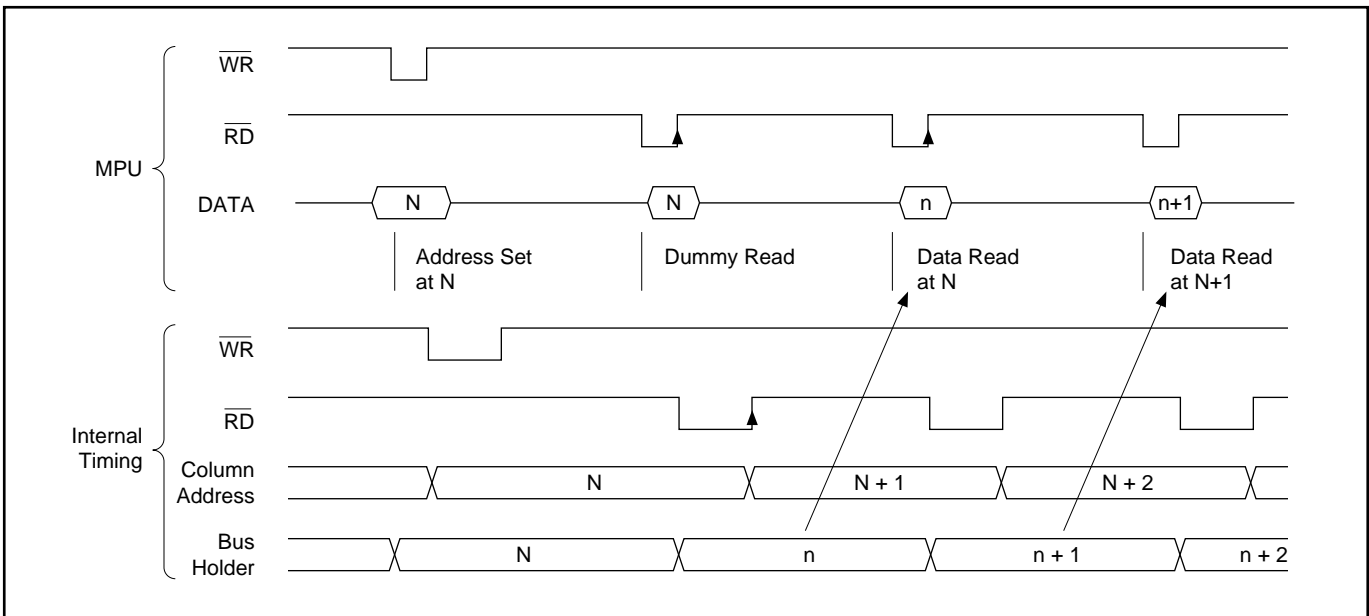
Also, consider the case where the MPU writes data to the display data RAM. In the first data write cycle, the data is held on the bus holder. The data is written to the display data RAM before the next data write cycle begins.

Therefore, MPU's access to the SED1520 is affected not by display data RAM access time (t_{ACC} , t_{DS}) but by cycle time (t_{CYC}). This leads to faster transfer of data to and from the MPU. If the cycle time requirement is not met, the MPU has only to execute the NOP instruction and this is apparently equivalent to execution of a waiting operation. However, there is a restriction on the read sequence of the display data RAM; when an address is set, its data is output not to the first read instruction (immediately following the address setting operation) but to the second read instruction. Thus, one dummy read cycle is necessary after an address set or write cycle. This relation is shown in Figures 2.3.1.4 and 2.3.1.5.

2.3.1.4 Write Timing Diagram



2.3.1.5 Read Timing Diagram



2.3.2 Busy Flag

Busy flag being “1” means that the SED1520 is performing its internal operation and any instruction other than Read Status is disabled. The busy flag is output to pin D7 by a Read Status instruction. As long as the cycle time (t_{CYC}) requirement is met, the flag need not be checked before each command and this dramatically improves the MPU performance.

2.3.3 Display Start Line Register

This register is a pointer which determines the start line corresponding to COM0 (normally, the uppermost line of display) for display of data in the display data RAM. It is used for scrolling the display or changing the page from one to another. Executing the Set Display Start Line command sets 5 bits of display start address in this register. Its content is preset in the line counter at each timing the FR signal changes. The line counter is incremented synchronously to a CL input, thus generating a line address for sequential reading of 80 bits of data from the display data RAM to the LCD driver circuit.

2.3.4 Column Address Counter

The column address counter is a 7-bit presettable counter which gives column addresses of the display data RAM as shown in Fig. 2.3.8.1. When a Read/Write Display Data command comes in, the counter is incremented by 1. For any nonexisting address over 50H, the counter is locked and not incremented.

The column address counter is independent from the page register.

2.3.5 Page Register

This register gives a page address of the display data RAM as shown in Fig. 2.3.8.1. The Set Page Address command permits the MPU to access a new page of the display data RAM.

2.3.6 Display Data RAM

Dot data for display is stored in this RAM. Since the MPU and LCD driver circuit operate independently of each other, data can be changed asynchronously without adverse effect on the display.

One bit of the display data RAM is assigned to one bit of LCD:

LCD on = “1”

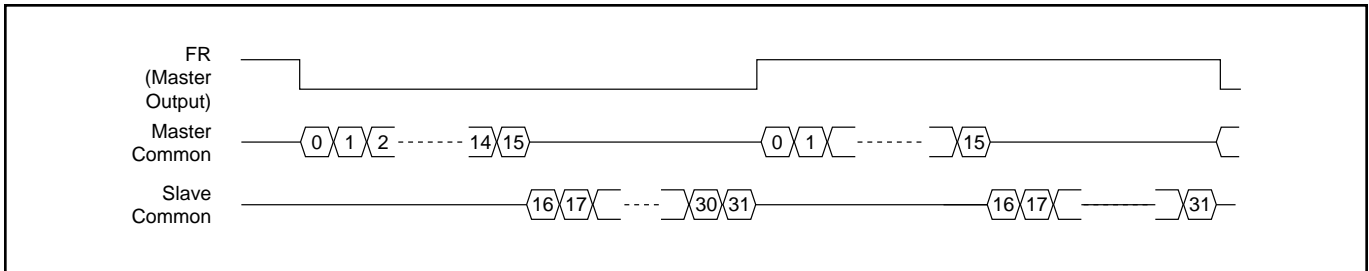
LCD off = “0”

The ADC command inverts the assignment relationship between a display data RAM column address and a segment output (see Fig. 2.3.8.1).

2.3.7 Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock (CL). The Select Duty command selects a duty of 1/16 or 1/32. The 1/32 duty is achieved by a two-chip (master and slave) configuration (common multi-chip system).

2.3.7.1 Common Timing Diagram



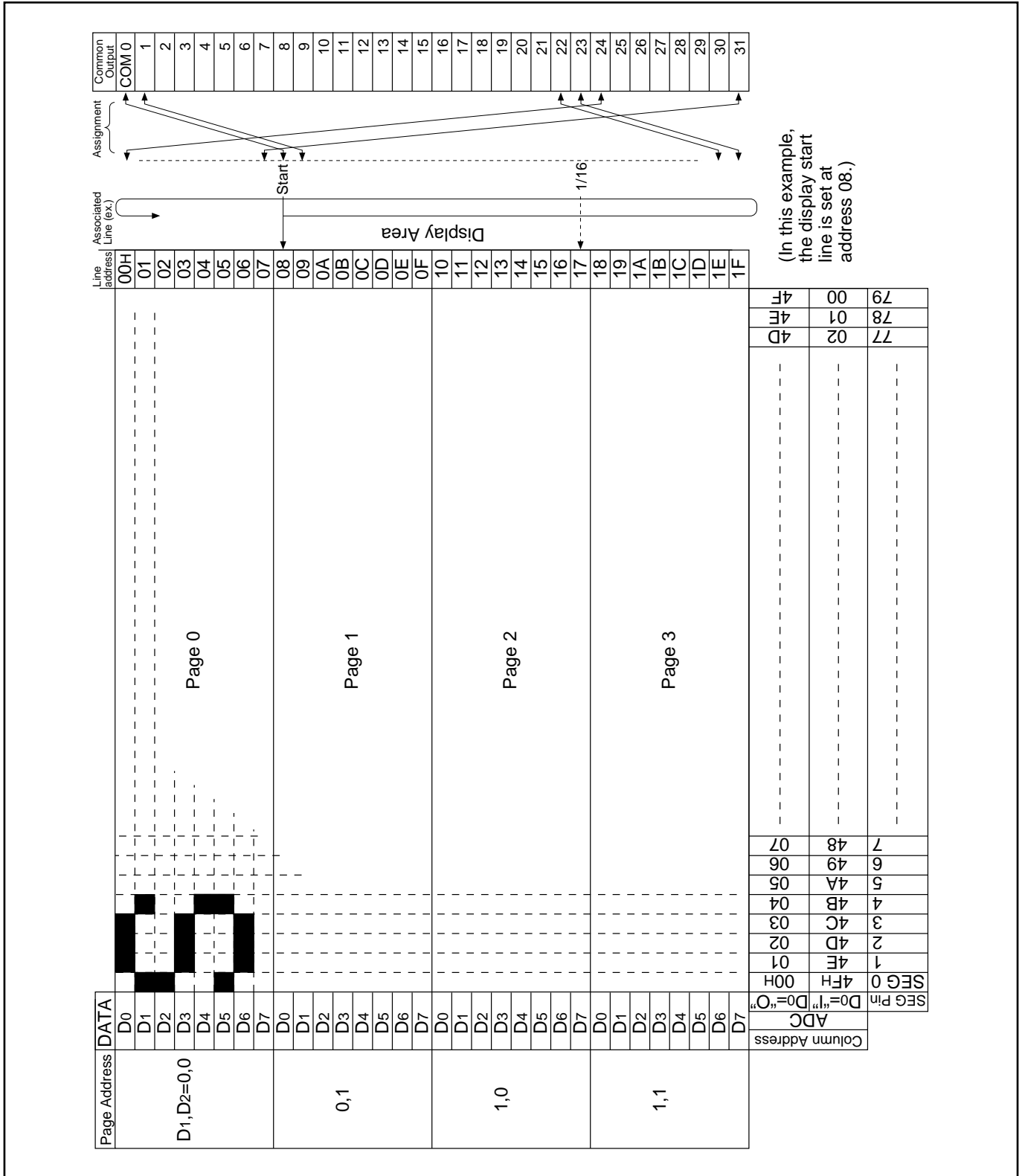
2.3.8 Display Data Latch Circuit

The display data latch circuit temporarily stores the data which will be output from the display data RAM to the LCD driver circuit at one-common intervals. The display ON/OFF and Static Driver ON/OFF commands control the latched data so that the data in the display data RAM remains unchanged.

2.0 Block Diagrams

2.3.8.1 – 2.3.8.1

2.3.8.1 Relationship between Display Data RAM Locations and Addresses (Display Start Line: 08)



2.3.9 LCD Driver Circuit

This circuit generates 80 sets of multiplexer that generate quartet levels for LCD driving. Display data in the display data latch, common timing generator output and FR signal are combined to output an LCD driving waveform.

2.3.10 Display Timing Generator

This circuit generates an internal display timing signal from the basic clock (CL) and frame signal (FR).

The frame signal FR makes the LCD driver circuit generate a dual frame AC driving waveform (type B) to drive LCD, while making both the line counter and common timing generator synchronized to the FR signal output LSI (dedicated common driver or the SED1520 master LSI). To achieve these functions, the FR signal must be a clock with a duty of 50% which is synchronized to the frame period.

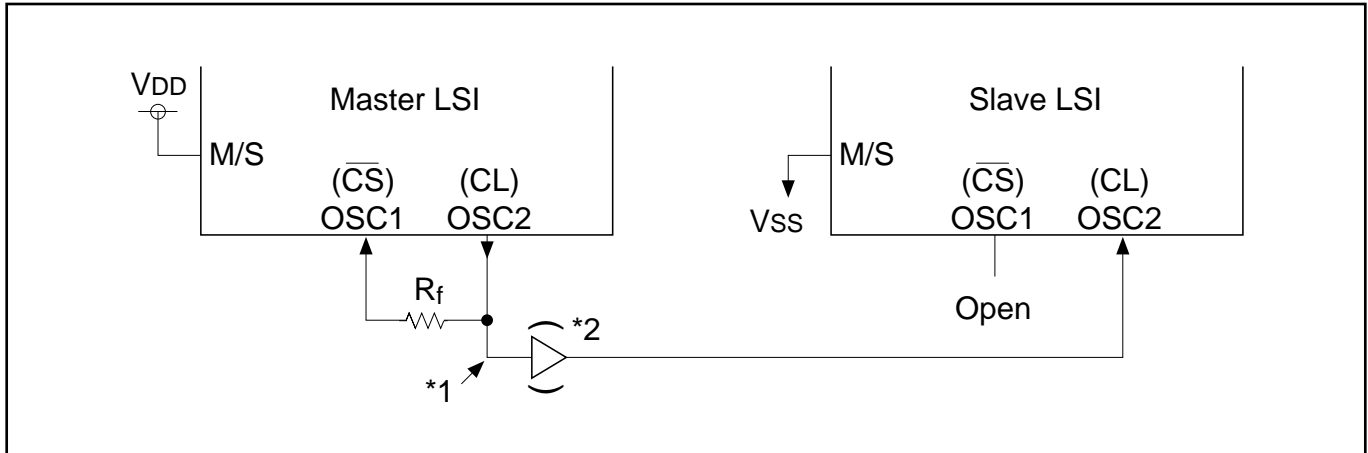
The clock CL is a clock used to operate the line counter. For a system in which both the SED1520 and SED1521F coexist, they should be of LSI types having the same clock frequency to be applied to pin CL.

2.3.11 Oscillation Circuit

This circuit is a low-power CR oscillator which uses an oscillation resistor R_f alone to adjust the oscillation frequency. It generates display timing signals. The SED1520 is available in two LSI types if classified by oscillation: one LSI type contains an oscillation circuit and the other uses an externally provided clock.

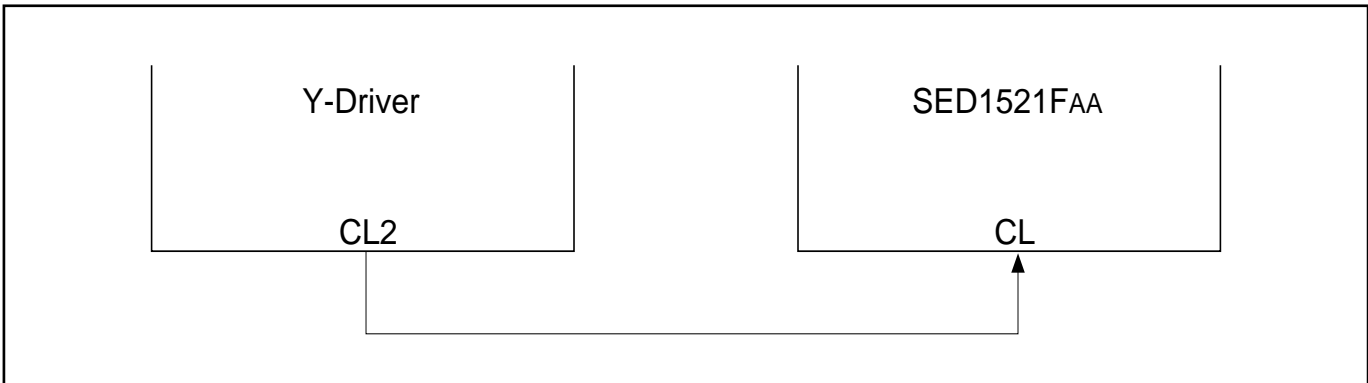
The oscillation resistor R_f is connected as shown below. Where an LSI containing an oscillation circuit is operated with an external clock, it is necessary to input the clock with the same phase as OSC2 of the master LSI to OSC2 of the slave LSI.

2.3.11.1 LSI Containing Oscillator



- * As the parasitic capacitance in this portion increases, the oscillation frequency will shift to a lower level. The R_f must have a smaller value than the specification.
- * For a system having two or more slave LSIs, a CMOS buffer is necessary.

2.3.11.2 LSI Operating with External Clock



2.3.12 Reset Circuit

This circuit senses the leading edge or trailing edge of $\overline{\text{RES}}$ and initializes the system when its power is switched on.

Initialization:

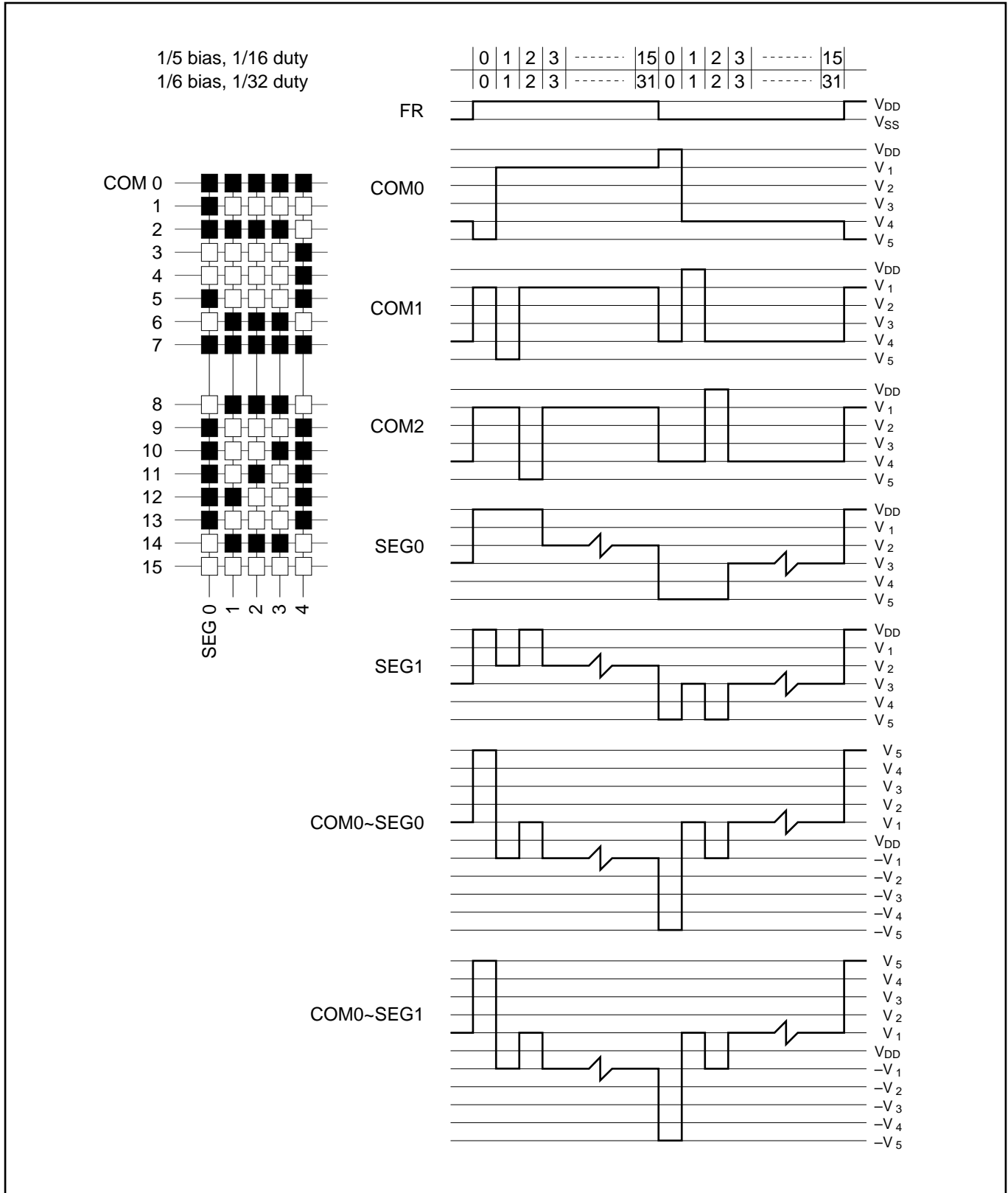
- (a) Display off
- (b) Display start line register: First line
- (c) Static drive off
- (d) Column address counter: Address 0
- (e) Page address register: Page 0
- (f) Select duty: 1/32
- (g) Select ADC: Forward (ADC command D0 = "0", ADC status flag = "1")
- (h) Read modify write off

The input at pin $\overline{\text{RES}}$ is level-sensed to select an MPU interface mode as shown in Table 1. For interfacing with an 80 family MPU, an "H" active reset signal is input to pin $\overline{\text{RES}}$. For interfacing with a 68 family MPU, an "L" active reset signal is input to the pin. (See Fig. 7.)?????

As exemplified in section 6 "MPU Interface", pin $\overline{\text{RES}}$ is connected to the MPU reset pin. Thus the SED1520 and the MPU are initialized at the same time. If system is initialized by pin $\overline{\text{RES}}$ at power-on, it may no longer be reset.

The Reset command causes initialization (b), (d) and (e).

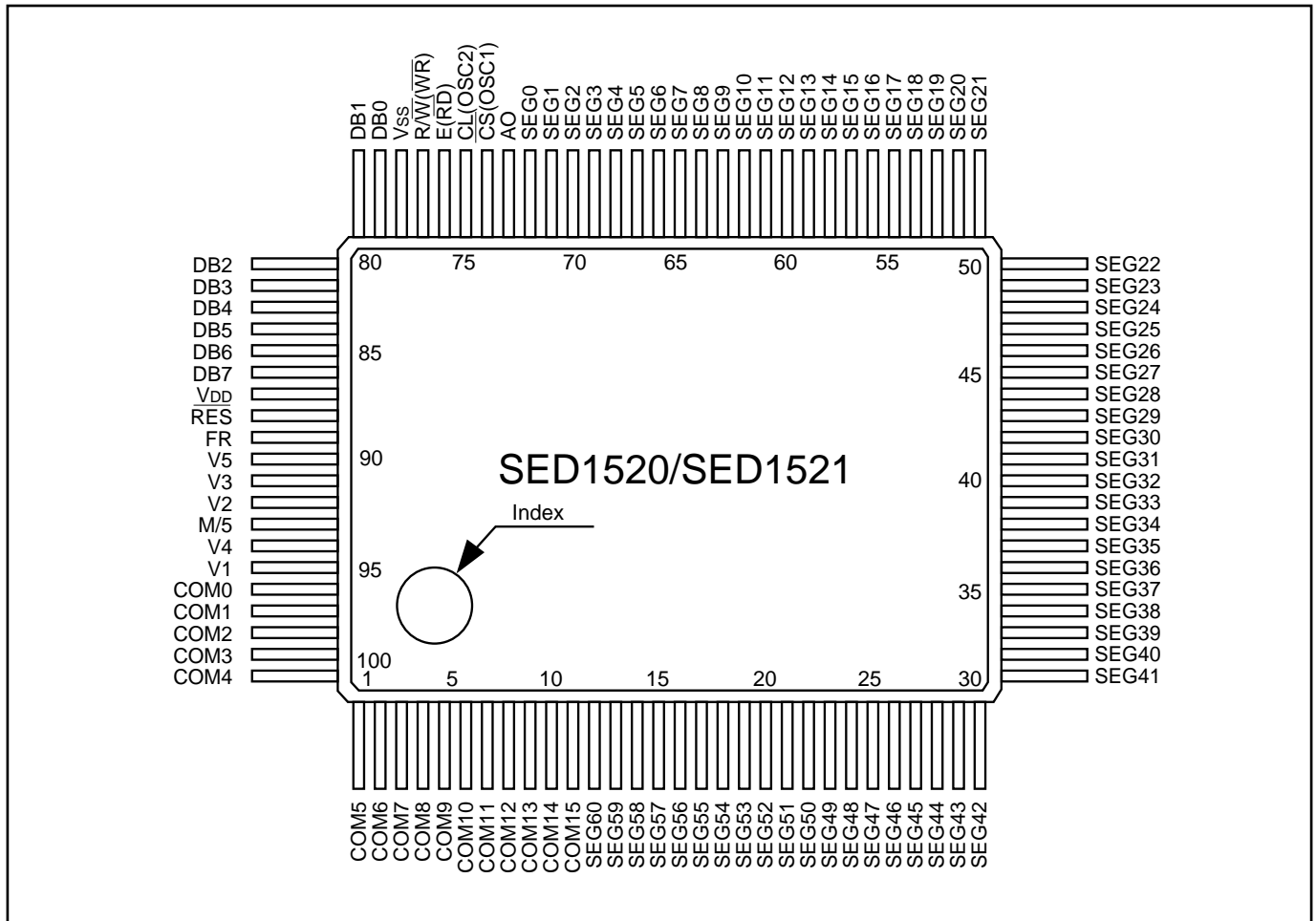
2.3.12.1 Example of LCD Driving Waveform



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3.0 PIN CONFIGURATION

3.1 PIN CONFIGURATION



3.2 PIN DESCRIPTION

| Product name | Pin No. | | | | | |
|--------------|-----------------|------|--------------|-------|----------------|----------------|
| | 74 | 75 | 96~100, 1~11 | 93 | 94 | 95 |
| SED1520FOA | OSC1 | OSC2 | COM0~COM15* | M/S | V ₄ | V ₁ |
| SED1521FOA | \overline{CS} | CL | SEG76~SEG61 | SEG79 | SEG78 | SEG77 |
| SED1520FAA | \overline{CS} | CL | COM0~COM15* | M/S | V ₄ | V ₁ |
| SED1521FAA | \overline{CS} | CL | SEG76~SEG61 | SEG79 | SEG78 | SEG77 |

* Master LSI common outputs COM0~COM15 correspond to slave LSI outputs COM31~COM16.

3.2.1 Power Signals

V_{DD} Connected to +5V power. Common to MPU power pin V_{CC}.

V_{SS} 0V, connected to system GND.

V₁~V₅ Multi-level power used to drive LCDs. Voltage specified to each LCD cell is divided by resistors or impedance-converted by an operational amplifier before being applied. Each voltage to be applied must be based on V_{DD}, while fulfilling the following conditions:

$$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$$

3.2.2 System Bus Interface Signals

D₇~D₀ 8-bit, tri-state, bi-directional I/O bus. Normally, connected to the data bus of an 8-/16-bit standard microcomputer.

A₀ Input pin. Normally, the LSB of the MPU address bus is connected to this input pin to provide data/command selection.

0: Display control data on D₇~D₀

1: Display data on D₇~D₀

\overline{RES} Input pin. The SED1520 can be reset or initialized by setting \overline{RES} to low level (if it is interfaced with a 68 family MPU) or high level (if with an 80 family MPU). This reset operation occurs when an edge of the \overline{RES} signal is sensed. The level input selects the type of interface with the 68 or 80 family MPU:

High level: Interface with 68 family MPU

Low level: Interface with 80 family MPU

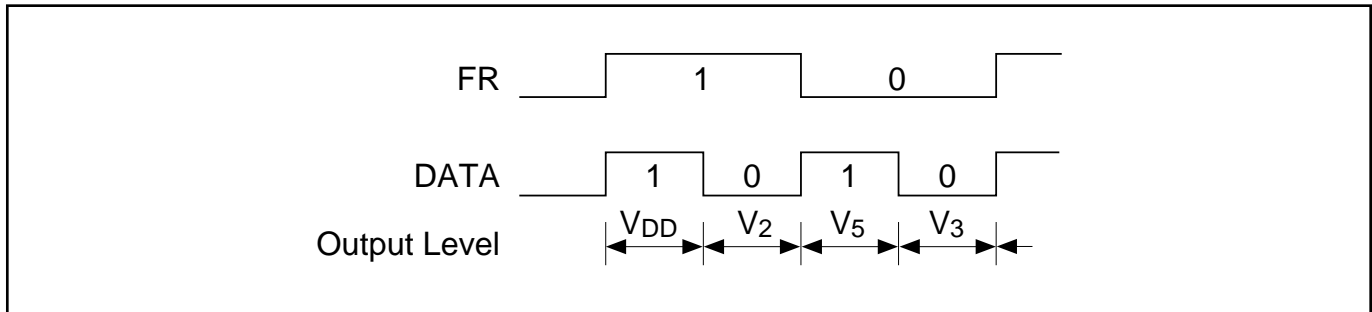
- \overline{CS} Chip Select input signal which is normally obtained by decoding an address bus signal. Effective with “L” active and a chip operating with external clocks. For a chip containing an oscillator, \overline{CS} works as an oscillation amplifier input pin to which an oscillation resistor (Rf) is connected. In this case, \overline{RD} , \overline{WR} and E must be a signal ANDed with CS.
- E(\overline{RD}) Chip interfaced with 68 family MPU:
Enable Clock signal input for the 68 family MPU.
- Chip interfaced with 80 family MPU:
“L” Active input pin to which the 80 family MPU \overline{RD} signal is connected.
With this signal held at “L”, the SED1520 data bus works as output.
- R/W (\overline{WR}) Chip interface with 68 family MPU:
Read/Write control signal input pin.
R/W = “H” : Read
R/W = “L” : Write
- Chip interfaced with 80 family MPU:
“L” Active input pin to which the 80 family \overline{WR} is connected. The signal on the data bus is fetched by the leading edge of \overline{WR} .

3.2.3 LCD Drive Circuit Signals

- CL Input signal effective with a chip using external clocks. This display data latch signal increments the line counter (at the trailing edge) or the common counter (at the leading edge). CL is connected to CL2 of the common driver. For a chip containing an oscillator, this pin works as the oscillation amplifier output pin to which an oscillation resistor (Rf) is connected.
- FR LCD AC signal I/O pin. Connected to pin M of the common driver.
- I/O selection:
- | | |
|--------------------------------|------------------|
| Chip containing commons | M/S = 1 : Output |
| | M/S = 0 : Input |
| Chip containing segments alone | : Input |

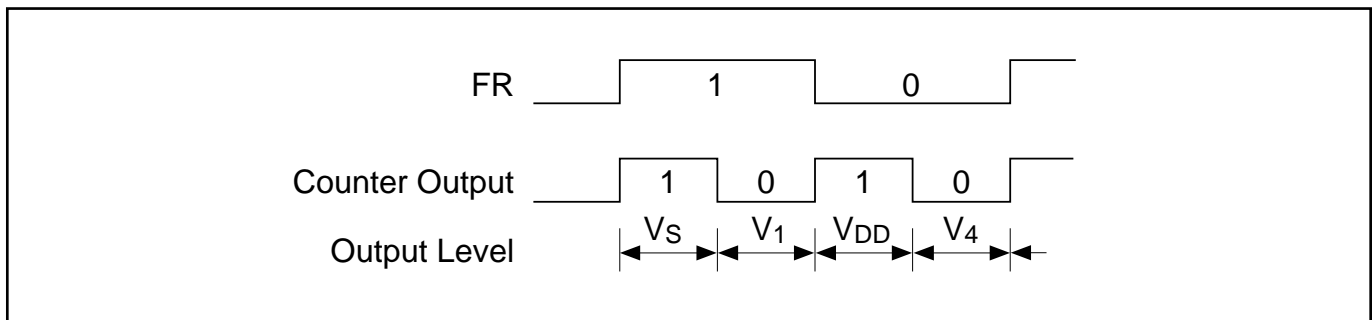
SEG0– LCD column (segment) driving output. One of the V_{DD}, V₂, V₃ and V₅ levels is
 SEG79 selected by a combination of the content of display RAM and the FR signal.

3.2.3.1 LCD Column (Segment) Driving Output Timing



COM0– LCD common (row) driving output. One of the V_{DD}, V₁, V₄ and V₅ levels is
 COM15 selected by a combination of the output of the common counter and the FR
 (COM31– signal. The common (row) scanning order for the slave LSI is reverse to that for
 COM16) the master LSI.

3.2.3.2 LCD common (row) driving output



M/S (SEG79) Input signal which selects the master or slave LSI. Connected to V_{DD} or V_{SS}.

M/S = V_{DD}: Master
 M/S = V_{SS} : Slave

M/S selection changes the function of pins FR, COM0–COM15, OSC1 (\overline{CS}) and OSC2 (CL):

| M/S | FR | COM output | OSC1 | OSC2 |
|-----------------|--------|-------------|-------|--------|
| V _{DD} | Output | COM0–COM15 | Input | Output |
| V _{SS} | Input | COM31–COM16 | NC | Input |

The common scanning order for the slave driver is reverse to that for master.

4.0 COMMANDS

Table 3 lists the commands used with the SED1520. This LSI uses a combination of A0, R/W (\overline{RD} , \overline{WR}) to identify a data bus signal. Interpretation and execution of a command depends not on external clock but on internal timing alone. Therefore, a command can be executed so fast that no busy check is needed.

A detailed description of commands follows.

4.1 DISPLAY ON/OFF

This command forces all display to turn on or off.

| | | | | | | | | | | |
|-----|-----------------|-----------------|----|-------|---|---|---|---|---|----|
| R/W | | | | | | | | | | |
| A0 | \overline{RD} | \overline{WR} | D7 | _____ | | | | | | D0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

D 0 = Display OFF
 1 = Display ON

4.2 DISPLAY START LINE

This command specifies a line address (shown in Fig. 2.3.8.1) thus marking the display line that corresponds to COM0. Display begins with the specified line address and covers as many lines as match the display duty in address ascending order. Dynamic line address change with the Display Start Line command enables column-wise scrolling or page change.

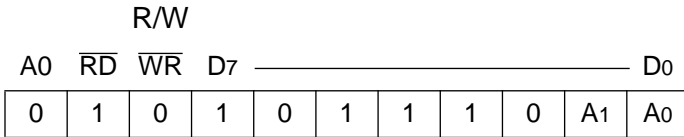
| | | | | | | | | | | |
|-----|-----------------|-----------------|----|-------|---|----|----|----|----|----|
| R/W | | | | | | | | | | |
| A0 | \overline{RD} | \overline{WR} | D7 | _____ | | | | | | D0 |
| 0 | 1 | 0 | 1 | 1 | 0 | A4 | A3 | A2 | A1 | A0 |

– High-order bits

| A4 | A3 | A2 | A1 | A0 | Line address |
|----|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| | | — | | | — |
| | | — | | | — |
| 1 | 1 | 1 | 1 | 1 | 31 |

4.3 SET PAGE ADDRESS

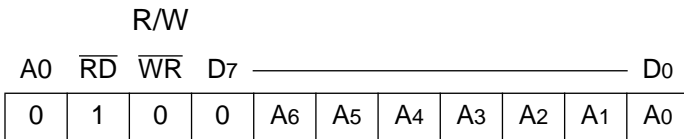
This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM. A required bit of the display data RAM can be accessed by specifying its page address and column address. Changing the page address causes no change in display.



| A1 | A0 | Page |
|----|----|------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

4.4 COLUMN ADDRESS

This command specifies a display data RAM column address. The column address is incremented by 1 each time the MPU accesses from the set address to the display data RAM. Thus, it is possible for the MPU to gain continuous access to only the data. This incrementing stops with address 80; the page address is not continuously changed.



| A6 | A5 | A4 | A3 | A2 | A1 | A0 | Column address |
|----|----|----|----|----|----|----|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | — | | | | — |
| | | | — | | | | — |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 79 |

4.5 READ STATUS

| R/W | | | | | | | | | | |
|-----|-----------------|-----------------|------|-----|--------|-------|---|----|---|---|
| A0 | \overline{RD} | \overline{WR} | D7 | | | | | D0 | | |
| 0 | 0 | 1 | Busy | ADC | ON/OFF | Reset | 0 | 0 | 0 | 0 |

BUSY: BUSY being “1” means that system is performing an internal operation or is reset. No command is accepted before BUSY = “0”. As long as the cycle time requirement is met, no BUSY check is needed.

ADC: Indicates assignment of column addresses to segment drivers.

0: Inverted (column address 79-n ↔ segment driver n)

1: Forward (column address n ↔ segment driver n)

ON/OFF: Indicates display on or off.

0: Display on

1: Display off

This bit has polarity reverse to the Display ON/OFF command.

RESET: Indicates that system is being initialized by the \overline{RES} signal or the Reset command.

0: Display mode

1: Being reset

4.6 WRITE DISPLAY DATA

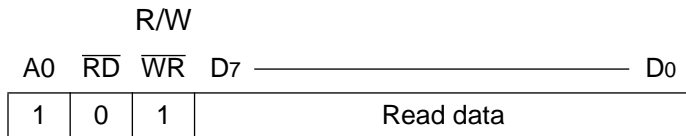
This command allows the MPU to write 8 bits of data into the display data RAM. Once the data is written, the column address is automatically incremented by 1; this enables the MPU to write multi-word data continuously.

| R/W | | | | | | | | | | |
|-----|-----------------|-----------------|------------|--|--|--|--|----|--|--|
| A0 | \overline{RD} | \overline{WR} | D7 | | | | | D0 | | |
| 1 | 1 | 0 | Write data | | | | | | | |

4.7 READ DISPLAY DATA

This command allows the MPU to read 8 bits of data from the display data RAM location specified by a column address and a page address. Once the data is read, the column address is automatically incremented by 1; this enables the MPU to read multi-word data continuously.

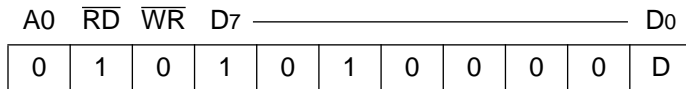
A dummy read is needed immediately after the column address is set. For details, see 3. (1)–(c).??



4.8 SELECT ADC

This command inverts the relation of assignment between display data RAM column addresses and segment driver outputs. In other words, the Select ADC command can software-invert the order of segment driver output pins, reducing the restrictions on the configuration of ICs at LCD module assembly. For details, see Fig. 2.3.8.1.

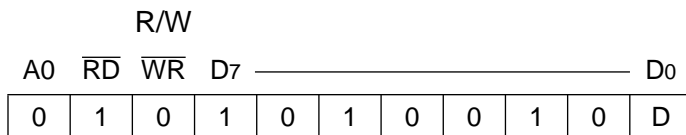
Incrementing the column address by 1, which takes place after the MPU writing or reading display data, follows the sequence of column addresses specified in Fig. 2.3.8.1.



- D = 0: Clockwise output (forward)
- D = 1: Counterclockwise output (reverse)

4.9 STATIC DRIVE ON/OFF

This command forces all display to be on and, at the same time, all common output to be selected.



- D = 0: Static drive off
- D = 1: Static drive on

4.10 SELECT DUTY

This command is used to select the duty (degree of multiplexity) of LCD driving. It is valid for the SED1520F (actively operating LSI) only, not valid for the SED1521F (passively operating LSI). The SED1521F operates with any duty determined by the FR signal.

| | | | | | | | | | | |
|-----|-----------------|-----------------|----|-------|---|---|---|---|---|----|
| R/W | | | | | | | | | | |
| A0 | \overline{RD} | \overline{WR} | D7 | _____ | | | | | | D0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | D |

D = 0: Duty 1/16

D = 1: Duty 1/32

If the system contains both SED1520FOA (internal oscillation) and the SED1521FOA LSIs, they must have the same duty.

4.11 READ MODIFY WRITE

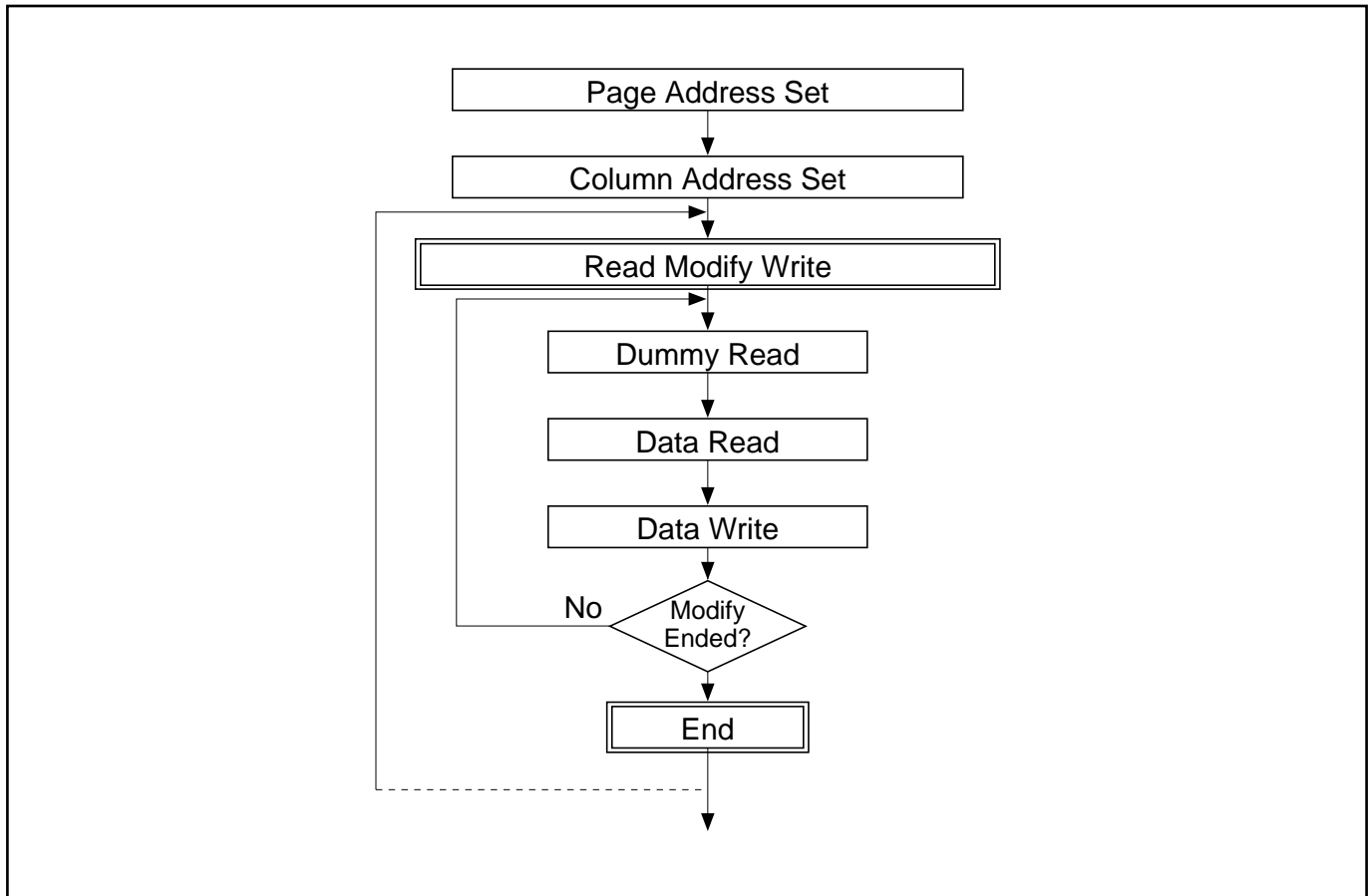
This command is used with the End command in a pair. Once it has been entered, the column address will be incremented not by the Read Display Data command but by the Write Display Data command only. This mode will stay until the End command is entered.

Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered. This function lessens the load of the MPU when the data in a specific display area are repeatedly updated (as blinking cursor).

| | | | | | | | | | | |
|-----|-----------------|-----------------|----|-------|---|---|---|---|---|----|
| R/W | | | | | | | | | | |
| A0 | \overline{RD} | \overline{WR} | D7 | _____ | | | | | | D0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

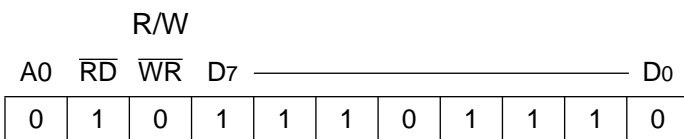
Even in the Read Modify Write mode, any command other than Read/Write Data and Set Column Address may be used.

4.11.1 Cursor Blinking Sequence

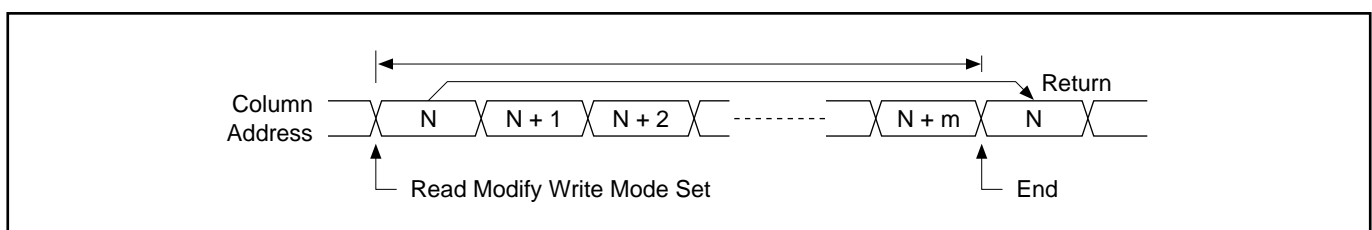


4.12 END

This command cancels the Read Modify Write command, returning the column address to the initial mode address.



4.12.1 End Timing



4.13 RESET

This command initializes the display start line register, column address counter, and page address counter without any effect on the display data RAM. For details, see section 2.3.12.

The reset operation follows entry of the Reset command.

| | | | | | | | | | | | | | |
|----|-----------------|-----------------|----|---|---|---|---|---|---|----|--|--|--|
| | | R/W | | | | | | | | | | | |
| A0 | \overline{RD} | \overline{WR} | D7 | | | | | | | D0 | | | |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | | | |

Initialization at power-on is performed not by the Reset command but by a reset signal applied to the \overline{RES} pin.

4.14 SAVE POWER (COMBINED COMMAND)

Static drive going on with display off invokes power-saving mode, reducing current consumption to nearly static current level. During this mode, the SED1520 holds the following conditions:

- (a) It stops driving the LCD; the segment and common driver outputs are at VDD level.
- (b) Oscillation and external clock input are disabled; OSC2 is in floating condition.
- (c) The display data and operational mode are held.

The power-saving mode is cancelled by display on or static drive off.

If an external resistor division circuit is used to give LCD driving voltage level, the current flowing into the resistors must be cut off by the power-save signal.

4.14.1 External Resistor Division Circuit

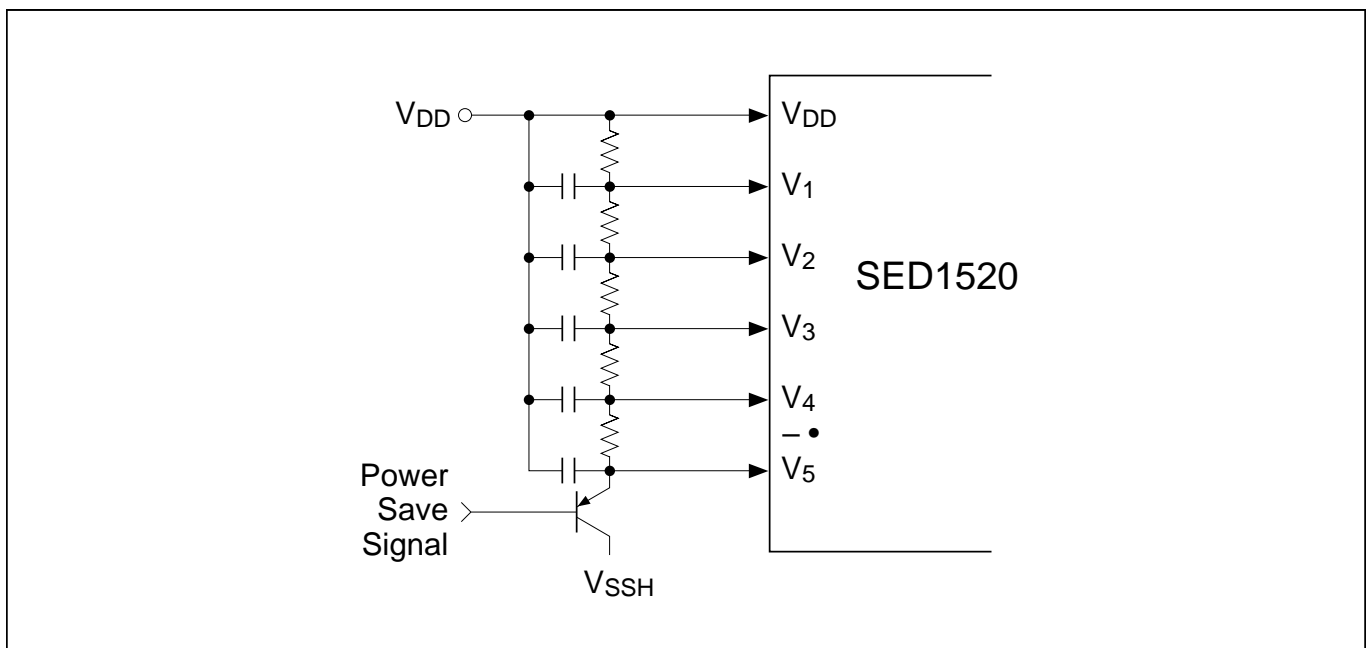


Table 3 Commands

| | Command | Code | | | | | | | | | | | Function |
|------|------------------------------|------|----|----|------------|-----------------------|--------|------------------------------|----|----|------------|-----|---|
| | | A0 | RD | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (1) | Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | Turns all display on or off, independently of display RAM data or internal status. 1: ON 0: OFF (Power-saving mode with static drive on)* |
| (2) | Display start line | 0 | 1 | 0 | 1 | 1 | 0 | Display Start Address (0–31) | | | | 0 | Specifies RAM line corresponding to uppermost line (COM0) of display. |
| (3) | Set page address | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Page (0–3) | | Sets display RAM page in page address register. |
| (4) | Set column (segment) address | 0 | 1 | 0 | 0 | Column Address (0–79) | | | | | | 0 | Sets display RAM column address in column address register. |
| (5) | Read status | 0 | 0 | 1 | Busy | ADC | ON/OFF | RESET | 0 | 0 | 0 | 0 | Reads the following status: BUSY 1: Internal operation, 0: Ready ADC 1: CW output (forward), 0: CCW output (reverse) ON/OFF 1: Display off, 0: Display on RESET 1: Being reset, 0: Normal |
| (6) | Write display data | 1 | 1 | 0 | Write Data | | | | | | | 0 | Writes data from data bus into display RAM. Display RAM location whose address has been preset is accessed. After access, the column address is incremented by 1. |
| (7) | Read display data | 1 | 0 | 1 | Read Data | | | | | | | 0 | |
| (8) | Select ADC | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | Used to invert relationship of assignment between display RAM column addresses and segment driver outputs. 0: CW output (forward) 1: CCW output (reverse) |
| (9) | Static drive ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0/1 | Selects normal display or static driving operation. 1: Static drive (power-saving mode) 0: Normal driving |
| (10) | Select duty | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0/1 | Selects LCD cell driving duty. 1: 1/32 0: 1/16 |
| (11) | Read modify write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Increments column address counter by 1 when display data is written. (This is not done when data is read.) |
| (12) | End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Clears read modify write mode. |
| (13) | Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Sets display start line register on the first line. Also sets column address counter and page address counter to 0. |

* With display off (command (1)), static drive going on (9) invokes power-saving mode.

5.0 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Standard | Unit |
|----------------------------|--|------------------------------|--------|
| Supply voltage (1) | V _{SS} | -8.0 ~ +0.3 | V |
| Supply voltage (2) | V ₅ | -16.5 ~ +0.3 | V |
| Supply voltage (3) | V ₁ , V ₄ V ₂ , V ₃ | V ₅ ~ +0.3 | V |
| Input voltage | V _{IN} | V _{SS} - 0.3 ~ +0.3 | V |
| Output voltage | V _O | V _{SS} - 0.3 ~ +0.3 | V |
| Allowable loss | P _D | 250 | mW |
| Operating temperature | T _{OPR} | -30 ~ +85 | °C |
| Storage temperature | T _{STG} | -65 ~ +150 | °C |
| Soldering temperature/time | T _{SOLDER} | 260/10 (at leads) | °C/Sec |

Notes:

- All voltages are based on VDD = 0V.
- The following condition must always hold true with voltages V₁, V₂, V₃, V₄ and V₅:
 $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
- The LSI may be permanently damaged if used with any value in excess of the absolute maximum ratings. During normal operation, the LSI should preferably be used within the specified electrical characteristics. Failure to meet them can cause the LSI to malfunction or lose its reliability.
- Generally, flat package LSIs may have moisture resistance lowered when solder dipped. In mounting LSIs on a board, it is recommended to use a method which is least unlikely to give thermal stress on the package resin.

5.2 DC CHARACTERISTICS

V_{DD} = 0V, T_a = -20 ~ 75°C

| Parameter | | Symbol | Condition | Min. | Typ. | Max. | Unit | Applicable pin |
|-----------------------------|---------------------|--|-----------------------------------|-----------------------|------|-----------------------|------|-----------------------------------|
| Operating voltage (1)*1 | Recommended | V _{SS} | | -5.5 | -5.0 | -4.5 | V | V _{SS} |
| | Allowable | | | -7.0 | | -2.4 | | |
| Operating voltage (2) | Recommended | V ₅ | | -13.0 | | -3.5 | V | V ₅ *10 |
| | Allowable | | | -13.0 | | | | |
| | Allowable | V ₁ , V ₂ | | 0.6 × V ₅ | | V _{DD} | V | V ₁ , V ₂ |
| | Allowable | V ₃ , V ₄ | | V ₅ | | 0.4 × V ₅ | V | V ₃ , V ₄ |
| High level input voltage | | V _{IHT} | | V _{SS} + 2.0 | | V _{DD} | V | *2 *3 |
| | | V _{IHC} | | 0.2 × V _{SS} | | V _{DD} | | |
| Low level input voltage | | V _{ILT} | | V _{SS} | | V _{SS} + 0.8 | V | *2 *3 |
| | | V _{ILC} | | V _{SS} | | 0.8 × V _{SS} | | |
| High level output voltage | | V _{OHT} | I _{OH} = -3.0mA | V _{SS} + 2.4 | | | V | *4 *5 OSC2 |
| | | V _{OHC1} | I _{OH} = -2.0mA | V _{SS} + 2.4 | | | | |
| | | V _{OHC2} | I _{OH} = -120μA | 0.2 × V _{SS} | | | | |
| Low level output voltage | | V _{OLT} | I _{OL} = 3.0mA | | | V _{SS} + 0.4 | V | *4 *5 OSC2 |
| | | V _{OLC1} | I _{OL} = 2.0mA | | | V _{SS} + 0.4 | | |
| | | V _{OLC2} | I _{OL} = 120μA | | | 0.8 × V _{SS} | | |
| Input leakage current | | I _{LI} | | -1.0 | | 1.0 | μA | *6 |
| Output leakage current | | I _{LO} | | -3.0 | | 3.0 | μA | *7 |
| LCD driver ON resistor | R _{ON} | T _a = 25°C | V ₅ = -5.0V | | 5.0 | 7.5 | KΩ | SEG 0 ~ 79 *11 COM 0 ~ 15 |
| | | | V ₅ = -3.5V | | 10.0 | 50.0 | | |
| Static current dissipation | | I _{DDQ} | $\overline{CS} = CL = V_{DD}$ | | 0.05 | 1.0 | μA | V _{DD} |
| Dynamic current dissipation | I _{DD} (1) | During display V ₅ = -5.0V | f _{CL} = 2KHz | | 2.0 | 5.0 | μA | V _{DD} *12 *13 *14 |
| | | | R _f = 1MΩ | | 9.5 | 15.0 | | |
| | | | f _{CL} = 18KHz | | 5.0 | 10.0 | | |
| | I _{DD} (2) | During access t _{CYC} = 200KHz | | | 300 | 500 | μA | *8 |
| Input pin capacitance | | C _{IN} | T _a = 25°C f = 1MHz | | 5.0 | 8.0 | pF | All input pins |

5.0 Electrical Characteristics

5.2 – 5.2

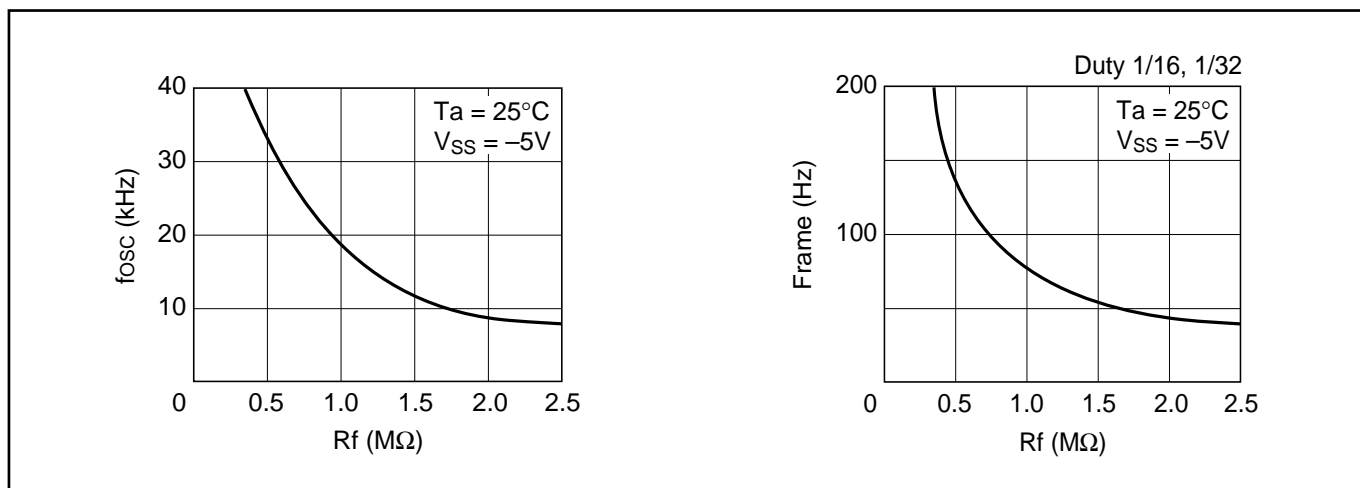
(Continued)

$V_{DD} = 0V$, $T_a = -20 \sim 75^\circ C$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Applicable pin |
|-----------------------|--------|--|------|------|------|---------|------------------|
| Oscillation frequency | fosc | $R_f = 1.0M\Omega \pm 2\%$ $V_{SS} = -5.0V$ | 15 | 18 | 21 | KHz | *9 |
| | | $R_f = 1.0M\Omega \pm 2\%$ $V_{SS} = -3.0V$ | 11 | 16 | 21 | | |
| Reset time | tR | | 1.0 | | 1000 | μs | \overline{RES} |

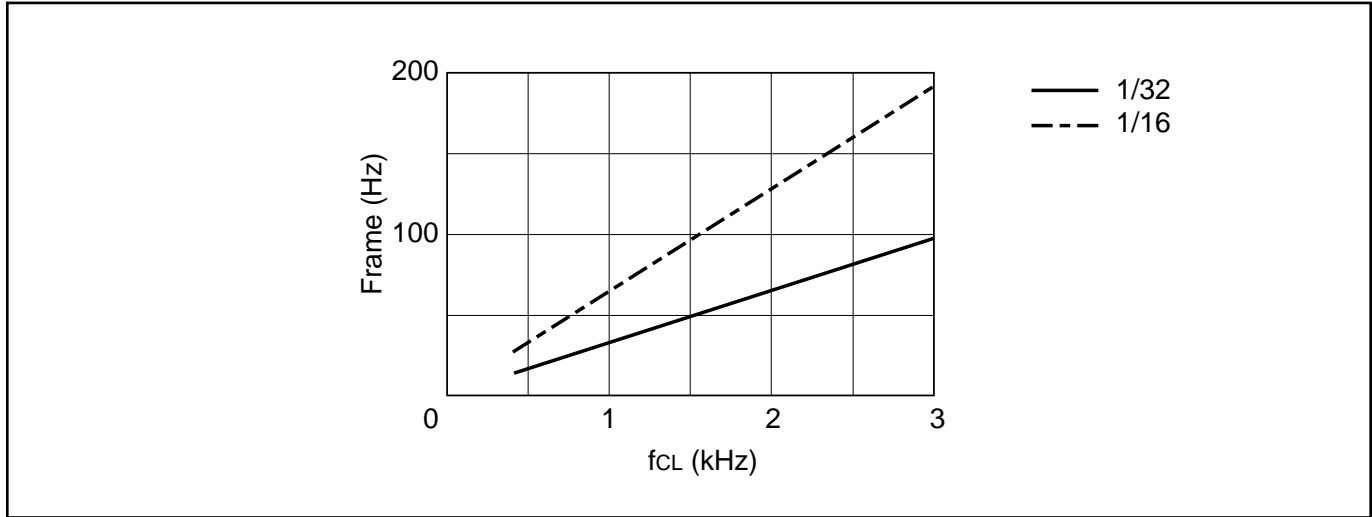
Notes:

- *1. Operation over a wide range of voltages is guaranteed except where a sudden voltage change occurs during access.
- *2. Pins A0, D0–D7, E(\overline{RD}), R/W (\overline{WR}) and \overline{CS}
- *3. Pins CL, FR, M/S and \overline{RES}
- *4. Pins D0–D7
- *5. Pin FR
- *6. Pins A0, E (\overline{RD}), R/W (\overline{WR}), CS, CL and \overline{RES}
- *7. Applicable when pins D0–D7 and FR are at high impedance.
- *8. This value is current consumption when a vertical stripe pattern is written at tcyc. Current consumption during access is nearly proportionate to access frequency (tcyc). Only TDD (1) is consumed while no access is made.
- *9. Relationship between oscillation frequency, frame and R_f (SED1520FOA)

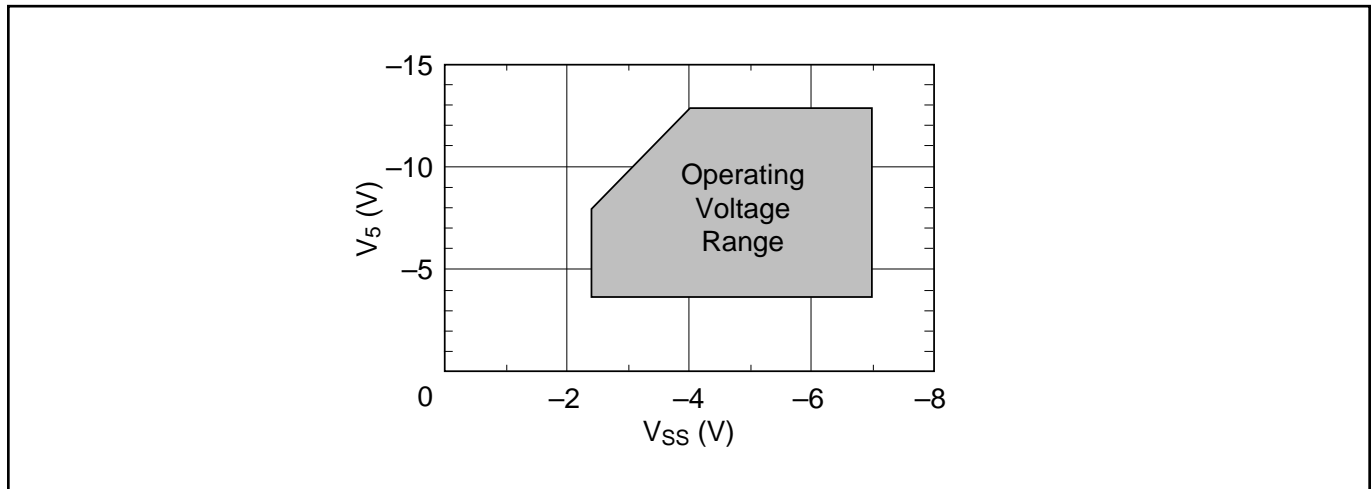


Notes (continued):

Relationship between external clock (f_{CL}) and frame (SED1520FAA)



*10. Operating voltage ranges of V_{SS} and V_S



*11. Resistance with a voltage of 0.1V applied between the output pin (SEG, COM) and each power pin (V₁, V₂, V₃, V₄). It is specified within the operating voltage range.

*12, 13, 14. Current consumed by each discrete IC, not including LCD panel and wiring capacitances.

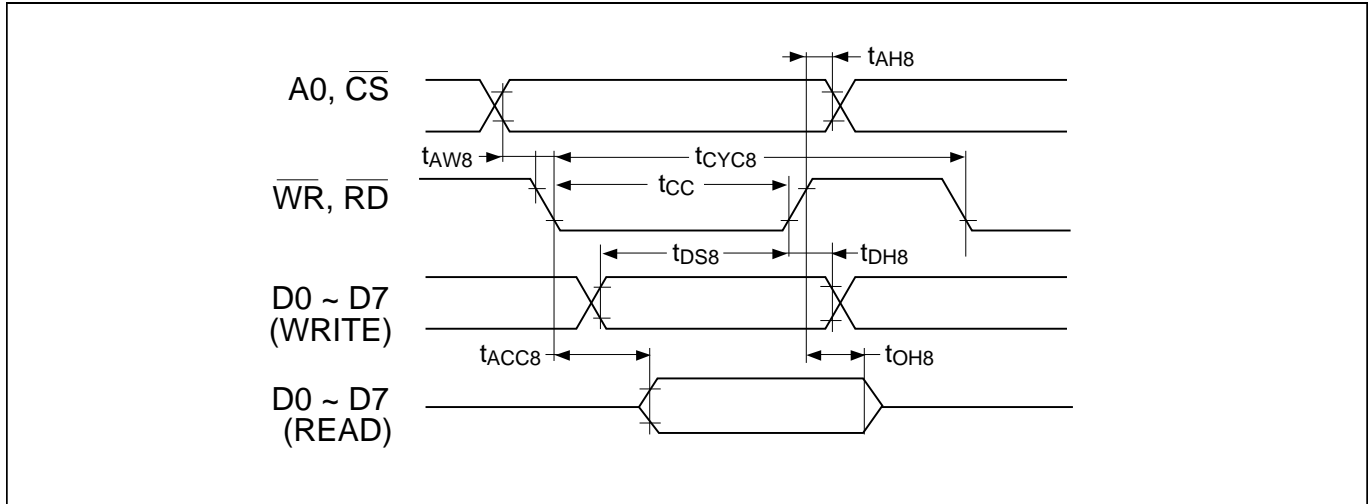
*12. Applicable to SED1520FAA and SED1521FAA

*13. Applicable to SED1520FOA

*14. Applicable to SED1521FOA

5.3 TIMING CHARACTERISTICS

5.3.1 System Bus Read/Write I (80 Family MPU)



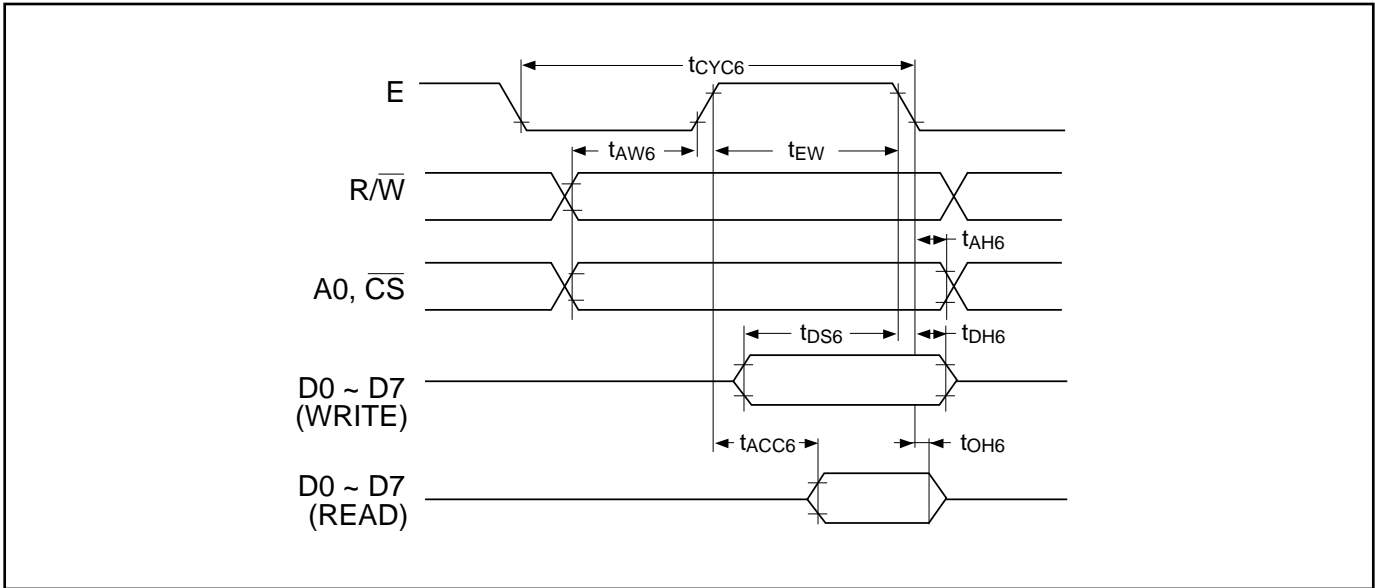
Ta = -20 to 75°C, Vss = -5.0V ± 10%, Unit: ns

| Signal | Symbol | Parameter | Min. | Max. | Condition |
|-----------------------------------|--------|-----------------------------|------|------|------------|
| A0, \overline{CS} | t AH8 | Address hold time | 10 | | |
| | t AW8 | Address setup time | 20 | | |
| \overline{WR} , \overline{RD} | t CYC8 | System cycle time | 1000 | | |
| | t CC | Control pulse width | 200 | | |
| D0–D7 | t DS8 | Data setup time | 80 | | |
| | t DH8 | Data hold time | 10 | | |
| | t ACC8 | \overline{RD} access time | | 90 | |
| | t OH8 | Output disable time | 10 | 60 | |
| | | | | | CL = 100pF |

*1. Each of the values where Vss = -3.0V is about 200% of that where Vss = -5.0V (i.e., the listed value).

*2. The rise or fall time of input signals should be less than 15 ns.

5.3.2 System Bus Read/Write II (68 Family MPU)

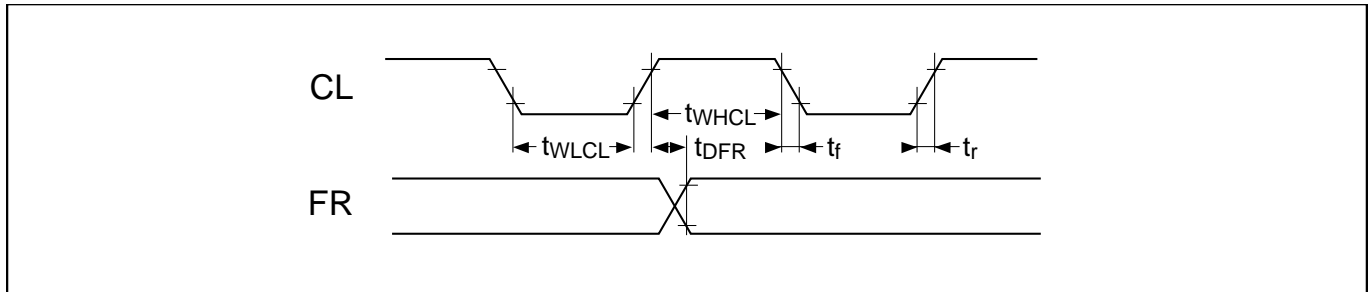


Ta = -20 to 75°C, Vss = -5.0V ± 10%, Unit: ns

| Signal | Symbol | Parameter | Min. | Max. | Condition |
|--|-----------------|---------------------|-------|------|------------|
| A0, \overline{CS} R/ \overline{W} | t_{CYC6}^{*1} | System cycle time | 1000 | | CL = 100pF |
| | t_{AW6} | Address setup time | 20 | | |
| | t_{AH6} | Address hold time | 10 | | |
| D0-D7 | t_{DS6} | Data setup time | 80 | | |
| | t_{DH6} | Data hold time | 10 | | |
| | t_{OH6} | Output disable time | 10 | 60 | |
| | t_{ACC6} | Access time | | 90 | |
| E | t_{EW} | Enable pulse width | Read | 100 | |
| | | | Write | 80 | |

- *1. t_{CYC6} indicates the cycle time during which $CS \cdot E = "H"$. It does not mean the cycle time of signal E.
- *2. Each of the values where $V_{SS} = -3.0V$ is about 200% of that where $V_{SS} = -5.0V$ (i.e., the listed value).
- *3. The rise or fall time of input signals should be less than 15 ns.

5.3.3 Display Control Timing



5.3.3.1 Input Timing

$T_a = -20$ to 75°C , $V_{SS} = -5.0\text{V} \pm 10\%$
 Unit: μs (t_{WLCL} , t_{WHCL} , t_{DFR}), ns (t_r , t_f)

| Signal | Symbol | Parameter | Min. | Typ. | Max. | Condition |
|--------|------------|------------------------|------|------|------|-----------|
| CL | t_{WLCL} | Low level pulse width | 35 | | | |
| | t_{WHCL} | High level pulse width | 35 | | | |
| | t_r | Rise time | | 30 | 150 | |
| | t_f | Fall time | | 30 | 150 | |
| FR | t_{DFR} | FR delay time | -2.0 | 0.2 | 2.0 | |

5.3.3.2 Output Timing

$T_a = -20$ to 75°C , $V_{SS} = -5.0\text{V} \pm 10\%$, Unit: μs

| Signal | Symbol | Parameter | Min. | Typ. | Max. | Condition |
|--------|-----------|---------------|------|------|------|------------|
| FR | t_{DFR} | FR delay time | | 0.2 | 0.4 | CL = 100pF |

*1. The listed FR input delay time applies to the SED1521 and SED1520 (slave).

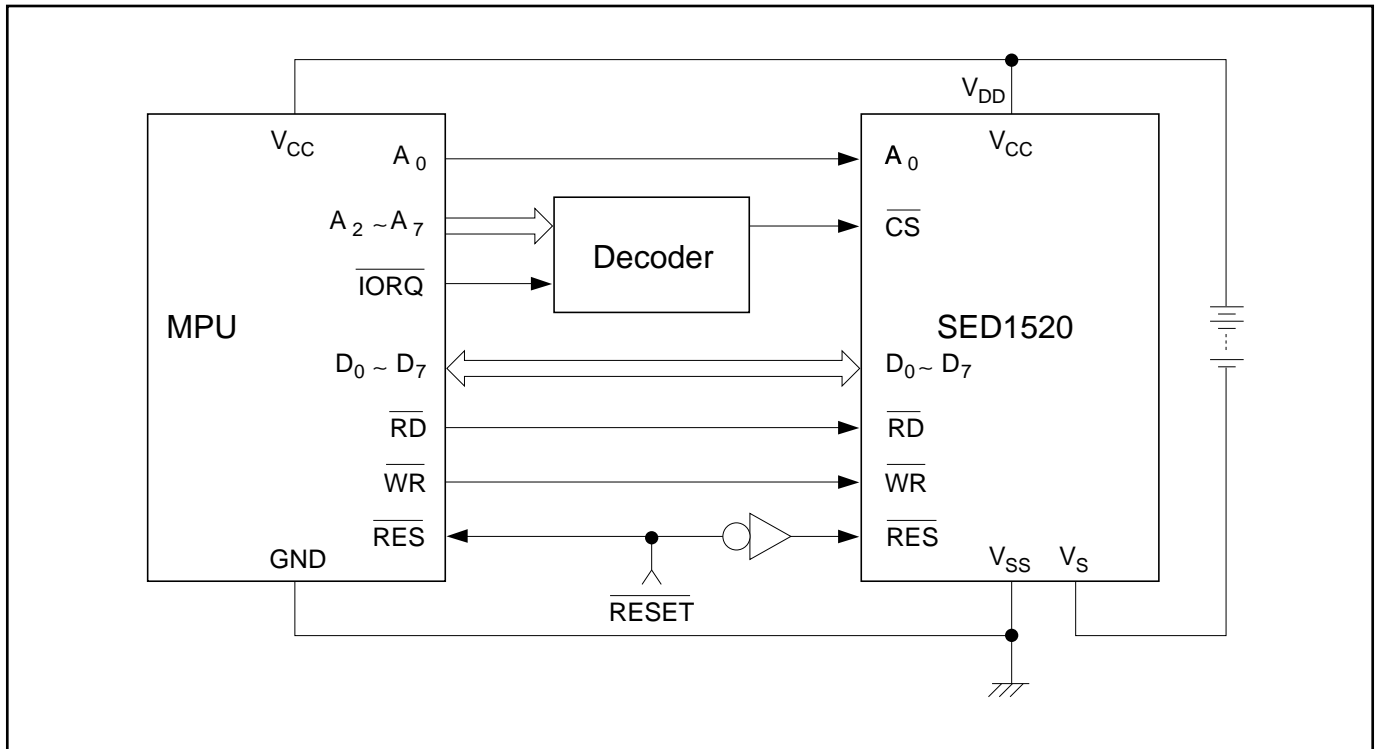
The listed FR output delay time applies to the SED1520 (master).

*2. Each of the values where $V_{SS} = -3.0\text{V}$ is about 200% of that where $V_{SS} = -5.0\text{V}$ (i.e., the listed value).

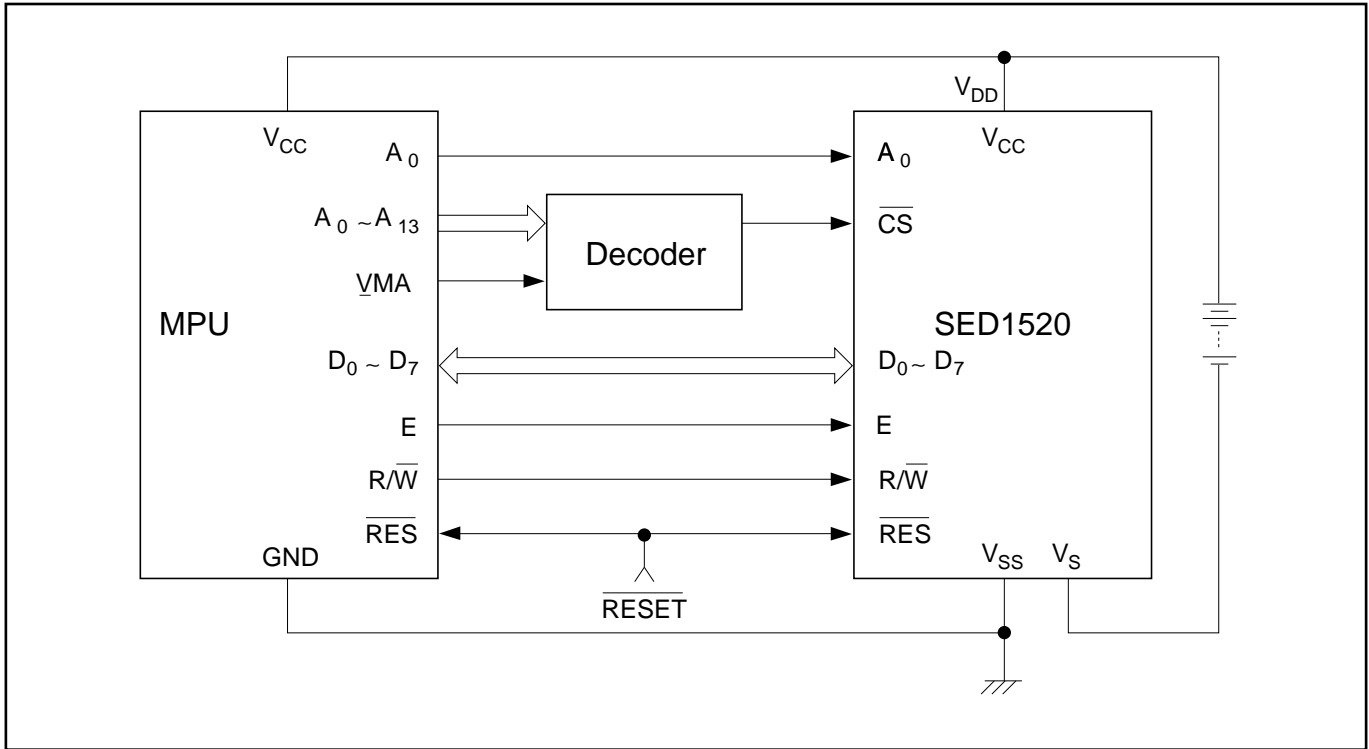
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6.0 MPU INTERFACE

6.1 80 FAMILY MPU

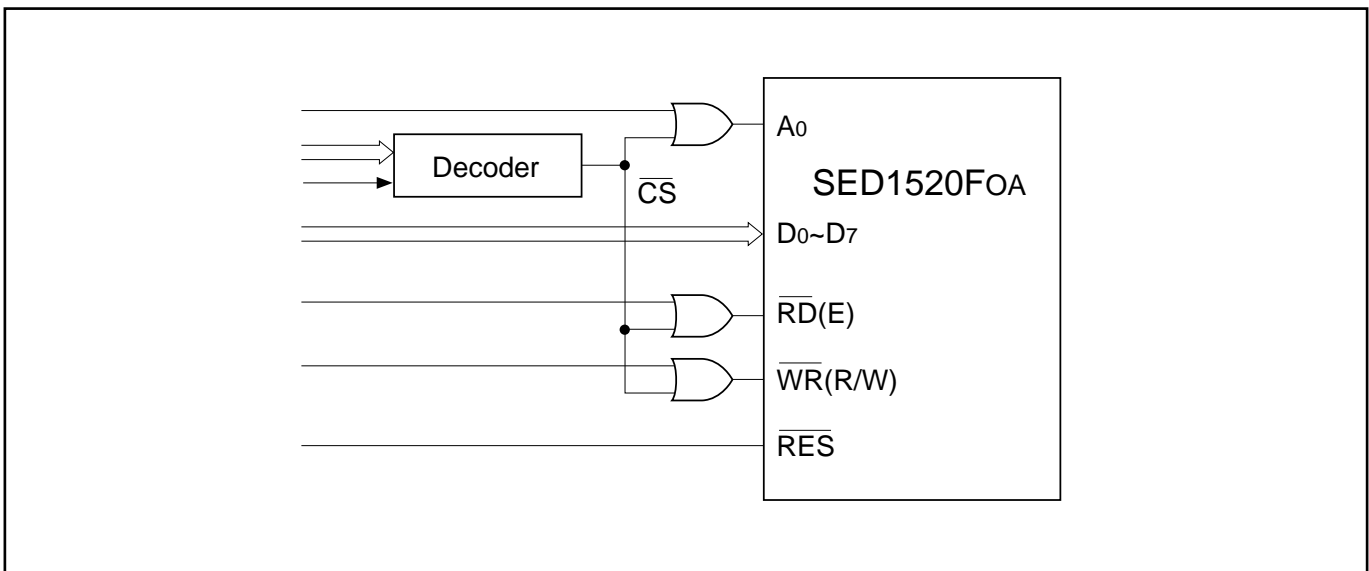


6.2 68 FAMILY MPU



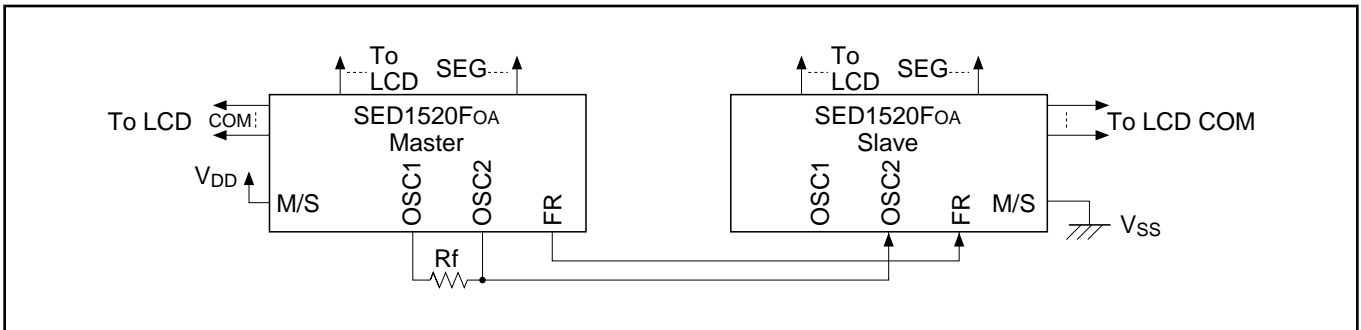
* These examples also apply to the SED1521FOA/SED1521FAA.

* The SED1520 (containing an oscillator) does not have pin \overline{CS} . The output ORed with \overline{CS} must be applied to pins A_0 , \overline{RD} (E) and \overline{WR} (R/W).

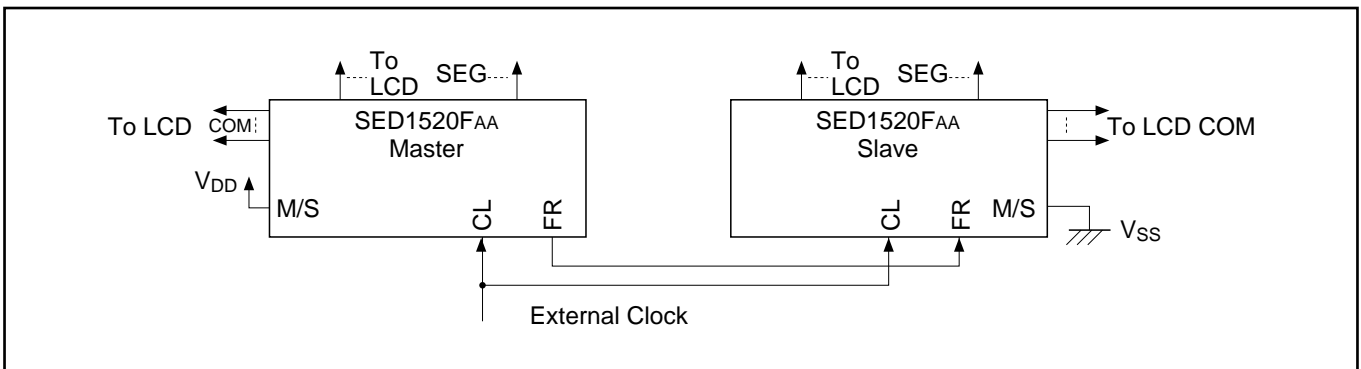


7.0 LCD DRIVER INTERCONNECTIONS

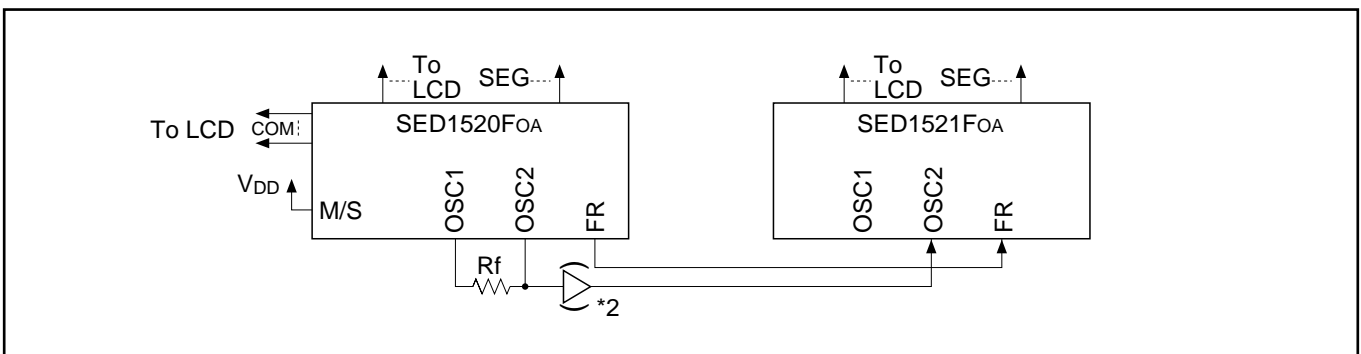
7.1 SED1520FoA - SED1520FoA



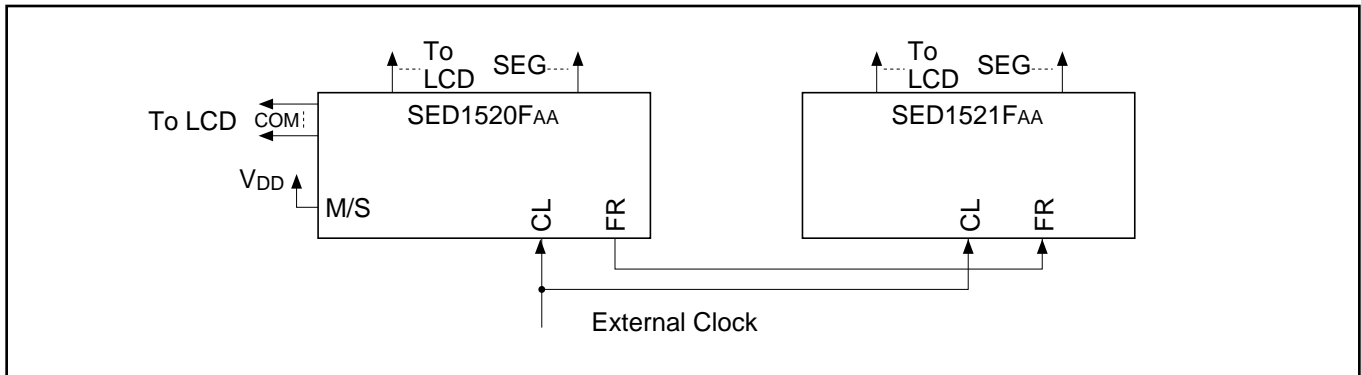
7.2 SED1520FAA - SED1520FAA



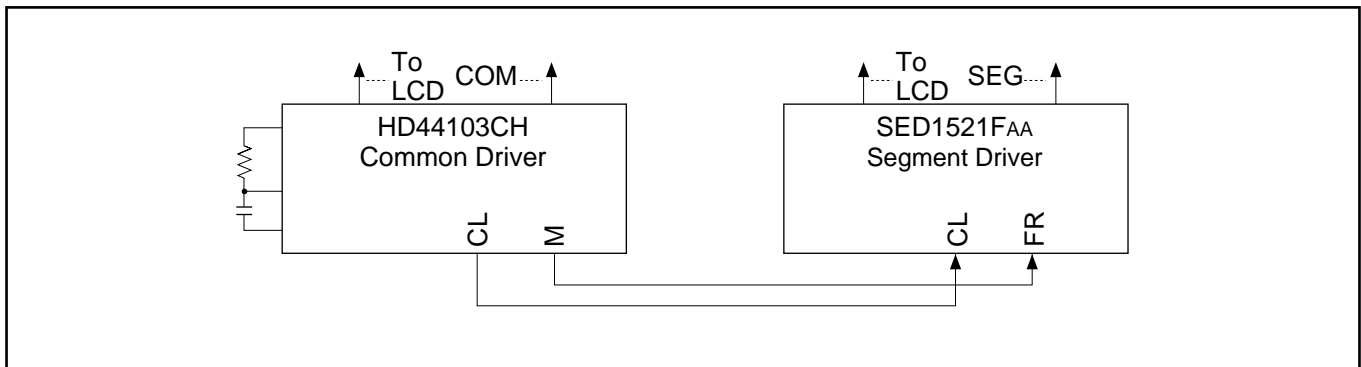
7.3 SED1520FoA - SED1521FoA *1



7.4 SED1520FAA - SED1521FAA



7.5 HD44103CH - SED1521FAA

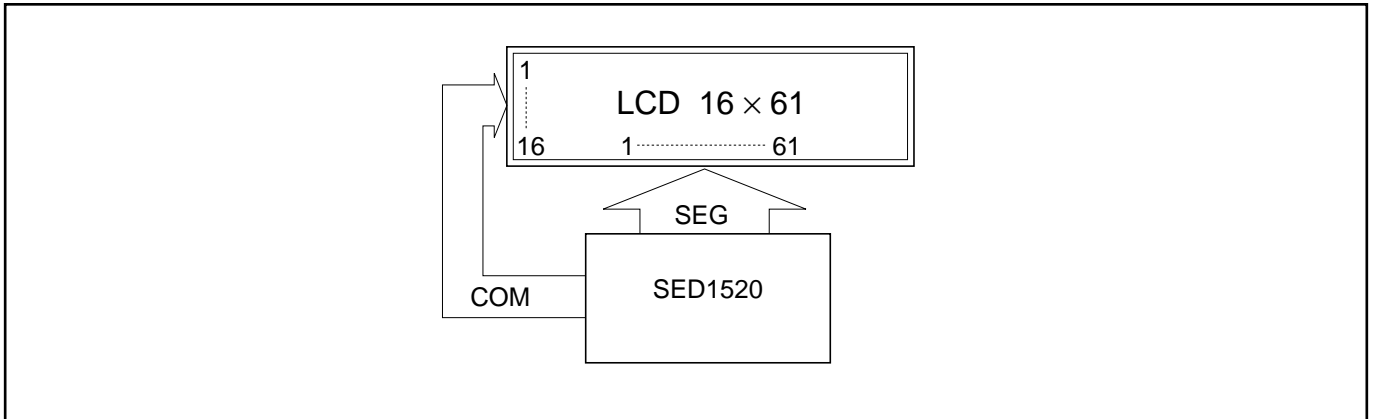


- *1. In this connection, the duty of the SED1521FOA must be the same as that of the SED1520FOA.
- *2. A CMOS buffer is needed for a system having two or more slave LSIs.

8.0 TYPICAL CONNECTIONS WITH LCD PANEL

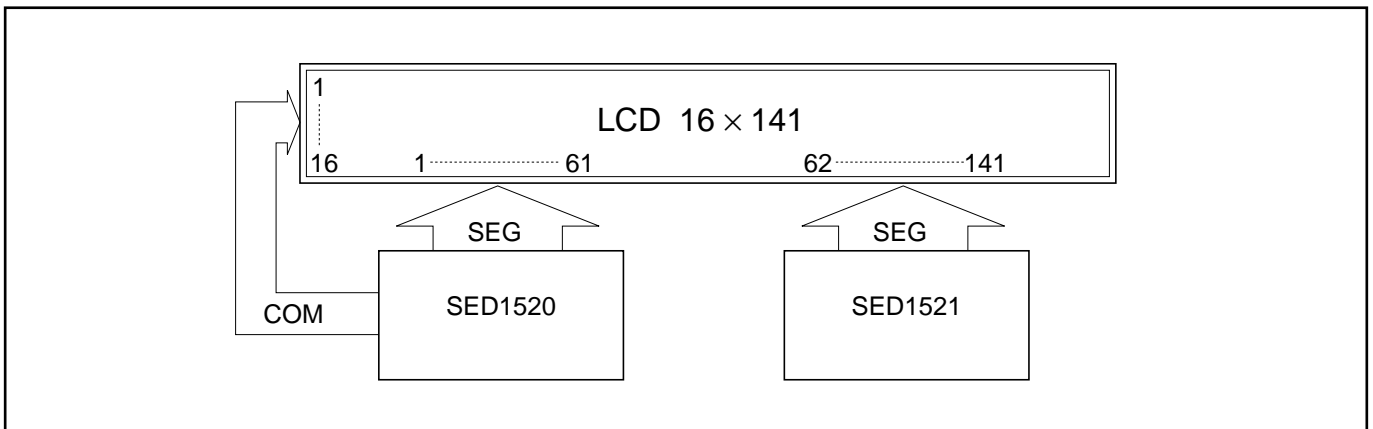
8.1 DUTY 1/16, 10 CHARACTERS X 2 LINES

(Full dot LCD panel: 1 character = 6 × 8 dots)



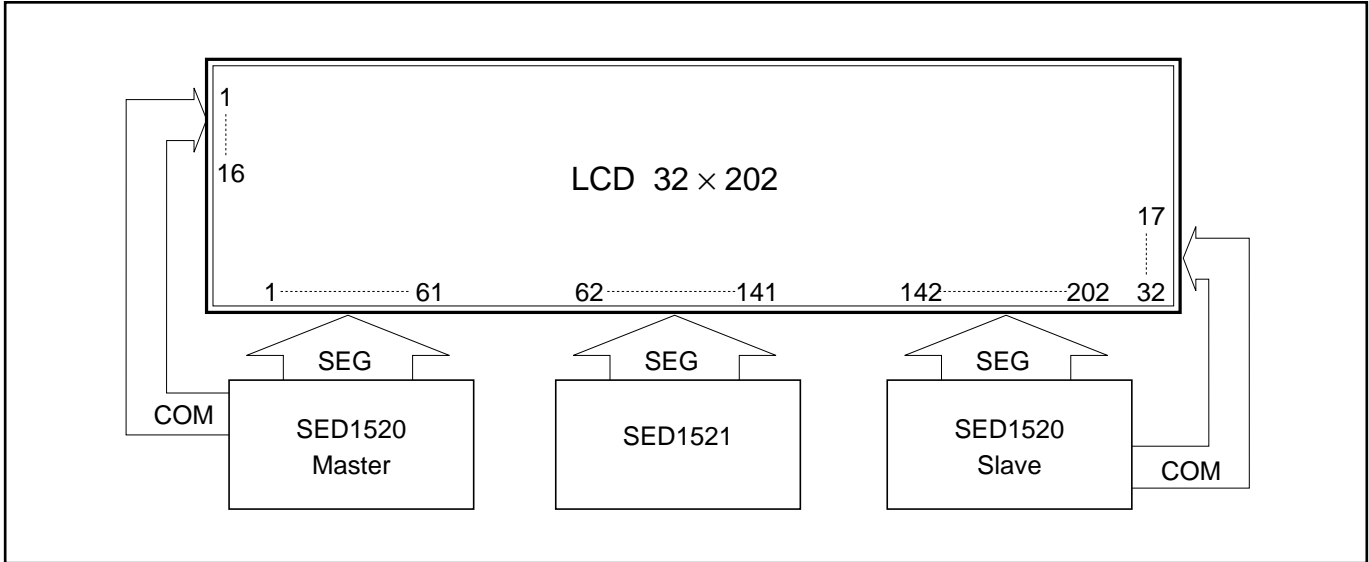
8.2 DUTY 1/16, 23 CHARACTERS X 2 LINES

(Full dot LCD panel: 1 character = 6 × 8 dots)



8.3 DUTY 1/32, 33 CHARACTERS X 4 LINES

(Full dot LCD panel: 1 character = 6 × 8 dots)

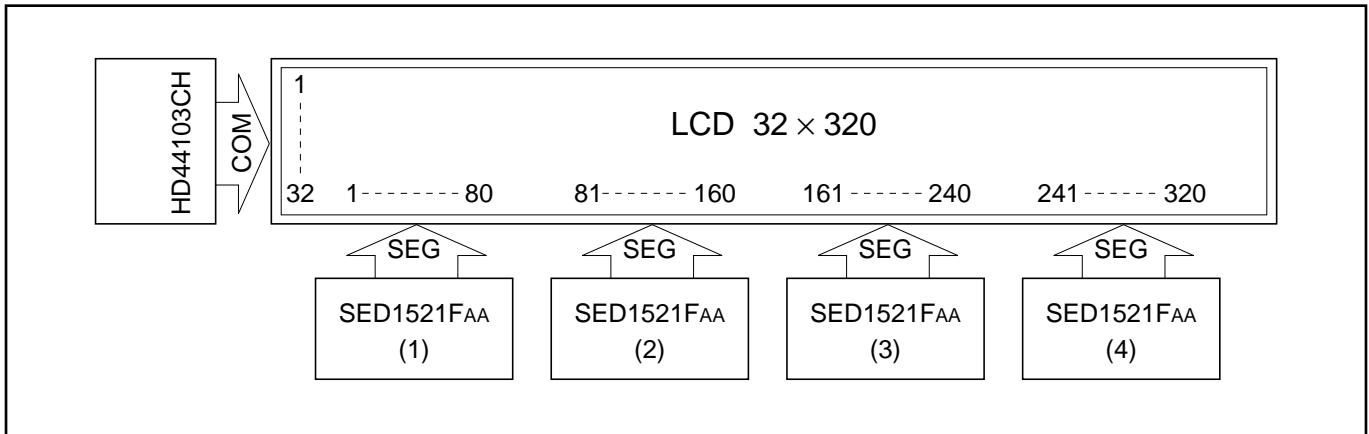


* SED1521F may be omitted. If it is not used, the panel consists of 32 × 122 dots.

Note: Type AA (using external clock) and type 0A (containing an oscillator) cannot coexist for the same panel.

8.4 DUTY 1/32, 20 KANJI CHARACTERS X 2 LINES

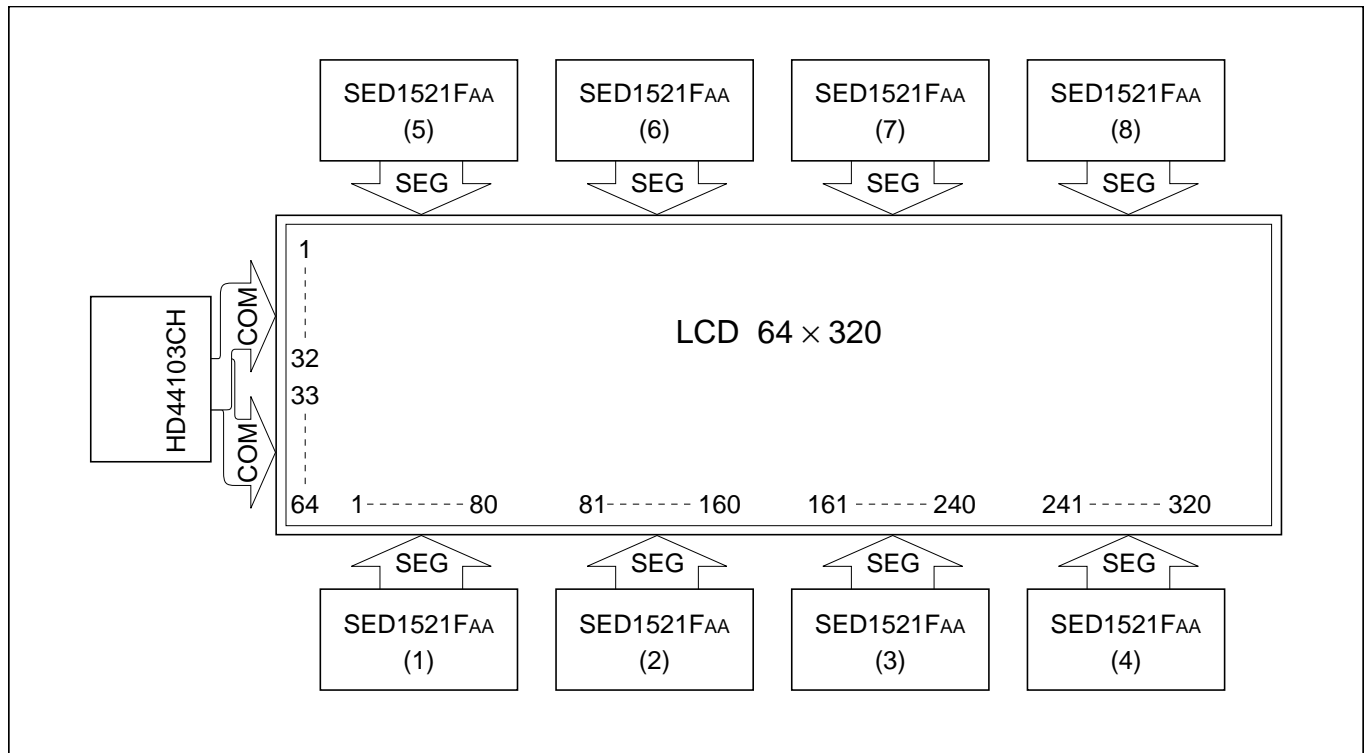
(Kanji – Character 16 x 16 dots)



8.0 Typical Connections with LCD Panel

8.5 – 8.5

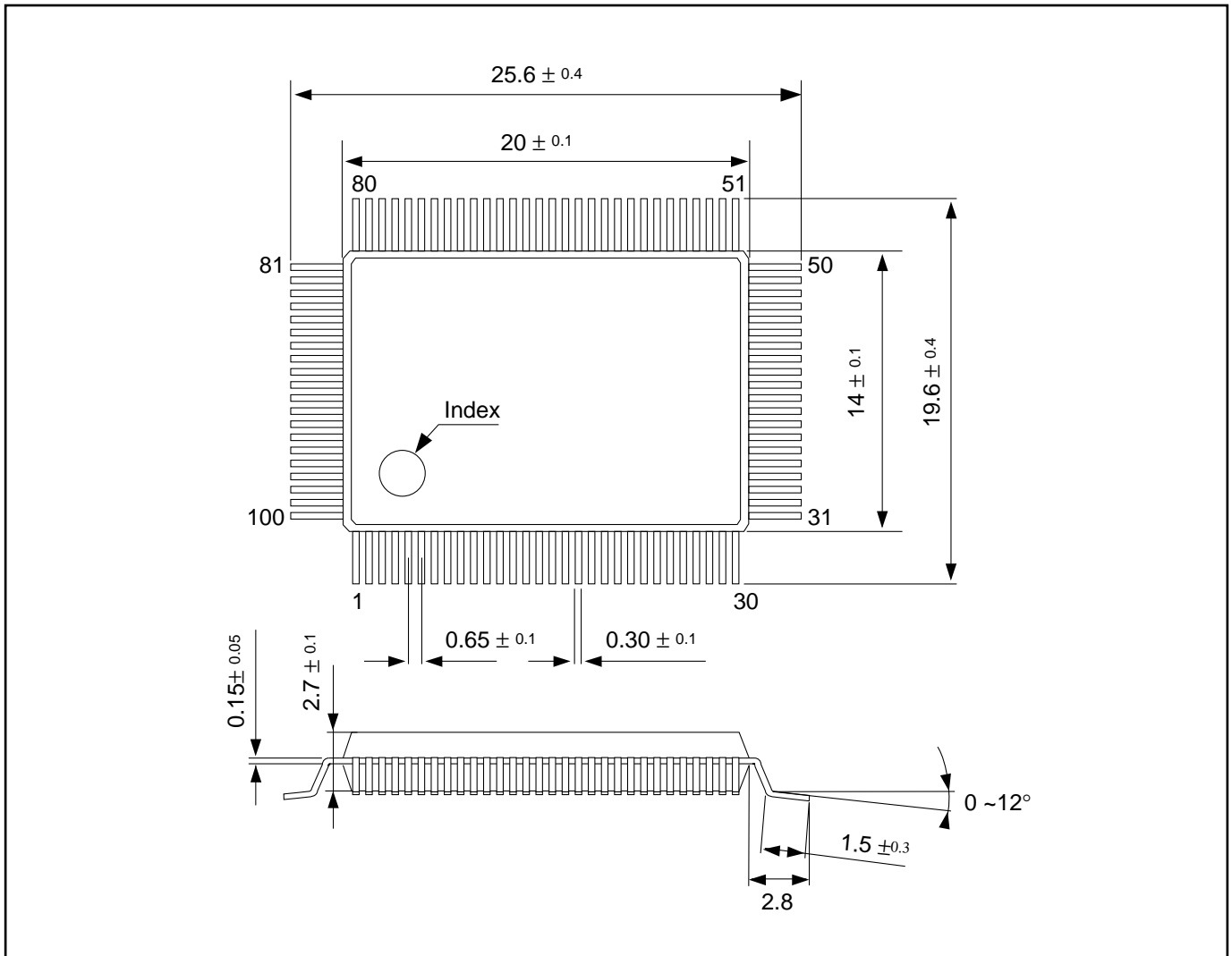
8.5 DUTY 1/32, 2-SCREEN DISPLAY, 20 KANJI CHARACTERS X 4 LINES



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9.0 PACKAGE DIMENSIONS

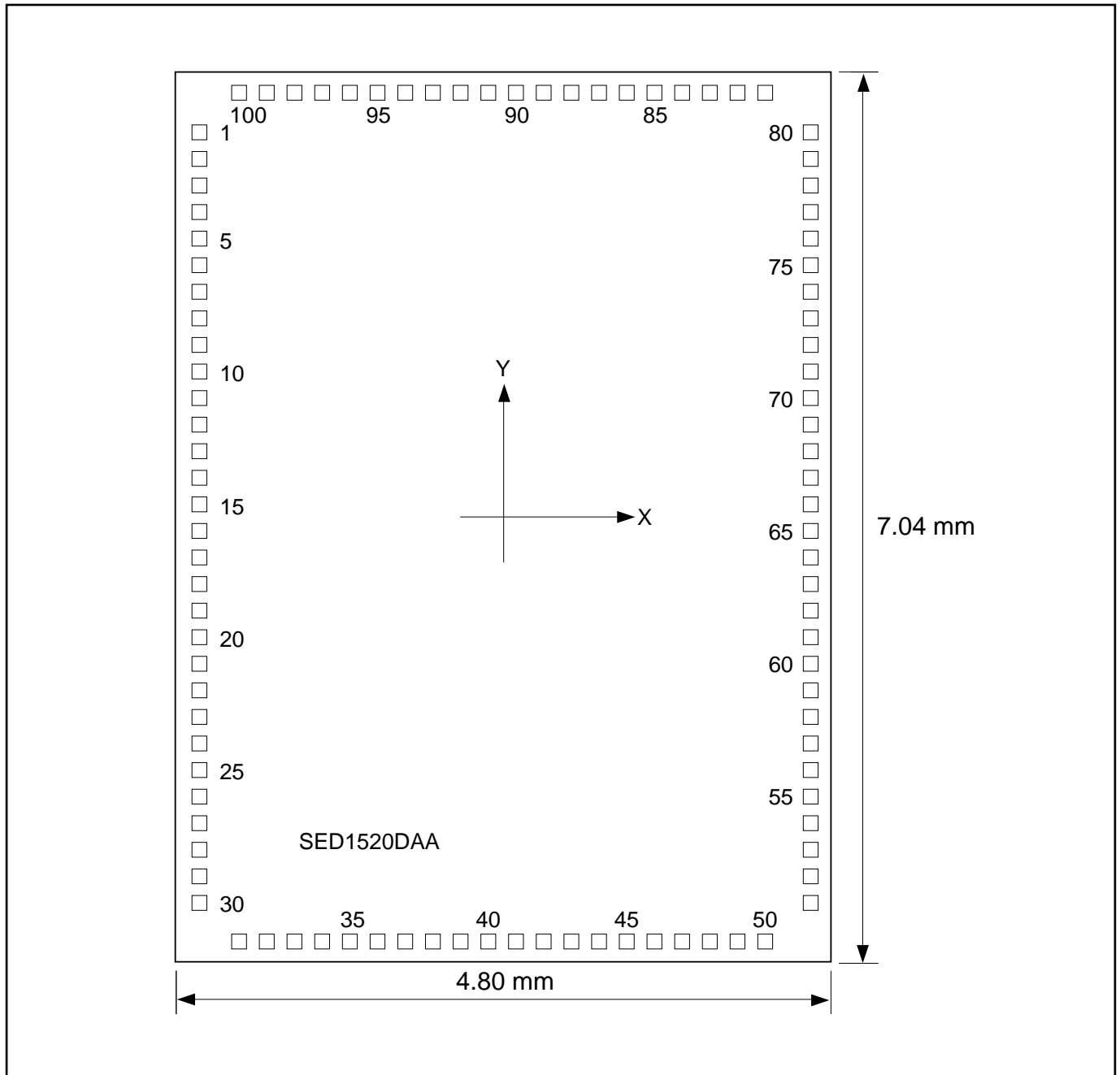
9.1 PLASTIC QFP 5-100 PIN



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10.0 PAD LAYOUT

10.1 PAD LAYOUT (SED1520D/SED1521D)



10.1.1 Al Pad

| Chip Specification | Dimensions (mm) |
|---------------------------|------------------------|
| Chip size | 7.04 × 4.80 |
| Chip thickness | 0.400 ± 0.025 |
| Pad size | 0.10 × 0.10 |

10.1.2 Au Bump Pad

| Chip Specification | Dimensions (mm) |
|---------------------------|------------------------|
| Chip size | 7.04 × 4.80 |
| Chip thickness | 0.525 ± 0.025 |
| Pad size | 0.132 × 0.111 |
| Pad pitch | 0.199 min |
| Bump height | 0.020 + 0.01 to -0.005 |

10.0 Pad Layout

10.2 – 10.2

10.2 PAD COORDINATES (SED1520DAB)

| Pad | | X | Y | Pad | | X | Y | Pad | | X | Y |
|-----|-------|------|------|-----|-------|------|------|-----|-------------------------|------|------|
| No. | Name | | | No. | Name | | | No. | Name | | |
| 1 | COM5 | 159 | 6507 | 35 | SEG37 | 1302 | 159 | 69 | SEG3 | 4641 | 4148 |
| 2 | COM6 | 159 | 6308 | 36 | SEG36 | 1502 | 159 | 70 | SEG2 | 4641 | 4347 |
| 3 | COM7 | 159 | 6108 | 37 | SEG35 | 1701 | 159 | 71 | SEG1 | 4641 | 4547 |
| 4 | COM8 | 159 | 5909 | 38 | SEG34 | 1901 | 159 | 72 | SEG0 | 4641 | 4789 |
| 5 | COM9 | 159 | 5709 | 39 | SEG33 | 2100 | 159 | 73 | A0 | 4641 | 5048 |
| 6 | COM10 | 159 | 5510 | 40 | SEG32 | 2300 | 159 | 74 | \overline{CS} | 4641 | 5247 |
| 7 | COM11 | 159 | 5310 | 41 | SEG31 | 2499 | 159 | 75 | CL | 4641 | 5447 |
| 8 | COM12 | 159 | 5111 | 42 | SEG30 | 2699 | 159 | 76 | $E(\overline{RD})$ | 4641 | 5646 |
| 9 | COM13 | 159 | 4911 | 43 | SEG29 | 2898 | 159 | 77 | R/W (\overline{WR}) | 4641 | 5846 |
| 10 | COM14 | 159 | 4712 | 44 | SEG28 | 3098 | 159 | 78 | Vss | 4641 | 6107 |
| 11 | COM15 | 159 | 4512 | 45 | SEG27 | 3297 | 159 | 79 | DB0 | 4641 | 6307 |
| 12 | SEG60 | 159 | 4169 | 46 | SEG26 | 3497 | 159 | 80 | DB1 | 4641 | 6506 |
| 13 | SEG59 | 159 | 3969 | 47 | SEG25 | 2696 | 159 | 81 | DB2 | 4295 | 6884 |
| 14 | SEG58 | 159 | 3770 | 48 | SEG24 | 3896 | 159 | 82 | DB3 | 4095 | 6884 |
| 15 | SEG57 | 159 | 3570 | 49 | SEG23 | 4095 | 159 | 83 | DB4 | 3896 | 6884 |
| 16 | SEG56 | 159 | 3371 | 50 | SEG22 | 4295 | 159 | 84 | DB5 | 3696 | 6884 |
| 17 | SEG55 | 159 | 3075 | 51 | SEG21 | 4641 | 482 | 85 | DB6 | 3497 | 6884 |
| 18 | SEG54 | 159 | 2876 | 52 | SEG20 | 4641 | 681 | 86 | DB7 | 3297 | 6884 |
| 19 | SEG53 | 159 | 2676 | 53 | SEG19 | 4641 | 881 | 87 | VDD | 3098 | 6884 |
| 20 | SEG52 | 159 | 2477 | 54 | SEG18 | 4641 | 1080 | 88 | \overline{RES} | 2898 | 6884 |
| 21 | SEG51 | 159 | 2277 | 55 | SEG17 | 4641 | 1280 | 89 | FR | 2699 | 6884 |
| 22 | SEG50 | 159 | 2078 | 56 | SEG16 | 4641 | 1479 | 90 | V5 | 2699 | 6884 |
| 23 | SEG49 | 159 | 1878 | 57 | SEG15 | 4641 | 1679 | 91 | V3 | 2300 | 6884 |
| 24 | SEG48 | 159 | 1679 | 58 | SEG14 | 4641 | 1878 | 92 | V2 | 2100 | 6884 |
| 25 | SEG47 | 159 | 1479 | 59 | SEG13 | 4641 | 2078 | 93 | M/S | 1901 | 6884 |
| 26 | SEG46 | 159 | 1280 | 60 | SEG12 | 4641 | 2277 | 94 | V4 | 1701 | 6884 |
| 27 | SEG45 | 159 | 1080 | 61 | SEG11 | 4641 | 2477 | 95 | V1 | 1502 | 6884 |
| 28 | SEG44 | 159 | 881 | 62 | SEG10 | 4641 | 2676 | 96 | COM0 | 1302 | 6884 |
| 29 | SEG43 | 159 | 681 | 63 | SEG9 | 4641 | 2876 | 97 | COM1 | 1103 | 6884 |
| 30 | SEG42 | 159 | 482 | 64 | SEG8 | 4641 | 3075 | 98 | COM2 | 903 | 6884 |
| 31 | SEG41 | 504 | 159 | 65 | SEG7 | 4641 | 3275 | 99 | COM3 | 704 | 6884 |
| 32 | SEG40 | 704 | 159 | 66 | SEG6 | 4641 | 3474 | 100 | COM4 | 504 | 6884 |
| 33 | SEG39 | 903 | 159 | 67 | SEG5 | 4641 | 3674 | | | | |
| 34 | SEG38 | 1103 | 159 | 68 | SEG4 | 4641 | 3948 | | | | |

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