

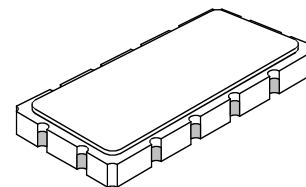


- **Designed for WCDMA 3G IF Applications**
- **Excellent Size-to-Performance Ratio**
- **Balanced or Unbalanced Input and Output**
- **Hermetic 13.3 x 6.5 mm Surface-mount Case**
- **Complies with Directive 2002/95/EC (RoHS)**



SF1124A

190 MHz SAW Filter



SMP-53

Absolute Maximum Ratings

Rating	Value	Units
Maximum Incident Power in Passband	+10	dBm
Max. DC voltage between any 2 terminals	30	VDC
Storage Temperature Range	-40 to +85	°C
Suitable for lead-free soldering - Max. Soldering Profile	260°C for 30 s	

Electrical Characteristics

Characteristic	Sym	Notes	Min	Typ	Max	Units
Nominal Center Frequency	f_c	1	190.000			MHz
Passband	Insertion Loss at f_c	IL		12	14.0	dB
	1 db Passband	BW_1	4.6	5.1		MHz
	3 db Passband	BW_3	5.1	5.7		
	Amplitude Ripple over $f_c \pm 2.4$ MHz			.70	1.0	dB _{p-p}
	Phase Linearity over $f_c \pm 2.4$ MHz			4	10	° _{p-p}
	Group Delay Variation over $f_c \pm 2.4$ MHz	GDV		75	120	ns _{p-p}
Rejection	$f_c - 4.1$ to $f_c - 3.65$ and $f_c + 3.4$ to $f_c + 3.8$ MHz	1, 2, 3	10			dB
	$f_c - 5.0$ to $f_c - 4.1$ and $f_c + 3.8$ to $f_c + 5.0$ MHz		30			
	$f_c - 10.0$ to $f_c - 5.0$ and $f_c + 5.0$ to $f_c + 10.0$ MHz		40			
	$f_c - 20.0$ to $f_c - 10.0$ and $f_c + 10.0$ to $f_c + 20.0$ MHz		40			
	At 157.6 MHz		40			
	At 165.7 MHz		40			
	$f_c - 60$ MHz to $f_c - 20$ MHz		40			
	$f_c + 20$ MHz to $f_c + 60$ MHz		40			
Part to Part Average Group Delay Variation					±5	nsec
Operating Temperature Range	T_A	1	-10	+25	+85	°C
Frequency Temperature Coefficient	FTC			-18		ppm/°C
Impedance Matching to 50Ω Unbalanced	External L-C					
Case Style	SMP-53 13.3 x 6.5 mm Nominal Footprint					
Lid Symbolization (YY = year, WW = week)	RFM SF1124A YYWW					

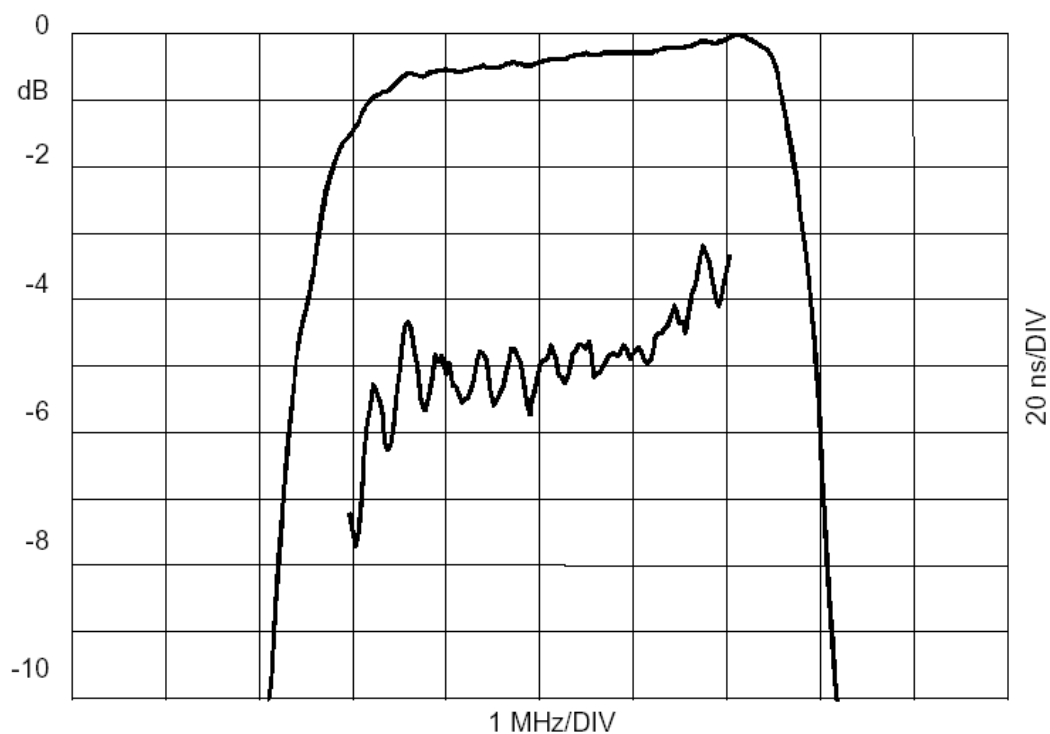
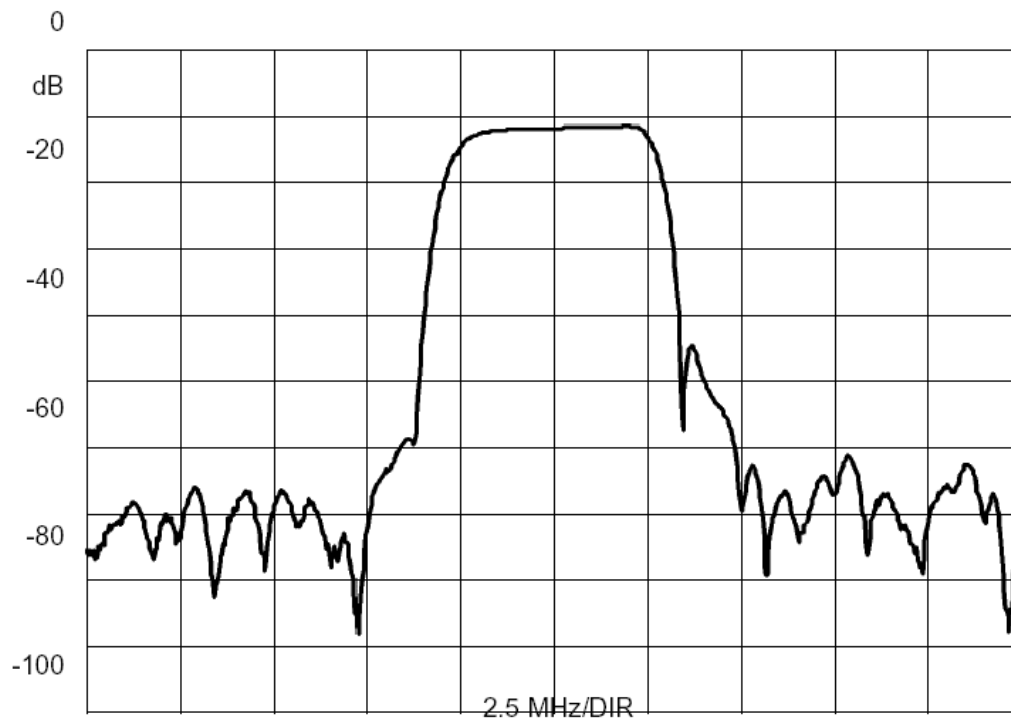
Notes:

1. Unless noted otherwise, all specifications apply over the operating temperature range with filter soldered to the specified demonstration board with impedance matching to 50 Ω and measured with 50 Ω network analyzer.
2. Unless noted otherwise, all frequency specifications are referenced to the nominal center frequency, f_c .
3. Rejection is measured as attenuation below the minimum IL point in the passband. Rejection in final user application is dependent on PCB layout and external impedance matching design. See Application Note No. 42 for details.
4. "LRIP" or "L" after the part number indicates "low rate initial production" and "ENG" or "E" indicates "engineering prototypes."
5. The design, manufacturing process, and specifications of this filter are subject to change.
6. Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
7. US and international patents may apply.
8. Electrostatic Sensitive Device. Observe precautions for handling.



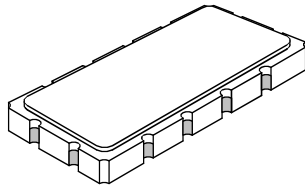
Electrical Connections

Connection	Terminals
Port 1 Hot	11
Port 1 Gnd Return	12
Port 2 Hot	5
Port 2 Gnd Return	6
Case Ground	All others



SMP-53 Case

12-Terminal Ceramic Surface-Mount Case
13.3 x 6.5 mm Nominal Footprint



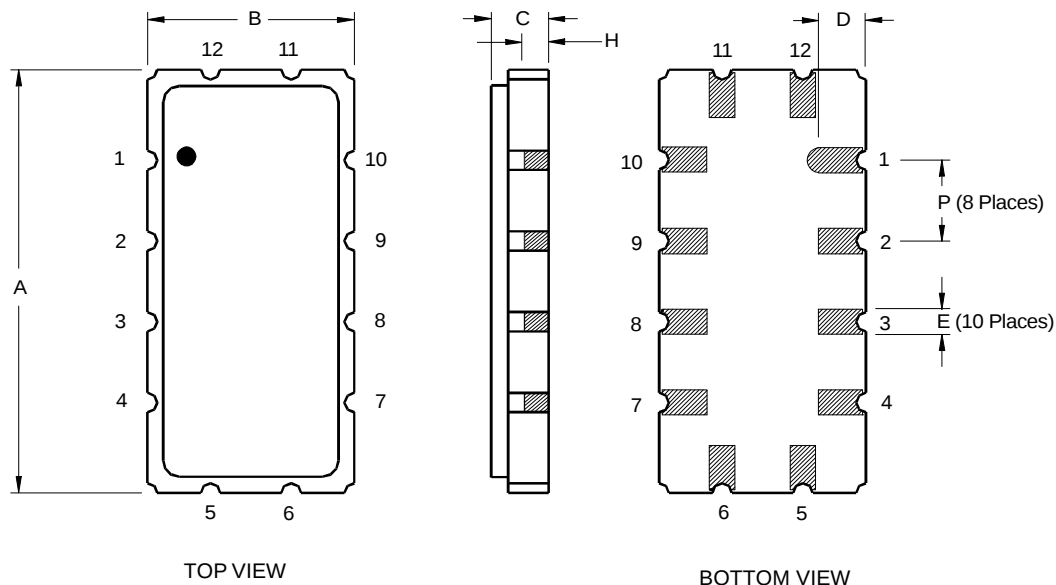
Case Dimensions

Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	13.08	13.31	13.60	0.515	0.524	0.535
B	6.27	6.50	6.80	0.247	0.256	0.268
C		1.91	2.00		0.075	0.079
D		1.50			0.059	
E		0.79			0.031	
H		1.0			0.039	
P		2.54			0.100	

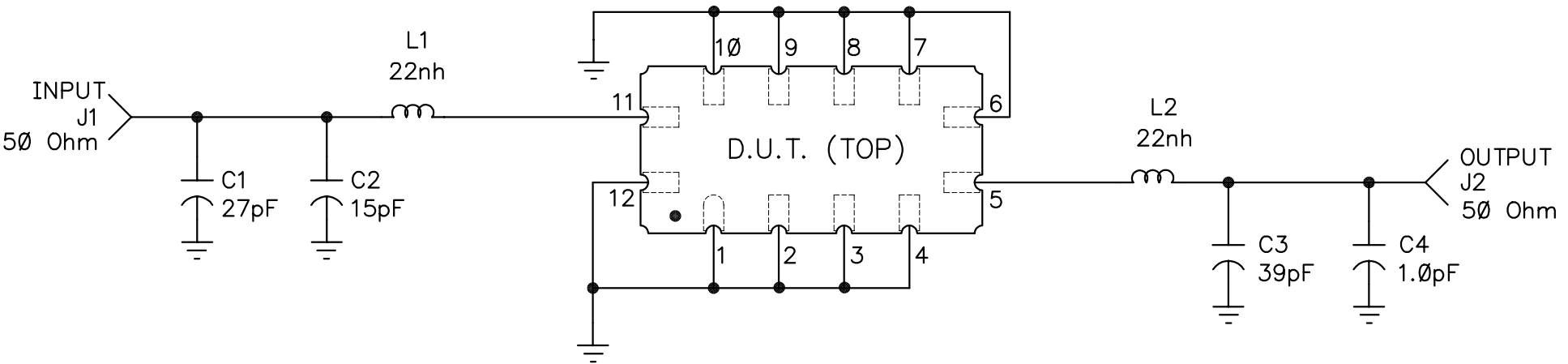
Materials	
Solder Pad Termination	Au plating 30 - 60 ulnches (76.2-152 uM) over 80-200 ulnches (203-508 uM) Ni.
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 ulnches Thick
Body	Al ₂ O ₃ Ceramic
Pb Free	

Electrical Connections

Connection		Terminals
Port 1	Input or Return	11
	Return or Input	12
Port 2	Output or Return	5
	Return or Output	6
Ground		All others
Single Ended Operation		Return is ground
Differential Operation		Return is hot



REV	ECN NO.	DESCRIPTION	APP/DATE
A	9188	INITIAL RELEASE	29nov00



DRAWN BY/DATE: J.F.Christopherson 29nov00

TITLE: SF1124A DEMO PCB

RF Monolithics, Inc.
DALLAS, TEXAS 75244

CHECKED/APPROVED

SIZE
A

CODE IDENT
2U874

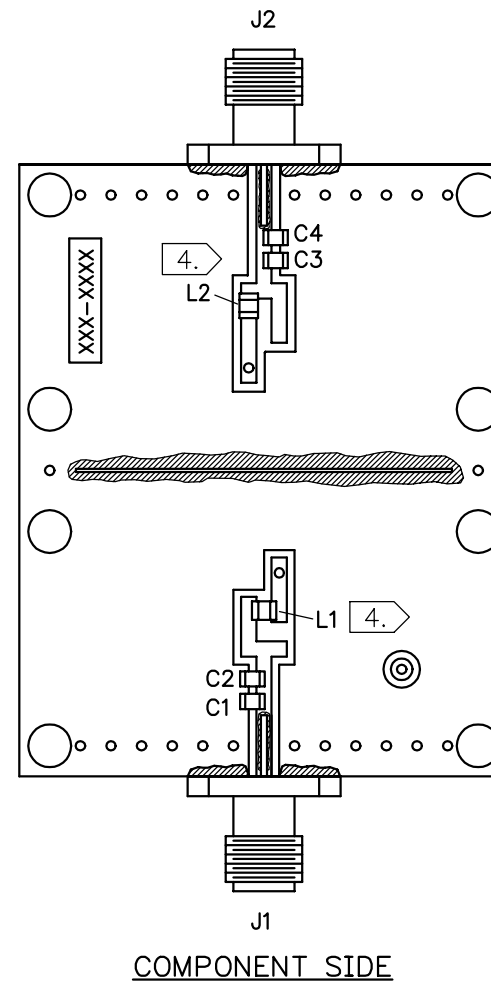
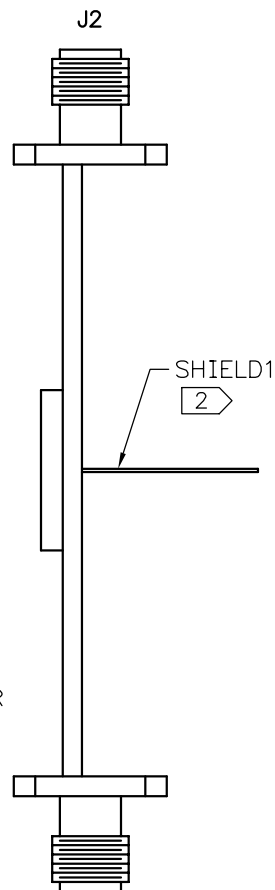
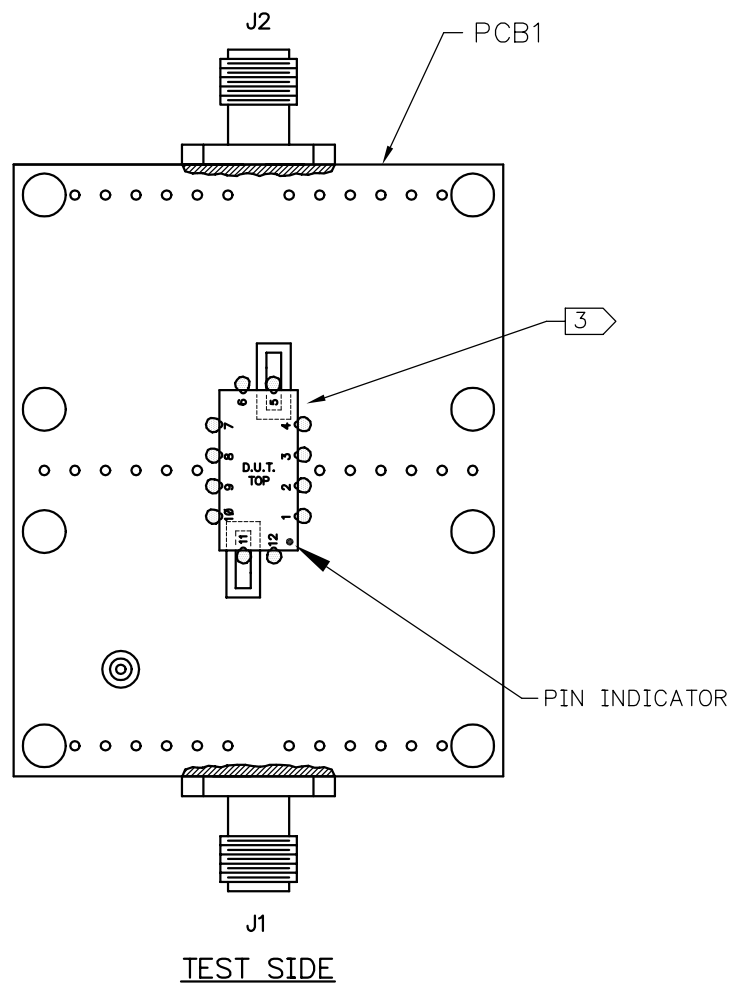
DWG. NO.
SF1124A-000

REV
A

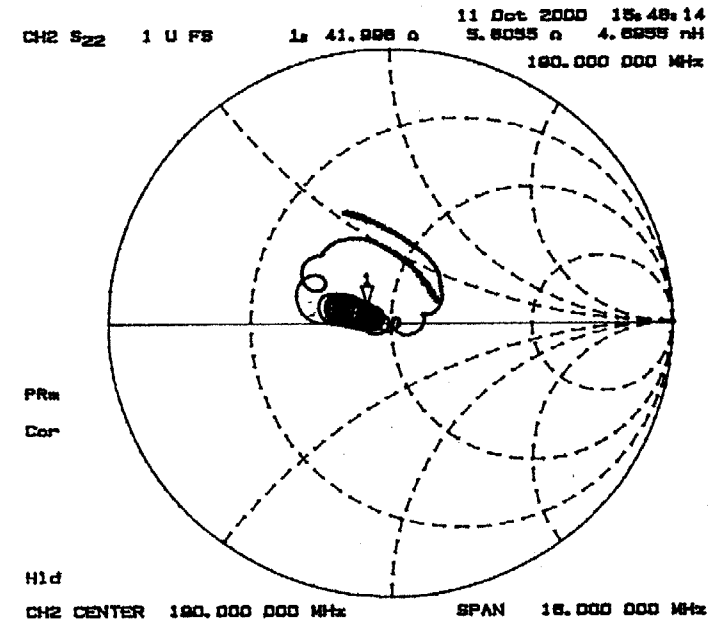
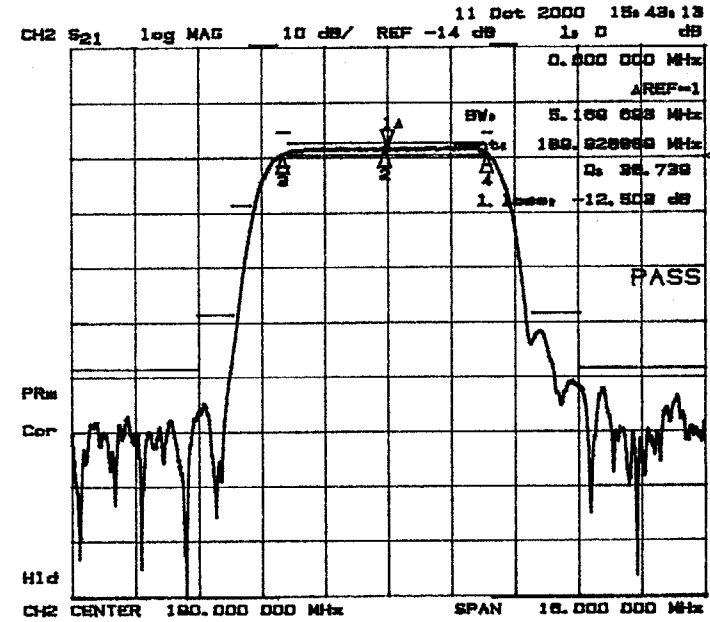
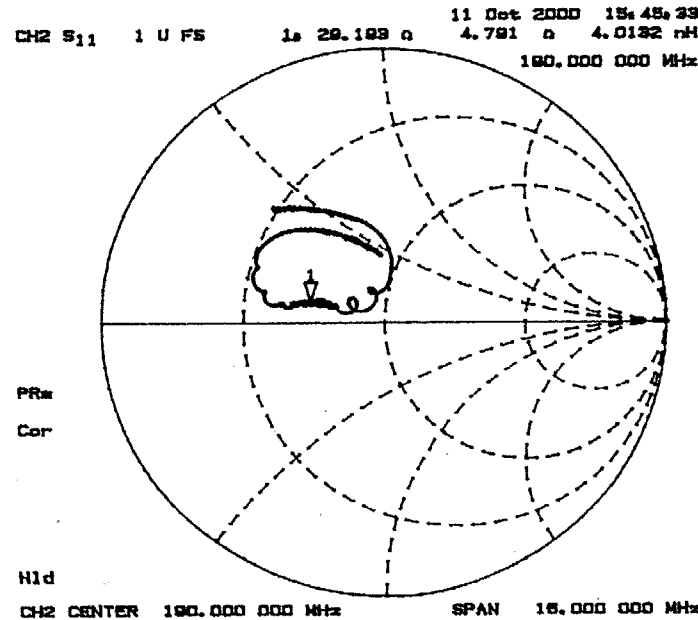
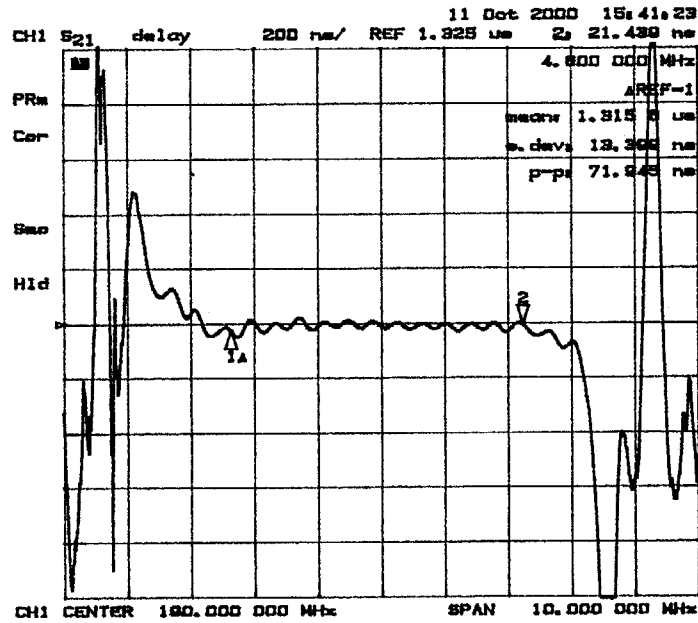
SHEET
1/3

NOTES:

1. SOLDER MOUNT COMPONENTS & CONNECTORS TO PCB1.
2. SOLDER SHIELD1 AS SHOWN AND TRIM TAB FROM SHIELD SO THAT IT IS FLUSH WITH PCB.
3. ORIENT THE FLTR1 AND SOLDER IT DOWN TO THE BOARD AS SHOWN.
4. L1 AND L2 INDUCTORS ARE 90° TO EACH OTHER.

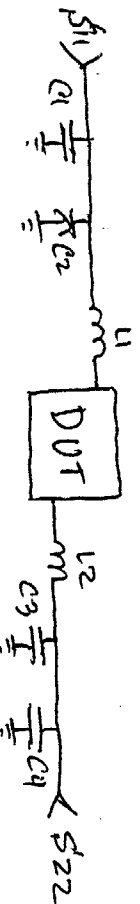


SF1124A
 DEMO#4
 10-11-00
 RT



C1=23pf
 C2=15pf
 C3=39pf
 C4=1pf

L1, L2=22nH



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