# SFC2309-200
# Flip Chip TVS Diode with T-Filter for Color LCD Interface Protection

**PROTECTION PRODUCTS**

## Description

The SFC2309-200 is a low pass filter array with integrated TVS diodes. It is designed to suppress unwanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for **protection of color LCD panels** in cellular phones and other portable electronics.

The device consists of ten identical circuits comprised of TVS diodes for ESD protection, and a resistor - capacitor network for EMI/RFI filtering. A series resistor value of 200Ω and a capacitance value of 45pF is used to achieve 25dB minimum attenuation from 800MHz to 3GHz. Each line features two stages of TVS diode protection. The TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±8kV (contact discharge) per IEC 61000-4-2, level 4.

The device is a 25-bump, 0.5mm pitch flip chip array with a 5x5 bump grid. It measures 2.6 x 2.6 x 0.65mm. The solder bumps have a nominal diameter of 0.315mm.

## Features

- Flip Chip bidirectional EMI/RFI filter with integrated ESD protection
- ESD protection to
  **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
  **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- Filter performance: 25dB minimum attenuation 800MHz to 3GHz
- TVS working voltage: 5V
- Resistor: 200Ω
- Input Capacitance:45pF
- Protection and filtering for ten lines

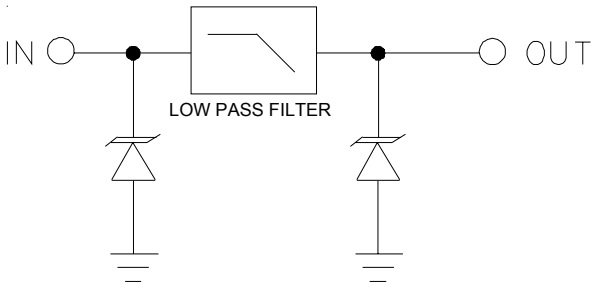
## Mechanical Characteristics

- JEDEC MO-211, Variation BF, 0.50 mm Pitch Flip Chip
- Nominal Dimensions: 2.6 x 2.6 x 0.65 mm
- Bump Diameter: 315±20 µm
- Marking : Marking code, dot at ball A1
- Packaging : Tape and Reel per EIA 481

## Applications

- Color LCD Panel Protection
- Cell Phone Handsets and Accessories
- Personal Digital Assistants (PDA's)
- Notebook & Hand Held Computers

## Circuit Diagram

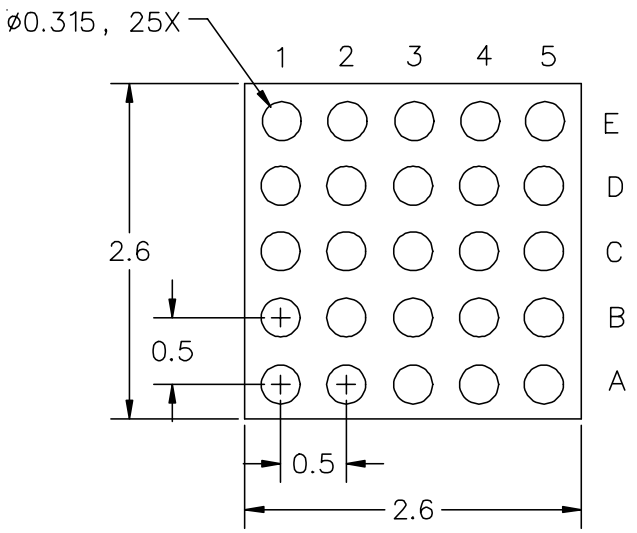



$C_{IN}$ 45pF

$R_S$ 200Ω

**Circuit 10x**

## PIN Configuration




**5 x 5 Grid Flip Chip (Ball Side View)**

## Absolute Maximum Rating

| Rating | Symbol | Value | Units |
|---|---|---|---|
| ESD per IEC 61000-4-2 (Air)<br>ESD per IEC 61000-4-2 (Contact) | $V_{ESD}$ | ± 15<br>± 12 | kV |
| Junction Temperature | $T_J$ | 125 | °C |
| Operating Temperature | $T_{op}$ | -40 to +85 | °C |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

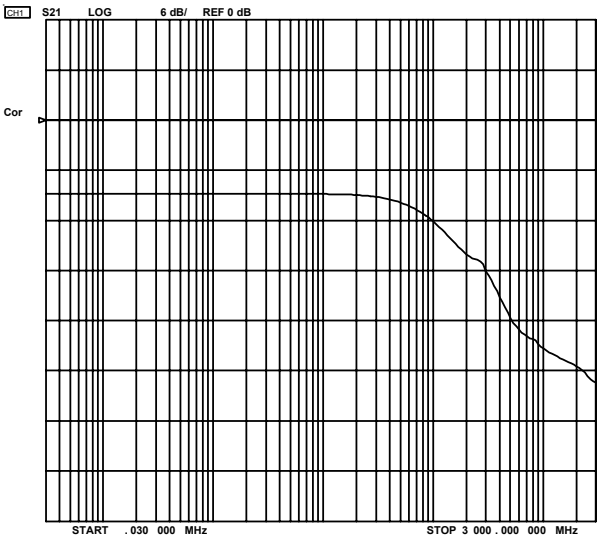
## Electrical Characteristics

**SFC2309-200**

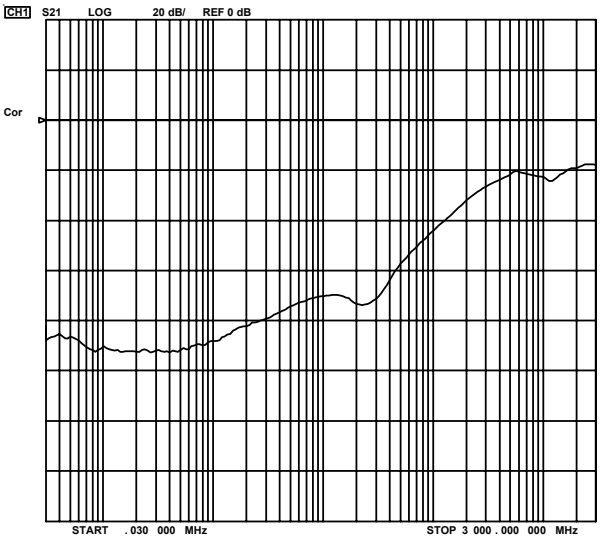
| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| TVS Reverse Stand-Off Voltage | $V_{RWM}$ | | | | 5 | V |
| TVS Reverse Breakdown Voltage | $V_{BR}$ | $I_t$ = 1mA | 6 | 8 | 10 | V |
| TVS Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 3.0V | | | 0.5 | µA |
| Total Series Resistance | R | Each Line | 170 | 200 | 230 | Ω |
| Total Capacitance | $C_{in}$ | Input to Ground,<br>Each Line<br>$V_R$ = 0V, f = 1MHz | | 45 | 50 | pF |

## Typical Characteristics

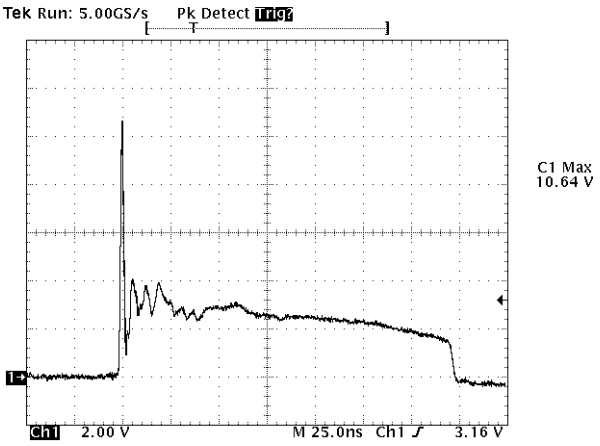
### Typical Insertion Loss S21 (Each Line)



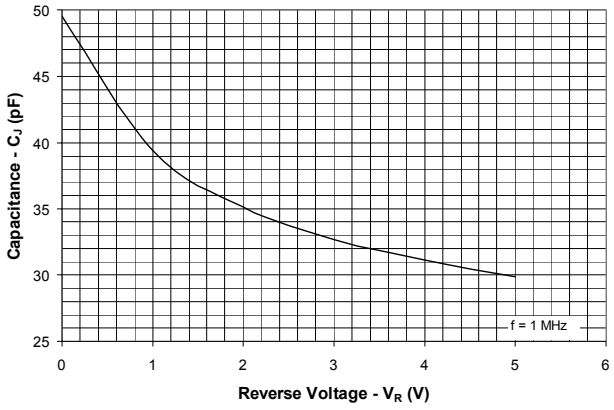

### Analog Crosstalk (Each Line)




### ESD Clamping (8kV Contact)




### Capacitance vs. Reverse Voltage



## Applications Information

### Device Connection Options

The SFC2309-200 has solder bumps located in a 5 x 5 matrix layout on the active side of the device. The bumps are designated by the numbers 1 - 5 along the horizontal axis and letters A - E along the vertical axis. The input of the lines to be protected are connected at bumps A1 - A5 and B1 - B5. The line outputs are connected at bumps D1 - D5 and E1 - E5. Bumps C1 - C5 are connected to ground. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces.

### Wafer Level CSP TVS

CSP TVS devices are wafer level chip scale packages. They eliminate external plastic packages and leads and thus result in a significant board space savings. Manufacturing costs are minimized since they do not require an intermediate level interconnect or interposer layer for reliable operation. They are compatible with current pick and place equipment further reducing manufacturing costs. Certain precautions and design considerations have to be observed however for maximum solder joint reliability. These include solder pad definition, board finish, and assembly parameters.

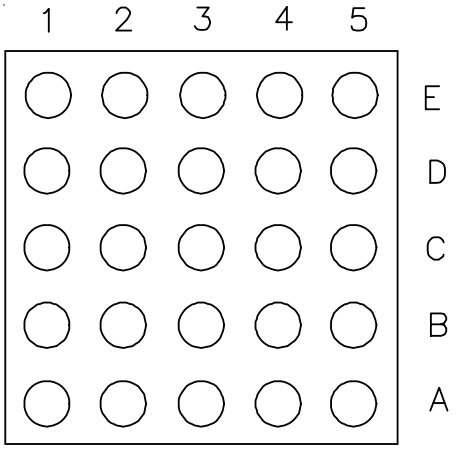
### Printed Circuit Board Mounting

Non-solder mask defined (NSMD) land patterns are recommended for mounting flip chip devices. Solder mask defined (SMD) pads produce stress points at the solder mask to solder ball interface that can result in solder joint cracking when exposed to extreme fatigue conditions. The recommended pad size is 0.275 ± 0.010 mm with a minimum solder mask opening of 0.325 mm.

### Grid Courtyard

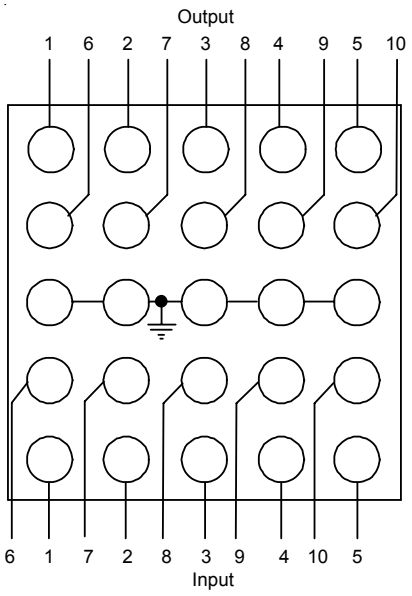
The recommended grid placement courtyard is 2.7 x 2.7 mm. The grid courtyard is intended to encompass the land pattern and the component body that is centered in the land pattern. When placing parts on a PCB, the highest recommended density is when one courtyard touches another.

### Pin Identification and Configuration (Ball Side View)




| Pin | Identification |
|---|---|
| A1 - A5 | Input, Lines 1, 2, 3, 4, 5 |
| B1 - B5 | Input, Lines 6, 7, 8, 9, 10 |
| C1 - C5 | Ground |
| D1 - D5 | Output, Lines 6, 7, 8, 9, 10 |
| E1 - E5 | Output, Lines 1, 2, 3, 4, 5 |

### Layout Example (Ball Side View)



## Applications Information

### Printed Circuit Board Finish

A uniform board finish is critical for good assembly yield. Two finishes that provide uniform surface coatings are immersion nickel gold and organic surface protectant (OSP). A non-uniform finish such as hot air solder leveling (HASL) can lead to mounting problems and should be avoided.

### Stencil Design

A properly designed stencil is key to achieving adequate solder volume without compromising assembly yields. A 0.100mmto 0.200mm thick, laser cut, electropolished stencil with 0.330mm apertures corners with rounded corners is recommended.

### Reflow Profile

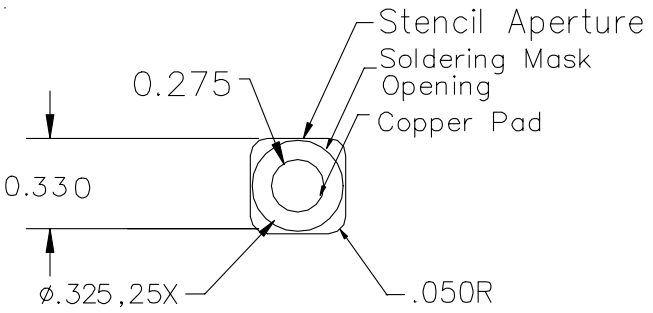
The flip chip TVS can be assembled using standard SMT reflow processes. As with any component, thermal profiles at specific board locations can vary & must be determined by the manufacturer. The flip chip TVS peak reflow temperature is 230 ± 10 °C for a maximum time of 10 seconds. Time above eutectic temperature (183 °C) should be 50 ± 10 seconds. During reflow, the component self-aligns itself on the pad.

### Circuit Board Layout Recommendations for Suppression of ESD

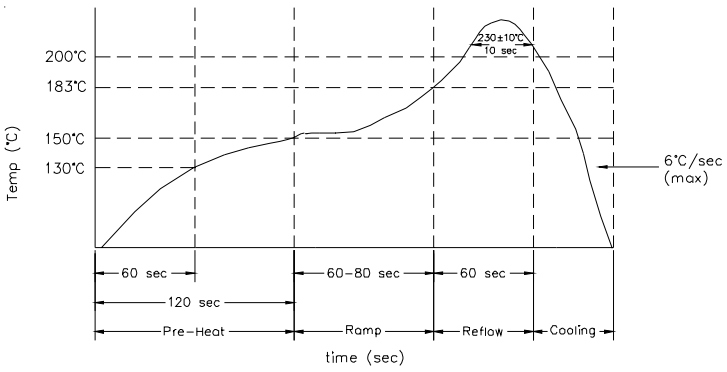
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

### Recommended NSMD Pad and Stencil Aperture



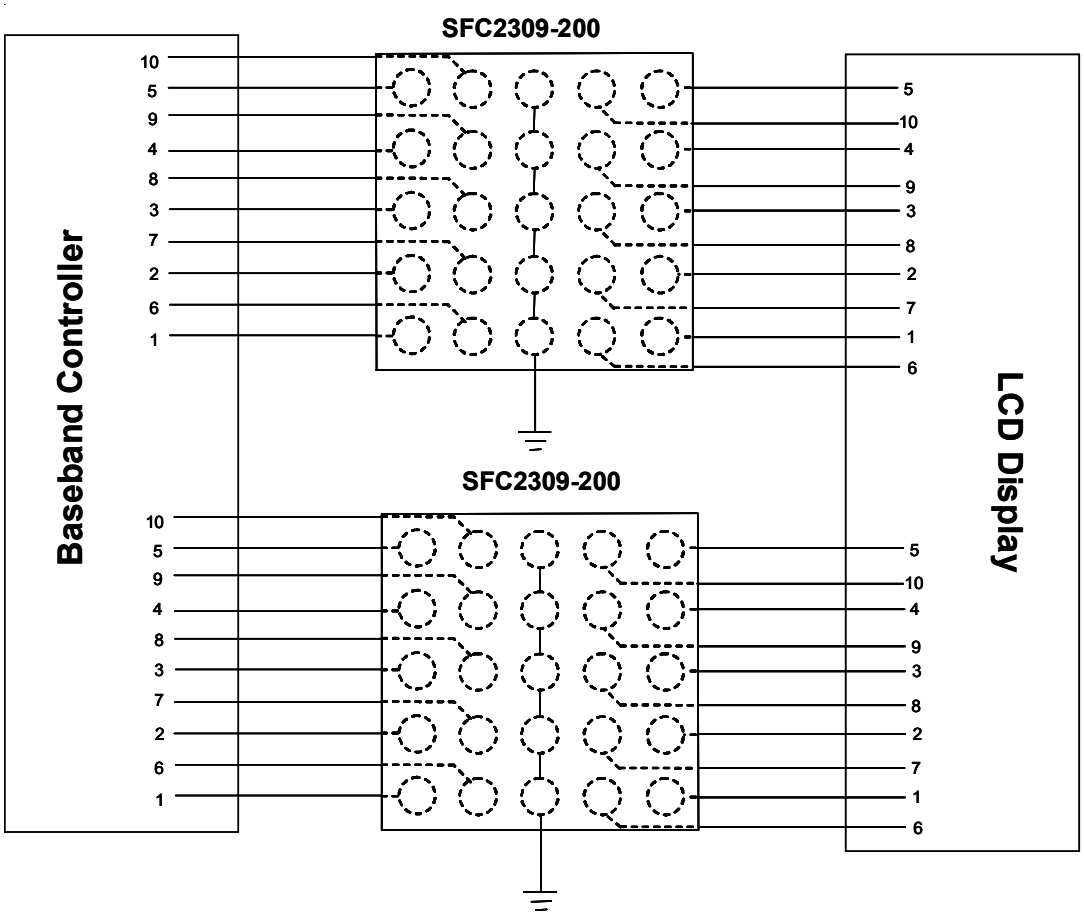

### Solder Reflow Profile




Typical solder reflow profile for OSP finish FR-4 bond.

| | |
|---|---|
| Pre-heat to 150°C | 120 sec max |
| Time to eutectic (183°C) | 60-80 sec |
| Time above eutectic | 50±10 sec |
| Peak reflow temp | 230±10°C |
| Time w/in 10°C of peak | 10 seconds |
| Ramp down rate | 6°C/sec max |

## Applications Information

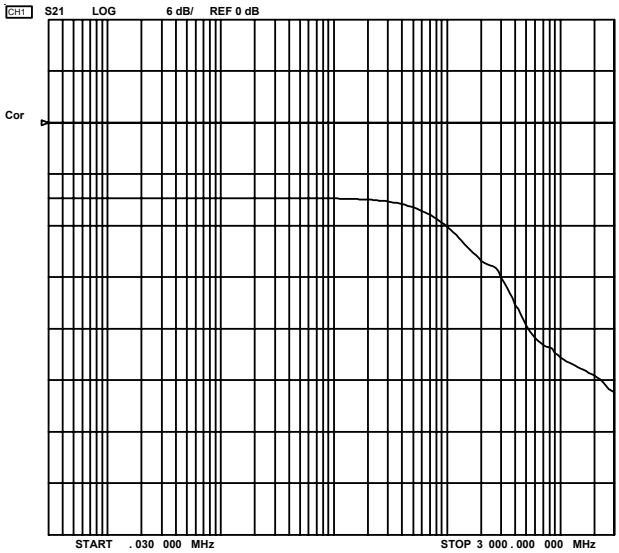



**Implementation Example**

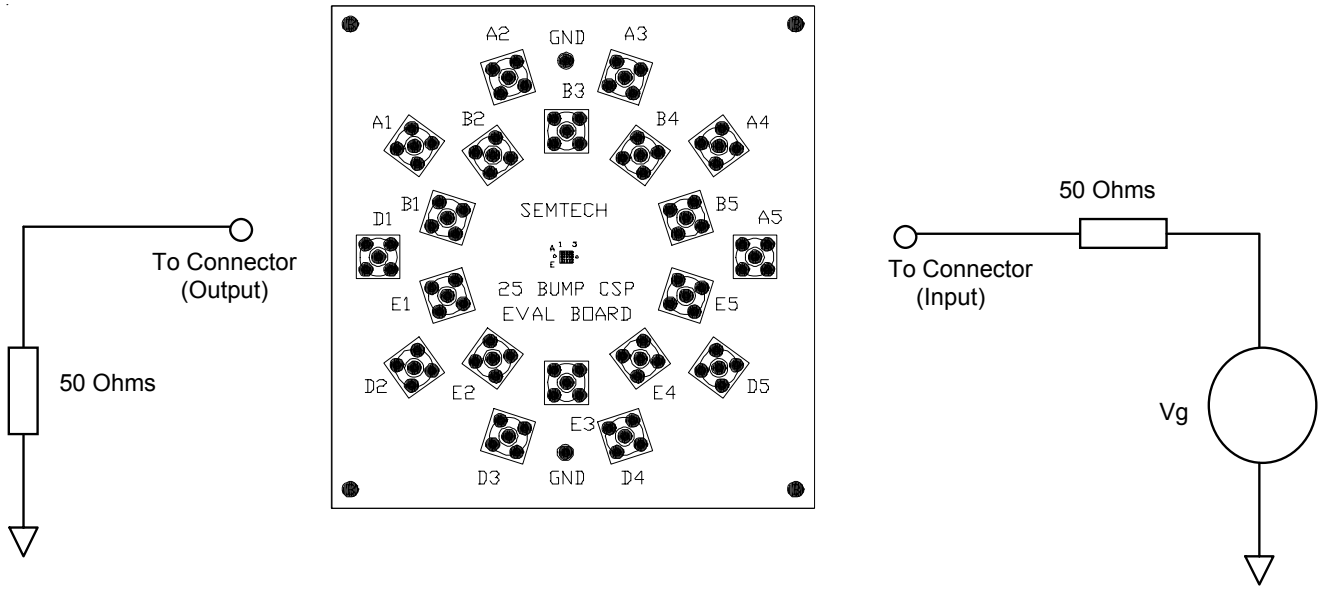
## Applications Information

### Insertion Loss

The insertion loss of the device is the ratio of the power delivered to the load with and without the filter in the circuit. This parameter is dependent upon the impedance of the source and the load. The standard impedance of test equipment that is used to measure filter frequency response is 50Ω. In order to obtain an accurate measurement of the filter performance, an evaluation board with 50Ω transmission lines are used. The test conditions for the *SFC2309-200* are shown below. The evaluation board contains SMA connectors at each of the circuits inputs and outputs. The connections are made with 50Ω traces. An HP 8753E network analyzer with an internal spectrum analyzer and tracking generator is used. This equipment has the capability to sweep the device from 3kHz to 3GHz. The analyzer's source ($R_S$) impedance is equal to the load ($R_L$) impedance which is equal to 50Ω.



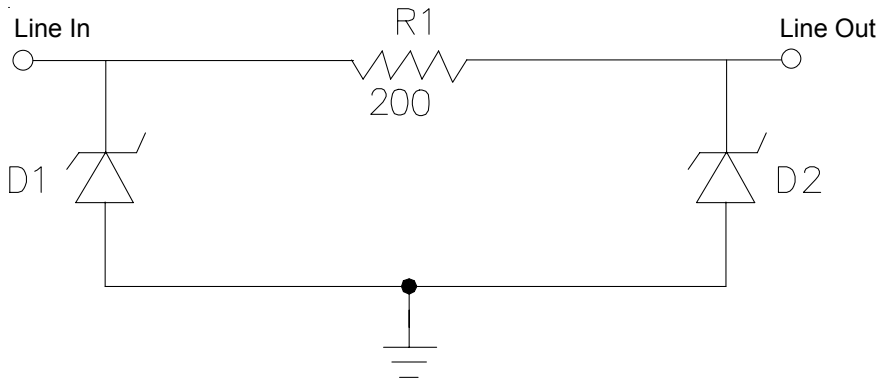

**Insertion Loss S21**




**Insertion Loss Measurement Conditions**

## Applications Information

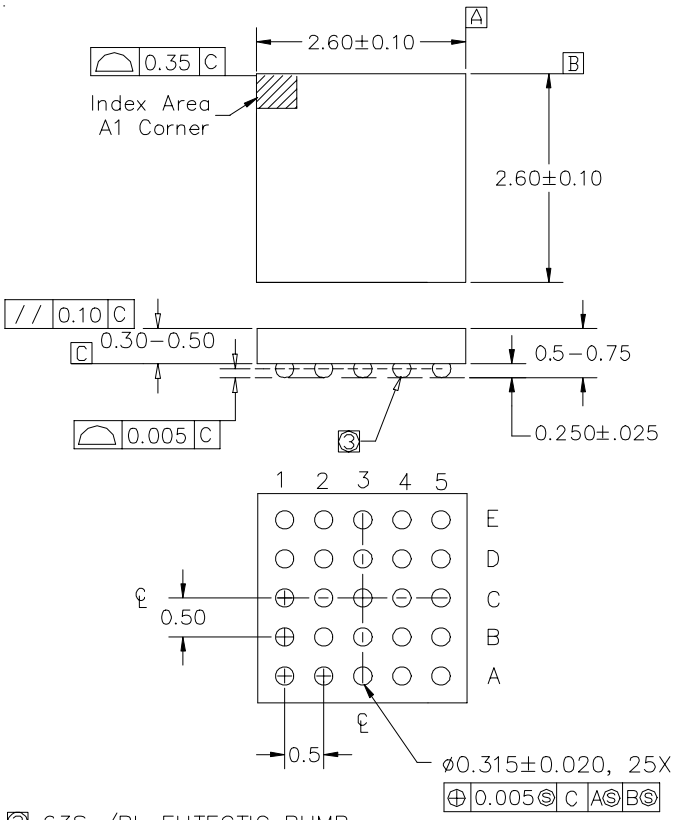
**SFC2309-200 Spice Model & Parameters**




**SFC2309-200 Spice Model**

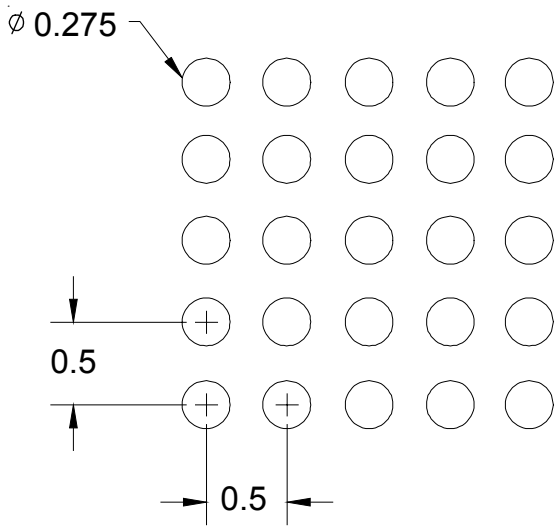
| SFC2309-200 Spice Parameters | | | |
|---|---|---|---|
| **Parameter** | **Unit** | **D1 (TVS)** | **D2 (TVS)** |
| IS | Amp | 1E-14 | 1E-14 |
| BV | Volt | 7.1 | 7.1 |
| VJ | Volt | 0.62 | 0.62 |
| RS | Ohm | 0.124 | 0.124 |
| IBV | Amp | 1E-3 | 1E-3 |
| CJO | Farad | 25E-12 | 25E-12 |
| TT | sec | 2.541E-9 | 2.541E-9 |
| M | -- | 0.108 | 0.108 |
| N | -- | 1.05 | 1.05 |
| EG | eV | 1.11 | 1.11 |

## Outline Drawing

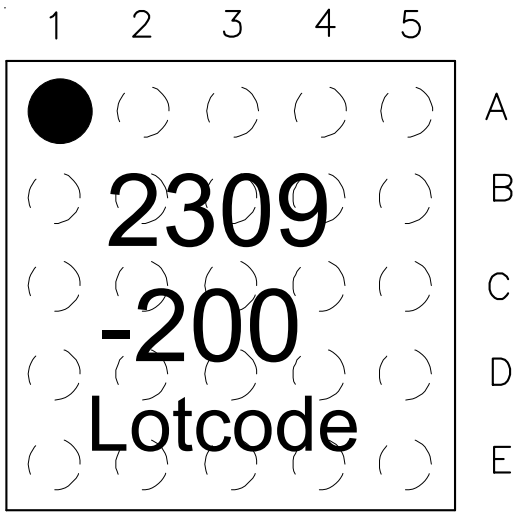



3 63Sn/Pb EUTECTIC BUMP.
2 REFERENCE JEDEC REGISTRATION MO–211, VARIATION BF.
1 CONTROLLING DIMENSION: MILLIMETERS.

## Land Pattern



## Marking



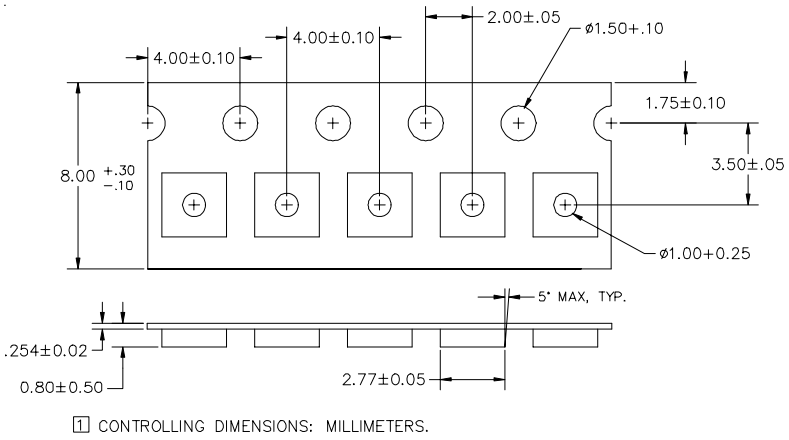

**Top View Showing Laser Mark**

## Ordering Information

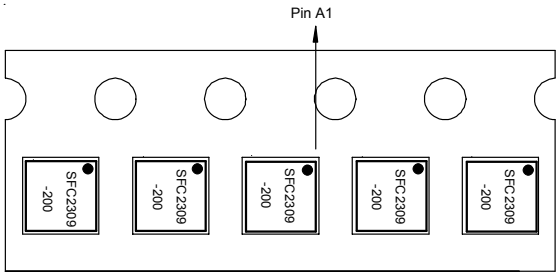
| Part Number | Series Resistor | Qty per Reel | Reel Size |
|---|---|---|---|
| SFC2309-200.TC | 200Ω | 3000 | 7 Inch |

Add “T” suffix for lead free bumps.
Ex: SFC2309-200.TCT

## Tape and Reel Specification




**Tape Specifications**




**Device Orientation in Tape**

## Contact Information

Semtech Corporation
Protection Products Division
200 Flynn Rd., Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804