

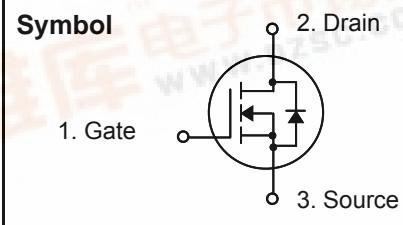


# SFD45N03L

## Logic N-Channel MOSFET

### Features

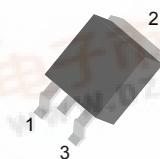
- Low  $R_{DS(on)}$  (0.018Ω) @  $V_{GS}=10V$
- Low Gate Charge (Typical 17.5nC)
- Low  $C_{RSS}$  (Typical 110pF)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Maximum Junction Temperature Range (150°C)



### General Description

This Power MOSFET is produced using SemiWell's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a low gate charge with superior switching performance, and rugged avalanche characteristics. This Power MOSFET is well suited for synchronous DC-DC Converters and Power Management in portable and battery operated products.

D-PACK (TO-252)



### Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$I_D$	Continuous Drain Current(@ $T_C = 25^\circ C$ )	37	A
	Continuous Drain Current(@ $T_C = 100^\circ C$ )	24	A
$I_{DM}$	Drain Current Pulsed (Note 1)	148	A
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	220	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
$P_D$	Total Power Dissipation(@ $T_A = 25^\circ C$ )	2.5	W
	Total Power Dissipation(@ $T_C = 25^\circ C$ )	45	W
	Derating Factor above 25 °C	0.36	W/°C
$T_{STG}, T_J$	Operating Junction Temperature & Storage Temperature	- 55 ~ 150	°C
$T_L$	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	°C

### Thermal Characteristics

Symbol	Parameter	Value			Units
		Min.	Typ.	Max.	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	-	2.78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	-	-	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	110	°C/W

\* When mounted on the minimum pad size recommended (PCB Mount)

# SFD45N03L

---

## Electrical Characteristics ( $T_C = 25^\circ\text{C}$ unless otherwise noted )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$	-	0.03	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 30V, V_{GS} = 0V$	-	-	1	$\mu\text{A}$
		$V_{DS} = 24V, T_C = 125^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	Gate-Source Leakage, Forward	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
	Gate-Source Leakage, Reverse	$V_{GS} = -20V, V_{DS} = 0V$	-	-	-100	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	-	3.0	V
$R_{DS(\text{ON})}$	Static Drain-Source On-state Resistance	$V_{GS} = 10V, I_D = 18.5\text{A}$	-	0.013	0.018	$\Omega$
		$V_{GS} = 5V, I_D = 18.5\text{A}$	-	0.017	0.025	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{MHz}$	-	880	1140	pF
$C_{oss}$	Output Capacitance		-	370	480	
$C_{rss}$	Reverse Transfer Capacitance		-	110	140	
<b>Dynamic Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15V, I_D = 22.5\text{A}, R_G = 50\Omega$ ※ see fig. 13. (Note 4, 5)	-	20	50	ns
$t_r$	Rise Time		-	60	130	
$t_{d(off)}$	Turn-off Delay Time		-	45	100	
$t_f$	Fall Time		-	60	130	
$Q_g$	Total Gate Charge	$V_{DS} = 24V, V_{GS} = 5V, I_D = 45\text{A}$ ※ see fig. 12. (Note 4, 5)	-	17.5	23	nC
$Q_{gs}$	Gate-Source Charge		-	5.0	-	
$Q_{gd}$	Gate-Drain Charge(Miller Charge)		-	7.5	-	

## Source-Drain Diode Ratings and Characteristics

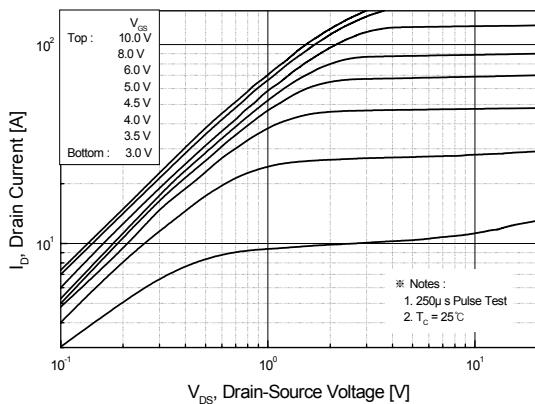
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
$I_S$	Continuous Source Current	Integral Reverse p-n Junction Diode in the MOSFET	-	-	37	A
	Pulsed Source Current		-	-	148	
$V_{SD}$	Diode Forward Voltage	$I_S = 37\text{A}, V_{GS} = 0V$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$I_S = 45\text{A}, V_{GS} = 0V, dI_F/dt = 100\text{A/us}$	-	35	-	ns
	Reverse Recovery Charge		-	30	-	nC

※ NOTES

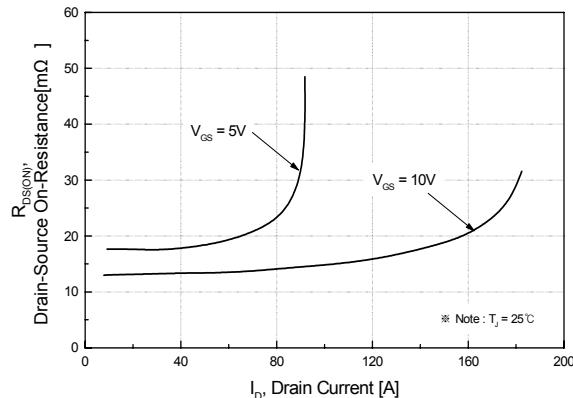
1. Repeatability rating : pulse width limited by junction temperature
2.  $L = 160\mu\text{H}, I_{AS} = 37\text{A}, V_{DD} = 15V, R_G = 0\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $ISD \leq 45\text{A}, di/dt \leq 300\text{A/us}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse Width  $\leq 300\text{us}$ , Duty Cycle  $\leq 2\%$
5. Essentially independent of operating temperature.

# SFD45N03L

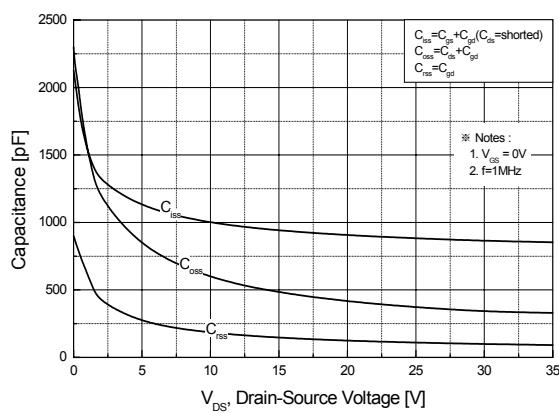
**Fig 1. On-State Characteristics**



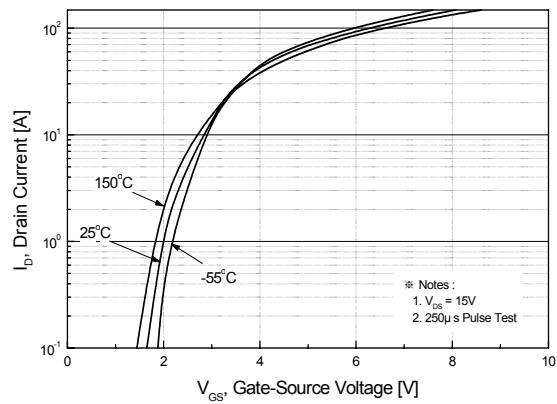
**Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage**



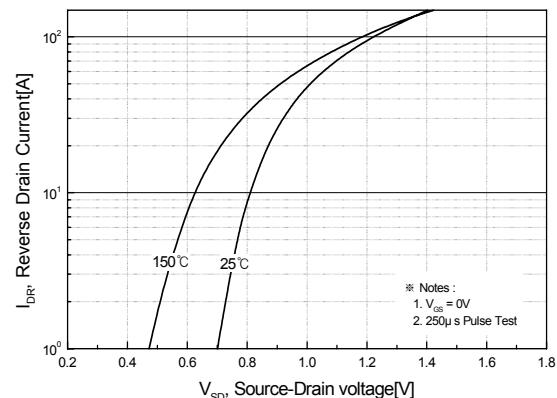
**Fig 5. Capacitance Characteristics**



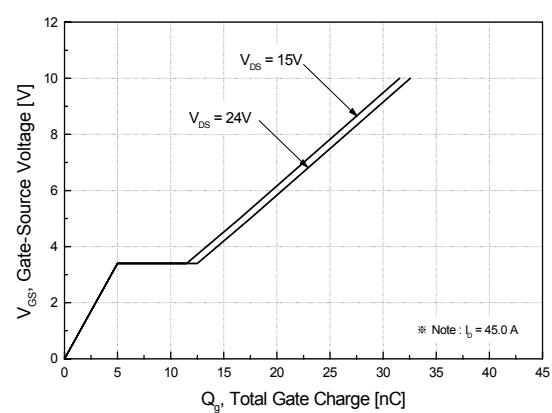
**Fig 2. Transfer Characteristics**



**Fig 4. On State Current vs. Allowable Case Temperature**

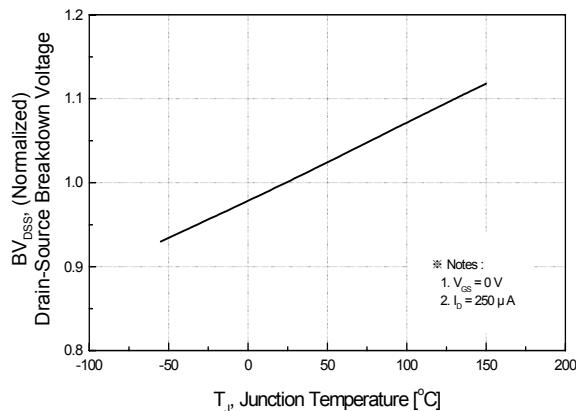


**Fig 6. Gate Charge Characteristics**

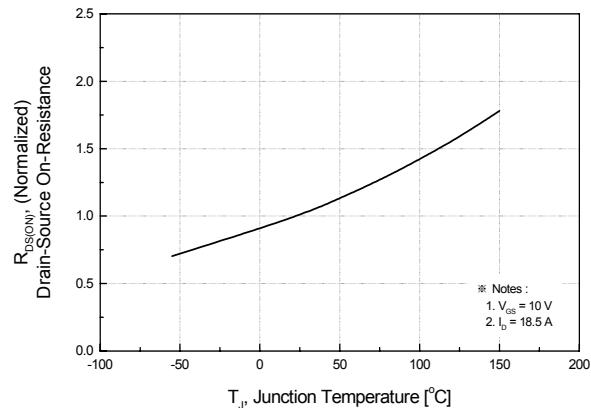


# SFD45N03L

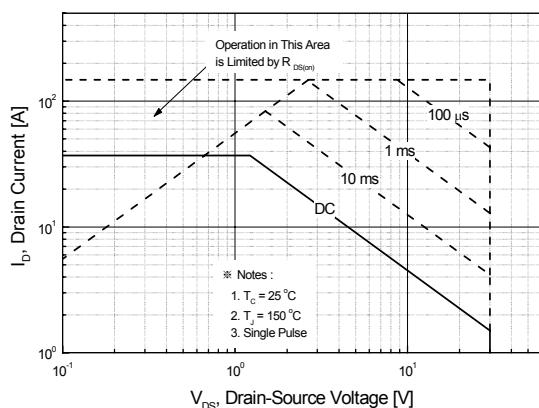
**Fig 7. Breakdown Voltage Variation vs. Junction Temperature**



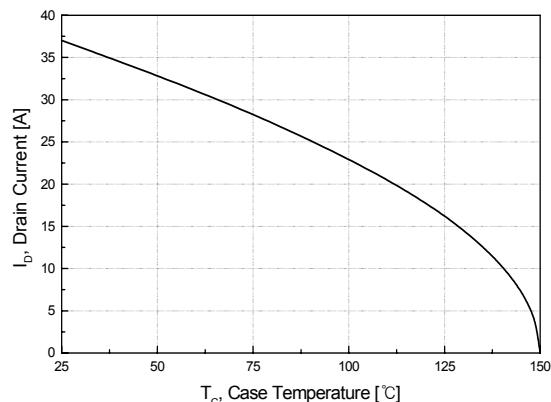
**Fig 8. On-Resistance Variation vs. Junction Temperature**



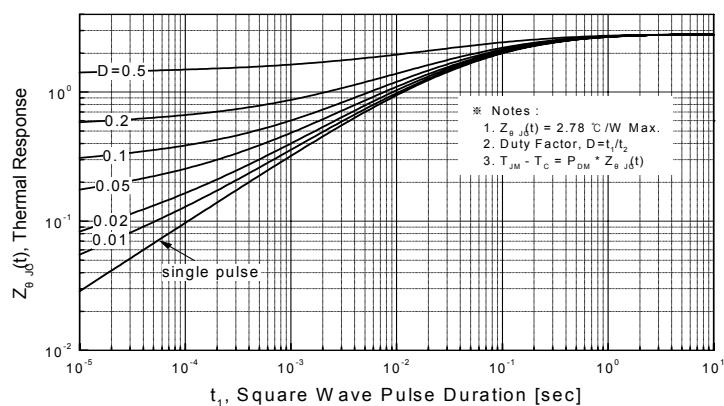
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Maximum Drain Current vs. Case Temperature**



**Fig 11. Transient Thermal Response Curve**



# SFD45N03L

Fig. 12. Gate Charge Test Circuit & Waveforms

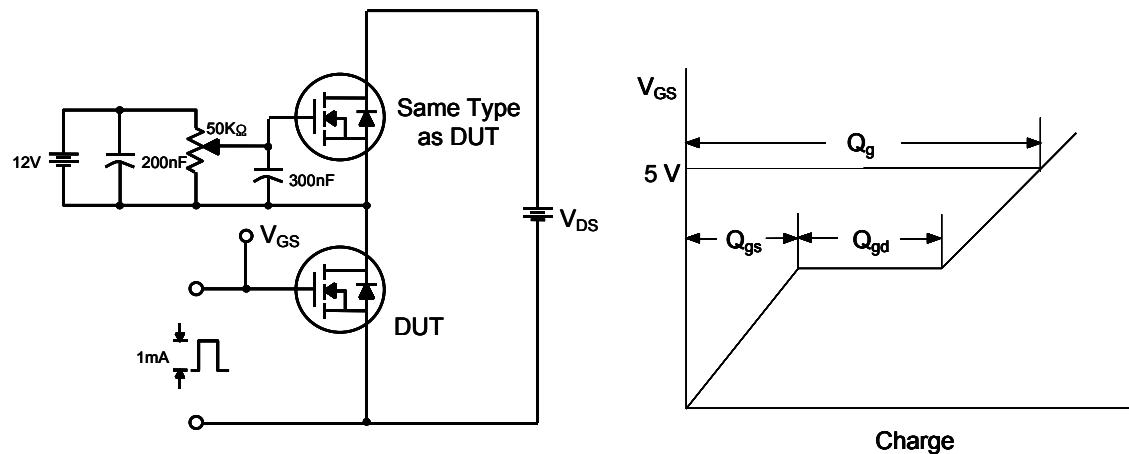


Fig 13. Switching Time Test Circuit & Waveforms

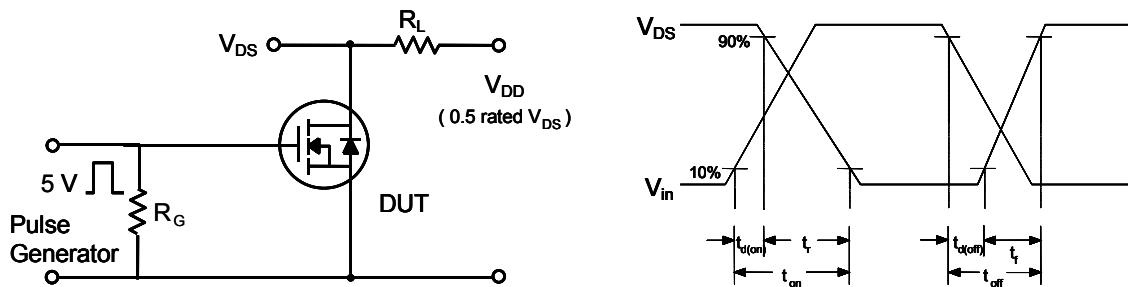
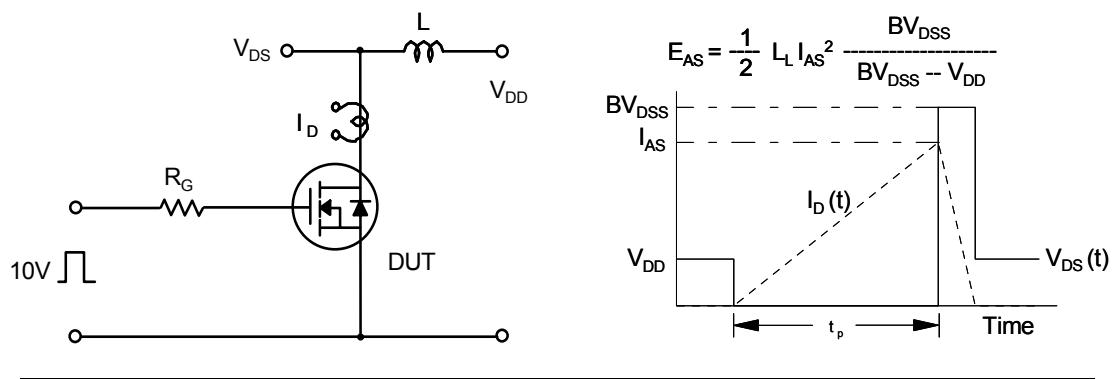


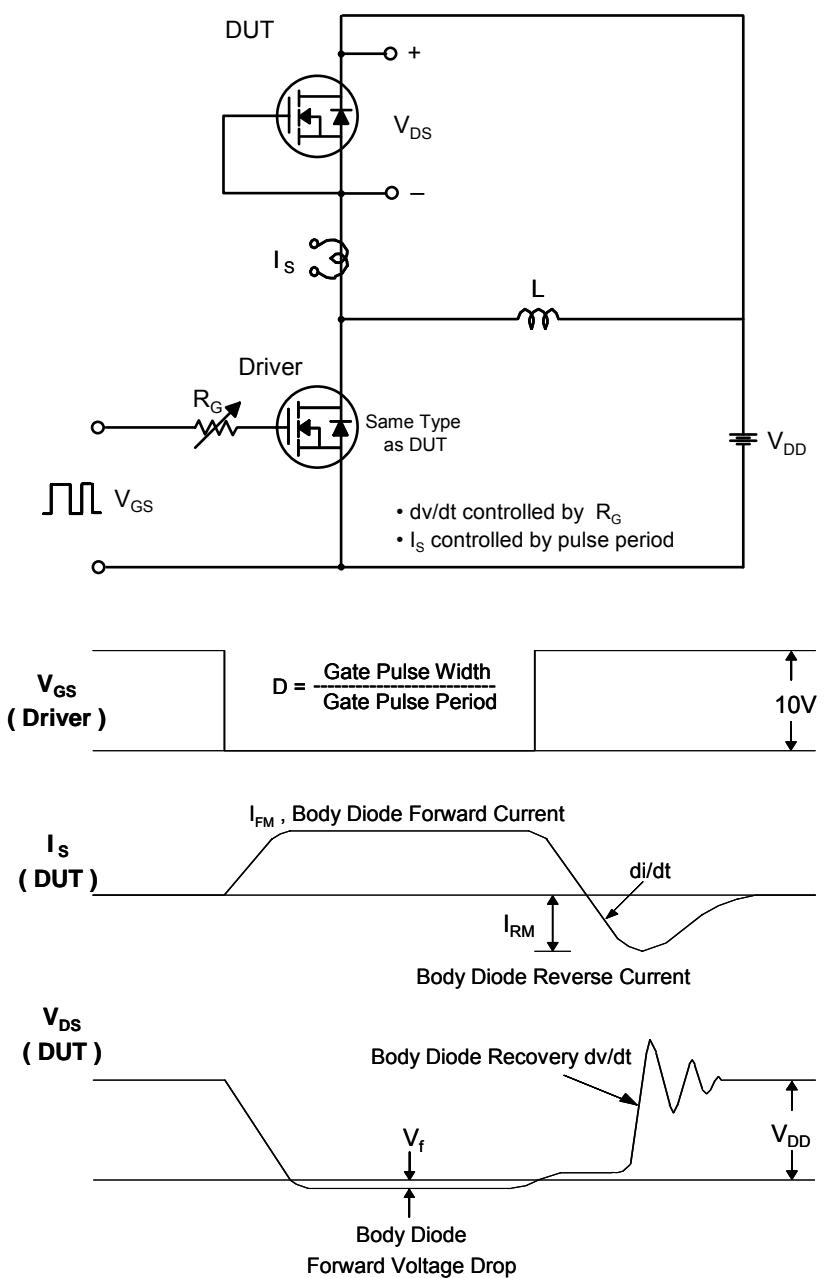
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



# SFD45N03L

---

Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



# SFD45N03L

## TO-252(D-PAK) Package Dimension

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	6.48	6.604	6.73	0.255	0.26	0.265
B	5.0	5.08	5.21	0.197	0.2	0.205
C	7.42	7.8	8.18	0.292	0.307	0.322
D	2.184	2.286	2.388	0.086	0.09	0.094
E	0.762	0.813	0.864	0.03	0.032	0.034
F	1.016	1.067	1.118	0.04	0.042	0.044
G		2.286			0.09	
H		2.286			0.09	
I	0.534	0.61	0.686	0.021	0.024	0.027
J	1.016	1.067	1.118	0.04	0.042	0.044
K		0.508			0.02	
L		0.762			0.03	
$\phi$		1.57			0.06	

