ANALOG DEVICES

High Resolution 14-Bit Sample and Hold Amplifier

SHA1144

FEATURES

- ±10V min Input/Output Range
- 50ns Aperture Delay
- 0.5ns Aperture Jitter
- 6μs Settling Time
- ±0.001% Max Gain Linearity Error
- Complete with Input Buffer

APPLICATIONS

- Track and Hold
- Peak Measurement Systems
- Data Acquisition Systems
- Simultaneous Sample-and-Hold

GENERAL DESCRIPTION

The SHA1144 is a fast sample-hold amplifier module with accuracy and dynamic performance appropriate for applications with fast 14-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" is appropriate to allow accurate conversion by 14-bit A/D converters having conversion times of up to 150μs.

DYNAMIC PERFORMANCE

The SHA1144 was designed to be compatible with fast 14-bit A/D converters such as the Analog Devices' ADC1130 and ADC1131 series, which convert 14 bits in 25μs and 12μs, respectively. Maximum acquisition time of 8μs for the SHA1144 permits high sampling rates for 14-bit conversions. The SHA1144 is guaranteed to have a maximum gain nonlinearity of ±0.001% of full scale to insure 1/2LSB accuracy in 14-bit systems. When in the "hold" mode, the droop rate is 1μV/μs, so the SHA1144 will hold an input signal to ±0.003% of full scale (20V p-p) for over 600μs.

PRINCIPLE OF OPERATION

The SHA1144 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch. It differs from typical sample-and-hold modules in one important respect; application versatility. The user completes the SHA1144 feedback circuit external to the module. Therefore, the module may be used in inverting or noninverting configurations and can easily be arranged to provide circuit gain of more than unity to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

A block diagram of the SHA1144 is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "hold" capacitor. The output amplifier isolates the "hold" capacitor and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA1144 can be connected as a follower with unity gain or potentiometric gain, as well as inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data listed in the specification table is based on this operating mode.

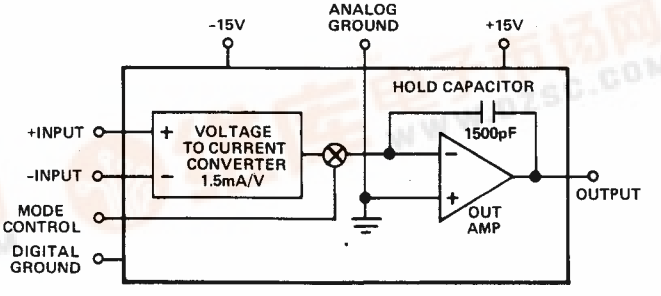


Figure 1. Block Diagram – SHA1144

SPECIFICATIONS (typical @ +25°C, gain = +1V/V and nominal supply voltages unless otherwise noted)

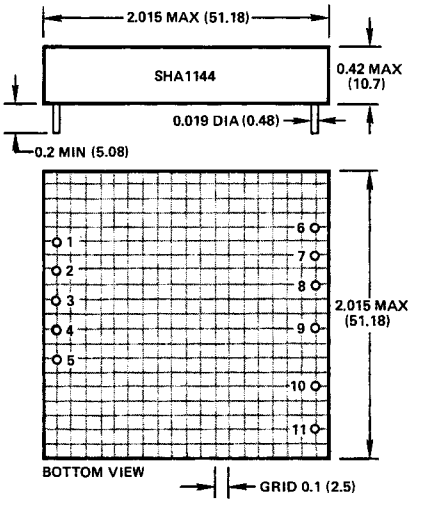
MODEL		SHA1144
ACCURACY		
Gain		+1V/V
Gain Error		±0.005%
Gain Nonlinearity		±0.0005% (±0.001% max)
Gain Temperature Coefficient (0 to +70°C)		±1ppm/°C (±2ppm/°C max)
INPUT CHARACTERISTICS		
Input Voltage Range		±10V
Impedance		$10^{11}\ \Omega \parallel 10pF$
Bias Current		0.5nA max
Initial Offset Voltage		Adjustable to Zero
Offset vs. Temperature (0 to +70°C)		±30μV/°C max
OUTPUT CHARACTERISTICS		
Voltage		±10V min
Current		±20mA min
Resistance		<1Ω
Capacitive load		350pF
Noise @ 100kHz Bandwidth		70μV p-p
@ 1MHz Bandwidth		175μV p-p
SAMPLE MODE DYNAMICS		
Frequency Response		
Small Signal (-3dB)		1MHz
Full Power		50kHz
Slew Rate		3V/μs
SAMPLE-TO-HOLD SWITCHING		
Aperture Delay Time		50ns
Aperture Uncertainty		0.5ns
Offset Step		1mV
Offset Nonlinearity		160μV
Switching Transient		
Amplitude		50mV
Settling Time to ±0.003%		1μs
HOLD MODE DYNAMICS		
Droop Rate		1μV/μs (2μV/μs max)
Variation with Temperature		double every +10°C
Feedthrough (for 20V p-p Input @ 1kHz)		-80dB
HOLD-TO-SAMPLE SWITCHING		
Acquisition Time to ±0.003%	(20V Step)	6μs (8μs max)
	(10V Step)	5μs
±0.01%	(20V Step)	5μs
	(10V Step)	4μs
DIGITAL INPUT		
Sample Mode (Logic "1")		+2V<Logic "1"<+5.5V @ 15nA max
Hold Mode (Logic "0")		0V<Logic "0"<+0.8V @ 5μA (20μA max)
POWER REQUIRED[1]		+15V ±3% @ 60mA
		-15V ±3% @ 45mA
TEMPERATURE RANGE		
Operating		0 to +70°C
Storage		-55°C to +85°C

[1] Recommended Power Supply ADI Model 902-2, ±15V @ ±100mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

1. TRIM
2. TRIM
3. +INPUT
4. -INPUT
5. TRIM
6. +15V
7. ANALOG GROUND
8. -15V
9. ANALOG OUTPUT
10. MODE CONTROL
11. DIGITAL GROUND

OFFSET ZERO ADJUST (OPTIONAL)

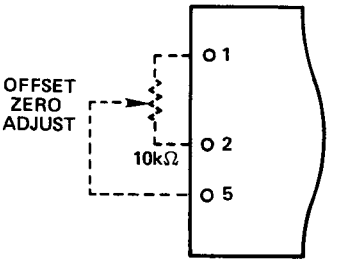


Figure 2 shows feedback connections to the SHA1144 for the unity gain follower mode. Output (pin 9) is connected to input (pin 4). Input signal is applied to pin 3.

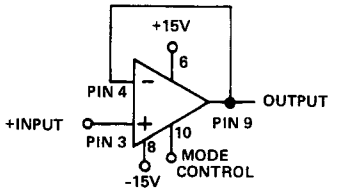


Figure 2. Unity Gain Follower

Figure 3 shows feedback connections for noninverting operation with potentiometric gain. When the indicated values are installed, gain will be +5. As in all operational amplifiers, gain-bandwidth product is a constant for a given sample-and-hold. Effective 3dB bandwidth will be inversely proportional to gain.

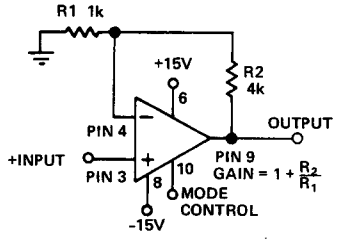


Figure 3. Noninverting Operation

By using conventional operational amplifier feedback connections, the SHA1144 can be connected for use as an inverter, with various gains (as determined by the R_F/R_1 ratio), or as a differential amplifier.

DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fast 14-bit models available cannot tolerate input signal frequencies of greater than a few Hz. For this reason, sample-and-hold amplifiers like the SHA1144 are connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1144 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal frequency. The SHA1144, with a typical aperture delay time of 50ns and an uncertainty of 0.5ns, will change from the sample mode to the hold mode 50 to 50.5ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 50ns early, then switching will actually occur within 0.5ns of the desired time as shown below.

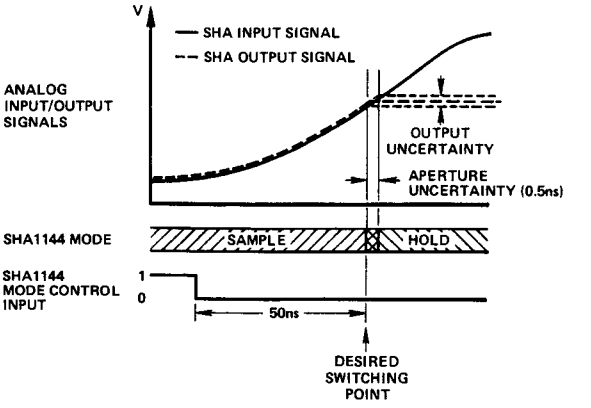


Figure 4. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 0.5ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{max} = \left(\frac{\Delta E}{E_{FS}}\right)\left(\frac{1}{2\pi\Delta t}\right) \cong 3.18 \times 10^8 \left(\frac{\Delta E}{E_{FS}}\right)$$

where: ΔE = the allowable voltage uncertainty

E_{FS} = the sinewave magnitude

For a system containing a SHA1144 and a 14-bit A/D with ±10V input signals and an allowable input uncertainty of ±1/2LSB (±620μV), the maximum allowable signal frequency will be 19.7kHz.

POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown shown below in Figure 5.

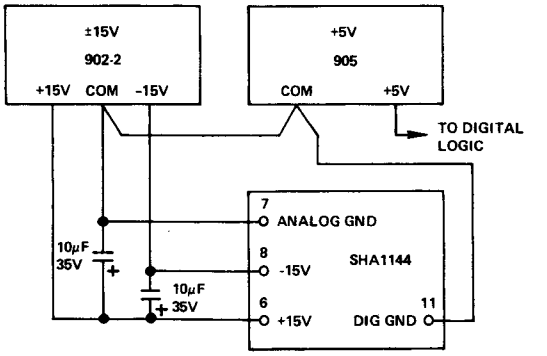


Figure 5. Power Supply and Grounding Connections

The ±15V power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.

OPERATION WITH AN A/D CONVERTER

Figure 6 below shows the appropriate connections between the SHA1144 and a successive approximation A/D converter in block diagram form.

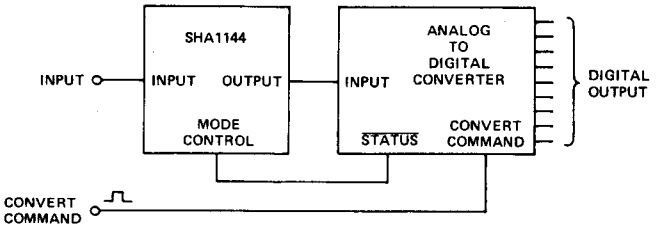


Figure 6. SHA1144 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 7.

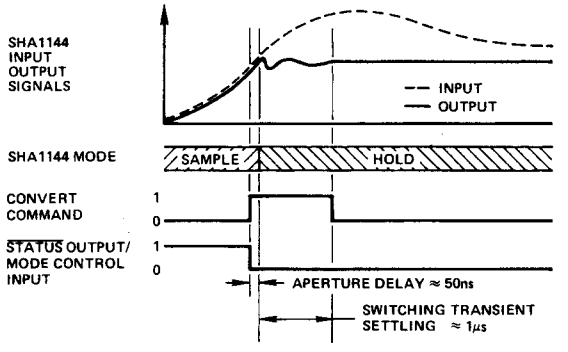


Figure 7. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's STATUS output to go to Logic "0" which in turn switches the SHA1144 from sample to hold. As discussed previously, the typical SHA1144 actually changes modes 50 to 50.5ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.003% of the final value in approximately 1μs. Once the transient has settled, the convert command input is returned to Logic "0" and the conversion proceeds. As shown in Figure 8, the STATUS signal returns to Logic "1" and the SHA1144 returns to the sample mode at the end of conversion. Within 6μs, it will have acquired the input signal to 0.003% accuracy and a new conversion cycle may be started.

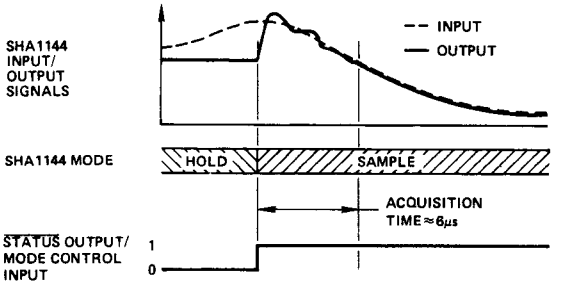


Figure 8. A/D and SHA Timing at End of Conversion

OPERATION WITH AN A/D AND MULTIPLEXER

The subsystem of Figure 9 may also be connected to a multiplexer like the Harris HI508A as shown below.

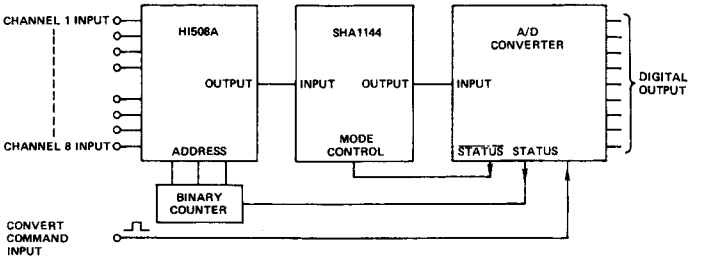


Figure 9. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the STATUS output to Logic "0" thereby switching the SHA1144 to "hold"; the corresponding change to Logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1144's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the multiplexer actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 10.

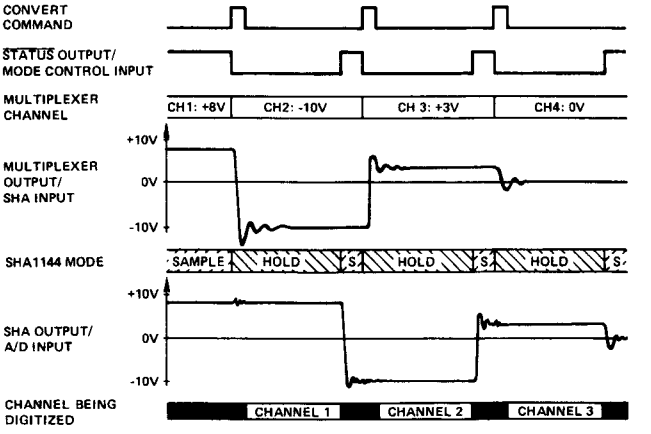


Figure 10. A/D, SHA, and MPX Timing

This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of the multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1144. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". Large multiplexer switching transients occuring during A/D conversion may introduce an error.

Mounting Card AC1580

GENERAL DESCRIPTION

High resolution, high speed data acquisition demands that considerable thought be given to wiring connections, even when simply evaluating the unit in a temporary laboratory bench set-up. To assist with such evaluations, an AC1580 is available. This 4 1/2" X 6" printed circuit card has sockets that allow a SHA1144 and ADC1130 or ADC1131 to be plugged directly onto it. It also has provisions for two optional Harris HI508A multiplexers. This card includes gain and offset adjustment potentiometers and power supply bypass capacitors. It mates with a Cinch 251-22-30-160 (or equivalent) edge connector (P1) and Cinch 251-06-30-160 (or equivalent) edge connector (P2) which are supplied with every card.

To use the AC1580, program as shown in the wiring chart of Table 1, by installing the appropriate jumpers. An outline drawing and schematic are provided for reference.

Calibration Procedure

Set up the SHA1144 for the desired gain per the wiring chart of Table 1. Short W9 which drives the SHA MODE CONTROL with the STATUS of the ADC. Calibrate offset and gain in the manner described below. When calibration is completed W9 may be removed and the SHA MODE CONTROL may be driven in accordance with the option chart.

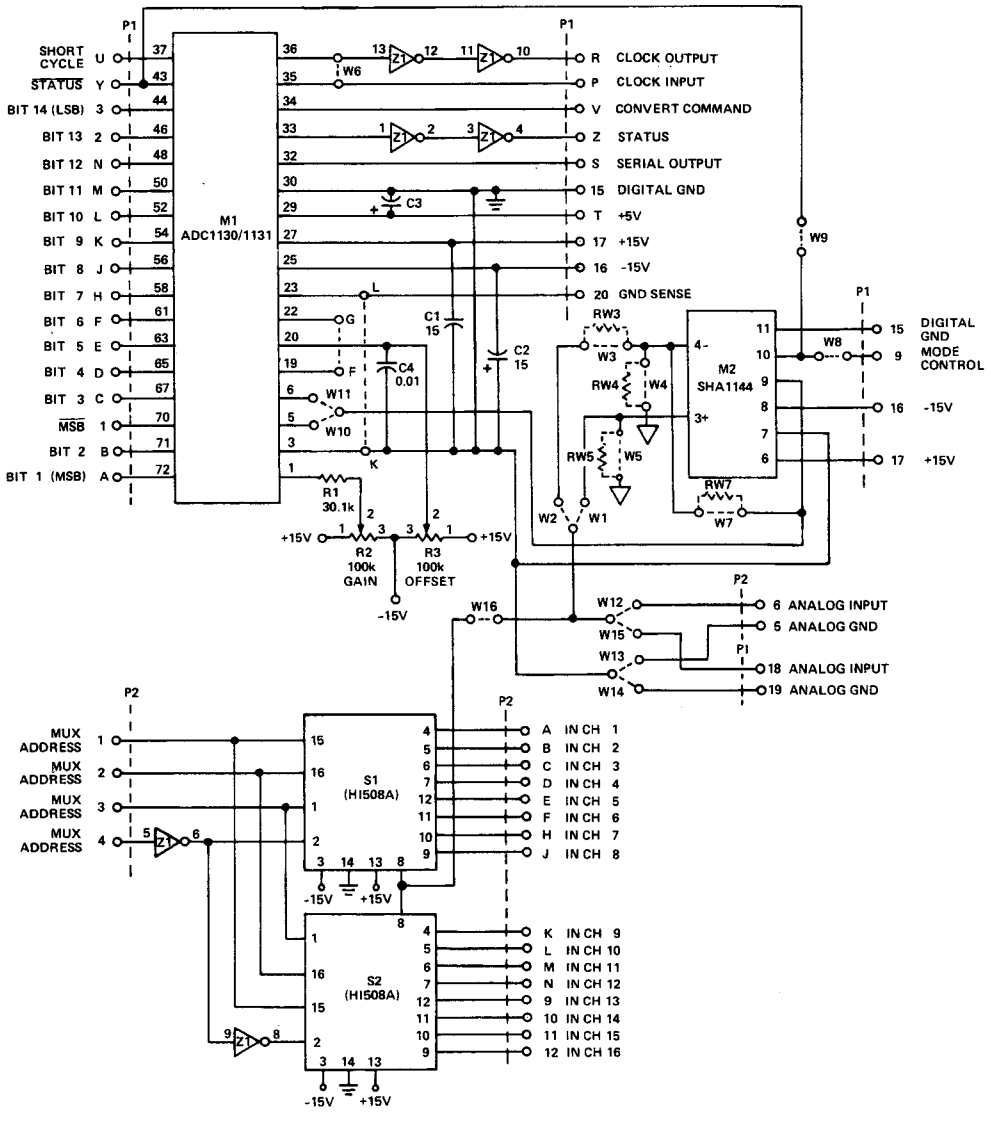
Offset Calibration

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00. . . . . 0 to 00. . . . . 1.

For the +5V bipolar range, set the input voltage precisely to −4.9997V; for ±10V units set it to −9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . . 0 to 00 . . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . . 0 to 100 . . . . . 1.

Gain Calibration

Set the input voltage precisely to +9.9991V for 0 to +10V units, +4.9991V for ±5V units or +9.9982V for ±10V units. Note that these values are 1 1/2LSB's less than the nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . . 0 to 11 . . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

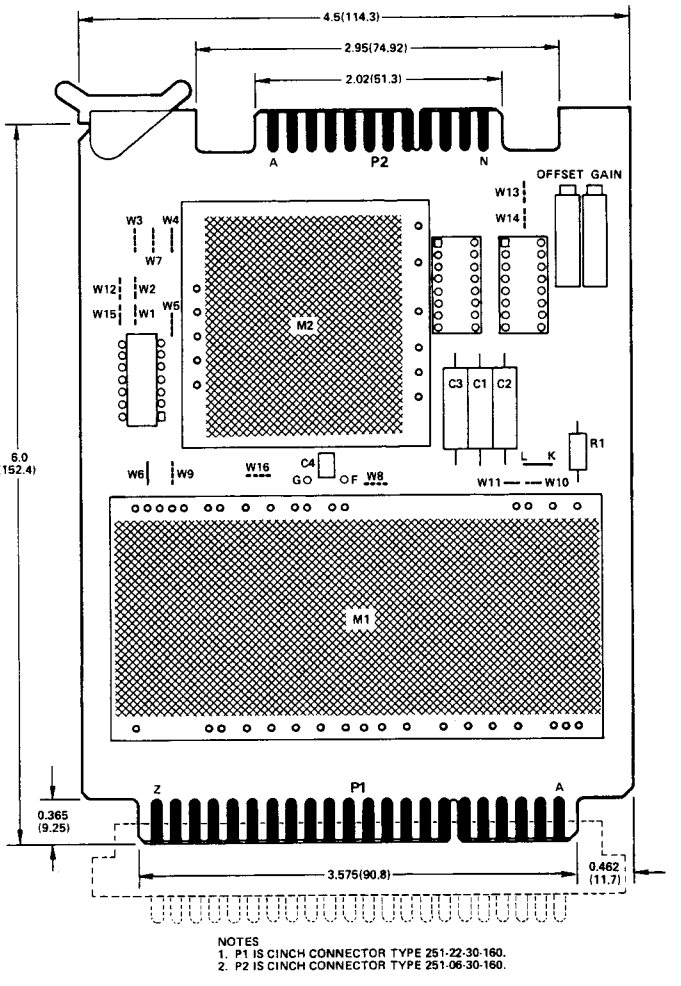


Figure 12. AC1580 Mounting Board

A to D Converter Options

Range	Jumpers
0V to 10V	Jumper W11
±5V	Jumper W11 and Jumper G to F on Board
±10V	Jumper W10 and Jumper G to F on Board

SHA Options

SHA Unity Gain (+1)	Jumper W1 and Jumper W7
SHA with Gain[1,3]	Jumper W1 and Install RW4 and RW7 in W4 and W7 Locations[3]
SHA as an Inverter[2,3]	Jumper W2 and Jumper W5 and Install RW3 and RW7 in W3 and W7 Locations[3]

SHA Mode Control

Internal (Driven from Status of the ADC)	Jumper W9
External (Apply External Signal to Pin 9 of Connector P1)	Jumper W8

Multiplexer Option

When Using Multiplexers — Jumper W16

INPUT OPTIONS

Inputs	From Connector P1	From Connector P2
Analog Input	Jumper W15	Jumper W12
Analog Ground	Jumper W14	Jumper W13

NOTES

[1] $G = 1 + \frac{RW7}{RW4}$ [2] $G = -\frac{RW7}{RW3}$

[3] See Figure 11 for appropriate gain setting resistor locations (RW3, RW4, RW7)

Table 1. Option Chart

"ON" Channel	1	2	3	4
1	L	L	L	L
2	L	L	H	L
3	L	H	L	L
4	L	H	H	L
5	H	L	L	L
6	H	L	H	L
7	H	H	L	L
8	H	H	H	L
9	L	L	L	H
10	L	L	H	H
11	L	H	L	H
12	L	H	H	H
13	H	L	L	H
14	H	L	H	H
15	H	H	L	H
16	H	H	H	H

L = TTL Logic "0" (0V ≤ "0" ≤ +0.8V)

H = TTL Logic "1" (+2V ≤ "1" ≤ +5.5V)

Table 2. Multiplexer Address