



查询SI1551DL供应商

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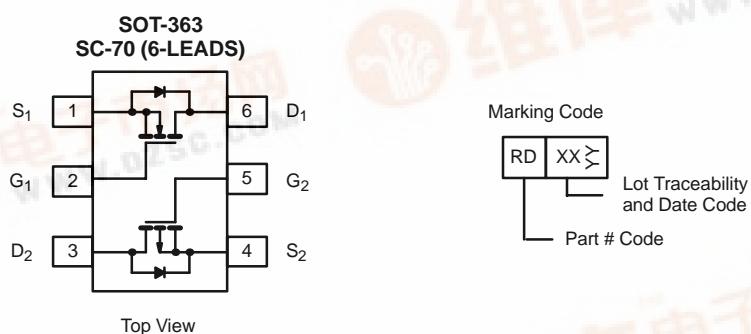
Si1551DL

Vishay Siliconix

Complementary 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	1.9 @ V _{GS} = 4.5 V	0.30
		3.7 @ V _{GS} = 2.7 V	0.22
		4.2 @ V _{GS} = 2.5 V	0.21
P-Channel	-20	0.995 @ V _{GS} = -4.5 V	-0.44
		1.600 @ V _{GS} = -2.7 V	-0.34
		1.800 @ V _{GS} = -2.5 V	-0.32

TrenchFET®
Power MOSFETs
2.5-V Rated



ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	N-Channel		P-Channel		Unit
			5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage		V _{DS}		20		-20	V
Gate-Source Voltage		V _{GS}			±12		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	0.30	0.29	-0.44	-0.41	A
	T _A = 85°C		0.22	0.21	-0.31	-0.30	
Pulsed Drain Current		I _{DM}		0.6		-1.0	
Continuous Source Current (Diode Conduction) ^a		I _S	0.25	0.23	-0.25	-0.23	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	0.30	0.27	0.30	0.27	W
	T _A = 85°C		0.16	0.14	0.16	0.14	
Operating Junction and Storage Temperature Range		T _J , T _{stg}			-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 5 sec	R _{thJA}	360	415	°C/W
	Steady State		400	460	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	300	350	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.



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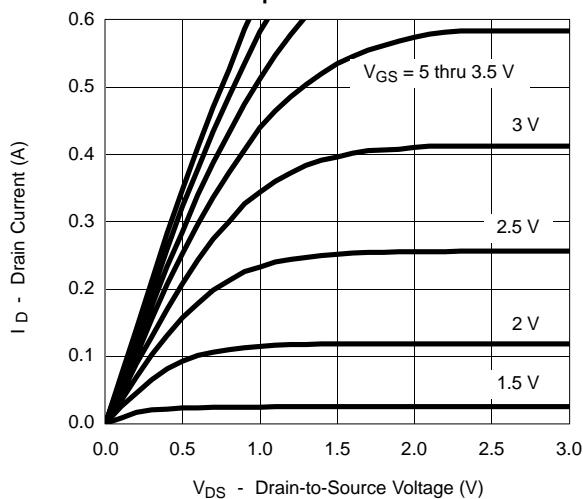
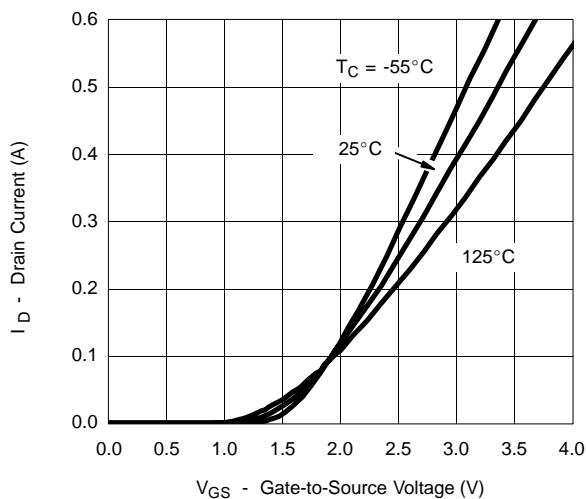
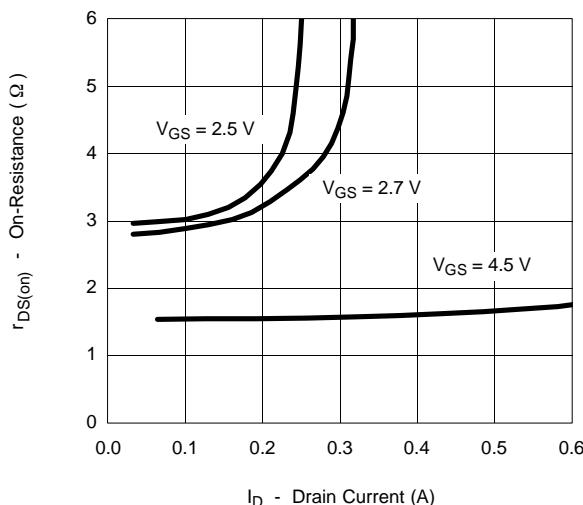
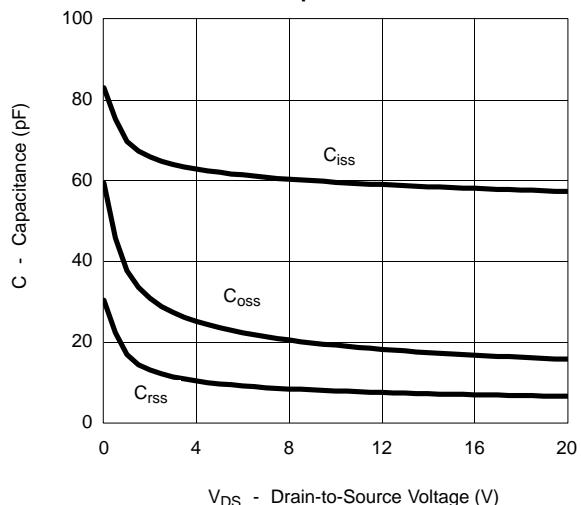
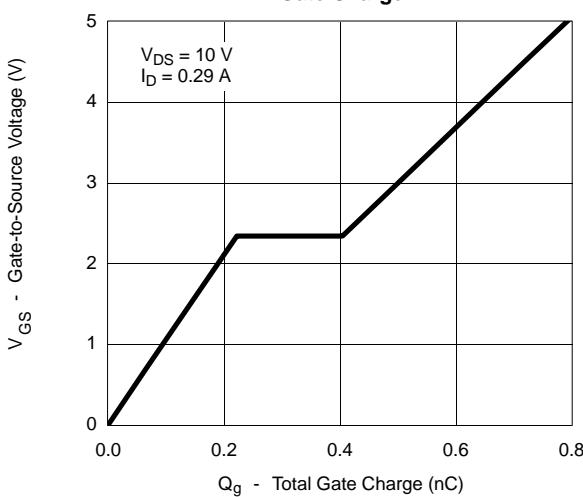
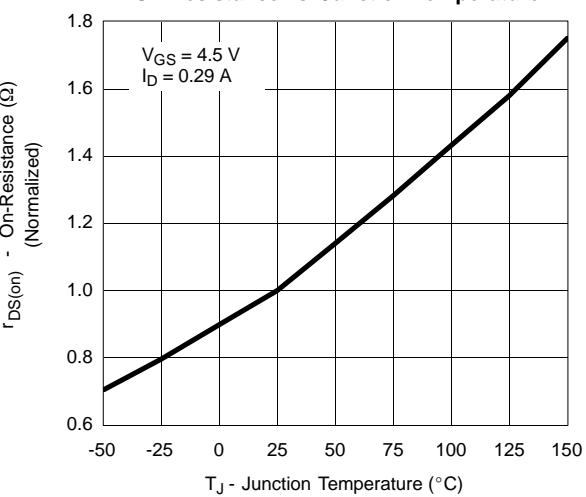


SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	0.6		
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-0.6		V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	N-Ch P-Ch		± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch		1	
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch		-1	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$	N-Ch		5	
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$	P-Ch		-5	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	0.6		A
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	-1.0		
Drain-Source On-State Resistance ^a	$r_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}, I_D = 0.29 \text{ A}$	N-Ch		1.55	1.9
		$V_{GS} = -4.5 \text{ V}, I_D = -0.41 \text{ A}$	P-Ch		0.850	0.995
		$V_{GS} = 2.7 \text{ V}, I_D = 0.1 \text{ A}$	N-Ch		2.8	3.7
		$V_{GS} = -2.7 \text{ V}, I_D = -0.25 \text{ A}$	P-Ch		1.23	1.600
		$V_{GS} = 2.5 \text{ V}, I_D = 0.1 \text{ A}$	N-Ch		3.0	4.2
		$V_{GS} = -2.5 \text{ V}, I_D = -0.25 \text{ A}$	P-Ch		1.4	1.800
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 0.29 \text{ A}$	N-Ch		0.3	
		$V_{DS} = -10 \text{ V}, I_D = -0.41 \text{ A}$	P-Ch		0.8	S
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.23 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch		0.8	1.2
		$I_S = -0.23 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch		-0.8	-1.2
Dynamic^b						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 0.29 \text{ A}$ P-Channel $V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -0.41 \text{ A}$	N-Ch		0.72	1.5
Gate-Source Charge	Q_{gs}		P-Ch		0.52	1.8
Gate-Drain Charge	Q_{gd}		N-Ch		0.22	
Gate-Drain Charge	Q_{gd}		P-Ch		0.11	
Turn-On Delay Time	$t_{d(\text{on})}$	N-Channel $V_{DD} = 10 \text{ V}, R_L = 20 \Omega$ $I_D \approx 0.5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$ P-Channel $V_{DD} = -10 \text{ V}, R_L = 20 \Omega$ $I_D \approx -0.5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$	N-Ch		23	40
Rise Time	t_r		P-Ch		7.5	15
Turn-Off Delay Time	$t_{d(\text{off})}$		N-Ch		30	60
Fall Time	t_f		P-Ch		20	40
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 0.23 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$	N-Ch		10	20
		$I_F = -0.23 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$	P-Ch		8.5	17
			N-Ch		15	30
			P-Ch		12	24
			N-Ch		20	40
			P-Ch		25	40

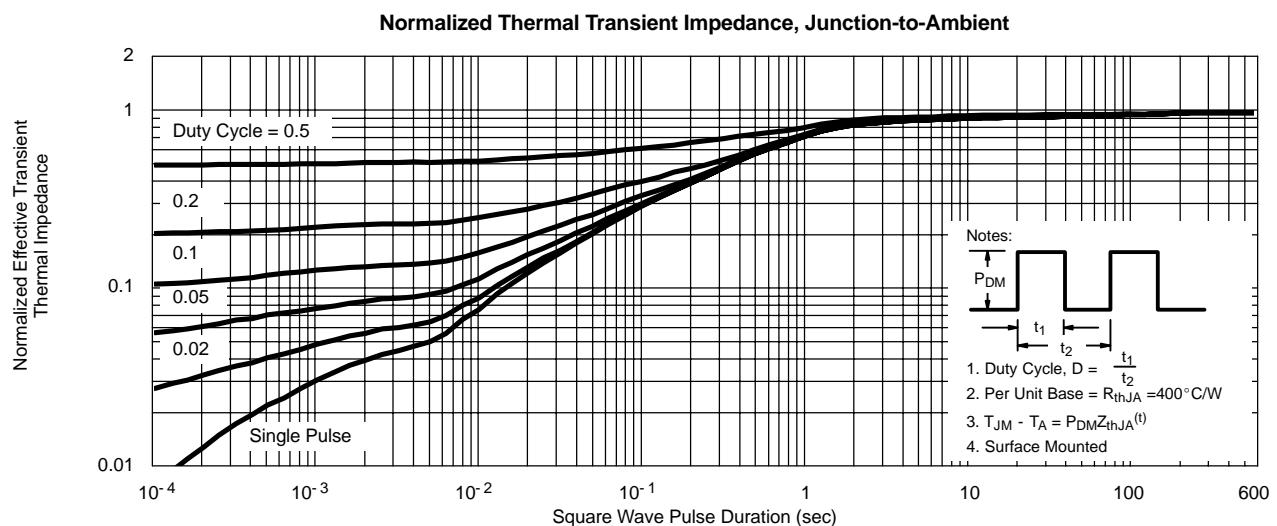
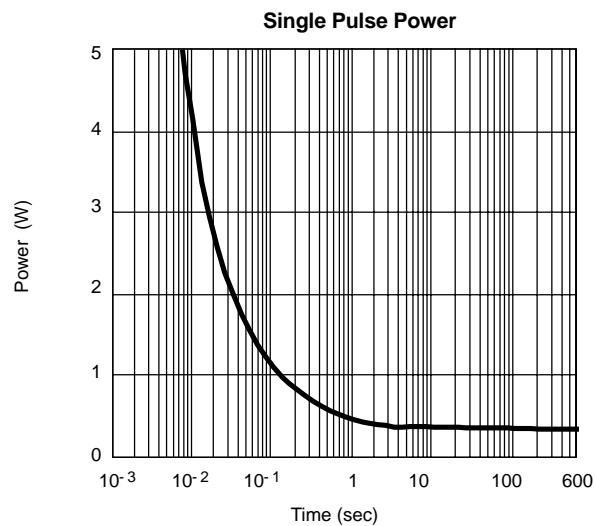
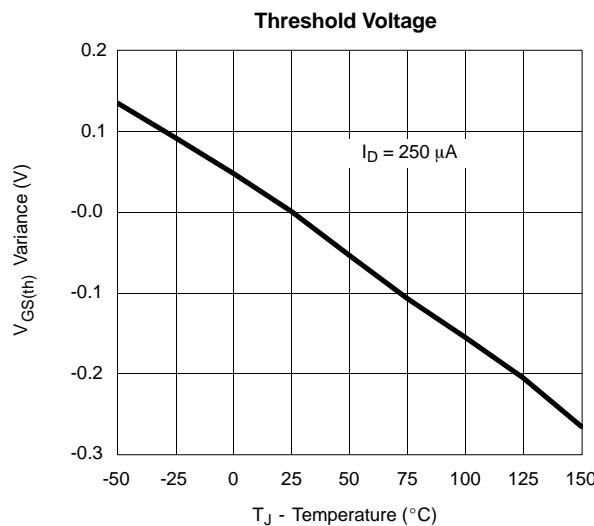
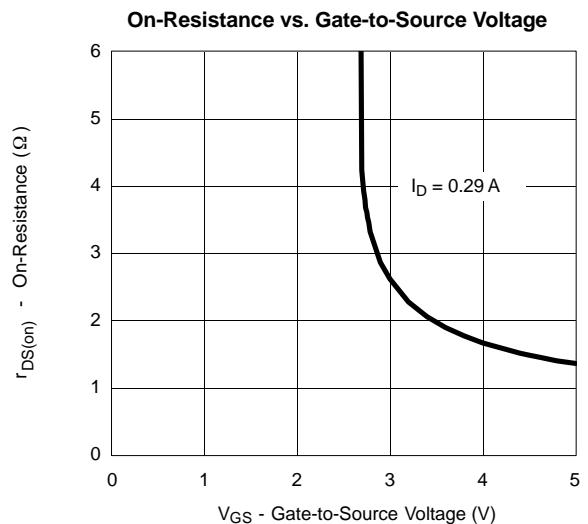
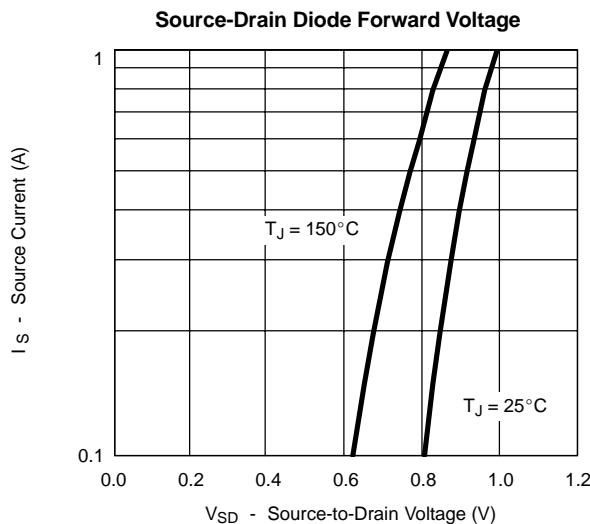
Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)
N-CHANNEL
Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature


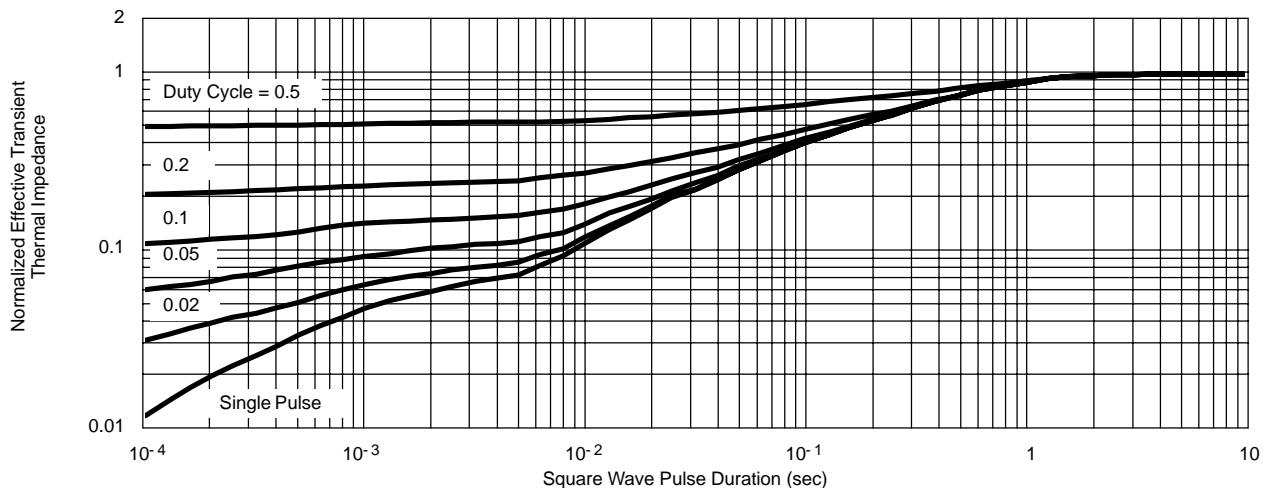
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL

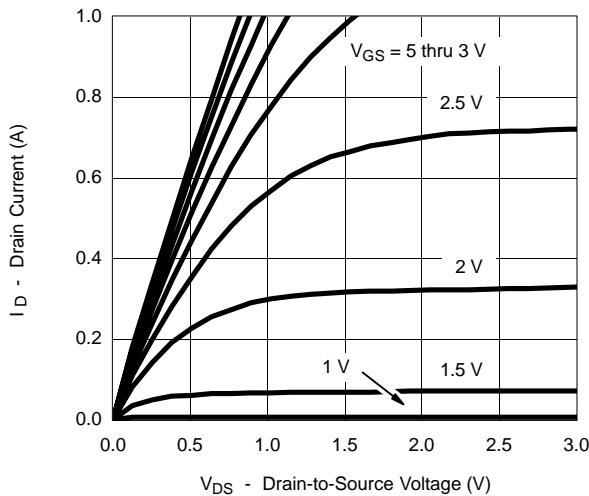


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)
N-CHANNEL

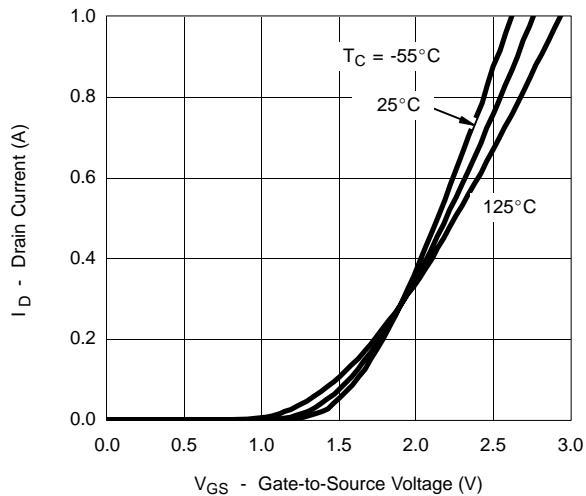
Normalized Thermal Transient Impedance, Junction-to-Foot


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)
P-CHANNEL

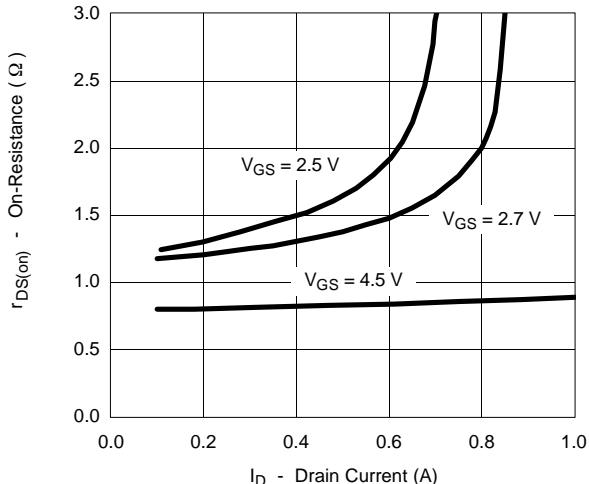
Output Characteristics



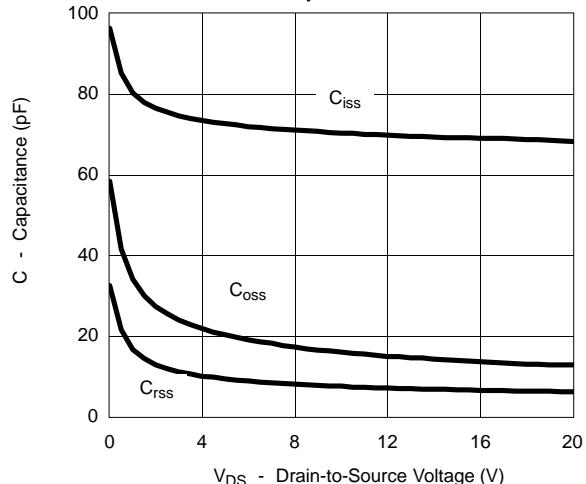
Transfer Characteristics



On-Resistance vs. Drain Current



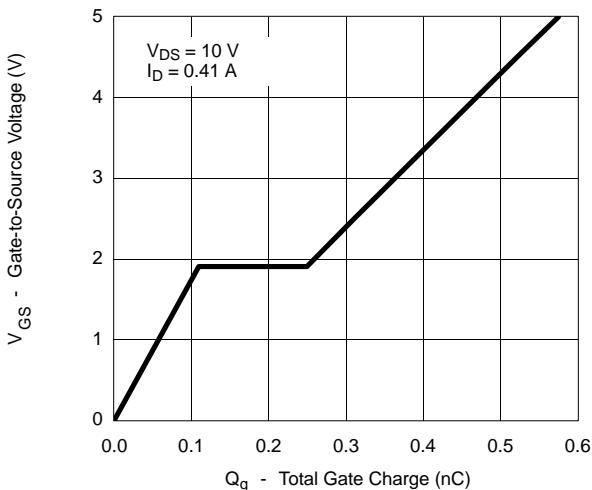
Capacitance



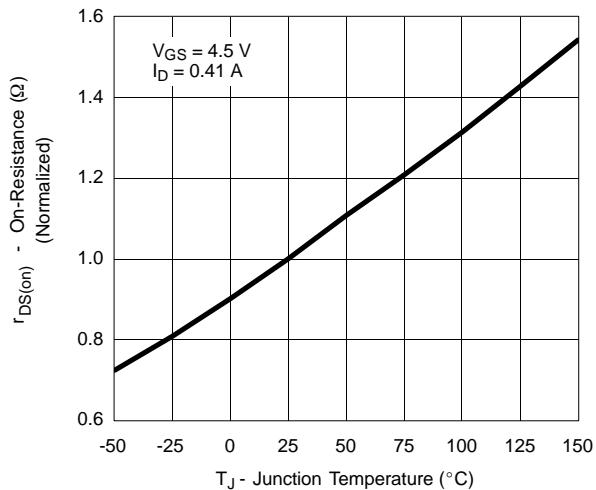
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL

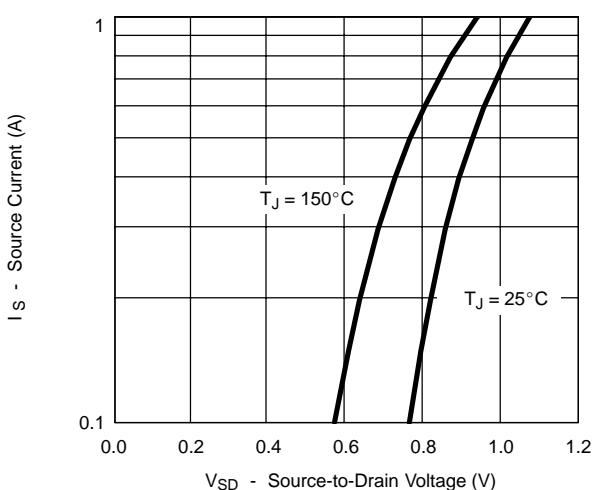
Gate Charge



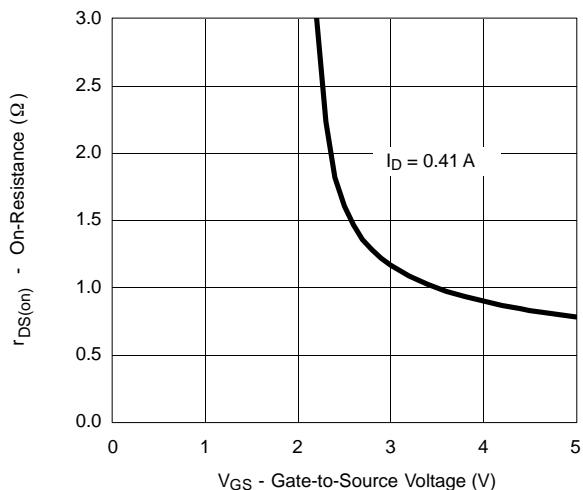
On-Resistance vs. Junction Temperature



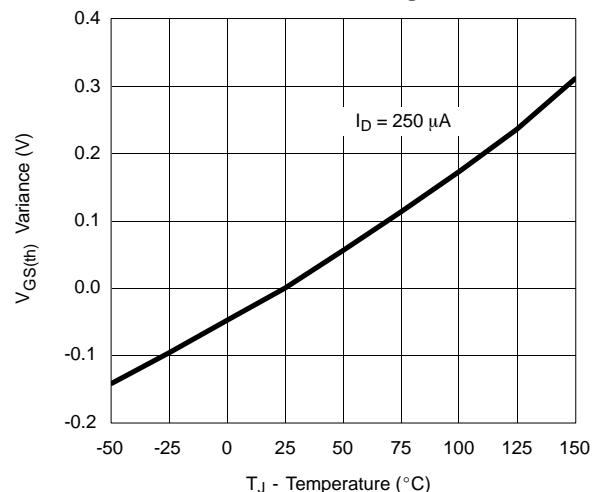
Source-Drain Diode Forward Voltage



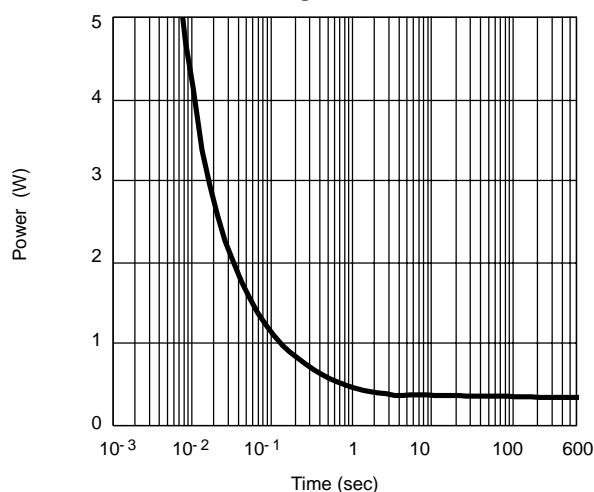
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power





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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL

