

VISHAY

Si3430DV

Vishay Siliconix

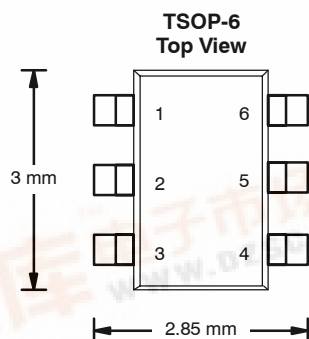
N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

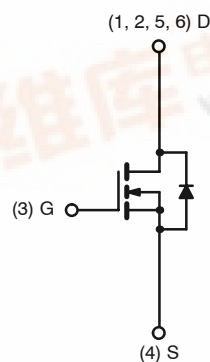
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.170 @ $V_{GS} = 10$ V	2.4
	0.185 @ $V_{GS} = 6.0$ V	2.3

FEATURES

- High-Efficiency PWM Optimized
- 100% R_g Tested



Ordering Information: Si3430DV-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	100		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 175°C) ^a	T _A = 25°C	I _D	2.4	1.8	A
	T _A = 85°C		1.7	1.3	
Pulsed Drain Current		I _{DM}	8		
Avalanche Current	L = 0.1 mH	I _{AR}	6		mJ
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)		E _{AR}	1.8		
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	1.0	A
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.0	1.14	W
	T _A = 85°C		1.0	0.59	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	45	62.5	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	30	

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.

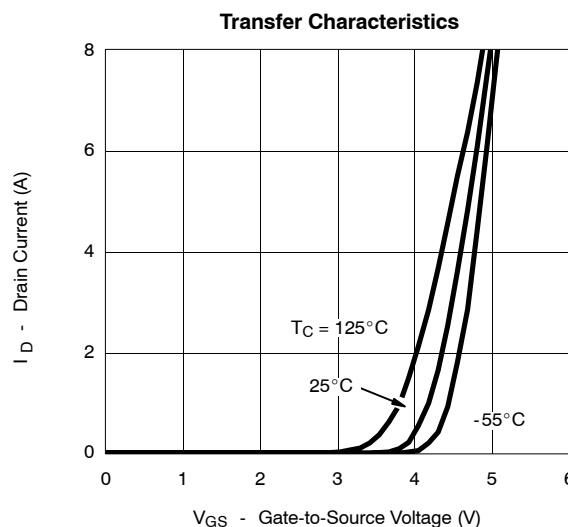
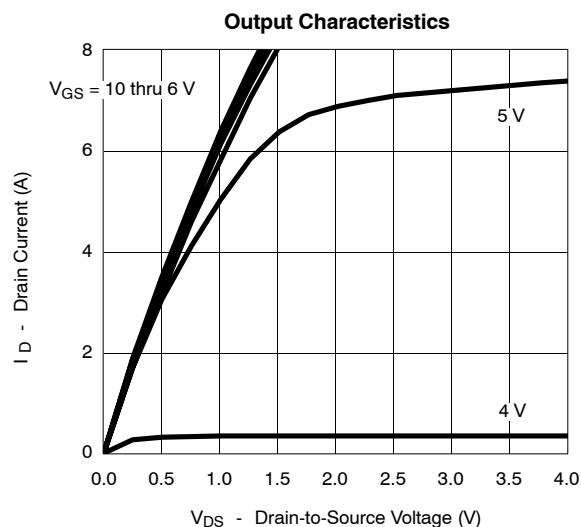
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 85 °C			25	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	8			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.4 A		0.148	0.170	Ω
		V _{GS} = 6.0 V, I _D = 2.3 A		0.160	0.185	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.4 A		7		S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 2.4 A		5.5	6.6	nC
Gate-Source Charge	Q _{gs}			1.5		
Gate-Drain Charge	Q _{gd}			1.4		
Gate Resistance	R _g		1		4	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		9	20	ns
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			16	30	
Fall Time	t _f			9	20	
Gate Resistance	R _g	V _{GS} = 0.1 V, f = 5 MHz		2.8		Ω
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs		50	80	ns

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

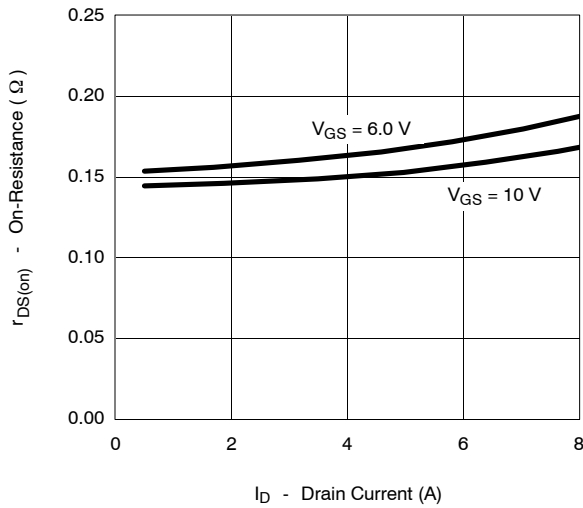
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



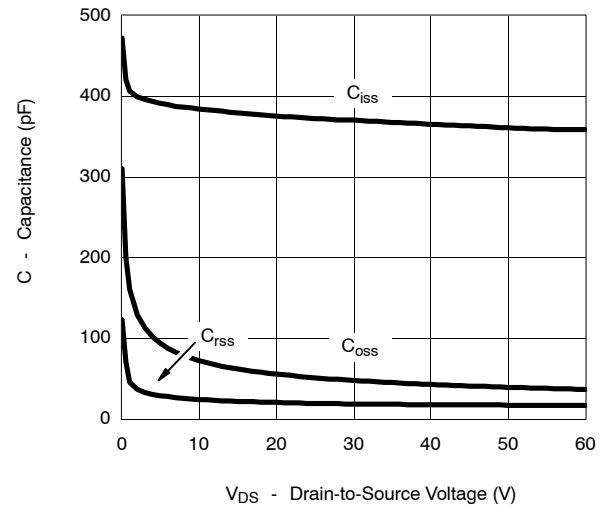


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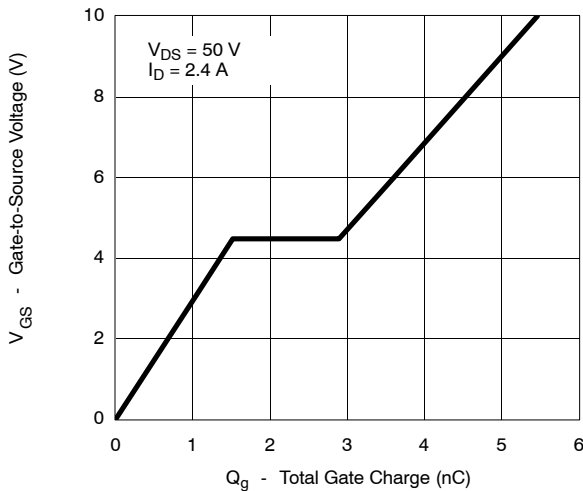
On-Resistance vs. Drain Current



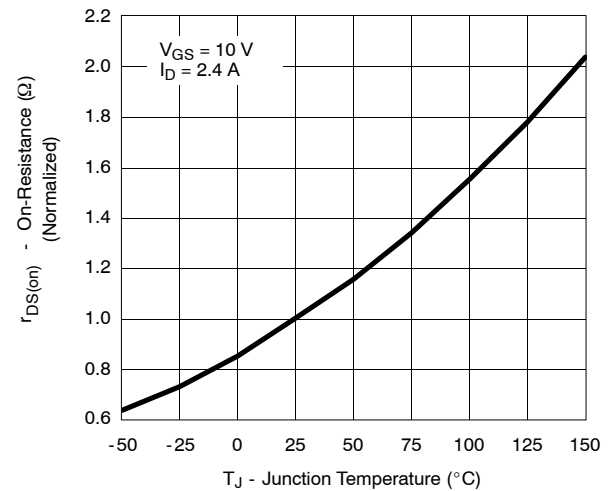
Capacitance



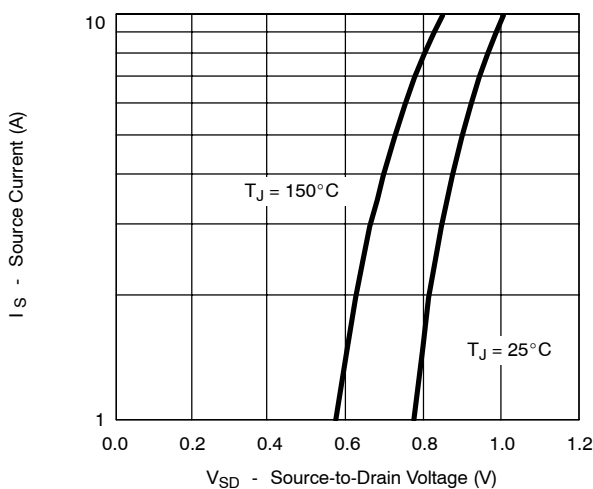
Gate Charge



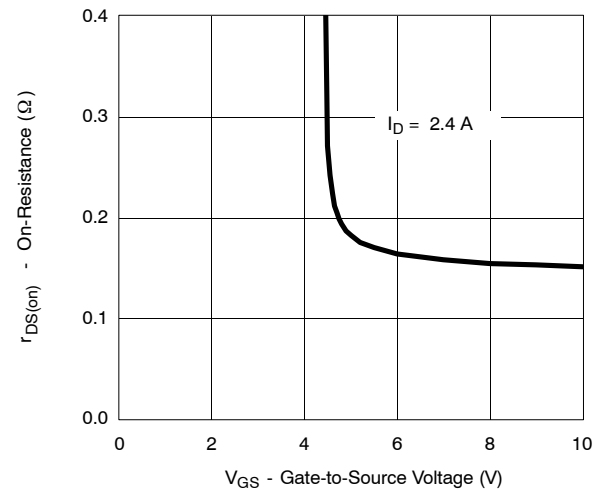
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

