Load Switch with Level-Shift

PRODUCT SUMMARY		
V_{DS2} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
1.8 to 8	0.080 @ V_{IN} = 4.5 V	±2.7
	0.110 @ V_{IN} = 2.5 V	±2.2
	0.175 @ V_{IN} = 1.8 V	±1.7

ESD Protected
3000 V
1.8-V Rated

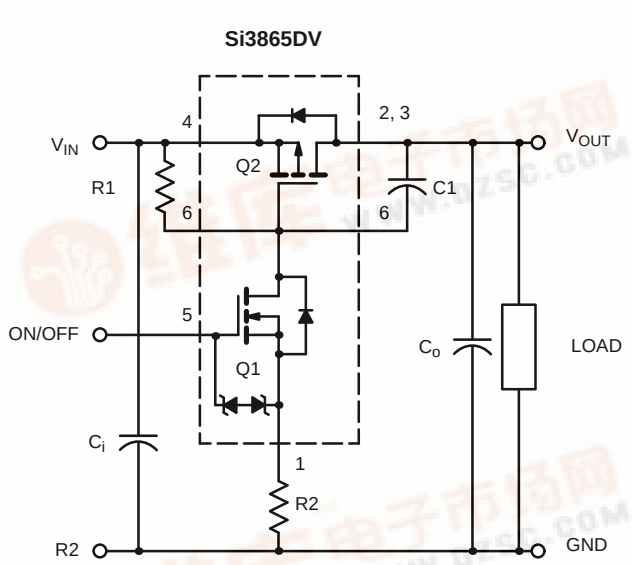
FEATURES

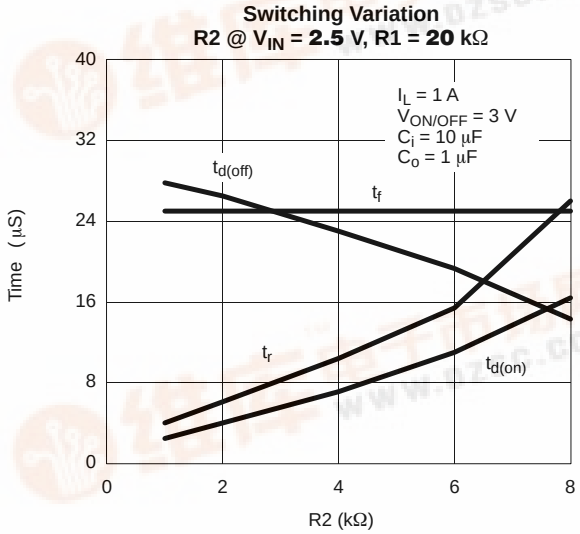
- 80-mΩ Low $r_{DS(on)}$ TrenchFET™
- 1.8 to 8-V Input
- 1.5 to 8-V Logic Level Control
- Low Profile, Small Footprint TSOP-6 Package
- 3000-V ESD Protection On Input Switch, $V_{ON/OFF}$
- Adjustable Slew-Rate

DESCRIPTION

The Si3865DV includes a p- and n-channel MOSFET in a single TSOP-6 package. The low on-resistance p-channel TrenchFET® is tailored for use as a load switch. The n-channel, with an external resistor, can be used as a level-shift to drive the p-channel load-switch. The n-channel MOSFET has internal ESD protection and can be driven by logic signals as low as 1.5-V. The Si3865DV operates on supply lines from 1.8 to 8-V, and can drive loads up to 2.7 A.

APPLICATION CIRCUITS





Note: For R2 switching variations with other V_{IN}/R1 combinations See Typical Characteristics

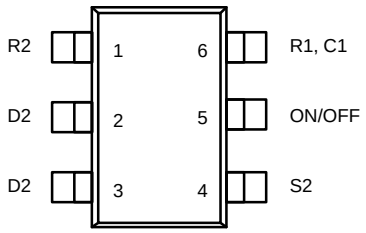
COMPONENTS		
R1	Pull-Up Resistor	Typical 10 kΩ to 1 mΩ*
R2	Optional Slew-Rate Control	Typical 0 to 100 kΩ*
C1	Optional Slew-Rate Control	Typical 1000 pF

*Minimum R1 value should be at least 10 x R2 to ensure Q1 turn-on.

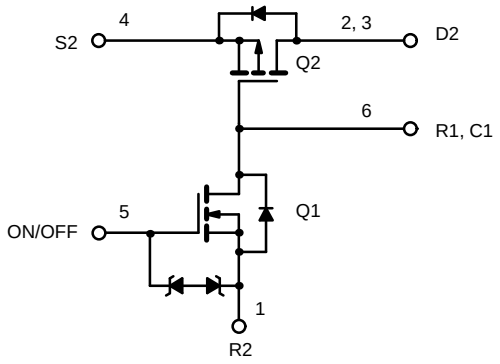
The Si3865DV is ideally suited for high-side load switching in portable applications. The integrated n-channel level-shift device saves space by reducing external components. The slew rate is set externally so that rise-times can be tailored to different load types.

FUNCTIONAL BLOCK DIAGRAM

TSOP-6
Top View



Si3865DV



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Input Voltage		V_{IN}	8	V
ON/OFF Voltage		$V_{ON/OFF}$	8	
Load Current	Continuous[a, b]	I_L	± 2.7	A
	Pulsed[b, c]		± 6	
Continuous Intrinsic Diode Conduction[a]		I_S	–1	
Maximum Power Dissipation[a]		P_D	0.83	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
ESD Rating, MIL-STD-883D Human Body Model (100 pF, 1500 Ω)		ESD	3	kV

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (continuous current)[a]	R_{thJA}	120	150	°C/W
Maximum Junction-to-Foot (Q2)	R_{thJC}	35	50	

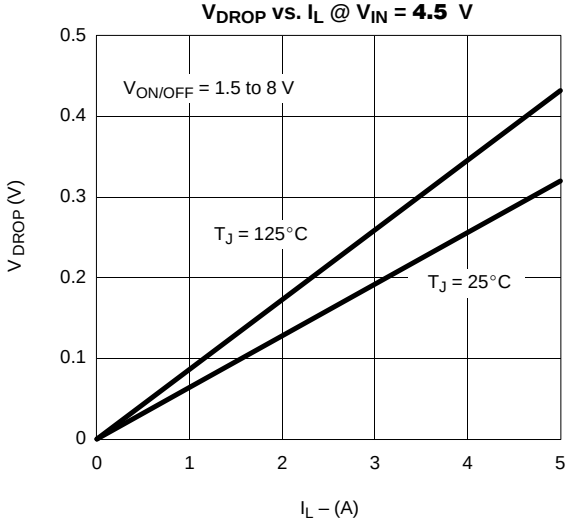
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF Characteristics							
Reverse Leakage Current	I_{FL}	V_{IN} = 8 V, $V_{ON/OFF}$ = 0 V				1	µA
Diode Forward Voltage	V_{SD}	I_S = –1 A			–0.7	–1	V
ON Characteristics							
Input Voltage Range	V_{IN}			1.8		8	V
On-Resistance (p-channel) @ 1 A	$r_{DS(on)}$	$V_{ON/OFF}$ = 1.5 V, I_D = 1 A	V_{IN} = 4.5 V		0.064	0.080	Ω
			V_{IN} = 2.5 V		0.092	0.110	
			V_{IN} = 1.8 V		0.135	0.175	
On-State (p-channel) Drain-Current	$I_{D(on)}$	V_{IN-OUT} ≤ 0.2 V, V_{IN} = 5 V, $V_{ON/OFF}$ = 1.5 V		1			A
		V_{IN-OUT} ≤ 0.3 V, V_{IN} = 3 V, $V_{ON/OFF}$ = 1.5 V		1			

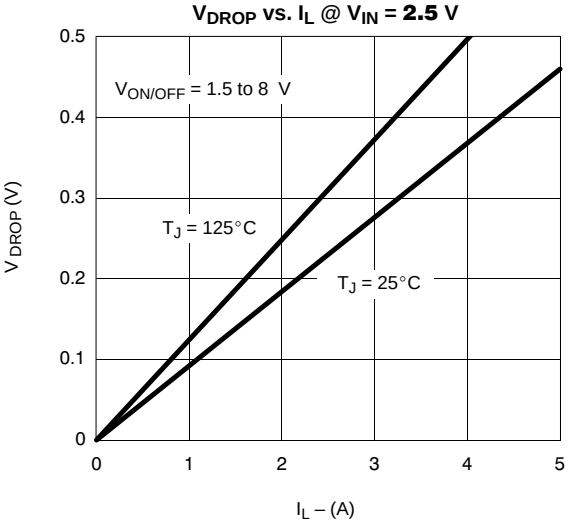
Notes
a. Surface Mounted on FR4 Board.
b. V_{IN} = 8 V, $V_{ON/OFF}$ = 8 V, T_A = 25°C.
c. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

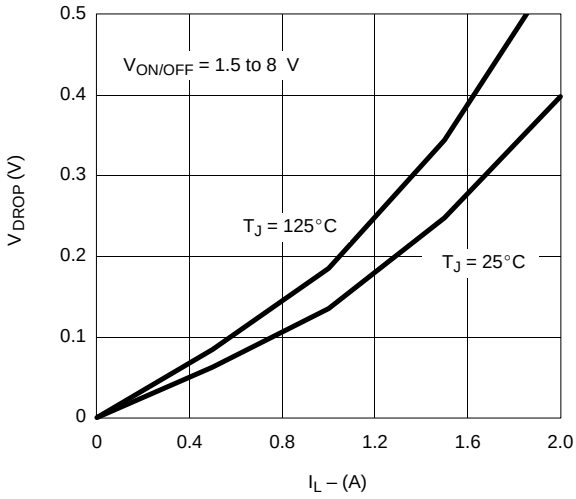
V_{DROP} vs. I_L @ V_{IN} = 4.5 V



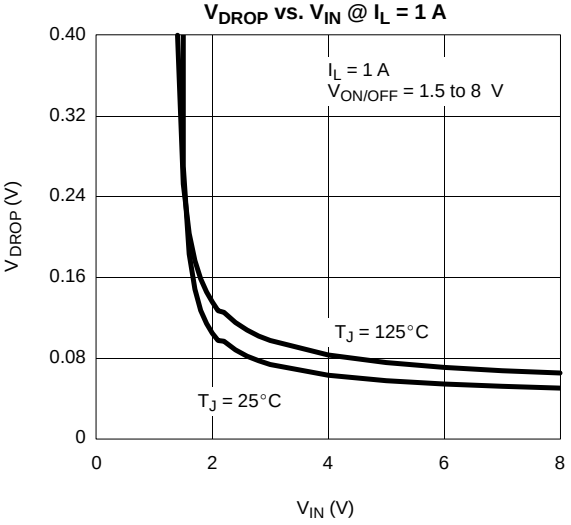
V_{DROP} vs. I_L @ V_{IN} = 2.5 V



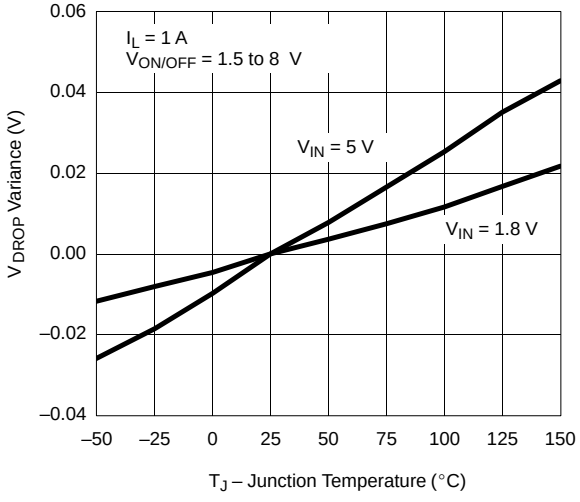
V_{DROP} vs. I_L @ V_{IN} = 1.8 V



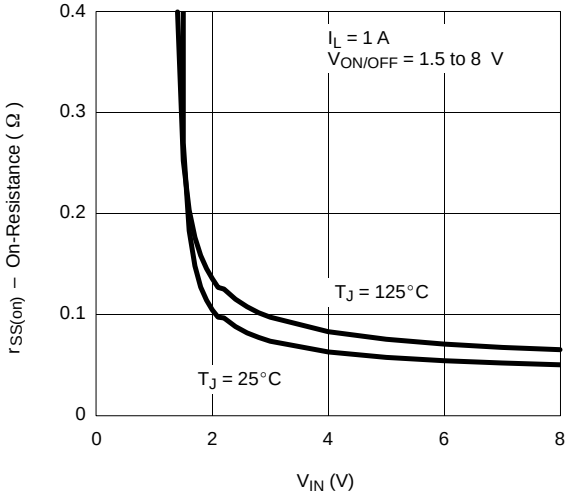
V_{DROP} vs. V_{IN} @ I_L = 1 A



V_{DROP} Variance vs. Junction Temperature

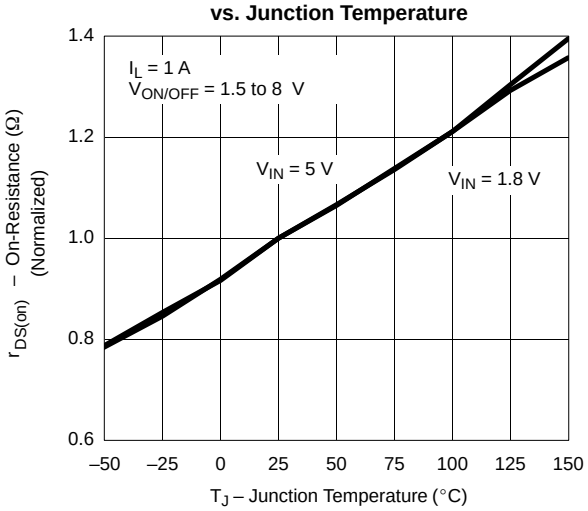


On-Resistance vs. Input Voltage

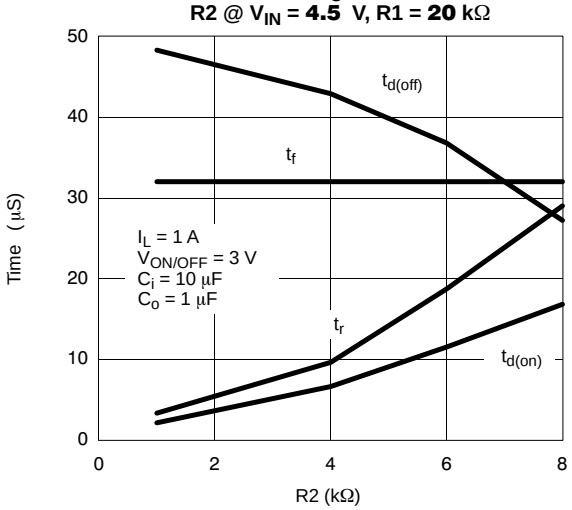


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

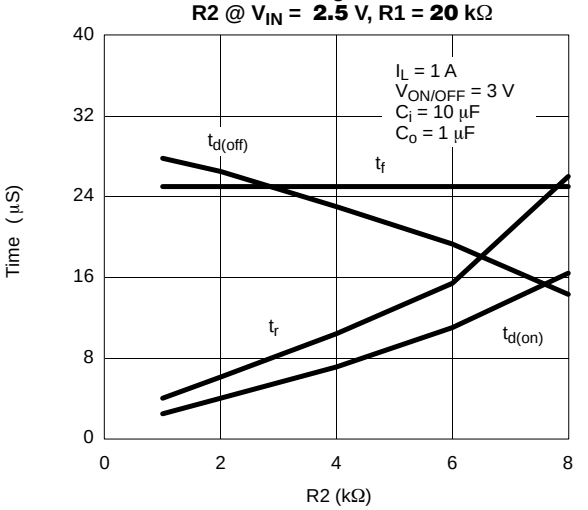
Normalized On-Resistance vs. Junction Temperature



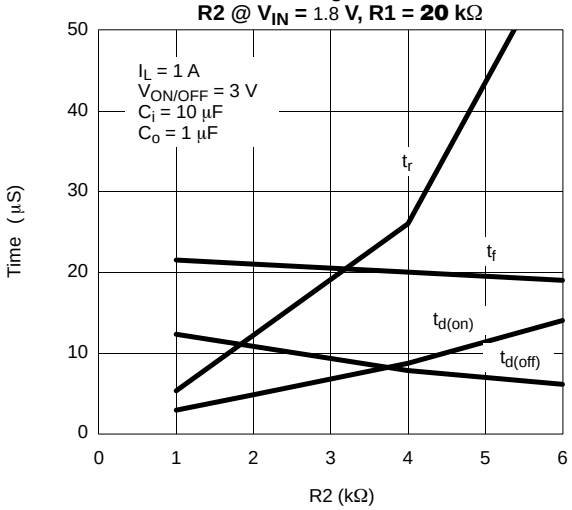
Switching Variation R2 @ V_{IN} = 4.5 V, R1 = 20 kΩ



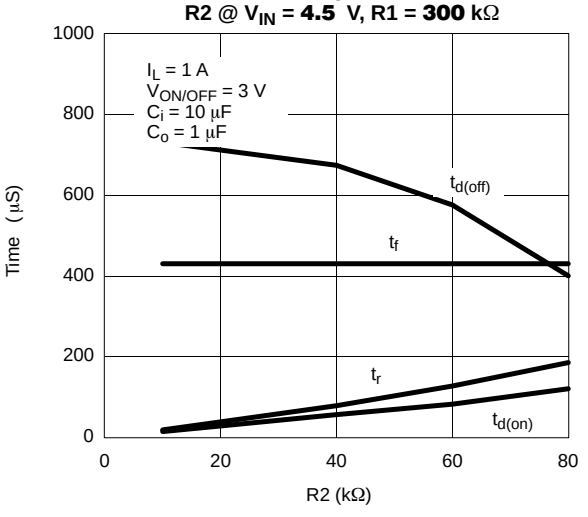
Switching Variation R2 @ V_{IN} = 2.5 V, R1 = 20 kΩ



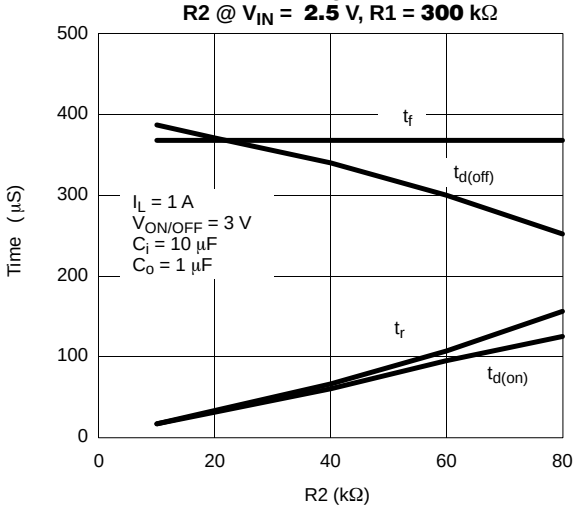
Switching Variation R2 @ V_{IN} = 1.8 V, R1 = 20 kΩ



Switching Variation R2 @ V_{IN} = 4.5 V, R1 = 300 kΩ



Switching Variation R2 @ V_{IN} = 2.5 V, R1 = 300 kΩ



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)