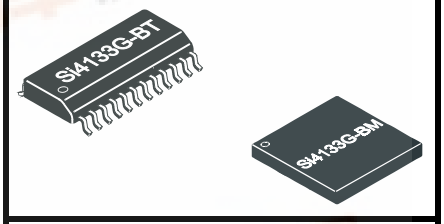
查询Si4112G供应商 捷多邦，专业PCB打样工厂，24小时加急出货

Si4133G
Si4123G/22G/13G/12G

Dual-Band RF Synthesizer With Integrated VCOs For GSM and GPRS Wireless Communications

Features

- Dual-Band RF Synthesizers
  - RF1: 900 MHz to 1.8 GHz
  - RF2: 750 MHz to 1.5 GHz
- IF Synthesizer
  - IF: 500 MHz to 1000 MHz
- Integrated VCOs, Loop Filters, Varactors, and Resonators
- Minimal External Components Required
- Fast Settling Time: 140 µs
- Low Phase Noise
- Programmable Power Down Modes
- 1 µA Standby Current
- 18 mA Typical Supply Current
- 2.7 V to 3.6 V Operation
- Packages: 24-Pin TSSOP and 28-Pin MLP



Ordering Information:
See page 28.

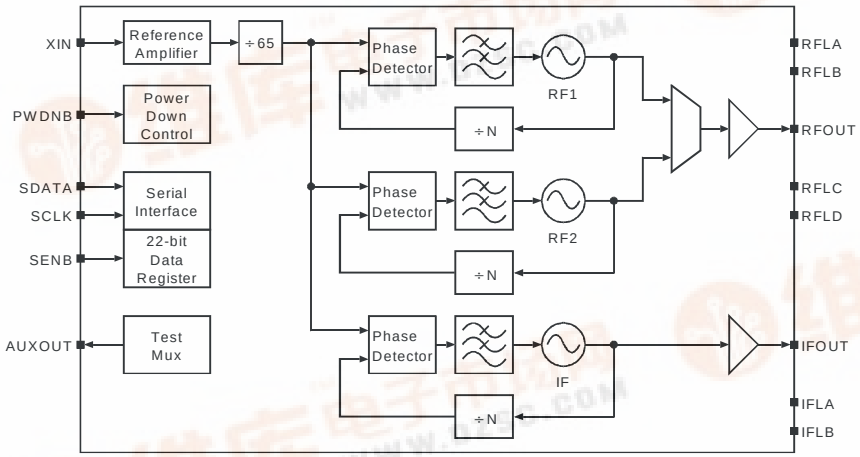
Applications

- GSM, DCS1800, and PCS1900 Cellular Telephones
- GPRS Data Terminals
- HSCSD Data Terminals

Description

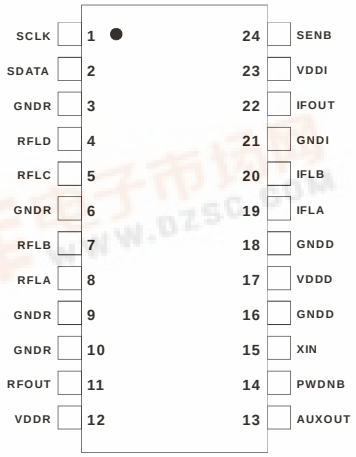
The Si4133G is a monolithic integrated circuit that performs both IF and dual-band RF synthesis for GSM and GPRS wireless communications applications. The Si4133G includes three VCOs, loop filters, reference and VCO dividers, and phase detectors. Divider and power down settings are programmable through a three-wire serial interface.

Functional Block Diagram

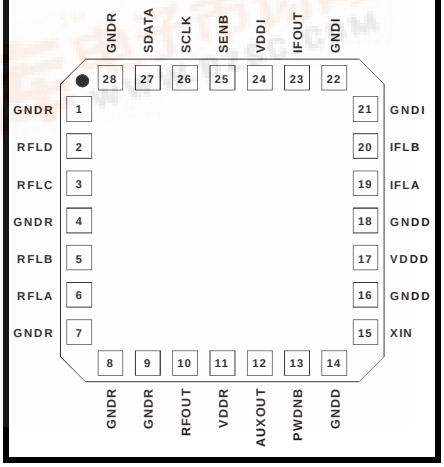


Pin Assignments

Si4133G-BT



Si4133G-BM



Patents pending

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Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–20	25	85	°C
Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Supply Voltages Difference	V_Δ	$(V_{DDR} – V_{DDD})$, $(V_{DDI} – V_{DDD})$	–0.3	—	0.3	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at 3.0 V and an operating temperature of 25°C unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 4.0	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	–55 to 150	^oC

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **This device is a high performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDATA, SENB, PWDNB and XIN.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Typical Supply Current[1]		RF1 and IF Operating	—	18	31	mA
RF1 Mode Supply Current[1]			—	13	17	mA
RF2 Mode Supply Current[1]			—	12	17	mA
IF Mode Supply Current[1]			—	10	14	mA
Standby Current		PWDNB = 0	—	1	—	µA
High Level Input Voltage[2]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[2]	I_{IH}	V_{IH} = 3.6 V, V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD}= 3.6 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OH} = 500 µA	—	—	0.4	V

Notes:
1. RF1 = 1.55 GHz, RF2 = 1.2 GHz, IF = 800 MHz
2. For signals SCLK, SDATA, SENB, and PWDNB.
3. For signal AUXOUT.

Table 4. Serial Interface Timing
(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{clk}	Figure 1	40	—	—	ns
SCLK Rise Time	t_r	Figure 1	—	—	50	ns
SCLK Fall Time	t_f	Figure 1	—	—	50	ns
SCLK High Time	t_h	Figure 1	10	—	—	ns
SCLK Low Time	t_l	Figure 1	10	—	—	ns
SDATA Setup Time to SCLK↑[2]	t_{su}	Figure 2	5	—	—	ns
SDATA Hold Time from SCLK↑[2]	t_{hold}	Figure 2	0	—	—	ns
SENB↓ to SCLK↑ Delay Time[2]	t_{en1}	Figure 2	10	—	—	ns
SCLK↑ to SENB↑ Delay Time[2]	t_{en2}	Figure 2	12	—	—	ns
SENB↑ to SCLK↑ Delay Time[2]	t_{en3}	Figure 2	12	—	—	ns
SENB Pulse Width	t_w	Figure 2	10	—	—	ns

Notes:
1. All timing is referenced to the 50% level of the waveform, unless otherwise noted.
2. Timing is not referenced to 50% level of waveform. See Figure 2.

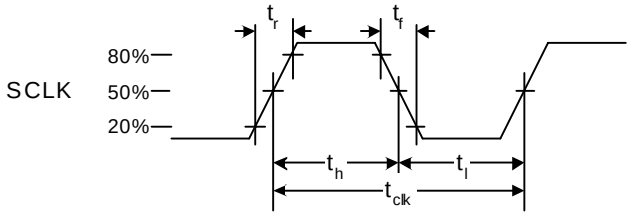


Figure 1. SCLK Timing Diagram

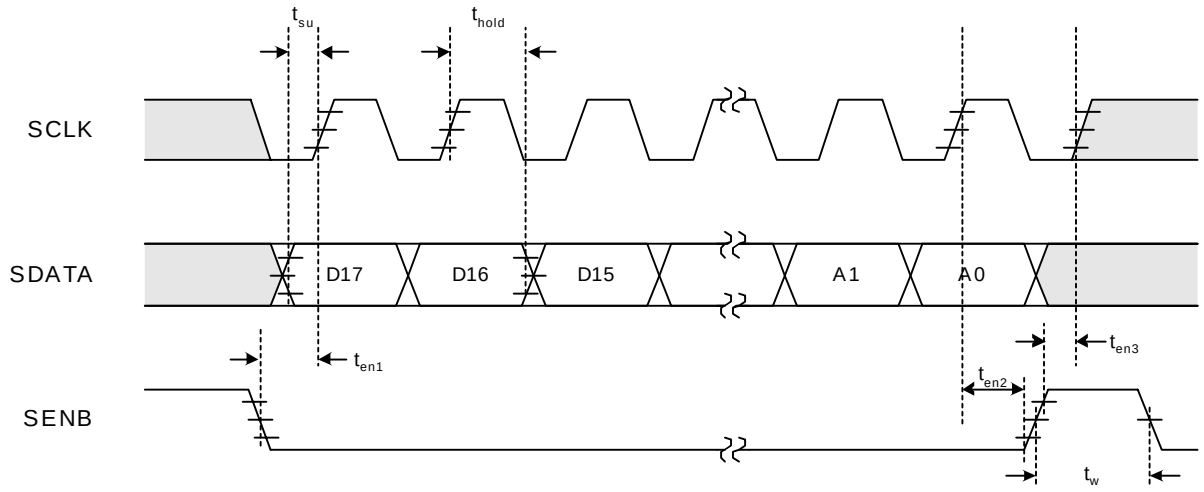


Figure 2. Serial Interface Timing Diagram

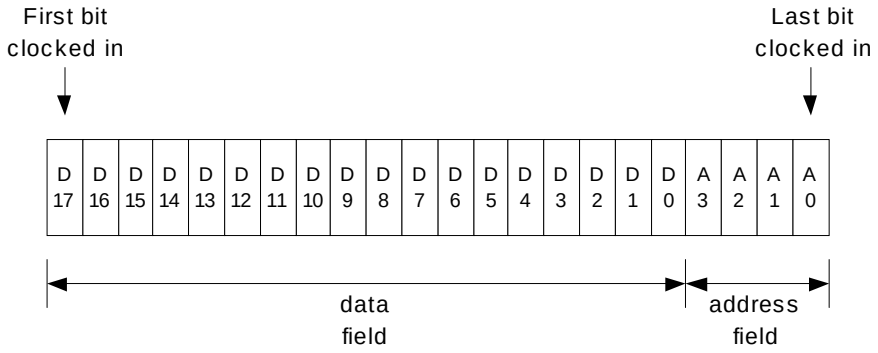


Figure 3. Serial Word Format

Table 5. RF and IF Synthesizer Characteristics

(V_{DD} = 2.7 to 3.6 V, T_A = –20 to 85°C)

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
XIN Input Frequency	f_{REF}		—	13	—	MHz
Reference Amplifier Sensitivity	V_{REF}		0.5	—	V_{DD} +0.3	V_{PP}
Phase Detector Update Frequency	f_ϕ	$f_\phi = f_{REF}/R$		200		KHz
RF1 Center Frequency Range	f_{CEN}		947	—	1720	MHz
RF2 Center Frequency Range	f_{CEN}		789	—	1429	MHz
IF VCO Center Frequency	f_{CEN}		526	—	952	MHz
Tuning Range from f_{CEN}		Note: L_{EXT} ±10%	–5	—	5	%
RF1 VCO Pushing		Open loop	—	0.5	—	MHz/V
RF2 VCO Pushing			—	0.4	—	MHz/V
IF VCO Pushing			—	0.3	—	MHz/V
RF1 VCO Pulling		VSWR = 2:1, all phases, open loop	—	0.4	—	MHz_{PP}
RF2 VCO Pulling			—	0.1	—	MHz_{PP}
IF VCO Pulling			—	0.1	—	MHz_{PP}
RF1 Phase Noise		1 MHz offset	—	–132	—	dBc/Hz
		3 MHz offset	—	–142	—	dBc/Hz
RF1 Integrated Phase Error		100 Hz to 100 kHz	—	0.9	—	deg rms
RF2 Phase Noise		1 MHz offset	—	–134	—	dBc/Hz
		3 MHz offset	—	–144	—	dBc/Hz
RF2 Integrated Phase Error		100 Hz to 100 kHz	—	0.7	—	deg rms
IF Phase Noise		100 kHz offset	—	–117	—	dBc/Hz
IF Integrated Phase Error		100 Hz to 100 kHz	—	0.4	—	deg rms
RF1 Harmonic Suppression		Second Harmonic	—	–26	—	dBc
RF2 Harmonic Suppression			—	–26	—	dBc
IF Harmonic Suppression			—	–26	—	dBc
RFOUT Power Level		Z_L = 50 Ω	–7	–2	1	dBm
IFOUT Power Level		Z_L = 50 Ω	–8	–6	–1	dBm
RF1 Reference Spurs		Offset = 200 kHz	—	–70	—	dBc
		Offset = 400 kHz	—	–75	—	dBc
		Offset = 600 kHz	—	–80	—	dBc
RF2 Reference Spurs		Offset = 200 kHz	—	–75	—	dBc
		Offset = 400 kHz	—	–80	—	dBc
		Offset = 600 kHz	—	–80	—	dBc
Power Up Request to Synthesizer Ready Time, RF1, RF2, IF[2]	t_{pup}	Figures 4, 5	—	140	—	µs
Power Down Request to Synthesizer Off Time[3]	t_{pdn}	Figures 4, 5	—	—	100	ns

Notes:

1. RF1 = 1.55 GHz, RF2 = 1.2 GHz, IF = 550 MHz for all parameters unless otherwise noted.
2. From power up request (PWDNB↑ or SENB↑ during a write of 1 to bits PDIB and PDRB in Register 2) to RF and IF synthesizers ready (settled to within 0.1 ppm frequency error). Typical settling time to 5 degrees phase error is 120 µs.
3. From power down request (PWDNB↓, or SENB↑ during a write of 0 to bits PDIB and PDRB in Register 2) to supply current equal to I_{PWDN}.

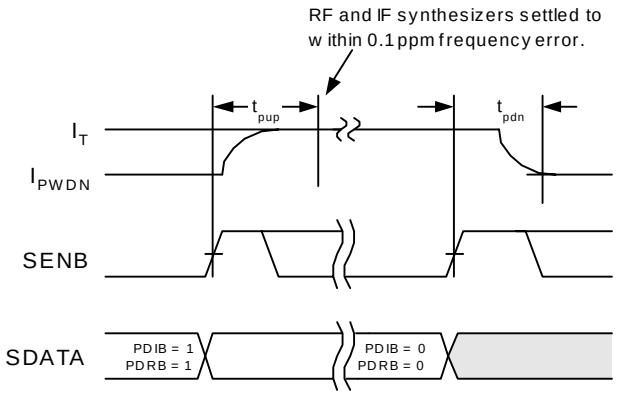


Figure 4. Software Power Management Timing Diagram

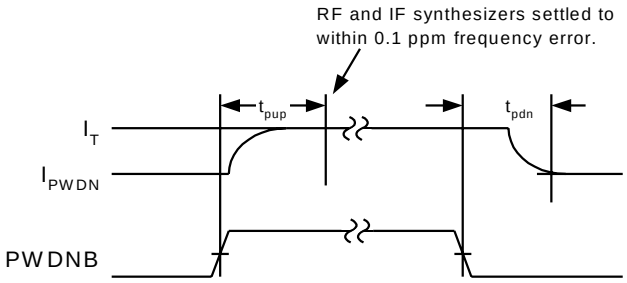


Figure 5. Hardware Power Management Timing Diagram

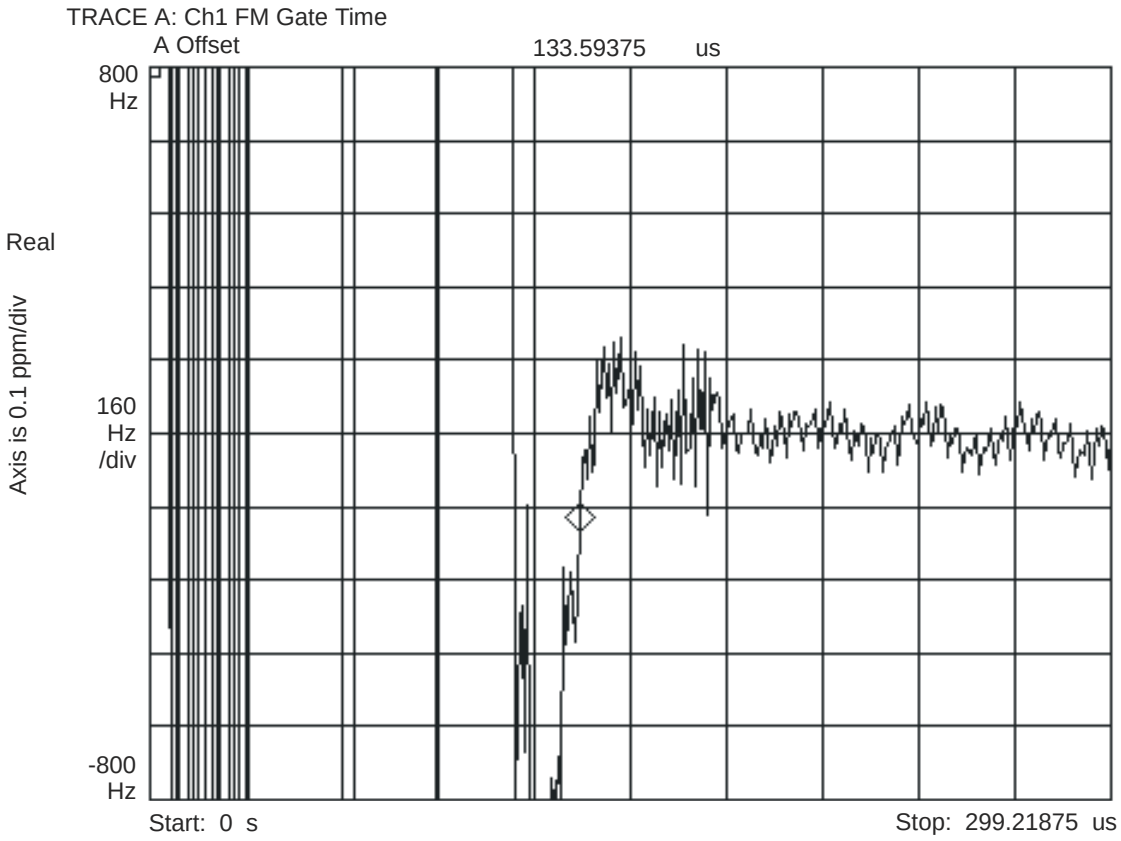


Figure 6. Typical Transient Response RF1 at 1.6 GHz with 200 kHz Phase Detector Update Frequency

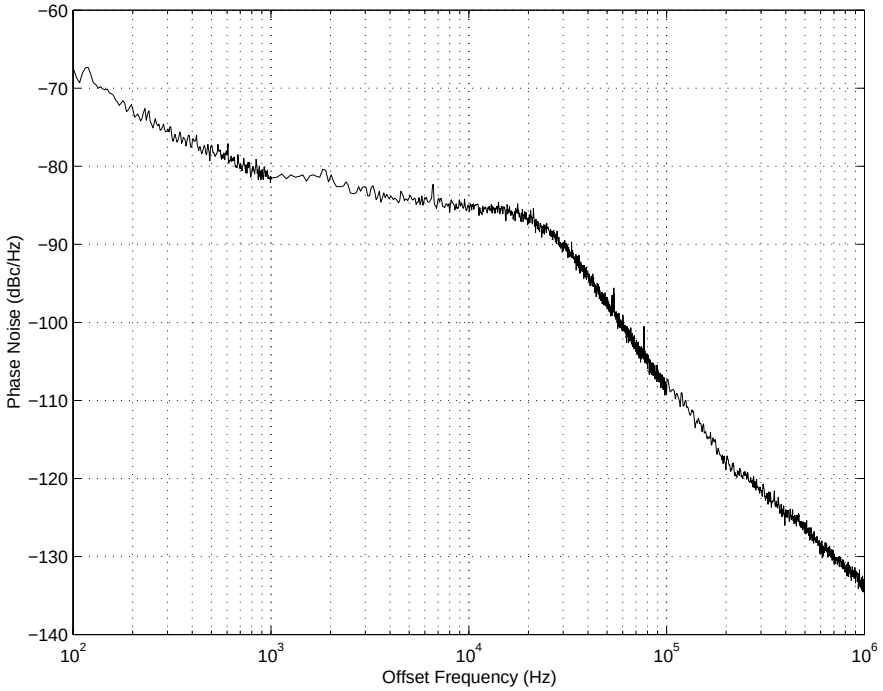


Figure 7. Typical RF1 Phase Noise at 1.6 GHz with 200 kHz Phase Detector Update Frequency

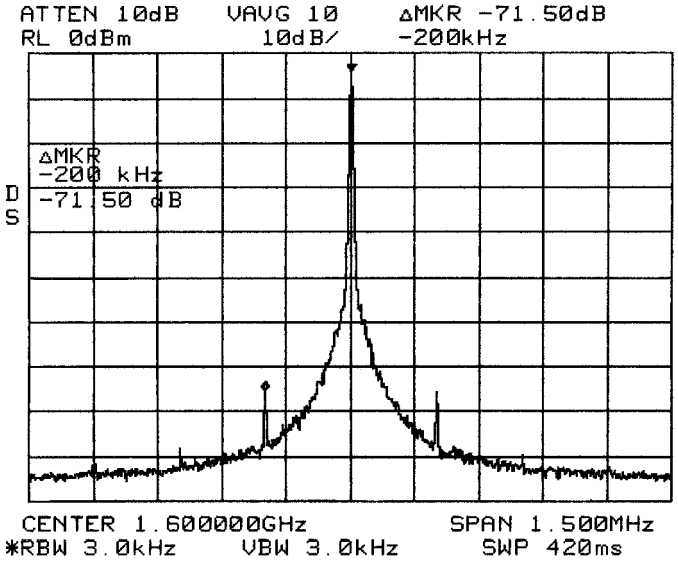


Figure 8. Typical RF1 Spurious Response at 1.6 GHz with 200 kHz Phase Detector Update Frequency

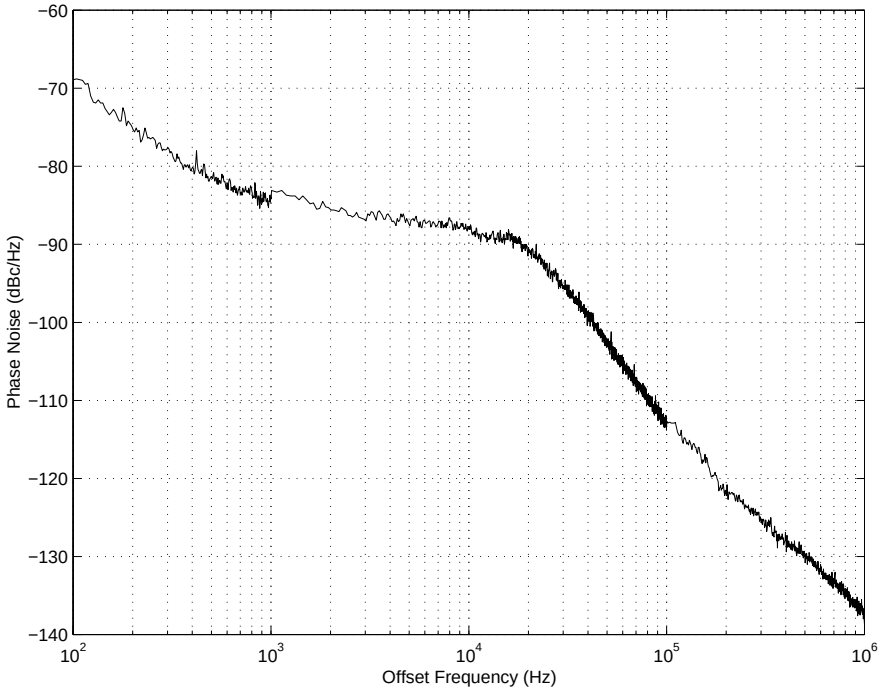


Figure 9. Typical RF2 Phase Noise at 1.2 GHz with 200 kHz Phase Detector Update Frequency

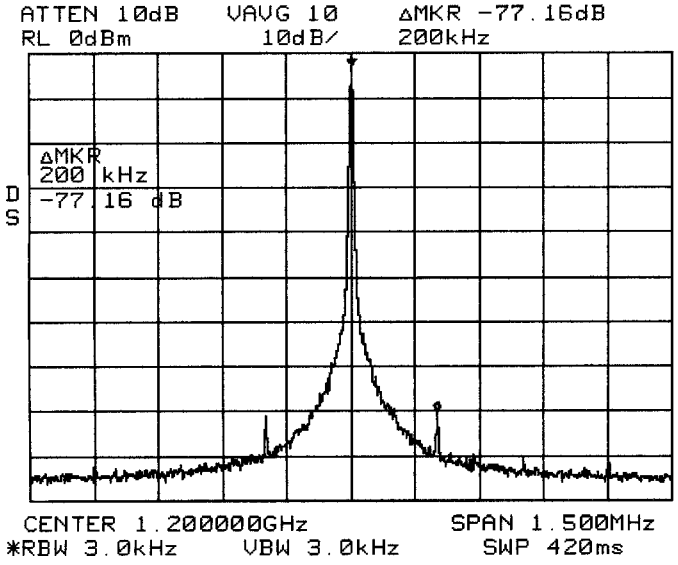


Figure 10. Typical RF2 Spurious Response at 1.2 GHz with 200 kHz Phase Detector Update Frequency

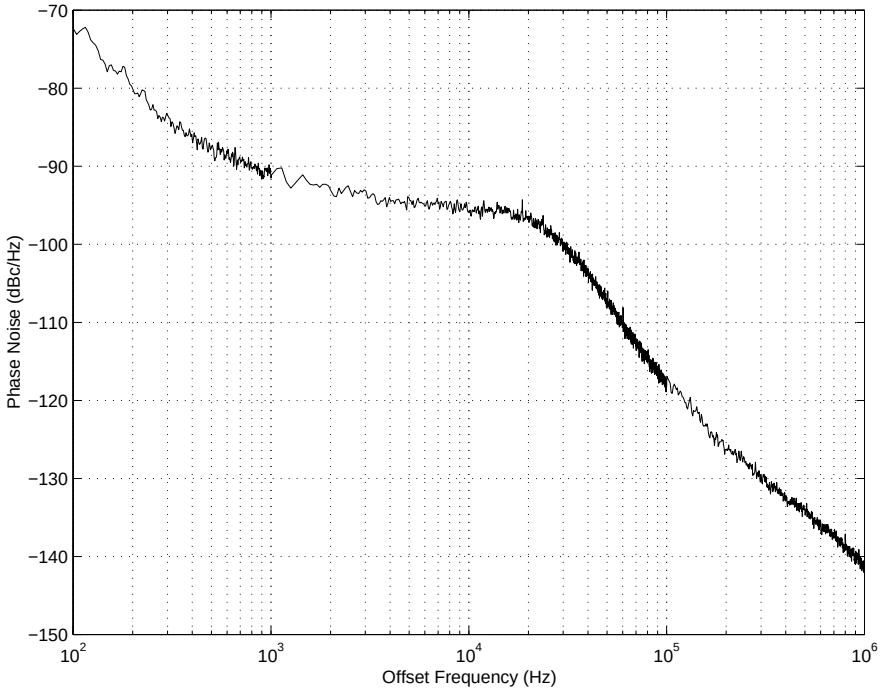


Figure 11. Typical IF Phase Noise at 550 MHz with 200 kHz Phase Detector Update Frequency

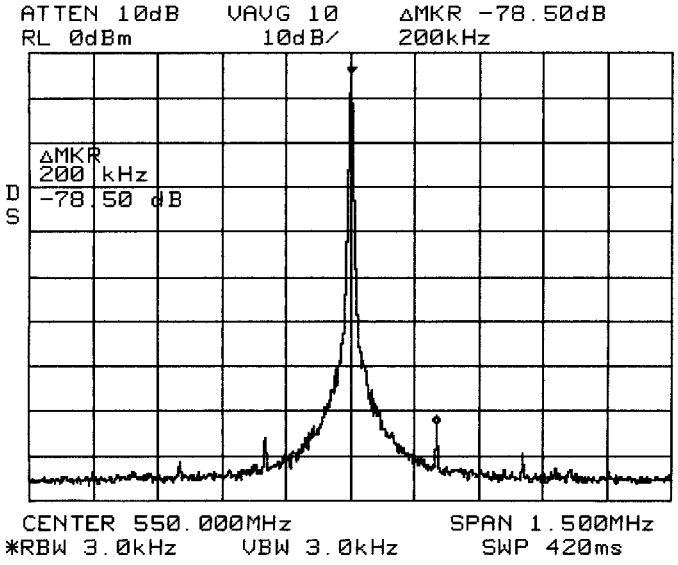


Figure 12. IF Spurious Response at 550 MHz with 200 kHz Phase Detector Update Frequency

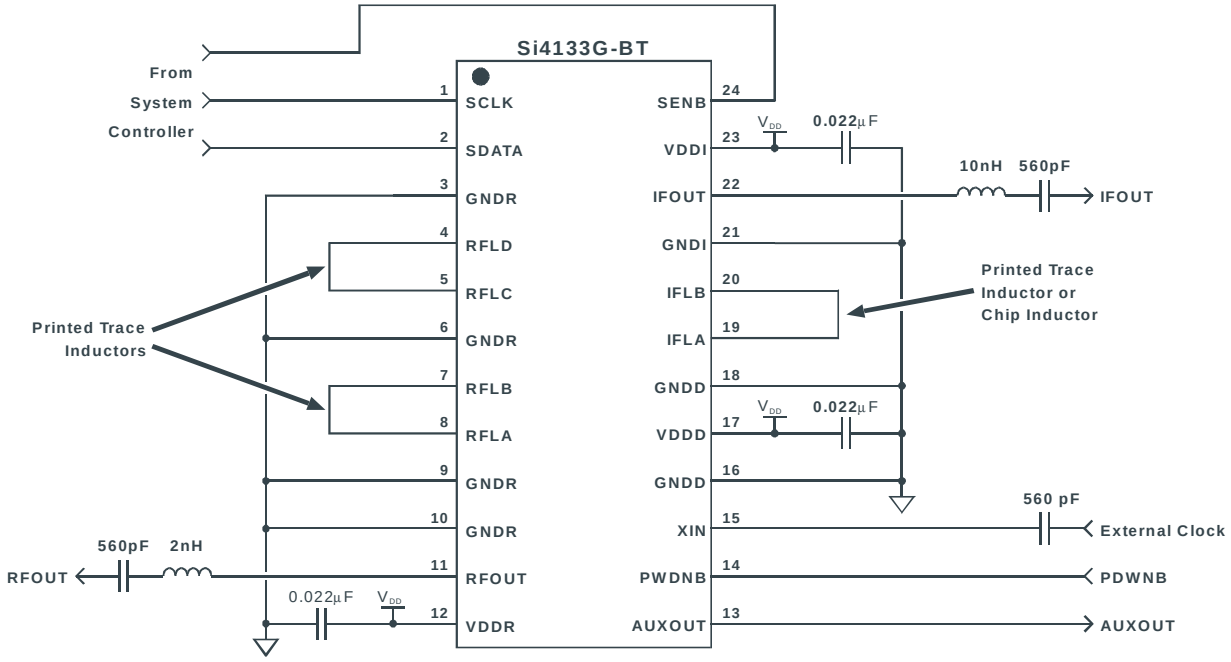


Figure 13. Typical Application Circuit: Si4133G-BT

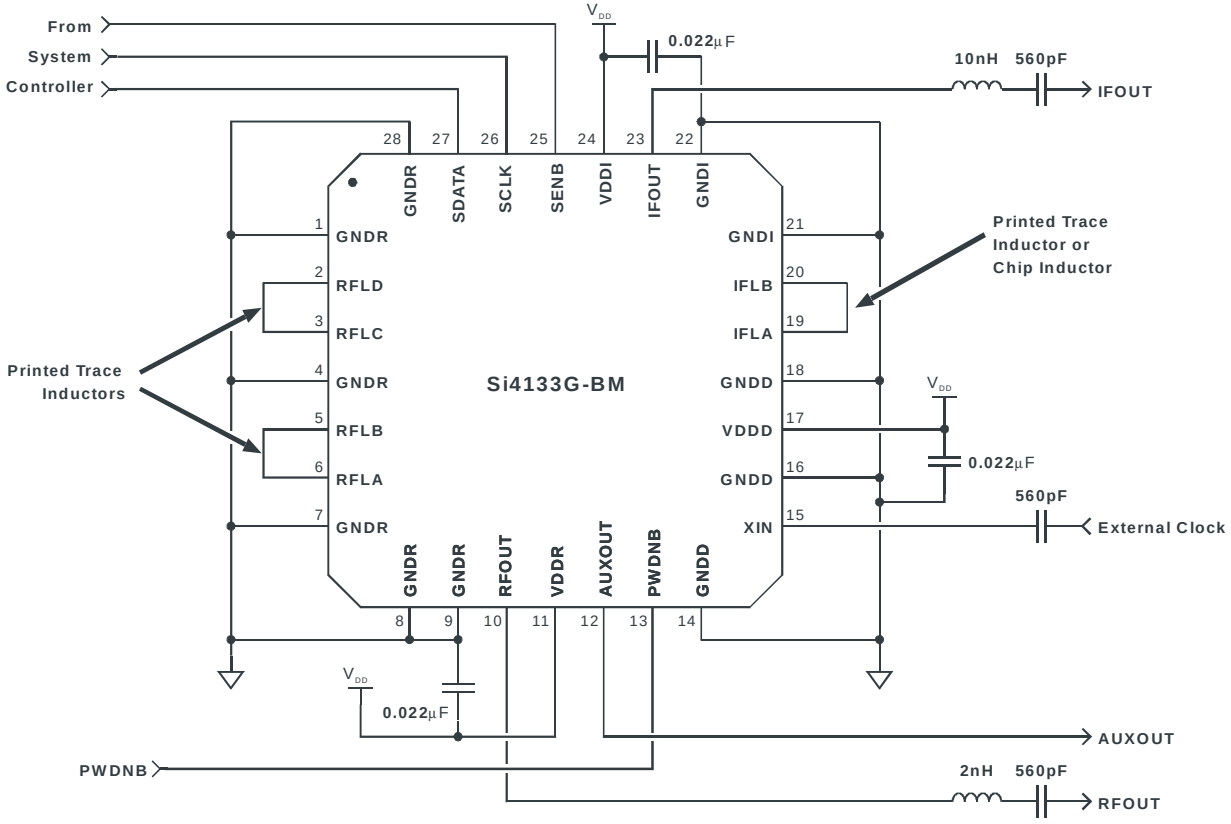


Figure 14. Typical Application Circuit: Si4133G-BM

Functional Description

The Si4133G is a monolithic integrated circuit that performs IF and dual-band RF synthesis for many wireless applications such as GSM, DCS1800, and PCS1900. Its fast transient response also makes the Si4133G especially well suited to GPRS and HSCSD multislot applications where channel switching and settling times are critical. This integrated circuit (IC), with a minimum number of external components, is all that is necessary to implement the frequency synthesis function.

The Si4133G has three complete phase-locked loops (PLLs) with integrated voltage-controlled oscillators (VCOs). The low phase noise of the VCOs makes the Si4133G suitable for use in demanding wireless communications applications. Also integrated are phase detectors, loop filters, and reference dividers. The IC is programmed through a three-wire serial interface.

One PLL is provided for IF synthesis, and two PLLs are provided for dual-band RF synthesis. One RF VCO is optimized to have its center frequency set between 947 MHz and 1720 MHz, while the second RF VCO is optimized to have its center frequency set between 789 MHz and 1429 MHz. The IF VCO is optimized to have its center frequency set between 526 MHz and 952 MHz. Each PLL can adjust its output frequency by ±5% relative to its VCO center frequency.

The center frequency of each of the three VCOs is set by connection of an external inductance. Inaccuracies in the value of the inductance are compensated for by the Si4133G's proprietary self-tuning algorithm. This algorithm is initiated each time the PLL is powered-up (by either the PWDNB pin or by software) and/or each time a new output frequency is programmed.

The two RF PLLs share a common output pin, so only one PLL is active at a given time. Because the two VCOs can be set to have widely separated center frequencies, the RF output can be programmed to service different frequency bands, thus making the Si4133G ideal for use in dual-band cellular handsets.

The unique PLL architecture used in the Si4133G produces a transient response that is superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs.

Serial Interface

A timing diagram for the serial interface is shown in Figure 2 on page 7. Figure 3 on page 7 shows the format of the serial word.

The Si4133G is programmed serially with 22-bit words comprised of 18-bit data fields and 4-bit address fields. When the serial interface is enabled (i.e., when SENB is low) data and address bits on the SDATA pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of SENB into the internal data register addressed in the address field. The serial interface is disabled when SENB is high.

Table 10 on page 20 summarizes the data register functions and addresses. The internal shift register will ignore any leading bits before the 22 required bits.

Setting the VCO Center Frequencies

The PLLs can adjust the IF and RF output frequencies ±5% with respect to their VCO center frequencies. Each center frequency is established by the value of an external inductance connected to the respective VCO. Manufacturing tolerances of ±10% for the external inductances are acceptable. The Si4133G will compensate for inaccuracies in each inductance by executing a self-tuning algorithm following PLL power-up or following a change in the programmed output frequency.

Because the total tank inductance is in the low nH range, the inductance of the package needs to be considered in determining the correct external inductance. The total inductance (L_{TOT}) presented to each VCO is the sum of the external inductance (L_{EXT}) and the package inductance (L_{PKG}). Each VCO has a nominal capacitance (C_{NOM}) in parallel with the total inductance, and the center frequency is as follows:

$$f_{CEN} = \frac{1}{2\pi\sqrt{L_{TOT} \cdot C_{NOM}}}$$

or

$$f_{CEN} = \frac{1}{2\pi\sqrt{(L_{PKG} + L_{EXT}) \cdot C_{NOM}}}$$

Tables 6 and 7 summarize these characteristics for each VCO.

Table 6. Si4133G-BT VCO Characteristics

VCO	Fcen Range (MHz)		Cnom (pF)	Lpkg (nH)	Lext Range (nH)	
	Min	Max			Min	Max
RF1	947	1720	4.3	2.0	0.0	4.6
RF2	789	1429	4.8	2.3	0.3	6.2
IF	526	952	6.5	2.1	2.2	12.0

Table 7. Si4133G-BM VCO Characteristics

VCO	Fcen Range (MHz)		Cnom (pF)	Lpkg (nH)	Lext Range (nH)	
	Min	Max			Min	Max
RF1	947	1720	4.3	1.5	0.5	5.1
RF2	789	1429	4.8	1.5	1.1	7.0
IF	526	952	6.5	1.6	2.7	12.5

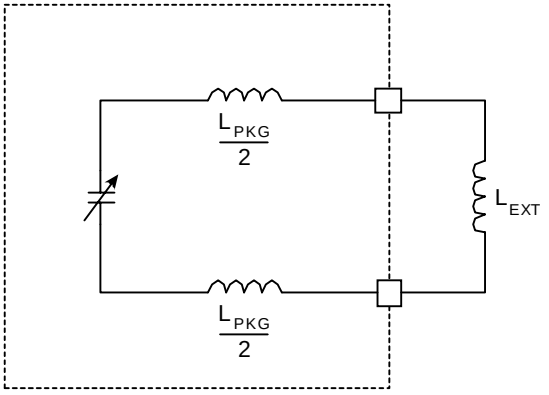


Figure 15. External Inductance Connection

As a design example, suppose it is desired to synthesize frequencies in a 25 MHz band between 1120 MHz and 1145 MHz. The center frequency should be defined as midway between the two extremes, or 1132.5 MHz. The PLL will be able to adjust the VCO output frequency ±5% of the center frequency, or ±56.6 MHz of 1132.5 MHz (i.e., from approximately 1076 MHz to 1189 MHz, more than enough for this example). The RF2 VCO has a C_{NOM} of 4.8 pF, and a 4.1 nH inductance (correct to two digits) in parallel with this capacitance will yield the desired center frequency. An external inductance of 1.8 nH should be connected between RFLC and RFLD as shown in Figure 15. This, in addition to 2.3 nH of L_{PKG} (Si4133G-BT), will present the correct total inductance to the VCO. In manufacturing, the external inductance can vary ±10% of its nominal value and the Si4133G will correct for the variation with the self-tuning algorithm.

In most cases, particularly for the RF VCOs, the requisite value of the external inductance is small enough to allow a PC board trace to be utilized. During initial board layout, a length of trace approximating the desired inductance can be used. For more information, please refer to Application Note 31.

Self-Tuning Algorithm

The self-tuning algorithm is initiated immediately following power-up of a PLL or, if the PLL is already powered, following a change in its programmed output frequency. This algorithm attempts to tune the VCO so that its free-running frequency is near the desired output frequency. In so doing, the algorithm will compensate for manufacturing tolerance errors in the value of the external inductance connected to the VCO. It will also reduce the frequency error for which the PLL must correct to get the precise desired output frequency. The self-tuning algorithm will leave the VCO oscillating at a frequency in error by somewhat less than 1% of the desired output frequency.

After self-tuning, the PLL controls the VCO oscillation frequency. The PLL will complete frequency locking, eliminating any remaining frequency error. Thereafter, it will maintain frequency-lock, compensating for effects caused by temperature and supply voltage variations.

The Si4133G's self-tuning algorithm will compensate for component value errors at any temperature within the specified temperature range. However, the ability of the PLL to compensate for drift in component values that occur *after* self-tuning is limited. For external inductances with temperature coefficients around ±150 ppm/^{o}C, the PLL will be able to maintain lock for changes in temperature of approximately ±30^{o}C.

Applications where the PLL is regularly powered down (such as GSM) or switched between channels minimize or eliminate the potential effects of temperature drift because the VCO is re-tuned when it is powered up or when a new frequency is programmed. In applications where the ambient temperature can drift substantially after self-tuning, it may be necessary to monitor the LDETB (lock-detect bar) signal on the AUXOUT pin to determine the locking state of the PLL. (See "Auxiliary Output (AUXOUT)" on page 18 for how to select LDETB.)

The LDETB signal is normally low after self-tuning is completed but will rise to a logic high condition when

either the IF or RF PLL nears the limit of its compensation range (LDETB will also be high when either PLL is executing the self-tuning algorithm). The output frequency will still be locked when LDETB goes high, but the PLL will eventually lose lock if the temperature continues to drift in the same direction. Therefore, if LDETB goes high both the IF and RF PLLs should promptly be re-tuned by initiating the self-tuning algorithm.

Output Frequencies

The IF and RF output frequencies are set by programming the N-Divider registers. Each RF PLL has its own N register and can be programmed independently. All three PLL R dividers are fixed at R = 65 to yield a 200 kHz phase detector update rate from a 13 MHz reference frequency. Programming the N-Divider register for either RF1 or RF2 automatically selects the associated output.

The reference frequency on the XIN pin is divided by R and this signal is the input to the PLL's phase detector. The other input to the phase detector is the PLL's VCO output frequency divided by N. The PLL works to make these frequencies equal. That is, after an initial transient

$$\frac{f_{OUT}}{N} = \frac{f_{REF}}{65}$$

or

$$f_{OUT} = \frac{N}{65} \cdot f_{REF}$$

For XIN = 13 MHz this simplifies to

$$f_{OUT} = N \cdot 200\ kHz$$

The integer N is set by programming the RF1 N-Divider register (Register 3), the RF2 N-Divider register (Register 4), and the IF N-Divider register (Register 5).

Each N divider is implemented as a conventional high speed divider. That is, it consists of a dual-modulus prescaler, a swallow counter, and a lower speed synchronous counter. However, the calculation of these values is done automatically. Only the appropriate N value needs to be programmed.

PLL Loop Dynamics

The transient response for each PLL has been optimized for a GSM application. VCO gain, phase detector gain, and loop filter characteristics are not programmable.

The settling time for each PLL is directly proportional to its phase detector update period Tϕ (Tϕ equals 1/fϕ). For a GSM application with a 13 MHz reference frequency, the RF and IF PLLs Tϕ = 5 µS. During the first 6.5 update periods, the Si4133G executes the self-tuning algorithm. Thereafter the PLL controls the output frequency. Because of the unique architecture of the Si4133G PLLs, the time required to settle the output frequency to 0.1 ppm error is approximately 21 update periods. Thus, the total time after power-up or a change in programmed frequency until the synthesized frequency is well settled (including time for self-tuning) is around 28 update periods or 140 µS.

RF and IF Outputs (RFOUT and IFOUT)

The RFOUT pin is driven by an amplifier that buffers the output pin from the RF VCOs, and must be coupled to its load through an AC coupling capacitor. The amplifier receives its input from either the RF1 or RF2 VCO, depending upon which N-Divider register was last written. For example, programming the N-Divider register for RF1 automatically selects the RF1 VCO output.

A matching network is required to maximize power delivered into a 50 Ω load. The network consists of a 2 nH series inductance, which may be realized with a PC board trace, connected between the RFOUT pin and the AC coupling capacitor. The network is made to provide an adequate match for both the RF1 and RF2 frequency bands, and also filters the output signal to reduce harmonic distortion. A 50 Ω load is not required for proper operation of the Si4133G. Depending on transceiver requirements, the matching network may not be needed. See Figure 16.

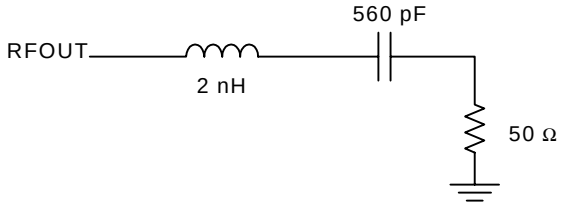


Figure 16. RFOUT 50 Ω Test Circuit

The IFOUT pin is driven by an amplifier that buffers the output pin from the IF VCO. The IFOUT pin must be coupled to its load through an AC coupling capacitor. A matching network is required to maximize power delivered into a 50 Ω load. See Figure 17.

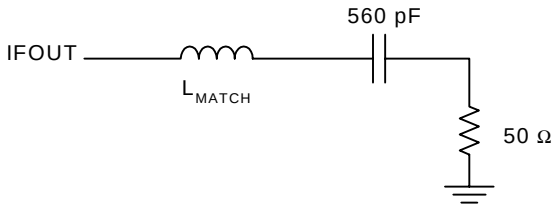


Figure 17. IFOUT 50 Ω Test Circuit

Table 8. L_{MATCH} Values

Frequency	L_{MATCH}
500–600 MHz	40 nH
600–800 MHz	27 nH
800–1 GHz	18 nH

The IF output level is dependent upon the load. Figure 18 displays the output level versus load resistance for a variety of output frequencies.

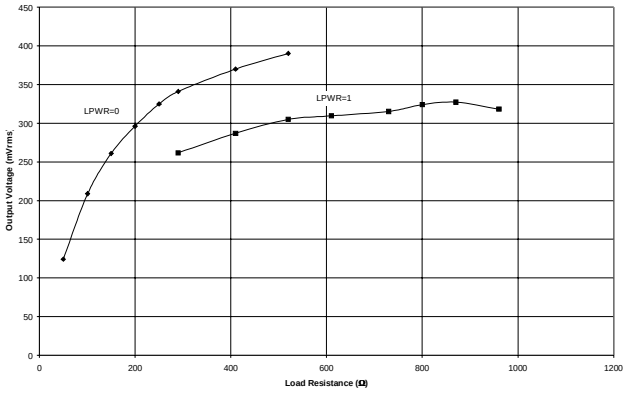


Figure 18. Typical IF Output Voltage vs. Load Resistance at 550 MHz

For resistive loads greater than 500 Ω the output level saturates and the bias currents in the IF output amplifier are higher than they need be. The LPWR bit in the Main Configuration register (Register 0) can be set to 1 to reduce the bias currents and therefore reduce the power dissipated by the IF amplifier. For loads less than 500 Ω LPWR should be set to 0 to maximize the output level.

Reference Frequency Amplifier

The Si4133G provides a reference frequency amplifier. If the driving signal has CMOS levels it can be connected directly to the XIN pin. Otherwise, the reference frequency signal should be AC coupled to the XIN pin through a 560 pF capacitor.

Power Down Modes

Table 9 summarizes the power down functionality. The Si4133G can be powered down by taking the PWDNB pin low or by setting bits in the Power Down register (Register 1). When the PWDNB pin is low, the Si4133G will be powered down regardless of the Power Down register settings. When the PWDNB pin is high, power management is under control of the Power Down register bits.

The reference frequency amplifier, IF, and RF sections of the Si4133G circuitry can be individually powered down by setting the Power Down register bits PDIB and PDRB low, respectively. The reference frequency amplifier will also be powered up if either of the PDRB or PDIB bits are high. Also, setting the AUTOPDB bit to 1 in the Main Configuration register (Register 0) is equivalent to setting both bits in the Power Down register to 1. The serial interface remains available and can be written in all power down modes.

Auxiliary Output (AUXOUT)

The signal appearing on AUXOUT is selected by setting the AUXSEL bits in the Main Configuration register (Register 0).

The LDETB signal can be selected by setting the AUXSEL bits to 11. As discussed previously, this signal can be used to indicate that the IF or RF PLL is about to lose lock due to excessive ambient temperature drift and should be re-tuned.

Table 9. Power Down Configuration

PWDNB Pin	AUTOPDB	PDIB	PDRB	IF Circuitry	RF Circuitry
PWDNB = 0	x	x	x	OFF	OFF
PWDNB = 1	0	0	0	OFF	OFF
	0	0	1	OFF	ON
	0	1	0	ON	OFF
	0	1	1	ON	ON
	1	x	x	ON	ON

Control Registers

Table 10. Register Summary

Register	Name	Bit 17	Bit 16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Main Configuration	0	0	0	0	AUXSEL [1:0]		0	0	0	0	0	0	LPWR	0	AUTO PDB	0	1	0
1	Reserved																		
2	Power Down	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB
3	RF1 N Divider	N_{RF1}[17:0]																	
4	RF2 N Divider	0	N_{RF}[16:0]																
5	IF N Divider	0	0	N_{IF}[15:0]															
6	Reserved																		
. . .																			
15	Reserved																		

Note: Registers 1 and 6–15 are reserved. Writes to these registers may result in unpredictable behavior. Any register not listed here is reserved and should not be written.

Register 0. Main Configuration Address Field = A[3:0] = 0000

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	AUXSEL [1:0]		0	0	0	0	0	0	LPWR	0	AUTO PDB	0	1	0

Bit	Name	Function
17:14	Reserved	Program to zero.
13:12	AUXSEL [1:0]	**Auxiliary Output Pin Definition.** 00 = Reserved. 01 = Force output low. 10 = Reserved. 11 = Lock Detect—LDETB.
11:6	Reserved	Program to zero.
5	LPWR	**Output Power-Level Settings for IF Synthesizer Circuit.** 0 = R_{LOAD} < 500 Ω—normal power mode. 1 = R_{LOAD} ≥ 500 Ω—low power mode.
4	Reserved	Program to zero.
3	AUTOPDB	**Auto Power Down** 0 = Software powerdown is controlled by Register 2. 1 = Equivalent to setting all bits in Register 2 = 1.
2	Reserved	Program to zero.
1	Reserved	Program to **one**.
0	Reserved	Program to zero.

Register 2. Power Down Address Field (A[3:0]) = 0010

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB

Bit	Name	Function
17:2	Reserved	Program to zero.
1	PDIB	**Power Down IF Synthesizer.** 0 = IF synthesizer powered down. 1 = IF synthesizer on. **Note:** Always program to 0 for Si4113G.
0	PDRB	**Power Down RF Synthesizer.** 0 = RF synthesizer powered down. 1 = RF synthesizer on. **Note:** Always program to 0 for Si4112G.

Register 3. RF1 N Divider Address Field (A[3:0]) = 0011

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	N_{RF1}[17:0]																	

Bit	Name	Function
17:0	N_{RF1}[17:0]	**N Divider for RF1 Synthesizer.** Register reserved for Si4112G, Si4122G. Writes to this register may result in unpredictable behavior.

Register 4. RF2 N Divider Address Field = A[3:0] = 0100

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	N_{RF2}[16:0]																

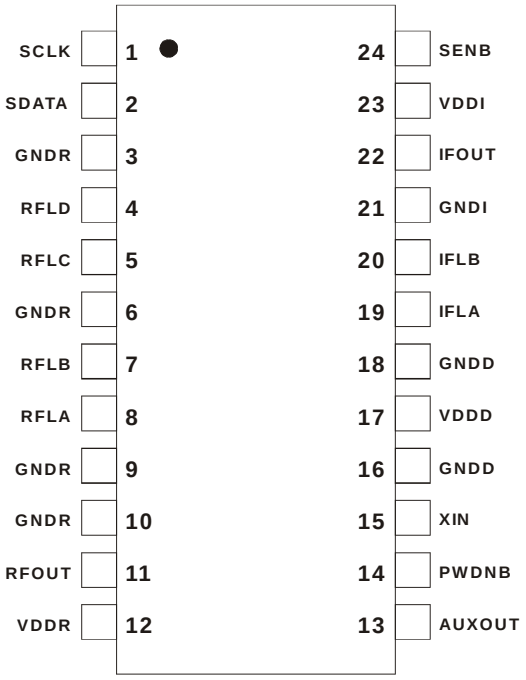
Bit	Name	Function
17	Reserved	Program to zero.
16:0	N_{RF2}[16:0]	**N Divider for RF2 Synthesizer.** Register reserved for Si4112G, Si4123G. Writes to this register may result in unpredictable behavior.

Register 5. IF N Divider Address Field (A[3:0]) = 0101

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	N_{IF}[15:0]															

Bit	Name	Function
17:16	Reserved	Program to zero.
15:0	N_{IF}[15:0]	**N Divider for IF Synthesizer.** Register reserved for Si4113G. Writes to this register may result in unpredictable behavior.

Pin Descriptions: Si4133G-BT

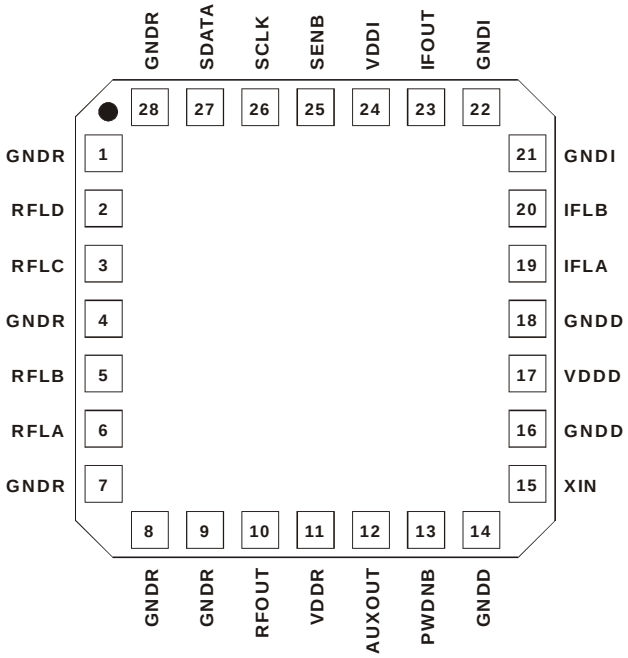


Pin Number(s)	Name	Description
1	SCLK	Serial clock input
2	SDATA	Serial data input
3, 6, 9, 10	GNDR	Common ground for RF analog circuitry
4, 5	RFLC, RFLD	Pins for inductor connection to RF2 VCO
7, 8	RFLA, RFLB	Pins for inductor connection to RF1 VCO
11	RFOUT	Radio frequency (RF) output of the selected RF VCO
12	VDDR	Supply voltage for the RF analog circuitry
13	AUXOUT	Auxiliary output
14	PWDNB	Power down input pin
15	XIN	Reference frequency amplifier input
16, 18	GNDD	Common ground for digital circuitry
17	VDDD	Supply voltage for digital circuitry
19, 20	IFLA, IFLB	Pins for inductor connection to IF VCO
21	GNDI	Common ground for IF analog circuitry
22	IFOUT	Intermediate frequency (IF) output of the IF VCO
23	VDDI	Supply voltage for IF analog circuitry
24	SENB	Enable serial port input

Table 11. Pin Descriptions for Si4133G Derivatives—TSSOP

Pin Number	Si4133G-BT	Si4123G-BT	Si4122G-BT	Si4113G-BT	Si4112G-BT
1	SCLK	SCLK	SCLK	SCLK	SCLK
2	SDATA	SDATA	SDATA	SDATA	SDATA
3	GNDR	GNDR	GNDR	GNDR	GNDD
4	RFLD	GNDR	RFLD	RFLD	GNDD
5	RFLC	GNDR	RFLC	RFLC	GNDD
6	GNDR	GNDR	GNDR	GNDR	GNDD
7	RFLB	RFLB	GNDR	RFLB	GNDD
8	RFLA	RFLA	GNDR	RFLA	GNDD
9	GNDR	GNDR	GNDR	GNDR	GNDD
10	GNDR	GNDR	GNDR	GNDR	GNDD
11	RFOUT	RFOUT	RFOUT	RFOUT	GNDD
12	VDDR	VDDR	VDDR	VDDR	VDDD
13	AUXOUT	AUXOUT	AUXOUT	AUXOUT	AUXOUT
14	PWDNB	PWDNB	PWDNB	PWDNB	PWDNB
15	XIN	XIN	XIN	XIN	XIN
16	GNDD	GNDD	GNDD	GNDD	GNDD
17	VDDD	VDDD	VDDD	VDDD	VDDD
18	GNDD	GNDD	GNDD	GNDD	GNDD
19	IFLA	IFLA	IFLA	GNDD	IFLA
20	IFLB	IFLB	IFLB	GNDD	IFLB
21	GNDI	GNDI	GNDI	GNDD	GNDI
22	IFOUT	IFOUT	IFOUT	GNDD	IFOUT
23	VDDI	VDDI	VDDI	VDDD	VDDI
24	SENB	SENB	SENB	SENB	SENB

Pin Descriptions: Si4133G-BM



Pin Number(s)	Name	Description
1, 4, 7–9, 28	GNDR	Common ground for RF analog circuitry
2, 3	RFLC, RFLD	Pins for inductor connection to RF2 VCO
5,6	RFLA, RFLB	Pins for inductor connection to RF1 VCO
10	RFOUT	Radio frequency (RF) output of the selected RF VCO
11	VDDR	Supply voltage for the RF analog circuitry
12	AUXOUT	Auxiliary output
13	PWDNB	Power down input pin
14, 16, 18	GNDD	Common ground for digital circuitry
15	XIN	Reference frequency amplifier input
17	VDDD	Supply voltage for digital circuitry
19, 20	IFLA, IFLB	Pins for inductor connection to IF VCO
21, 22	GNDI	Common ground for IF analog circuitry
23	IFOUT	Intermediate frequency (IF) output of the IF VCO
24	VDDI	Supply voltage for IF analog circuitry
25	SENB	Enable serial port input
26	SCLK	Serial clock input
27	SDATA	Serial data input

Table 12. Pin Descriptions for Si4133G Derivatives—MLP

Pin Number	Si4133G-BM	Si4123G-BM	Si4122G-BM	Si4113G-BM	Si4112G-BM
1	GNDR	GNDR	GNDR	GNDR	GNDD
2	RFLD	GNDR	RFLD	RFLD	GNDD
3	RFLC	GNDR	RFLC	RFLC	GNDD
4	GNDR	GNDR	GNDR	GNDR	GNDD
5	RFLB	RFLB	GNDR	RFLB	GNDD
6	RFLA	RFLA	GNDR	RFLA	GNDD
7	GNDR	GNDR	GNDR	GNDR	GNDD
8	GNDR	GNDR	GNDR	GNDR	GNDD
9	GNDR	GNDR	GNDR	GNDR	GNDD
10	RFOUT	RFOUT	RFOUT	RFOUT	GNDD
11	VDDR	VDDR	VDDR	VDDR	VDDD
12	AUXOUT	AUXOUT	AUXOUT	AUXOUT	AUXOUT
13	PWDNB	PWDNB	PWDNB	PWDNB	PWDNB
14	GNDD	GNDD	GNDD	GNDD	GNDD
15	XIN	XIN	XIN	XIN	XIN
16	GNDD	GNDD	GNDD	GNDD	GNDD
17	VDDD	VDDD	VDDD	VDDD	VDDD
18	GNDD	GNDD	GNDD	GNDD	GNDD
19	IFLA	IFLA	IFLA	GNDD	IFLA
20	IFLB	IFLB	IFLB	GNDD	IFLB
21	GNDI	GNDI	GNDI	GNDD	GNDI
22	GNDI	GNDI	GNDI	GNDD	GNDI
23	IFOUT	IFOUT	IFOUT	GNDD	IFOUT
24	VDDI	VDDI	VDDI	VDDD	VDDI
25	SENB	SENB	SENB	SENB	SENB
26	SCLK	SCLK	SCLK	SCLK	SCLK
27	SDATA	SDATA	SDATA	SDATA	SDATA
28	GNDR	GNDR	GNDR	GNDR	GNDD

Ordering Guide

Ordering Part Number	Description	Operating Temperature
Si4133G-BT* Si4133G-BM	RF1/RF2/IF	–20 to 85°C
Si4123G-BT* Si4123G-BM	RF1/IF	–20 to 85°C
Si4122G-BT* Si4122G-BM	RF2/IF	–20 to 85°C
Si4113G-BT* Si4113G-BM	RF1/RF2	–20 to 85°C
Si4112G-BT* Si4112G-BM	IF	–20 to 85°C
***Note:** TSSOP not recommended for new designs.		

Si4133G Derivative Devices

The Si4133G performs both IF and dual-band RF frequency synthesis. The Si4112G, Si4113G, Si4122G, and the Si4123G are derivatives of this device. Table 13 outlines which synthesizers each derivative device features as well as which pins and registers coincide with each synthesizer.

Table 13. Si4133G Derivatives

Name	Synthesizer	Pins	Registers
Si4112G	IF	IFLA, IFLB	N_{IF}, R_{IF}, PDIB, IFDIV, LPWR, AUTOPDB = 0, PDRB = 0
Si4113G	RF1, RF2	RFLA, RFLB, RFLC, RFLD	N_{RF1}, N_{RF2}, R_{RF1}, R_{RF2}, PDRB, AUTOPDB = 0, PDIB = 0
Si4122G	RF2, IF	RFLC, RFLD, IFLA, IFLB	N_{RF2}, R_{RF2}, PDRB, N_{IF}, R_{IF}, PDIB, LPWR
Si4123G	RF1, IF	RFLA, RFLB, IFLA, IFLB	N_{RF1}, R_{RF1}, PDRB, N_{IF}, R_{IF}, PDIB, LPWR
Si4133G	RF1, RF2, IF	RFLA, RFLB, RFLC, RFLD, IFLA, IFLB	N_{RF1}, N_{RF2}, R_{RF1}, R_{RF2}, PDRB, N_{IF}, R_{IF}, PDIB, LPWR

Package Outline: Si4133G-BT

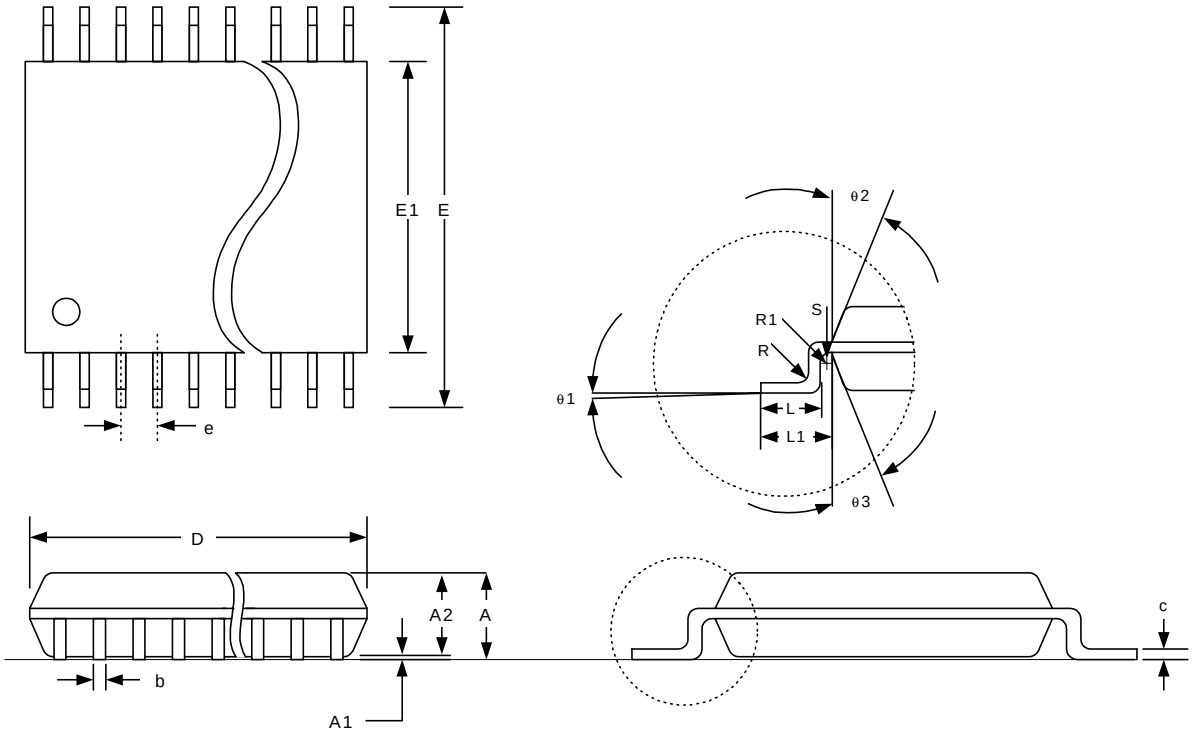


Figure 19. 24-pin Thin Small Shrink Outline Package (TSSOP)

Table 14. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	1.10	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	7.70	7.80	7.90
e	0.65 BSC		
E	6.40 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.00 REF		
R	0.09	—	—
R1	0.09	—	—
S	0.20	—	—
θ1	0	—	8
θ2	12 REF		
θ3	12 REF		

Package Outline: Si4133G-BM

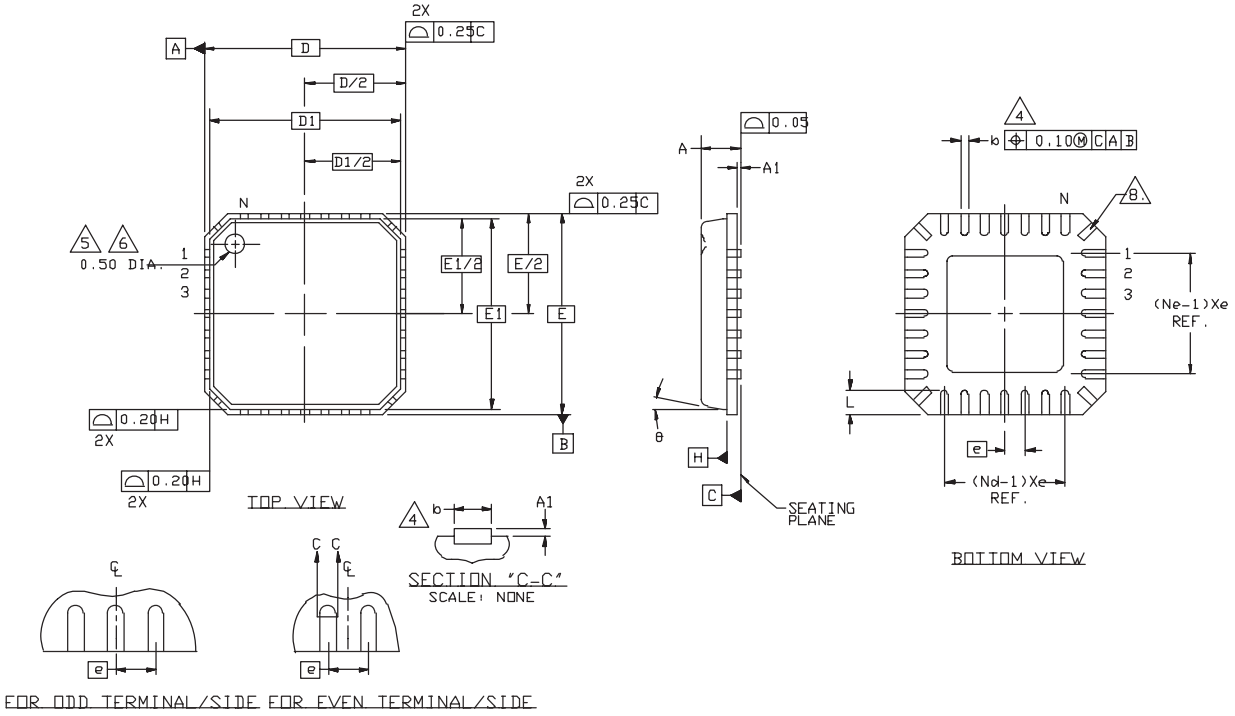


Figure 20. 28-Pin Micro Leadframe Package (MLP)

Table 15. Package Dimensions

Controlling Dimension: mm

Symbol	Millimeters		
	Min	Nom	Max
A	—	0.90	1.00
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D		5.00 BSC	
D1		4.75 BSC	
E		5.00 BSC	
E1		4.75 BSC	
N		28	
Nd		7	
Ne		7	
e		0.50 BSC	
L	0.50	0.60	0.75
θ			12°

NOTES:

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