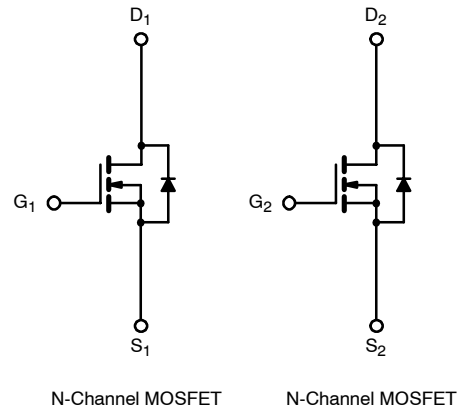
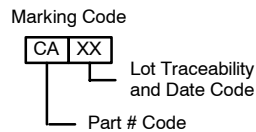
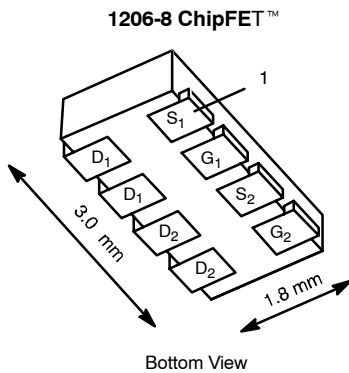




Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.085 @ $V_{GS} = 10$ V	± 3.9
	0.143 @ $V_{GS} = 4.5$ V	± 3.0

TrenchFET[®]
Power MOSFETs



Ordering Information: Si5902DC-T1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 3.9	A
		$T_A = 85^\circ\text{C}$	± 2.8	
Pulsed Drain Current	I_{DM}	± 10		
Continuous Source Current (Diode Conduction) ^a	I_S	1.8	0.9	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.1	W
		$T_A = 85^\circ\text{C}$	1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ sec	50	$^\circ\text{C/W}$
		Steady State	90	
Maximum Junction-to-Foot	R_{thJF}	30	40	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

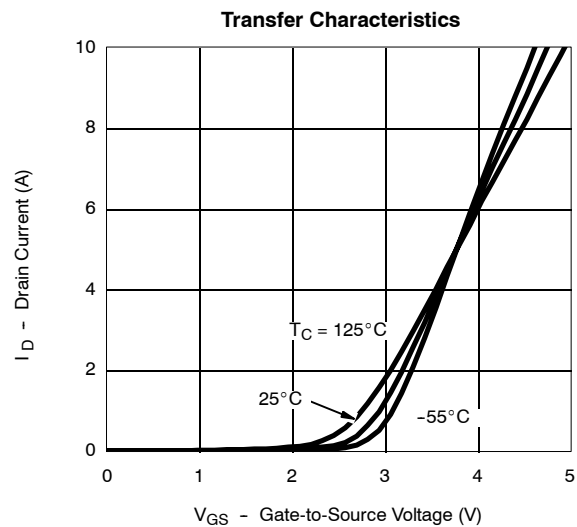
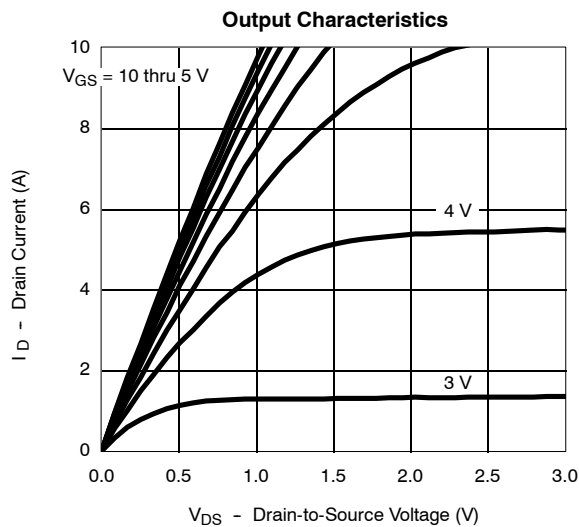
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 85 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	10			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.9 A		0.072	0.085	Ω
		V _{GS} = 4.5 V, I _D = 2.2 A		0.120	0.143	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.9 A		20		S
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 2.9 A		5	7.5	nC
Gate-Source Charge	Q _{gs}			0.8		
Gate-Drain Charge	Q _{gd}			1.0		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		7	11	ns
Rise Time	t _r			12	18	
Turn-Off Delay Time	t _{d(off)}			12	18	
Fall Time	t _f			7	11	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs		40	80	

Notes

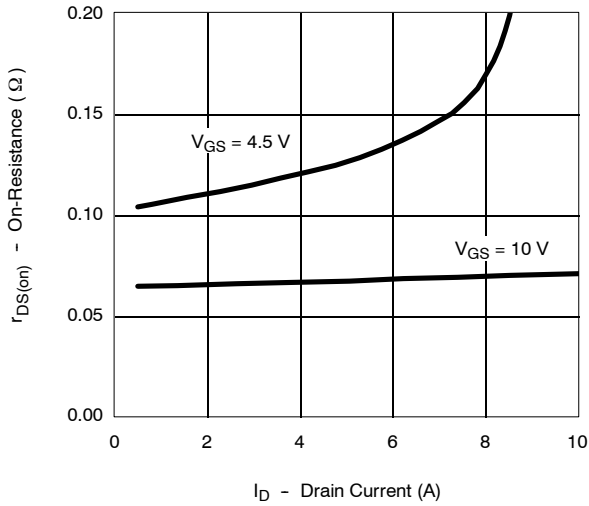
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

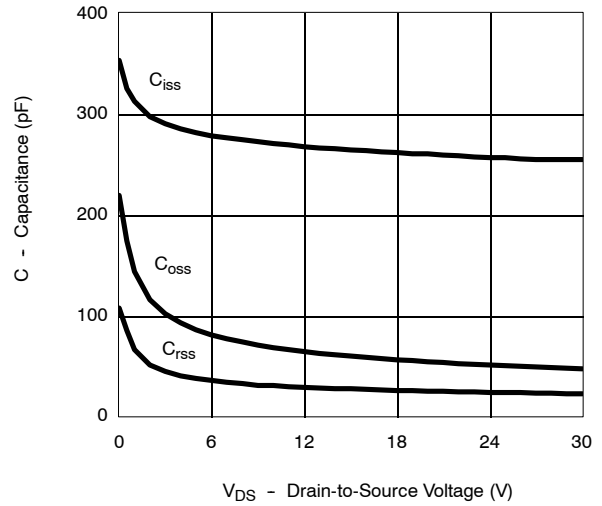


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

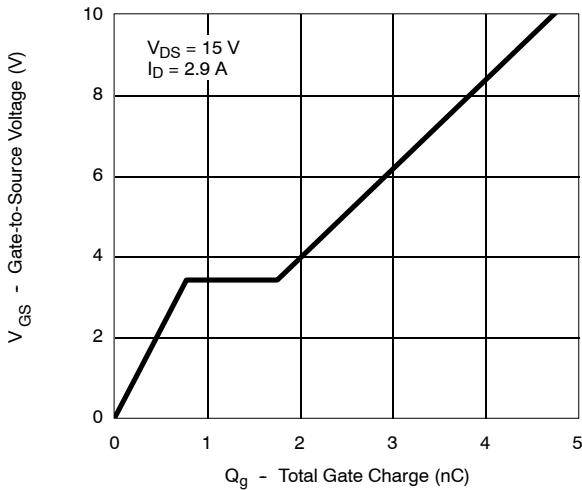
On-Resistance vs. Drain Current



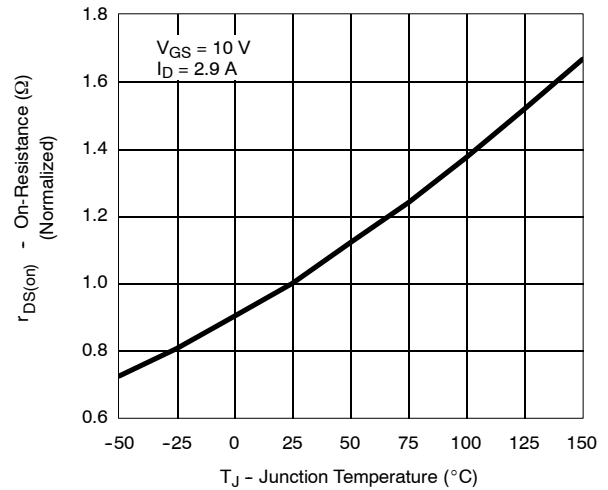
Capacitance



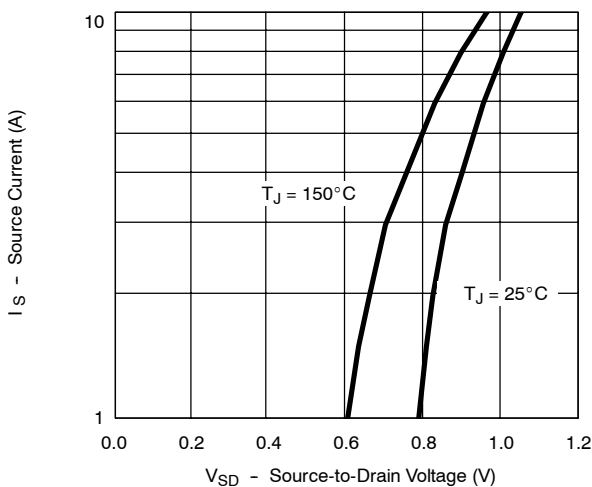
Gate Charge



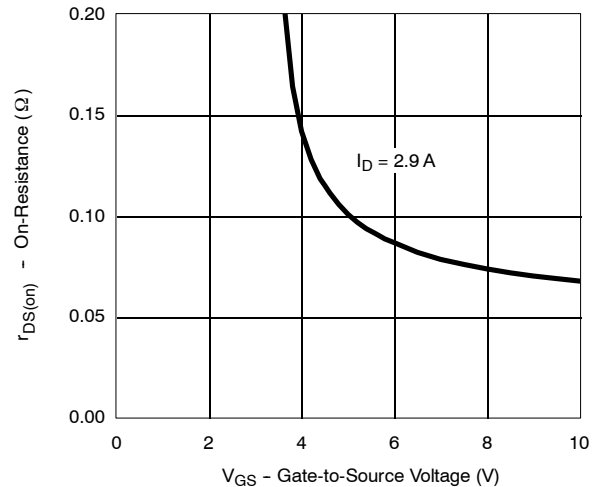
On-Resistance vs. Junction Temperature



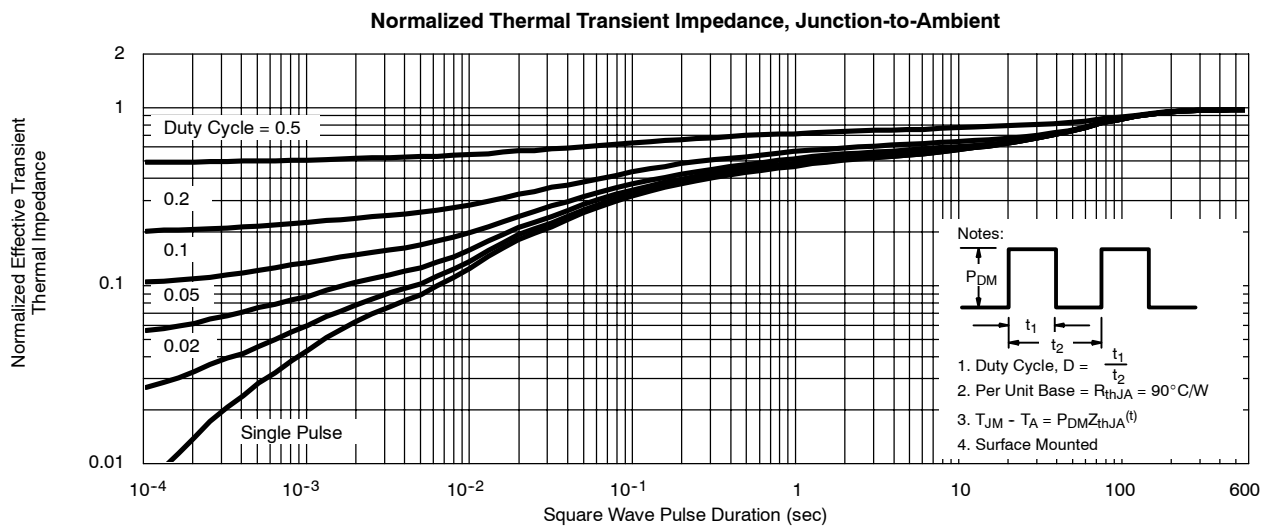
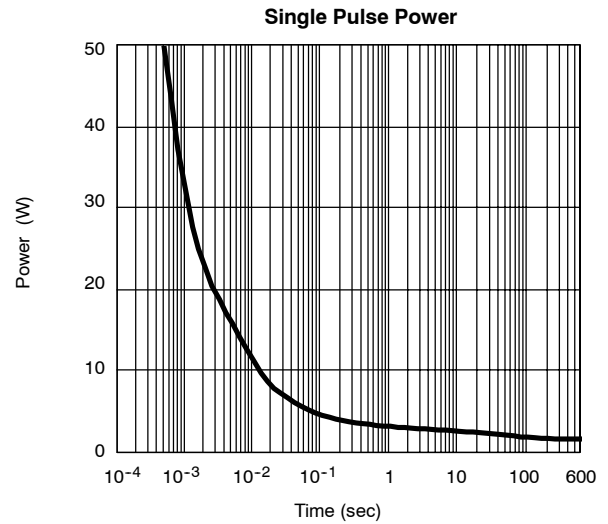
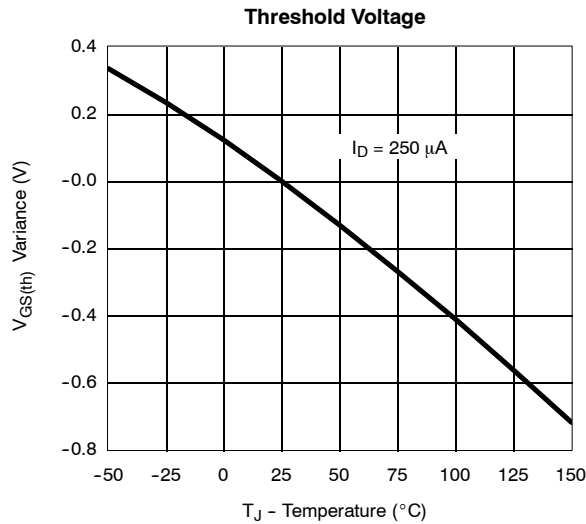
Source-Drain Diode Forward Voltage



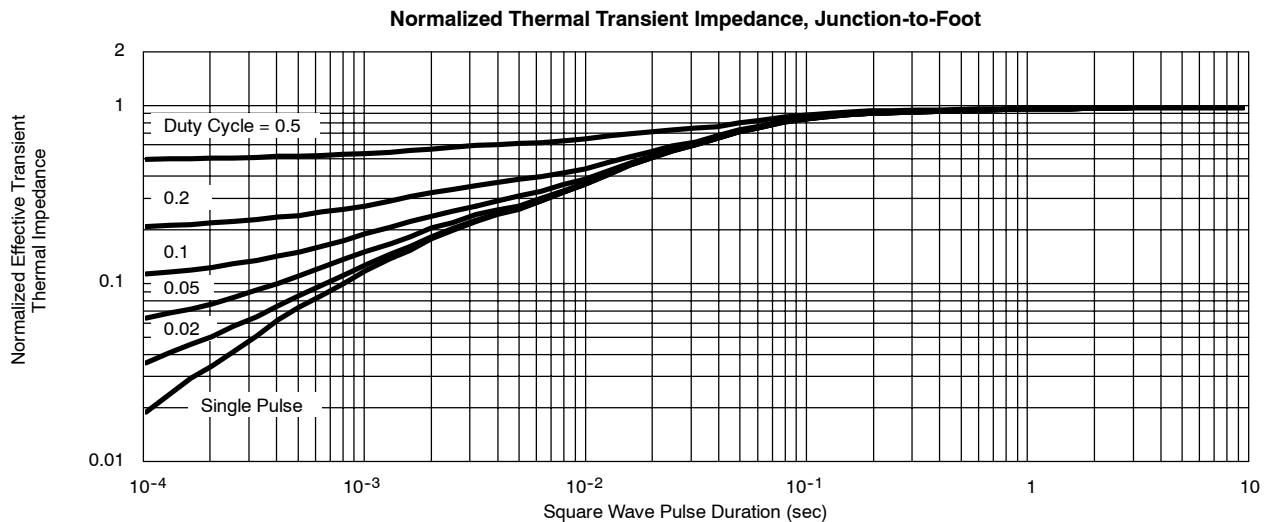
On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



1000



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