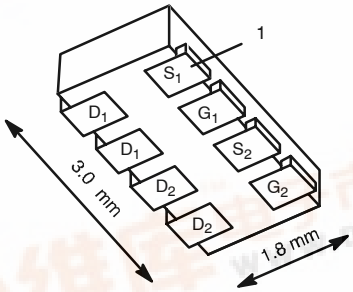
Dual P-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.155 @ V_{GS} = -4.5 V	±2.9
	0.180 @ V_{GS} = -3.6 V	±2.7
	0.260 @ V_{GS} = -2.5 V	±2.2

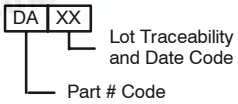
TrenchFET® Power MOSFETs 2.5-V Rated

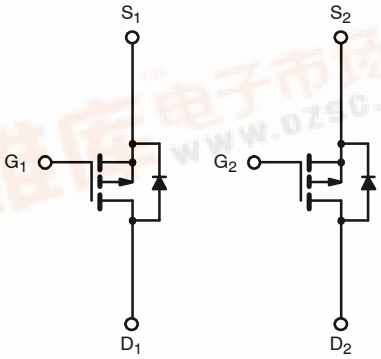
1206-8 ChipFET™



Bottom View

Marking Code





P-Channel MOSFET P-Channel MOSFET

Ordering Information: Si5903DC-T1

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±2.9	±2.1	A
	T_A = 85°C		±2.1	±1.5	
Pulsed Drain Current		I_{DM}	±10		
Continuous Source Current (Diode Conduction)[a]		I_S	-1.8	-0.9	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.1	1.1	W
	T_A = 85°C		1.1	0.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	50	60	°C/W
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

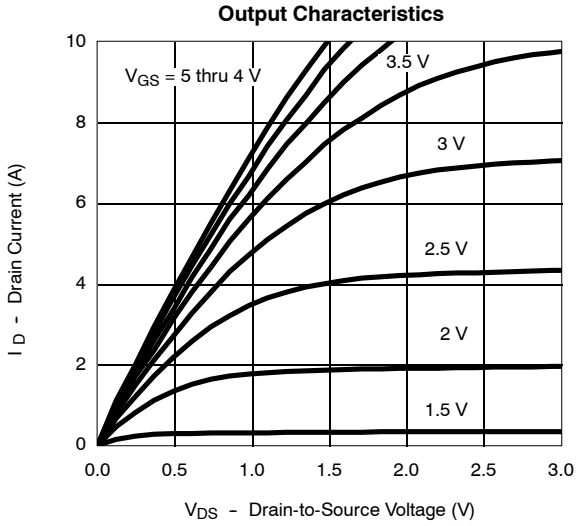
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

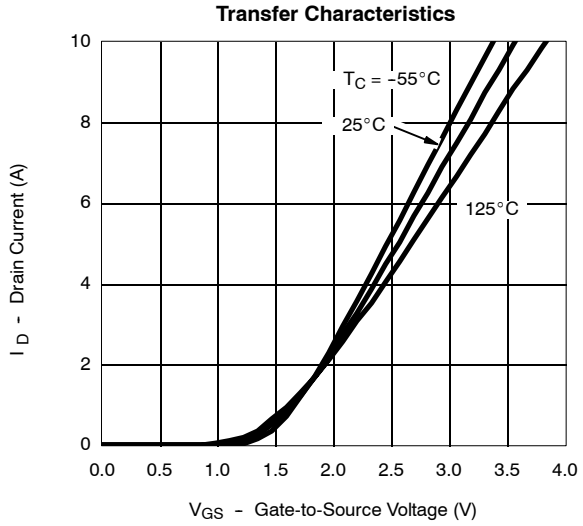
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16$ V, $V_{GS} = 0$ V			−1	μA
		$V_{DS} = -16$ V, $V_{GS} = 0$ V, $T_J = 85°C$			−5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq -5$ V, $V_{GS} = -4.5$ V	−10			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -2.1$ A		0.130	0.155	Ω
		$V_{GS} = -3.6$ V, $I_D = -2.0$ A		0.150	0.180	
		$V_{GS} = -2.5$ V, $I_D = -1.7$ A		0.215	0.260	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -10$ V, $I_D = -2.1$ A		5		S
Diode Forward Voltage[a]	V_{SD}	$I_S = -0.9$ A, $V_{GS} = 0$ V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -2.1$ A		3	6	nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			0.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 10\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -4.5$ V, $R_G = 6\ \Omega$		13	20	ns
Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			25	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -0.9$ A, di/dt = 100 A/μs		40	80	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

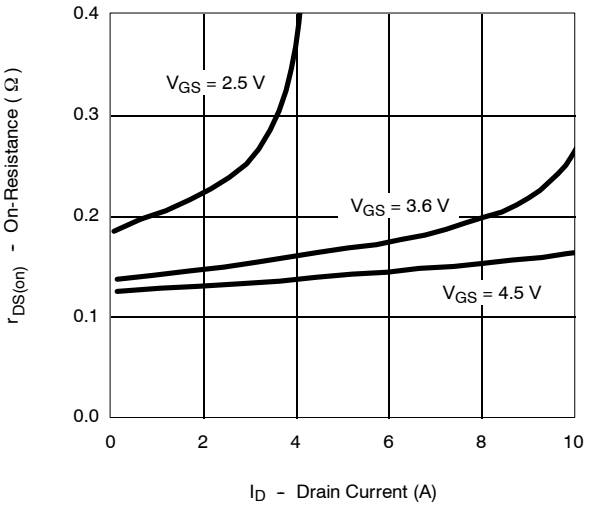
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



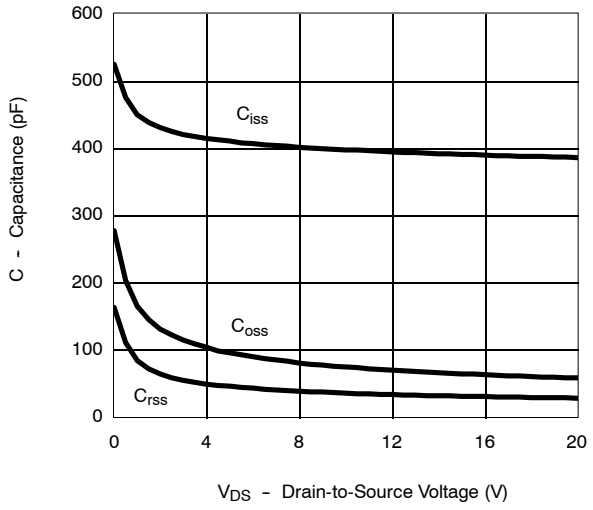


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

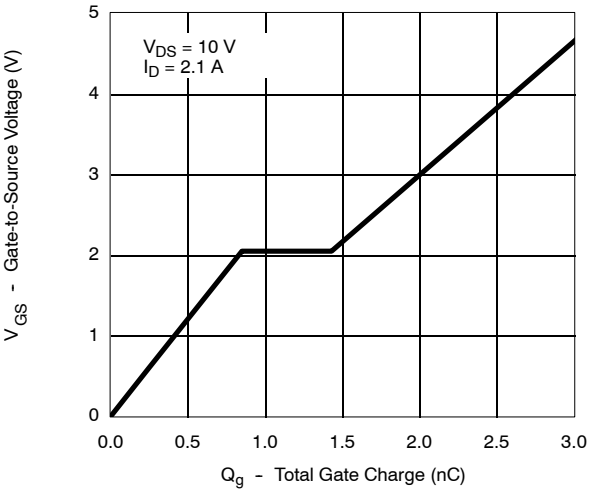
On-Resistance vs. Drain Current



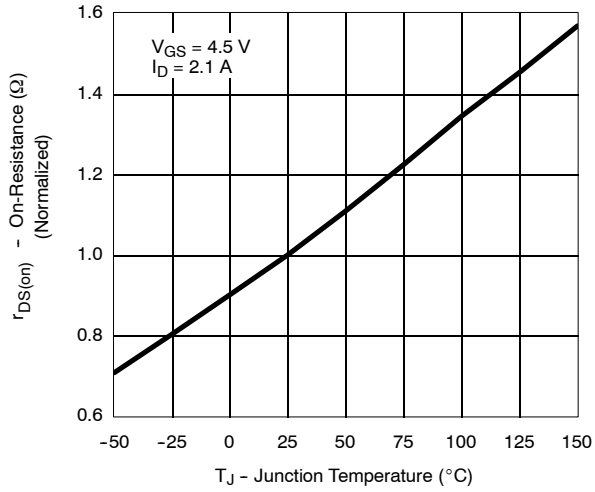
Capacitance



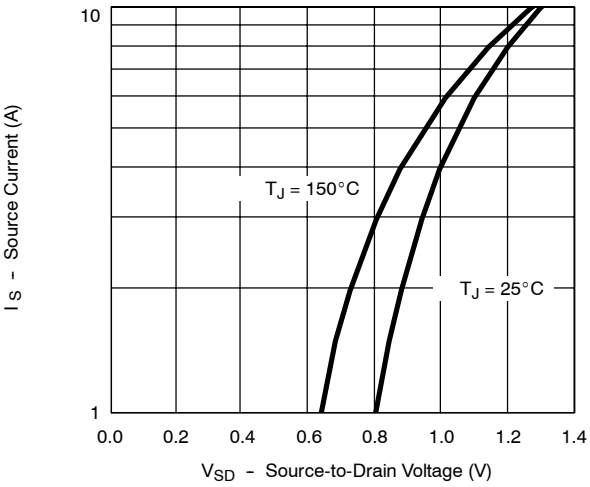
Gate Charge



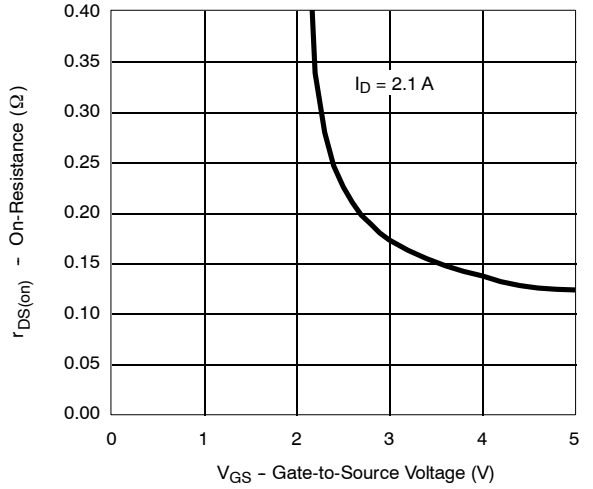
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

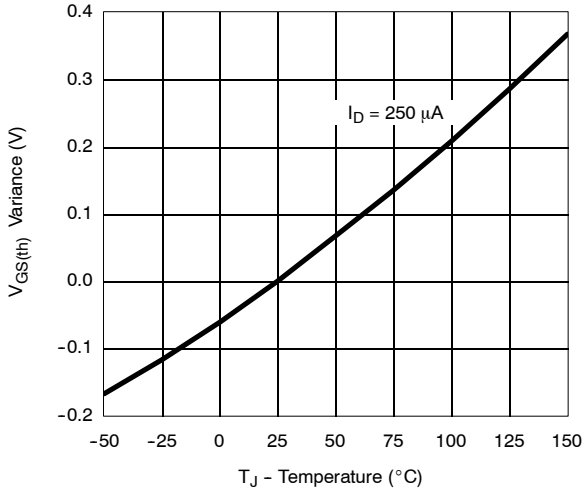


On-Resistance vs. Gate-to-Source Voltage

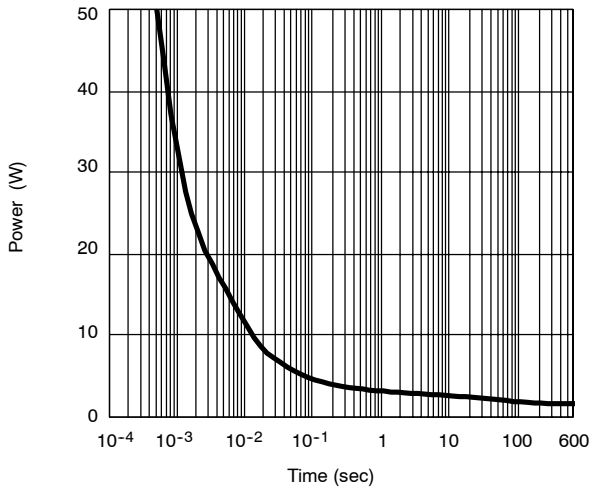


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

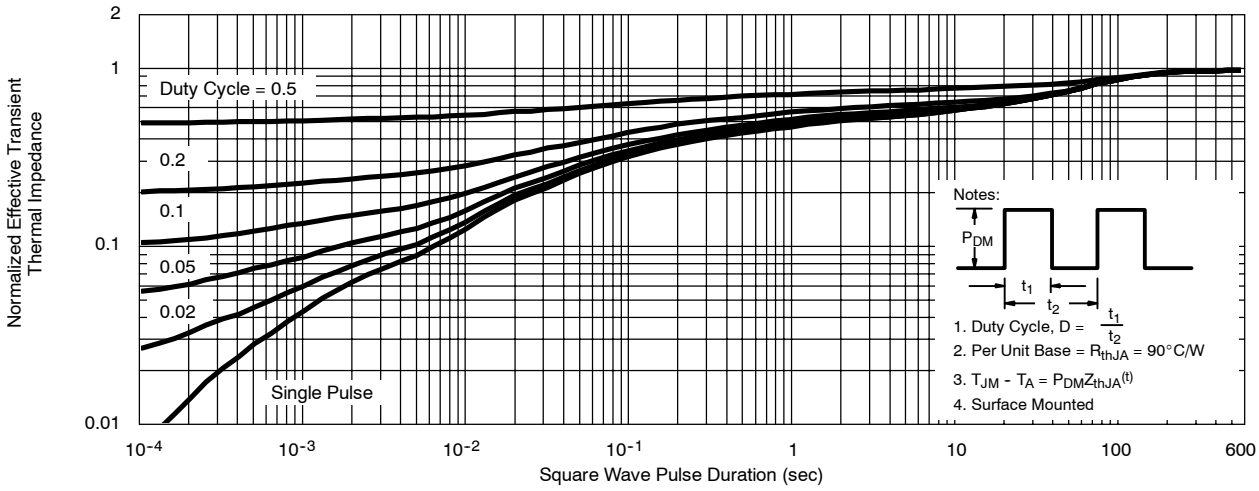
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot